The Future of Analog IC Technology®

MP28257

4A, Fast Transient, 4.2V-to-20V Input Synchronous Step-Down Converter 2mmx3mm QFN12

DESCRIPTION

The MP28257 is a fully-integrated, synchronous, step-down, switch-mode converter with a programmable frequency. It offers a very compact solution that can provide up to 4A of continuous output current over a wide input supply range with excellent load and line regulation, and can operate at high efficiency over a wide output current load range.

Constant-on-time control mode provides fast transient response and eases loop stabilization.

Protections include short-circuit protection, over-current protection, over-voltage protection, under-voltage protection, and thermal shut down.

The MP28257 requires a minimal number of readily-available standard external components.

The device is available in a space saving 2mmx3mm QFN12 package that complies with ROHS.

FEATURES

- Wide 4.2V-to-20V Operating Input Range
- 4A Continuous Output Current
- Internal 120mΩ High-Side, 50mΩ Low-Side Power MOSFETs
- Stable with Ceramic Output Capacitors
- Proprietary Switching Loss-Reduction Technology
- Power-Good Indicator
- Soft Startup/Shutdown
- Programmable Switching Frequency
- SCP, OCP, OVP, UVP Protection and Thermal Shutdown
- Output Adjustable from 0.815V to 13V
- Available in a 2mmx3mm QFN12 Package

APPLICATIONS

- Networking Systems
- Distributed Power Systems

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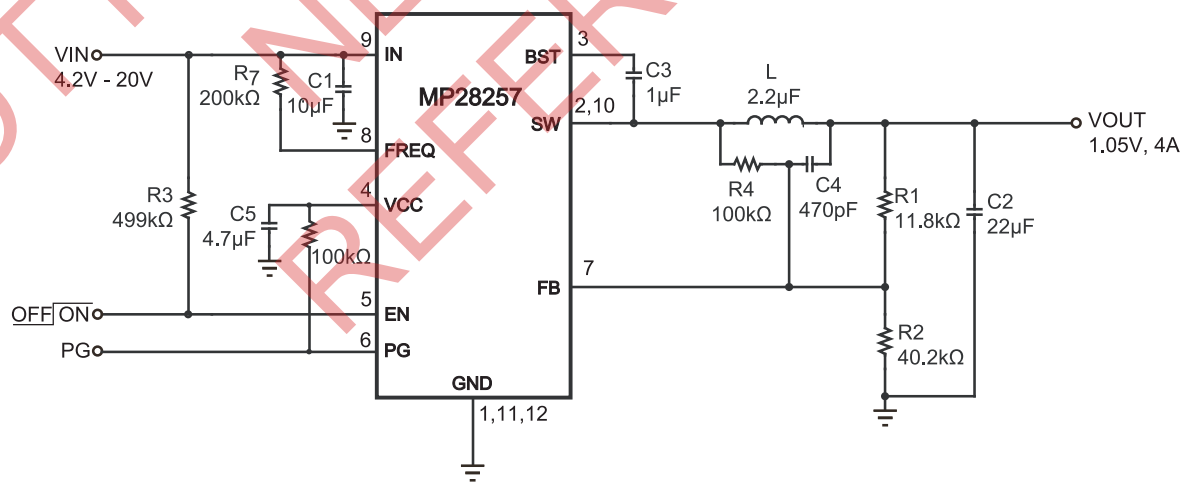
TYPICAL APPLICATION



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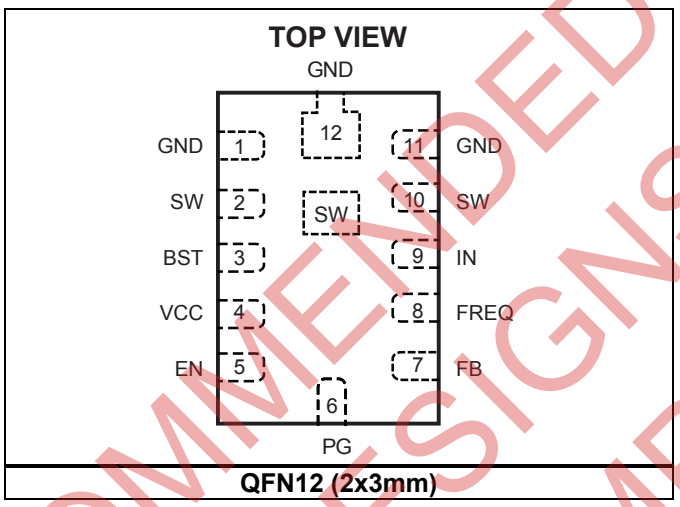
ORDERING INFORMATION

Part Number	OCP Protection	Package	Top Marking	Free Air Temperature (T_A)
MP28257DD*	Latch-off Mode	QFN12 (2x3mm)	ABF	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP28257DD–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP28257DD–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 22V
V_{SW} ..... -0.3V to (V_{IN} + 0.3V)
V_{BST} ..... V_{SW}+6V
All other pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = 25°C) (2)
QFN12 (2x3mm) 1.8W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.2V to 20V
Output Voltage V_{OUT} ..... 0.815V to 13V
Maximum Junction Temp. (T_J) ..... 125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN12 (2x3mm)	70	15	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		1		μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 0.9V		360		μA
HS switch-on resistance (5)	HS_{RDS-ON}			120		mΩ
LS Switch-on resistance (5)	LS_{RDS-ON}			50		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	10	μA
Current limit	I_{LIMIT}	After Soft-Start Time-out	5.5	7		A
One-shot on time	t_{ON}	R7 = 300kΩ, V_{OUT} = 1.2V		250		ns
Minimum off time	t_{OFF}			130	150	ns
Fold-back off time (5)	t_{FB}	I_{LIM} = 1		4.5		μs
OCP hold-off time (5)	t_{OC}	I_{LIM} = 1		50		μs
Feedback voltage	V_{FB}	T_A = 25°C	807	815	823	mV
		T_A = -40°C to 85°C	803		827	mV
Feedback current	I_{FB}	V_{FB} = 800mV		10	50	nA
Soft start time	t_{SS}			1		ms
EN rising threshold	EN_{Vth-Hi}		1.05	1.35	1.6	V
EN threshold hysteresis	$EN_{Vth-Hys}$			500		mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0V		0		
Power-good rising threshold	PG_{Vth-Hi}	Power-good		90		%
Power-good falling threshold	PG_{Vth-Lo}	Fault condition		85		%
Power-good delay	PGTd			500		μs
Power-good sink current	I_{PG}	PG = 0.4V		4		mA
Power-good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			10	nA
VIN under-voltage lockout threshold rising	$INUV_{Vth}$				3.1	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			300		mV
Thermal shutdown (5)	T_{SD}			150		°C
Thermal shutdown hysteresis (5)	T_{SD-HYS}			25		°C

Note:
5) Guaranteed by design.

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PIN FUNCTIONS

QFN12 (2x3mm) Pin #	Name	Description
9	IN	Supply Voltage. The MP28257 operates from a 4.2V to 20V input rail. C1 decouples the input rail. Use wide PCB traces and multiple vias to make the connection.
1, 11, 12	GND	System Ground. Reference ground for the regulated output voltage. These pins require special consideration during PCB layout.
2, 10, Exposed Pad	SW	Switch Output. Connect with wide PCB traces.
3	BST	Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
4	VCC	Internal Bias Supply. Decouple with a 1μF ceramic capacitor as close to the pin as possible.
5	EN	EN = 1 to enable the MP28257. For automatic start-up, connect EN pin to VIN with a pull-up resistor.
7	FB	Feedback. Sets the output voltage when connected to the tap of an external resistor divider, connected between output and GND.
8	FREQ	Frequency. Set during CCM operation. Connect a resistor R7 to IN to set the switching frequency. Decouple with a 1nF capacitor.
6	PG	Power-Good Output. The output of this pin is an open drain that goes high if the output voltage is higher than 90% of the nominal voltage. There is a 0.5ms delay between when the feedback exceeds 90% to when the PG pin goes high.

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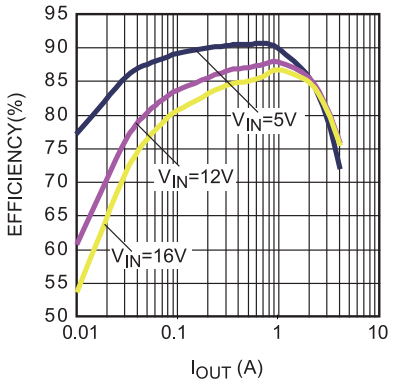
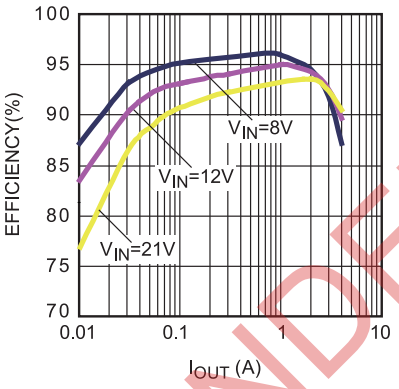
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 2μH, T_A = 25°C, unless otherwise noted.

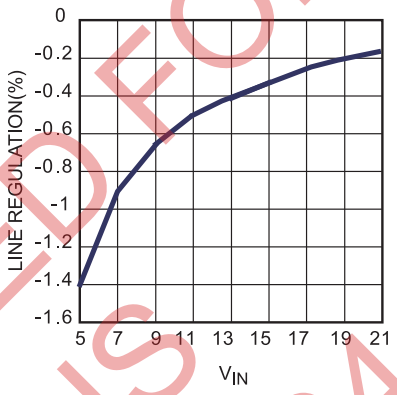
Efficiency vs. Load Current
F_{SW}=500kHz



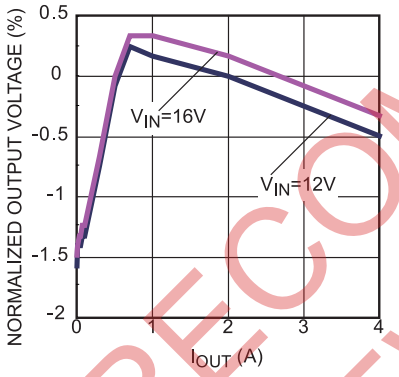
Efficiency vs. Load Current
V_{OUT}=5V, F_{SW}=550kHz, L=3.3μH



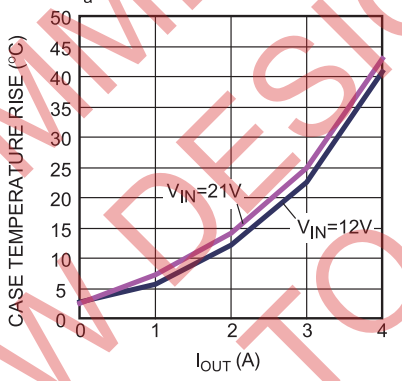
Line Regulation
I_{OUT}=4A



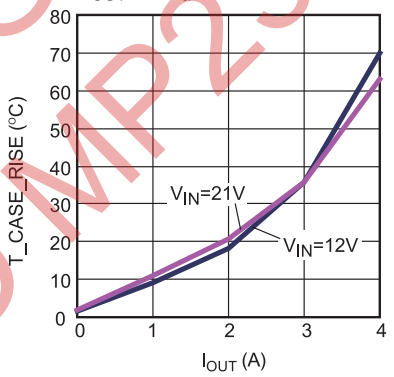
Load Regulation



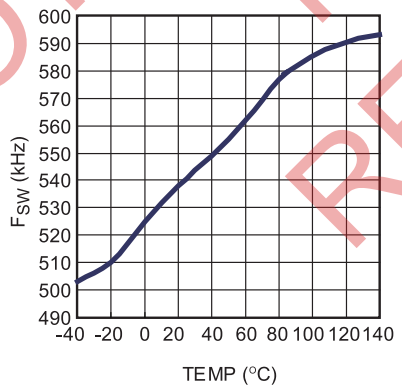
Case Temp Rise
T_a=+27.4°C



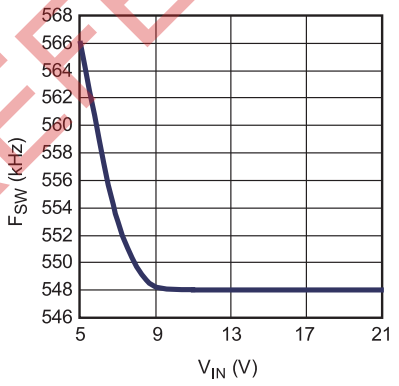
Case Temp Rise
V_{OUT}=5V, T_a=+27.4°C



Frequency vs. Temperature
RF_{SW}=274kΩ, I_{OUT}=4A



Frequency vs. Input Voltage
RF_{SW}=274kΩ, I_{OUT}=4A



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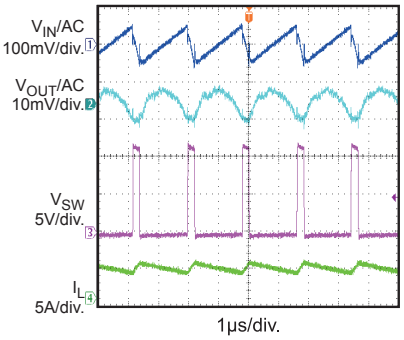
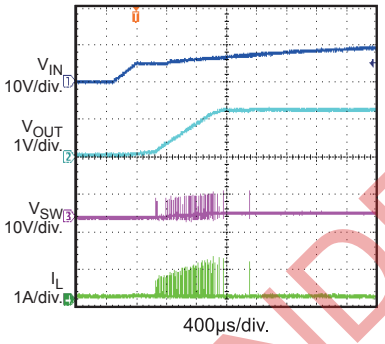
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 2μH, T_A = 25°C, unless otherwise noted.

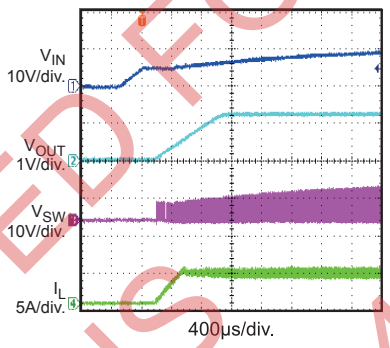
Input/Output Voltage Ripple
I_{OUT} = 4A



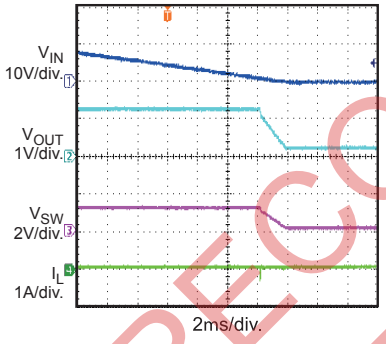
Start up through VIN
I_{OUT} = 0A



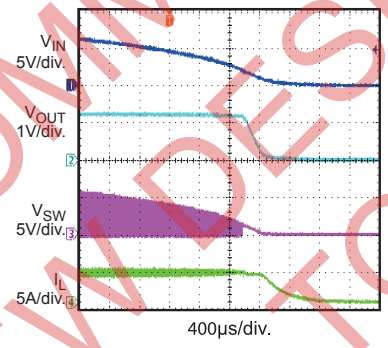
Start up through VIN
I_{OUT} = 4A



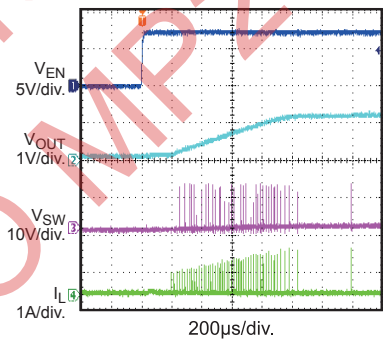
Shutdown through VIN
I_{OUT} = 0A



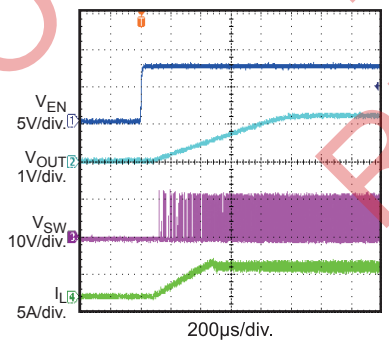
Shutdown through VIN
I_{OUT} = 4A



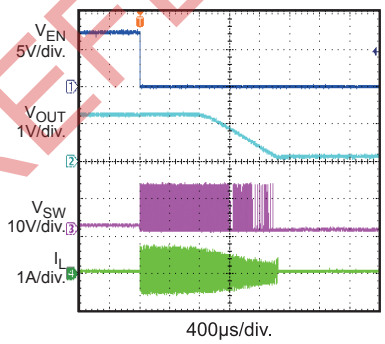
Start up through EN
I_{OUT} = 0A



Start up through EN
I_{OUT} = 4A



Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
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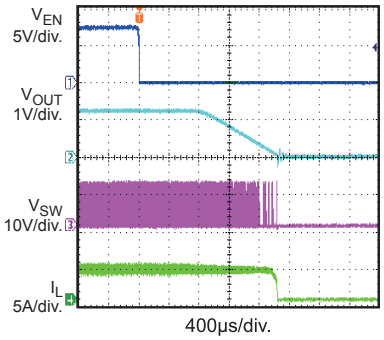

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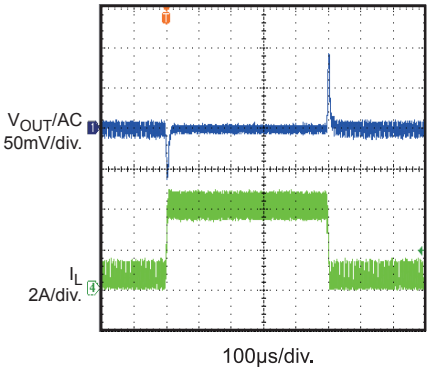
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 2μH, T_A = 25°C, unless otherwise noted.

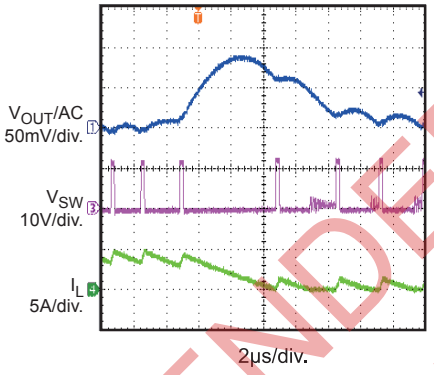
Transient

I_{OUT} = 0.4A~4A @ 2.5A/μs
F_{SW}=500kHz, C_{OUT}=2*22μF



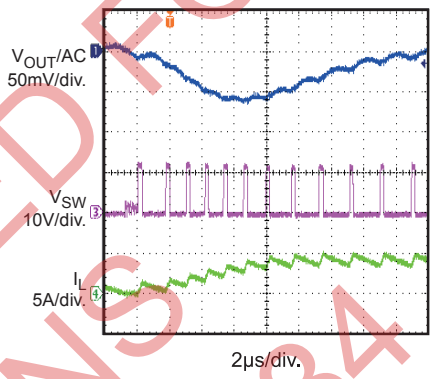
Transient

I_{OUT} = 0.4A~4A @ 2.5A/μs
F_{SW}=500kHz, C_{OUT}=2*22μF



Transient

I_{OUT} = 0.4A~4A @ 2.5A/μs
F_{SW}=500kHz, C_{OUT}=2*22μF



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BLOCK DIAGRAM

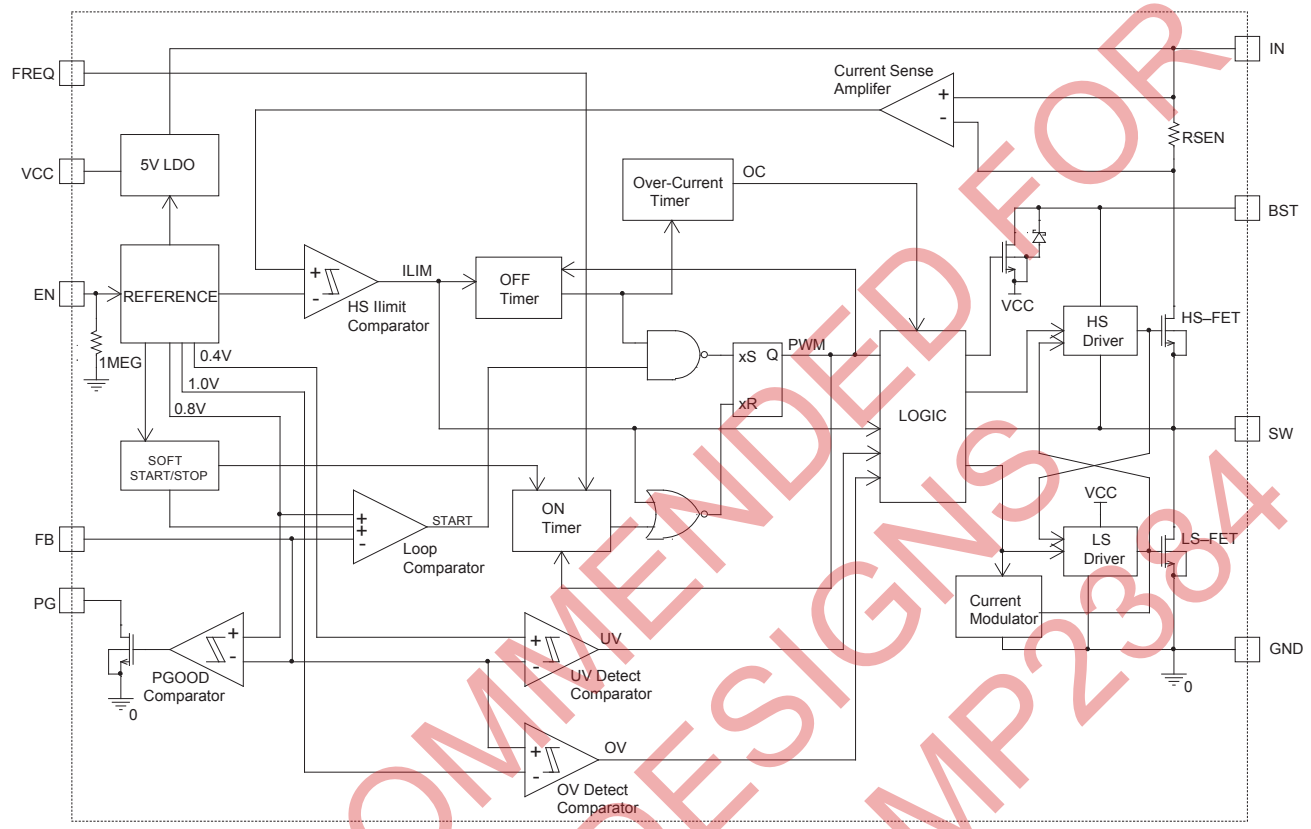

Figure 1: Functional Block Diagram

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OPERATION

PWM Operation

The MP28257 is a fully-integrated, synchronous, rectified, step-down switch converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON whenever the feedback voltage (V_{FB}) is lower than the reference voltage (V_{REF})—a low V_{FB} indicates insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$t_{ON}(ns) = \frac{9.3 \times R_7(k\Omega)}{V_{IN}(V) - 0.4} + 40ns \qquad (1)$$

After the ON period elapses, the HS-FET enters the OFF state. By cycling the HS-FET between the ON and OFF states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its OFF state to minimize the conduction loss.

Shoot-through occurs when there is both the HS-FET and LS-FET are turned on at the same time, causing a dead short between input and GND. Shoot-through dramatically reduces efficiency, and the MP28257 avoids this by internally generating a dead-time (DT) between when the HS-FET is off and the LS-FET is on, and when the LS-FET is off and the HS-FET is on. The device enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

Heavy-Load Operation

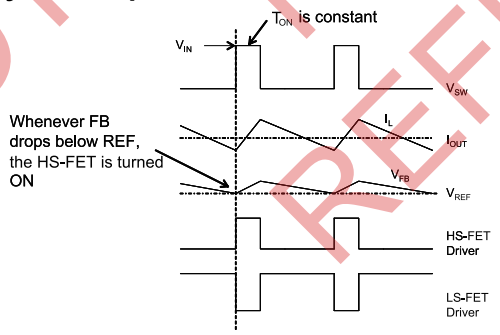

Figure 2: Heavy-Load Operation

During heavy-load operation—when the output current is high—the MP28257 enters continuous-conduction mode (CCM) where the HS-FET and LS-FET repeat the on/off operation described for PWM operation, the inductor current never goes to zero, and the switching frequency (f_{SW}) is fairly constant. Figure 2 shows the timing diagram during this operation.

Light-Load Operation

During light-load operation—when the output current is low—the MP28257 automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops near zero.. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z). The current modulator controls the LS-FET and limits the inductor current to around -1mA as shown in Figure 3. Hence, the output capacitors discharge slowly to GND through LS-FET, R_1, and R_2. This operation greatly improves device efficiency when the output current is low.

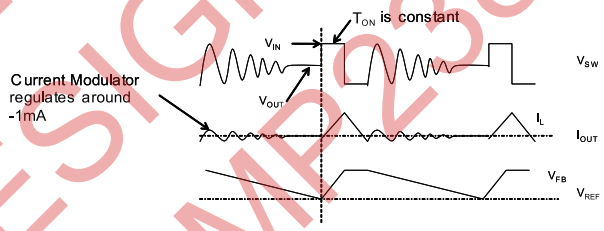

Figure 3: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current—as the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero, and can be determined using the following equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \qquad (2)$$

The device reverts to PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

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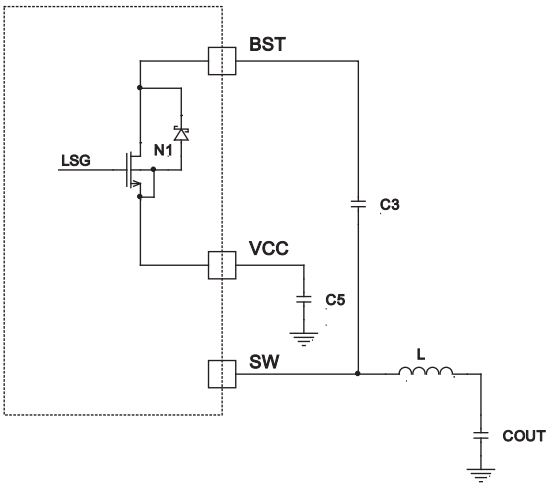

Figure 4: Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. The bootstrap capacitor is charges from VCC through N1 (Figure 4): N1 turns on when the LS-FET turns on, and turns off when the LS-FET turns off.

Switching Frequency

The MP28257 uses COT control because there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R_7. The duty ratio is kept as V_{OUT}/V_{IN}, and the switching frequency is fairly constant over the input voltage range. The switching frequency can be determined with the following equation:

$$f_{SW}(kHz) = \frac{10^6}{\frac{9.3 \times R_7(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + t_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay, and equals approximately 40ns.

The MP28257 is optimized to operate at a high switching frequency a high efficiency. The high switching frequency makes it possible to use small-sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope

Jitter occurs in both PWM and skip modes when noise in the V_{FB} ripple propagates a delay to the HS-FET driver, as shown in Figures 5 and 6. Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope. However, V_{FB} ripple does not directly affect noise immunity.

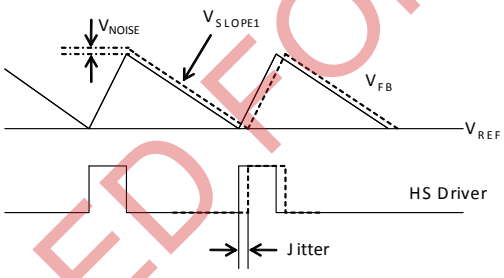

Figure 5—Jitter in PWM Mode

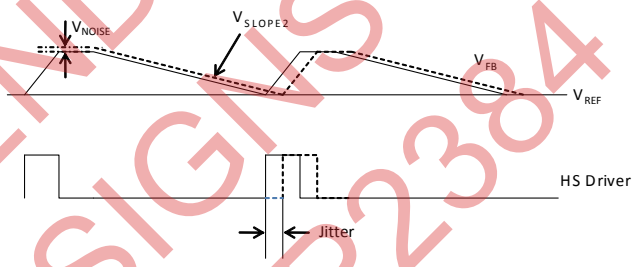

Figure 6—Jitter in Skip Mode

Ramp with Large ESR Cap

In the case of POSCAP or other types of capacitor with larger ESR is applied as output capacitor. The ESR ripple dominates the output ripple, and the slope on the FB is quite ESR related. Figure 7 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Turn to application information section for design steps with large ESR caps.

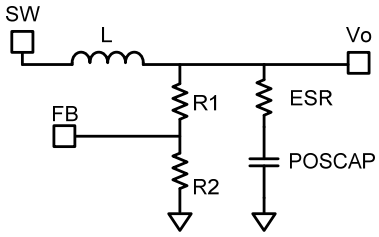

Figure 7—Simplified Circuit in PWM Mode without External Ramp Compensation

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To realize the stability when no external ramp is used, usually the ESR value should be chosen as follow:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}}{C_{OUT}} \quad (4)$$

T_{SW} is the switching period.

Ramp with small ESR Cap

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with small ESR caps

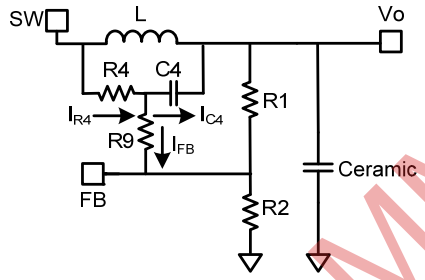

Figure 8—Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 8 shows a simplified external ramp compensation (R4 and C4) for PWM mode, with HS-FET off. Chose R1, R2, R9 and C4 of the external ramp to meet the following condition:

$$\frac{1}{2\pi\times F_{SW}\times C_4} < \frac{1}{5}\times\left(\frac{R_1\times R_2}{R_1+R_2}+R_9\right) \quad (5)$$

where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

And the Vramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN}-V_{OUT}}{R_4\times C_4}\times T_{ON}\times\frac{R_1//R_2}{R_1//R_2+R_9} \quad (7)$$

The downward slope of the V_{FB} ripple then follows

$$V_{SLOPE1} = \frac{-V_{RAMP}}{T_{off}} = \frac{-V_{OUT}}{R_4\times C_4} \quad (8)$$

As can be seen from equation 8, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to limitation from equation 5, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be design follow equation 9.

$$-V_{slope1} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}-R_{ESR}C_{OUT}}{2\times L\times C_{OUT}}V_{OUT}+\frac{Io\times10^{-3}}{T_{SW}-T_{on}} \quad (9)$$

Io is the load current.

In skip mode, the downward slope of the V_{FB} ripple is the same whether the external ramp is used or not. Figure9 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.

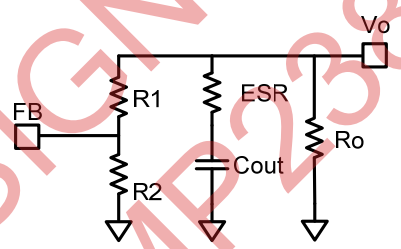

Figure 9—Simplified Circuit in skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as follow:

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1+R_2)//Ro)\times C_{OUT}} \quad (10)$$

where Ro is the equivalent load resistor.

As described in Figure 6, V_{SLOPE2} in the skip mode is lower than that is in the PWM mode, so it is reasonable that the jitter in the skip mode is larger. If one wants a system with less jitter during light load condition, the values of the V_{FB} resistors should not be too big, however, that will decrease the light load efficiency.

When using a large-ESR capacitor on, the output, add a ceramic capacitor with a value of 10uF or less to in parallel to minimize the effect of ESL.

Soft Start/Stop

MP28257 employs a soft-start/stop (SS) mechanism to ensure a smooth output during power up and power shut-down. When the EN pin goes high, the internal SS voltage slowly ramps up. The output voltage smoothly ramps up with the SS voltage. Once SS voltage rises

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above the V_{REF}, it continues to ramp up while the PWM comparator only compares the V_{REF} and the FB voltage. At this point, the soft-start finishes and it enters steady state operation. The SS time is set about 1ms internally.

When the EN pin goes low, an internal current source discharges the internal SS voltage. Once the SS voltage falls below the V_{REF}, the PWM comparator will only compare the V_{REF} to the SS voltage. The output voltage then decreases smoothly with the SS voltage until the voltage level zeros out.

Power-Good (PG)

The PG pin is the open drain of a MOSFET that connects to VCC or some other voltage source through a resistor (e.g.. 100kΩ). The MOSFET turns on with the application of an input voltage so that the PG pin is pulled to GND before SS is ready. After FB voltage reaches 90% of V_{REF}, the PG pin is pulled high after a 0.5ms delay.

When the FB voltage drops to 70% of V_{REF}, the PG pin will be pulled low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MP28257 has cycle-by cycle over-current limit control. It monitors the inductor current during the ON state. Once the inductor current exceeds the current limit, the HS-FET turns off and the OCP timer—set at 50μs—starts. The OCP triggers. If the inductor current reaches or exceeds the current limit every cycle if in those the 50μs, the device enters latch-off mode

The MP28257 SCP triggers when dead shorts occur—when the inductor current exceeds the current limit and the FB voltage is lower than 50% of the V_{REF}—and will trigger the OCP. The MP28257 needs power cycle to restart after it triggers OCP or SCP.

Over/Under-Voltage Protection (OVP/UVP)

MP28257 monitors the output voltage through a resistor-divided FB voltage to detect over- and under-voltage on the output. When the FB voltage is higher than 125% of the V_{REF}, it triggers the OVP. Once it triggers the OVP, the LS-FET is always on while the HS-FET is off. It needs to power cycle to turn on again. Conversely, the UVP triggers when the FB voltage falls below 50% of V_{REF} (0.815V). Usually UVP accompanies a drop in the current limit and this results in SCP.

UVLO Protection

MP28257 has under-voltage lock-out (UVLO) protection. The MP28257 powers up when the input voltage exceeds the UVLO rising threshold voltage. It shuts off when the input voltage falls below the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown

The MP28257 employs thermal shutdown by internally monitoring the junction temperature of the IC. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is non-latch protection. There is about 25°C hysteresis. Once the junction temperature drops around 125°C, it initiates a soft start.

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APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

For applications that electrolytic capacitor or POS capacitor with a controlled output of ESR is set as output capacitors. The output voltage is set by feedback resistors R1 and R2. As Figure 10 shows.

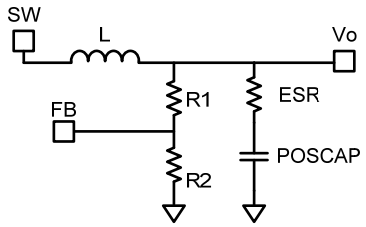

Figure10—Simplified Circuit of POS Capacitor

First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low, etc.,1.05V, and a smaller R2 when Vo is high. Then R1 is determined as follow with the output ripple considered:

$$R_1 = \frac{V_{OUT} - \frac{1}{2}\Delta V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \qquad (11)$$

ΔV_{OUT} is the output ripple determined by equation 20.

Setting the Output Voltage-Small ESR Caps

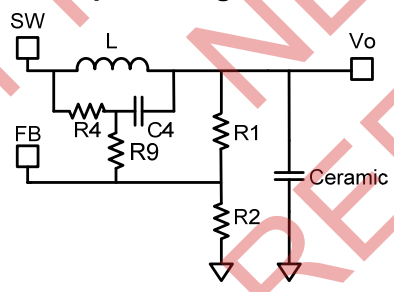

Figure11—Simplified Circuit of Ceramic Capacitor

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4.The output voltage is influenced by ramp voltage V_{RAMP} besides R divider as shown in Figure 11. The V_{RAMP} can be calculated as shown in equation 7. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low, etc.,1.05V, and a smaller R2 when Vo is high. And the value of R1 then is determined as follow:

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{(V_{OUT}-V_{FB(AVG)})} - \frac{R_2}{R_4+R_9}} \qquad (12)$$

The $V_{FB(AVG)}$ is the average value on the FB, $V_{FB(AVG)}$ varies with the Vin, Vo, and load condition, etc., its value on the skip mode would be lower than that of the PWM mode, which means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$,If one wants to gets a better load or line regulation, a lower Vramp is suggested once it meets equation 9.

For PWM operation, $V_{FB(AVG)}$ value can be deduced from equation 13.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2}V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \qquad (13)$$

Usually, R9 is set to 0Ω, and it can also be set following equation 14 for a better noise immunity. It should also set to be 5 timers smaller than R1//R2 to minimize its influence on Vramp.

$$R_9 = \frac{1}{2\pi \times C_4 \times 2F_{SW}} \qquad (14)$$

Using equation 12 to calculate the output voltage can be complicated. To simplify the calculation of R1 in equation 12, a DC-blocking capacitor Cdc can be added to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 15 for PWM mode operation.

$$R_1 = \frac{(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} R_2 \qquad (15)$$

Cdc is suggested to be at least 10 times larger than C4 for better DC blocking performance, and should also not larger than 0.47uF considering start up performance. In case one wants to use

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larger Cdc for a better FB noise immunity, combined with reduced R1 and R2 to limit the Cdc in a reasonable value without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still Vramp related.

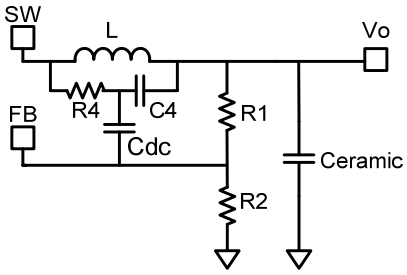

Figure12—Simplified Circuit of Ceramic Capacitor with DC blocking capacitor

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the V_{IN} pin as possible. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (16)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (17)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (19)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (20)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (21)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equation 5, 8 and 9.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value around 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (22)$$

Maximum output capacitor limitation should be also considered in design application. MP28258 has an around 1ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{o_max} can be limited approximately by:

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (23)$$

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Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (24)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

Recommend Design Example

Some design examples and recommended maximum output capacitor value with typical outputs are provided below when the ceramic capacitors is applied with R9=0ohm:

Table 1: 1.2V VOUT (L = 2μH)

V_{IN} (V)	V_{OUT} (V)	C1	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	1.2	10μF*1	300k	499k	220p	12.1k	24.3k	450k
5	1.2	10μF*1	300k	390k	220p	12.1k	24.3k	440k
3.3	1.2	10μF*1	300k	243k	220p	12.1k	24.3k	435k

Table 2: 1.8V VOUT (L = 2μH)

V_{IN} (V)	V_{OUT} (V)	C1	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	1.8	10μF*1	402k	499k	220p	30.1k	24.3k	480k
5	1.8	10μF*1	402k	390k	220p	30.1k	24.3k	460k
3.3	1.8	10μF*2	402k	280k	220p	30.1k	24.3k	450k

Note: For 1.8V V_{OUT} from 3.3V V_{IN}, a larger C1 is recommended to sustain maximum 4A load.

Table 3: 2.5V VOUT (L = 4.2μH)

V_{IN} (V)	V_{OUT} (V)	C1	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	2.5	10μF*1	500k	453k	390p	21.5k	10k	500k
5	2.5	10μF*1	500k	453k	390p	21.5k	10k	500k

Table 4: 3.3V VOUT (L = 6.5μH)

V_{IN} (V)	V_{OUT} (V)	C1	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	3.3	10μF*1	680k	470k	330p	31.6k	10k	500k
5	3.3	10μF*1	680k	470k	330p	31.6k	10k	500k

Table 5: 5V VOUT (L = 8.8μH)

V_{IN} (V)	V_{OUT} (V)	C1	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
12	5	10μF*1	1M	750k	330p	53.6k	10k	500k

The detailed application schematic is shown in Figure 13 when large ESR caps are used, and Figure14 and Figure 15 when low ESR caps are applied. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

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Typical Application Schematic

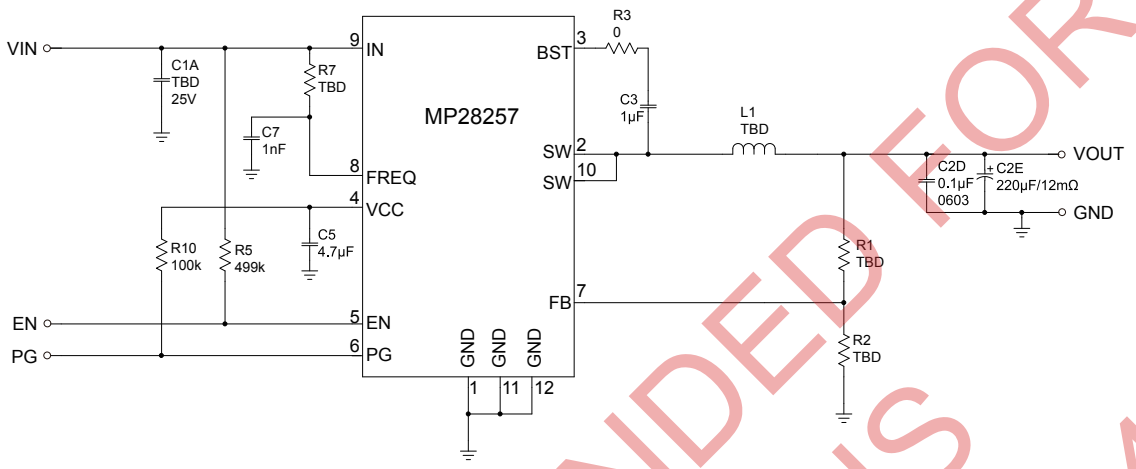

Figure 13—Typical Application Schematic with No External Ramp

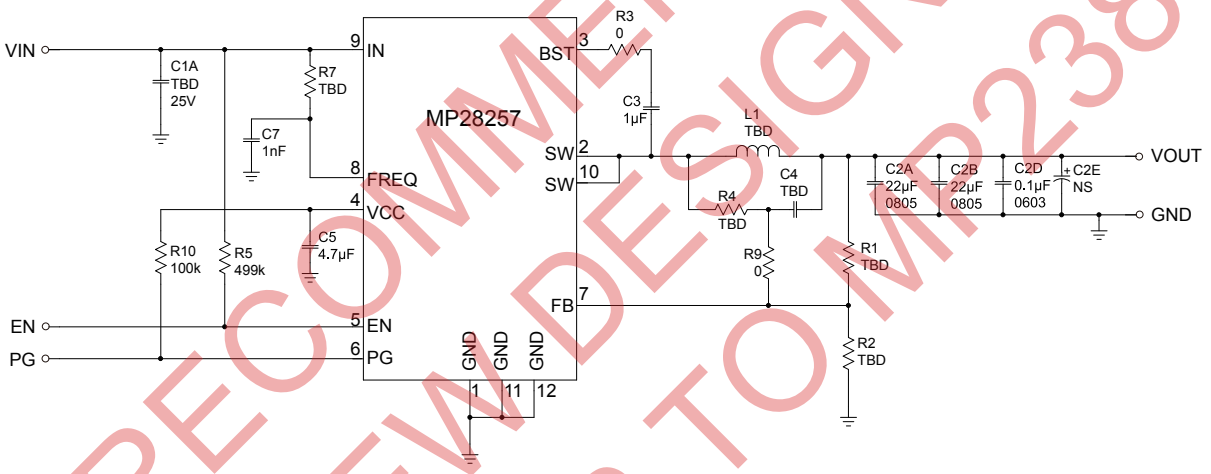

Figure 14—Typical Application Schematic with Low ESR Ceramic Capacitor

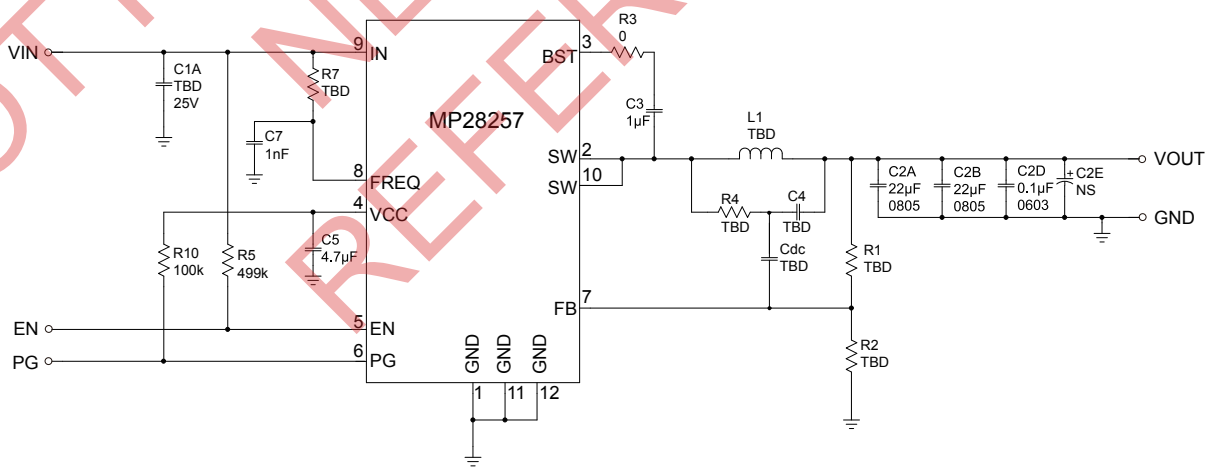

Figure 15—Typical Application Schematic with Low ESR Ceramic Capacitor\ and DC Blocking Capacitor.

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Layout Recommendation

1) The high current paths (GND, IN, and SW) should be placed very close to the device with short, wide, and direct traces.
2) Put the input capacitors as close to the IN and GND pins as possible.
3) Put the decoupling capacitor as close to the V_{CC} and GND pins as possible.
4) Keep the switching node SW short and away from the feedback network.
5) The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.
6) Keep the BST voltage path (BST, C3, and SW) as short as possible.
7) Four-layer layout is recommended to achieve better thermal performance.

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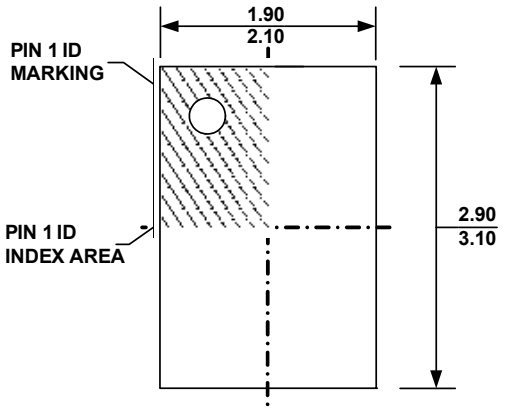
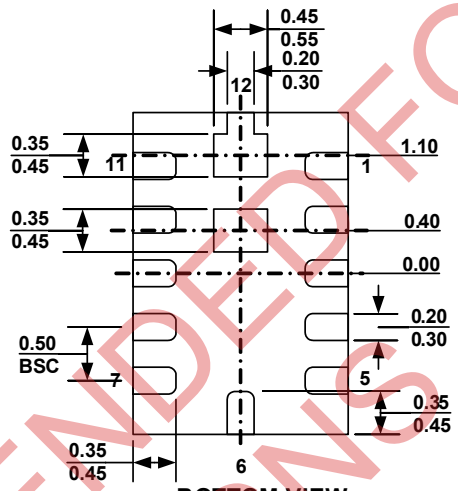
PACKAGE INFORMATION

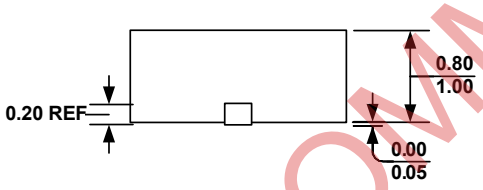
QFN12 (2x3mm)



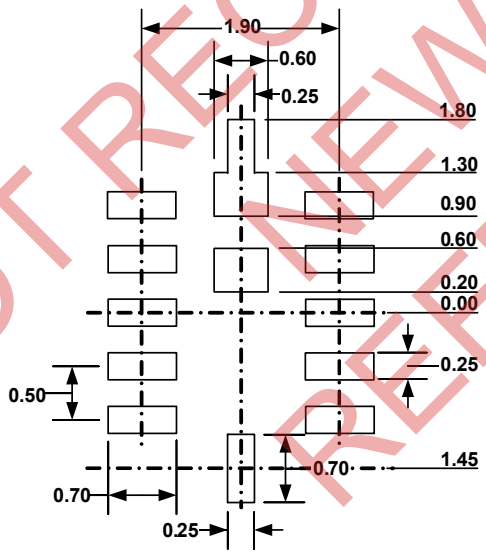
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
4) JEDEC REFERENCE DRAWING IS JEDEC MO-220
5) DRAWING IS NOT TO SCALE

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