# 500 MHz, Triple 16 × 9 Video Crosspoint Switch

Data Sheet

# AD8175

## FEATURES

- High channel count, triple 16 × 9 high speed, non-blocking switch array
- Differential or single-ended operation
- Supports sync-on common-mode and sync-on color operating modes
- Decoded HV sync outputs available
- G = +2 operation (differential input to differential output)
- Flexible power supplies: +5 V or ±2.5 V
  - Logic ground for convenient control interface
- Serial or parallel programming of switch array
- High impedance output disable allows connection of multiple devices with minimal loading on output bus
- Adjustable output CM and black level through external pins
- Excellent ac performance (to support 1600 × 1200 @ 85 Hz)
  - Bandwidth: 500 MHz
  - Slew rate: 1800 V/µs
  - Settling time: 4 ns to 1%
- Low power of 3.5 W
- Low all-hostile crosstalk
  - −88 dB @ 5 MHz
  - −46 dB @ 500 MHz
- Wide input common-mode range of 4 V
- Reset pin allows disabling of all outputs
- Fully populated 26 x 26 ball PBGA package (27 mm x 27 mm, 1 mm ball pitch)
- Convenient grouping of RGB signals for easy routing

## APPLICATIONS

- RGB video switching
- KVM
- Professional video

## FUNCTIONAL BLOCK DIAGRAM

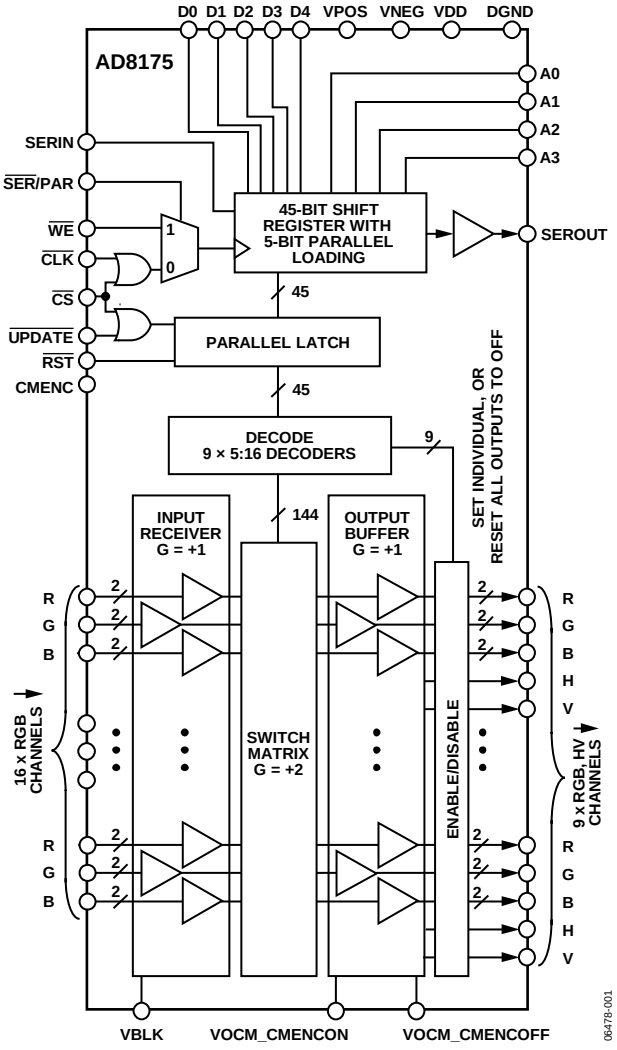



*Figure 1.*

## GENERAL DESCRIPTION

The AD8175 is a high speed, triple 16 × 9 video crosspoint switch matrix. It supports 1600 × 1200 RGB displays @ 85 Hz refresh rate, by offering a 500 MHz bandwidth and a slew rate of 1800 V/µs. With −88 dB of crosstalk and −94 dB isolation (@ 5 MHz), the AD8175 is useful in many high speed video applications.

The AD8175 supports two modes of operation: differential-in to differential-out mode with sync-on CM signaling passed through the switch and differential-in to differential-out mode with CM signaling removed through the switch. The output CM and black level can be conveniently set via external pins.

The independent output buffers of the AD8175 can be placed into a high impedance state to create larger arrays by paralleling crosspoint outputs. Inputs can be paralleled as well. The AD8175 offers both serial and parallel programming modes.

The AD8175 is packaged in a fully-populated 26 × 26 ball PBGA package and is available over the extended industrial temperature range of −40°C to +85°C.

**Rev. B**

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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# TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Timing Characteristics (Serial Mode) ... 5
Timing Characteristics (Parallel Mode) ... 6
Absolute Maximum Ratings ... 7
Thermal Resistance ... 7
Power Dissipation ... 7
ESD Caution ... 7
Pin Configuration and Function Descriptions ... 8
Truth Table and Logic Diagram ... 17
Equivalent Circuits ... 19
Typical Performance Characteristics ... 21
Theory of Operation ... 26
Applications ... 27
Operating Modes ... 27
Programming ... 28
Differential and Single-Ended Operation ... 30
Outline Dimensions ... 39
Ordering Guide ... 39

## REVISION HISTORY

**10/11—Rev. A to Rev. B**

Changes to Table 15 ... 17
Changes to Parallel Programming Description Section ... 29

**2/09—Rev. 0 to Rev. A**

Updated Outline Dimensions ... 39

**5/07—Revision 0: Initial Version**

# SPECIFICATIONS

$V_S$ = ±2.5 V at $T_A$ = 25°C, G = +2, $R_L$ = 100 Ω (each output), VBLK = 0 V, output CM voltage = 0 V, differential I/O mode, unless otherwise noted.

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | 200 mV p-p | | 500 | | MHz |
| | 2 V p-p | | 450 | | MHz |
| Gain Flatness | 0.1 dB, 200 mV p-p | | 25 | | MHz |
| Propagation Delay | 2 V p-p | | 1.3 | | ns |
| Settling Time | 1% , 2 V step | | 4 | | ns |
| Slew Rate, Differential Output | 2 V step | | 1800 | | V/µs |
| | 2 V step, 10% to 90% | | 1500 | | V/µs |
| Slew Rate, RGB Common Mode | 1 V step, 10% to 90% | | 300 | | V/µs |
| Slew Rate, HV Outputs | Rail-to-rail, TTL load | | 400 | | V/µs |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Crosstalk, All Hostile | $f$ = 5 MHz | | −88 | | dB |
| | $f$ = 10 MHz | | −82 | | dB |
| | $f$ = 100 MHz | | −58 | | dB |
| | $f$ = 500 MHz | | −46 | | dB |
| Off Isolation, Input-Output | $f$ = 5 MHz, $R_L$ = 100 Ω, one channel | | −94 | | dB |
| Input Voltage Noise | 0.01 MHz to 100 MHz | | 40 | | nV/√Hz |
| DC PERFORMANCE | | | | | |
| Gain Error | | | 1 | | % |
| Gain Matching | R, G, B same channel | | 0.5 | | % |
| Gain Temperature Coefficient | | | 40 | | ppm/°C |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Offset Voltage | CMENC on or off | | 10 | | mV |
| | Temperature coefficient | | 31 | | µV/°C |
| Output Offset Voltage, RGB Common Mode | CMENC on or off | | 10 | | mV |
| | Temperature coefficient | | −7.6 | | µV/°C |
| Output Impedance | Enabled, differential | | 1.5 | | Ω |
| | Disabled, differential | | 2.7 | | kΩ |
| Output Disable Capacitance | Disabled | | 2 | | pF |
| Output Leakage Current | Disabled | | 1 | | µA |
| Output Voltage Range | No load, differential | | | 4 | V p-p |
| Output Current | Short circuit | | 45 | | mA |
| INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range, Differential Mode | | 1 | 1.2 | | V p-p |
| Input Voltage Range, Common Mode | $V_{IN}$ = 1 V p-p, differential | | ±2.25 | | V |
| CMR, RGB Input | $\Delta V_{OUT, DM}/\Delta V_{IN, CM}$, $\Delta V_{IN, CM}$ = ±0.5 V, CMENC off | | −62 | | dB |
| | $\Delta V_{OUT, DM}/\Delta V_{IN, CM}$, $\Delta V_{IN, CM}$ = ±0.5 V, CMENC on | | −45 | | dB |
| CM Gain, RGB Input | $\Delta V_{OUT, CM}/\Delta V_{IN, CM}$, $\Delta V_{IN, CM}$ = ±0.5 V CMENC off | | −70 | | dB |
| | $\Delta V_{OUT, CM}/\Delta V_{IN, CM}$, $\Delta V_{IN, CM}$ = ±0.5 V, CMENC on | | 0 | | dB |
| Input Capacitance | Any switch configuration | | 2 | | pF |
| Input Resistance | Differential | | 3.33 | | kΩ |
| Input Offset Current | | | 1 | | µA |

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SWITCHING CHARACTERISTICS | | | | | |
| Enable On Time | 50% $\overline{\text{UPDATE}}$ to 50% output | | 80 | | ns |
| Switching Time, 2 V Step | 50% $\overline{\text{UPDATE}}$ to 50% output | | 70 | | ns |
| POWER SUPPLIES | | | | | |
| Supply Current | VPOS, outputs enabled, no load | | 600 | | mA |
| | Outputs disabled | | 290 | | mA |
| | VNEG, outputs enabled, no load | | 600 | | mA |
| | Outputs disabled | | 290 | | mA |
| | DVDD, outputs enabled, no load | | 4 | | mA |
| Supply Voltage Range | VPOS − VNEG | | 4.5 to 5.5 | | V |
| | VDD to DGND | | 3.3 to 5.5 | | V |
| PSR | $\Delta V_{OUT, DM}/\Delta V_{POS}$, $\Delta V_{POS}$ = ±0.5 V | | −55 | | dB |
| | $\Delta V_{OUT, DM}/\Delta V_{NEG}$, $\Delta V_{NEG}$ = ±0.5 V | | −55 | | dB |
| OPERATING TEMPERATURE RANGE | | | | | |
| Temperature Range | Operating (still air) | | −40 to +85 | | °C |
| $\theta_{JA}$ | Operating (still air) | | 15 | | °C/W |

## TIMING CHARACTERISTICS (SERIAL MODE)

Specifications subject to change without notice.

**Table 2.**

| Parameter | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Serial Data Setup Time | $t_1$ | 40 | | | ns |
| $\overline{\text{CLK}}$ Pulse Width | $t_2$ | 60 | | | ns |
| Serial Data Hold Time | $t_3$ | 50 | | | ns |
| $\overline{\text{CLK}}$ Pulse Separation | $t_4$ | 140 | | | ns |
| $\overline{\text{CLK}}$ to $\overline{\text{UPDATE}}$ Delay | $t_5$ | 10 | | | ns |
| $\overline{\text{UPDATE}}$ Pulse width | $t_6$ | 90 | | | ns |
| $\overline{\text{CLK}}$ to SEROUT Valid | $t_7$ | 120 | | | ns |
| Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On | | | 80 | | ns |
| Data Load Time, $\overline{\text{CLK}}$ = 5 MHz, Serial Mode | | 9 | | | µs |
| $\overline{\text{RST}}$ Time | | | 140 | 200 | ns |

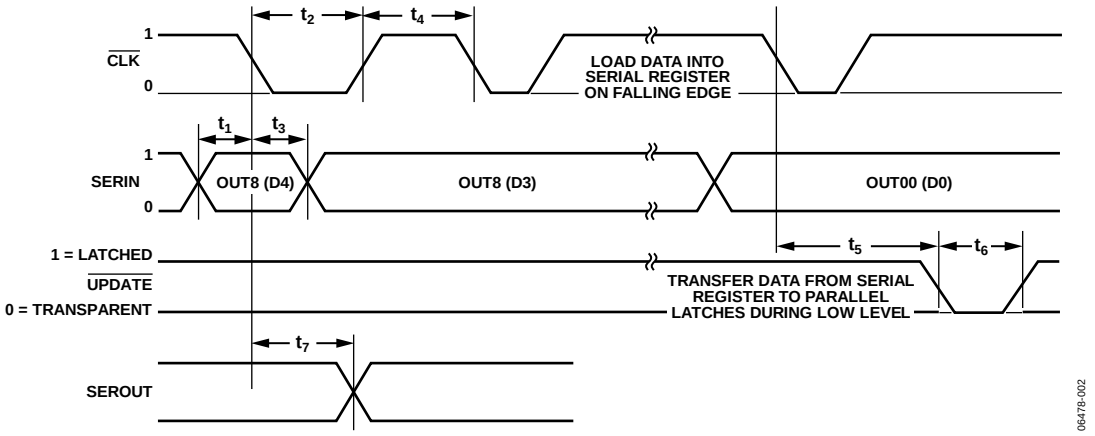



*Figure 2. Timing Diagram, Serial Mode*

**Table 3. Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{IH}$ | $V_{IL}$ | $V_{OH}$ | $V_{OL}$ | $I_{IH}$ | $I_{IL}$ | $I_{OH}$ | $I_{OL}$ |
|---|---|---|---|---|---|---|---|
| $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, SERIN, $\overline{\text{UPDATE}}$ | $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, SERIN, $\overline{\text{UPDATE}}$ | SEROUT | SEROUT | $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, SERIN, $\overline{\text{UPDATE}}$ | $\overline{\text{SER}}$/PAR, $\overline{\text{CLK}}$, SERIN, $\overline{\text{UPDATE}}$ | SEROUT | SEROUT |
| 2.0 V min | 0.6 V max | 2.8 V min | 0.4 V max | 20 µA max | –20 µA max | –1 mA min | 1 mA min |

**Table 4. H and V Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{OH}$ | $V_{OL}$ | $I_{OH}$ | $I_{OL}$ |
|---|---|---|---|
| 2.7 V min | 0.5 V max | –3 mA max | 3 mA max |

**Table 5. $\overline{\text{RST}}$ Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{IH}$ | $V_{IL}$ | $I_{IH}$ | $I_{IL}$ |
|---|---|---|---|
| 2.0 V min | 0.6 V max | –60 µA max | –120 µA max |

**Table 6. $\overline{\text{CS}}$ Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{OH}$ | $V_{OL}$ | $I_{IH}$ | $I_{OL}$ |
|---|---|---|---|
| 2.0 V min | 0.6 V max | 100 µA max | 40 µA max |

## TIMING CHARACTERISTICS (PARALLEL MODE)

Specifications subject to change without notice.

**Table 7.**

| Parameter | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Parallel Data Setup Time | $t_1$ | 80 | | | ns |
| $\overline{WE}$ Pulse Width | $t_2$ | 110 | | | ns |
| Parallel Hold Time | $t_3$ | 150 | | | ns |
| $\overline{WE}$ Pulse Separation | $t_4$ | 90 | | | ns |
| $\overline{WE}$ to $\overline{UPDATE}$ Delay | $t_5$ | 10 | | | ns |
| $\overline{UPDATE}$ Pulse Width | $t_6$ | 90 | | | ns |
| Propagation Delay, $\overline{UPDATE}$ to Switch On | | | 80 | | ns |
| $\overline{RST}$ Time | | | 140 | 200 | ns |

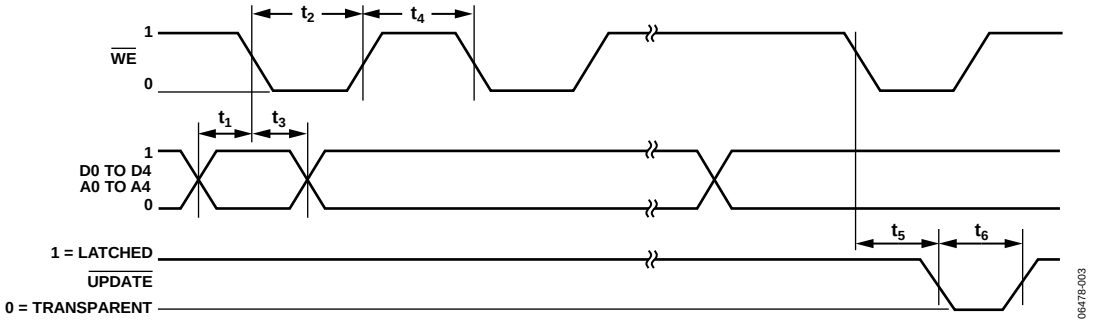



*Figure 3. Timing Diagram, Parallel Mode*

**Table 8. Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{IH}$ | $V_{IL}$ | $V_{OH}$ | $V_{OL}$ | $I_{IH}$ | $I_{IL}$ | $I_{OH}$ | $I_{OL}$ |
|---|---|---|---|---|---|---|---|
| $\overline{SER}$/PAR, $\overline{WE}$, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{UPDATE}$ | $\overline{SER}$/PAR, $\overline{WE}$, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{UPDATE}$ | SEROUT | SEROUT | $\overline{SER}$/PAR, $\overline{WE}$, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{UPDATE}$ | $\overline{SER}$/PAR, $\overline{WE}$, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{UPDATE}$ | SEROUT | SEROUT |
| 2.0 V min | 0.6 V max | Disabled | Disabled | 20 µA max | −20 µA max | Disabled | Disabled |

**Table 9. H and V Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{OH}$ | $V_{OL}$ | $I_{OH}$ | $I_{OL}$ |
|---|---|---|---|
| 2.7 V min | 0.5 V max | −3 mA max | 3 mA max |

**Table 10. $\overline{RST}$ Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{IH}$ | $V_{IL}$ | $I_{IH}$ | $I_{IL}$ |
|---|---|---|---|
| 2.0 V min | 0.6 V max | −60 µA max | −120 µA max |

**Table 11. $\overline{CS}$ Logic Levels, $V_{DD}$ = 3.3 V**

| $V_{OH}$ | $V_{OL}$ | $I_{IH}$ | $I_{OL}$ |
|---|---|---|---|
| 2.0 V min | 0.6 V max | 100 µA max | 40 µA max |

# ABSOLUTE MAXIMUM RATINGS

**Table 12.**

| Parameter | Rating |
|---|---|
| Analog Supply Voltage ($V_{POS}$ – $V_{NEG}$) | +6 V |
| Digital Supply Voltage ($V_{DD}$ – $D_{GND}$) | +6 V |
| Ground Potential Difference ($V_{NEG}$ – $D_{GND}$) | +0.5 V to −2.5 V |
| Maximum Potential Difference ($V_{DD}$ – $V_{NEG}$) | +8 V |
| Common-Mode Analog Input Voltage | ($V_{NEG}$ – 0.5 V) to ($V_{POS}$ + 0.5 V) |
| Differential Analog Input Voltage | ±2 V |
| Digital Input Voltage | $V_{DD}$ |
| Output Voltage (Disabled Analog Output) | ($V_{POS}$ – 1 V) to ($V_{NEG}$ + 1 V) |
| Output Short-Circuit Duration | Momentary |
| Storage Temperature | −65°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (Soldering 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 13. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| PBGA | 15 | °C/W |

## POWER DISSIPATION

The AD8175 is operated with ±2.5 V or +5 V supplies and can drive loads down to 100 Ω, resulting in a large range of possible power dissipations. For this reason, extra care must be taken derating the operating conditions based on ambient temperature.

Packaged in a 676-lead BGA, the AD8175 junction-to-ambient thermal impedance ($\theta_{JA}$) is 15°C/W. For long-term reliability, the maximum allowed junction temperature of the die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. The following curve shows the range of allowed internal die power dissipations that meet these conditions over the −40°C to +85°C ambient temperature range. When using Table 12, do not include external load power in the Maximum Power calculation, but do include load current dropped on the die output transistors.

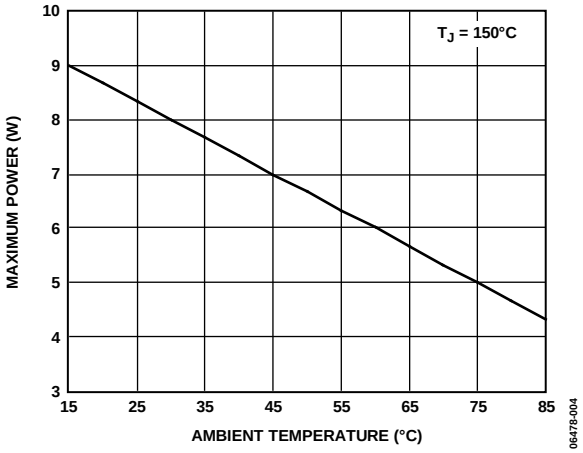



*Figure 4. Maximum Die Power Dissipation vs. Ambient Temperature*

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

| | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VNEG | VNEG | VNEG | OPR7 | ONB7 | VNEG | OPR8 | ONB8 | VPOS | IPR8 | INB8 | VNEG | IPR9 | INB9 | VPOS | IPR10 | INB10 | VNEG | IPR11 | INB11 | VPOS | IPR12 | INB12 | VNEG | VNEG | VNEG | A |
| B | VNEG | VNEG | VNEG | ONR7 | OPB7 | VNEG | ONR8 | OPB8 | VPOS | INR8 | IPB8 | VNEG | INR9 | IPB9 | VPOS | INR10 | IPB10 | VNEG | INR11 | IPB11 | VPOS | INR12 | IPB12 | VNEG | VNEG | VNEG | B |
| C | VNEG | VNEG | VNEG | OPG7 | ONG7 | VNEG | OPG8 | ONG8 | VPOS | IPG8 | ING8 | VNEG | IPG9 | ING9 | VPOS | IPG10 | ING10 | VNEG | IPG11 | ING11 | VPOS | IPG12 | ING12 | VNEG | VNEG | VNEG | C |
| D | VNEG | VNEG | VNEG | H7 | V7 | VPOS | H8 | V8 | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | IPG13 | INR13 | IPR13 | D |
| E | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VPOS | DGND | VDD | SEROUT | $\overline{CS}$ | $\overline{CLK}$ | SERIN | SERIPAR | A3 | A2 | A1 | A0 | VDD | DGND | VPOS | VPOS | ING13 | IPB13 | INB13 | E |
| F | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | F |
| G | ONB6 | OPB6 | ONG6 | V6 | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | G |
| H | OPR6 | ONR6 | OPG6 | H6 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | IPG14 | INR14 | IPR14 | H |
| J | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | ING14 | IPB14 | INB14 | J |
| K | ONB5 | OPB5 | ONG5 | V5 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | K |
| L | OPR5 | ONR5 | OPG5 | H5 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | IPG15 | INR15 | IPR15 | L |
| M | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | ING15 | IPB15 | INB15 | M |
| N | ONB4 | OPB4 | ONG4 | V4 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VOCM_CMENCON | VPOS | VPOS | VPOS | VPOS | N |
| P | OPR4 | ONR4 | OPG4 | H4 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VBLK | VPOS | VPOS | VPOS | VPOS | P |
| R | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VOCM_CMENCOFF | VPOS | IPG7 | INR7 | IPR7 | R |
| T | ONB3 | OPB3 | ONG3 | V3 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | ING7 | IPB7 | INB7 | T |
| U | OPR3 | ONR3 | OPG3 | H3 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | U |
| V | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | IPG6 | INR6 | IPR6 | V |
| W | ONB2 | OPB2 | ONG2 | V2 | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | ING6 | IPB6 | INB6 | W |
| Y | OPR2 | ONR2 | OPG2 | H2 | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | Y |
| AA | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | AA |
| AB | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VPOS | DGND | VDD | $\overline{RST}$ | $\overline{UPDATE}$ | $\overline{WE}$ | CMENC | D4 | D3 | D2 | D1 | D0 | VDD | DGND | VPOS | VPOS | IPG5 | INR5 | IPR5 | AB |
| AC | VNEG | VNEG | VNEG | V1 | H1 | VPOS | V0 | H0 | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | ING5 | IPB5 | INB5 | AC |
| AD | VNEG | VNEG | VNEG | ONG1 | OPG1 | VPOS | ONG0 | OPG0 | VNEG | ING0 | IPG0 | VPOS | ING1 | IPG1 | VNEG | ING2 | IPG2 | VPOS | ING3 | IPG3 | VNEG | ING4 | IPG4 | VNEG | VNEG | VNEG | AD |
| AE | VNEG | VNEG | VNEG | OPB1 | ONR1 | VPOS | OPB0 | ONR0 | VNEG | IPB0 | INR0 | VPOS | IPB1 | INR1 | VNEG | IPB2 | INR2 | VPOS | IPB3 | INR3 | VNEG | IPB4 | INR4 | VNEG | VNEG | VNEG | AE |
| AF | VNEG | VNEG | VNEG | ONB1 | OPR1 | VPOS | ONB0 | OPR0 | VNEG | INB0 | IPR0 | VPOS | INB1 | IPR1 | VNEG | INB2 | IPR2 | VPOS | INB3 | IPR3 | VNEG | INB4 | IPR4 | VNEG | VNEG | VNEG | AF |
| | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

06478-005

*Figure 5. Package Bottom View*

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VNEG | VNEG | VNEG | INB12 | IPR12 | VPOS | INB11 | IPR11 | VNEG | INB10 | IPR10 | VPOS | INB9 | IPR9 | VNEG | INB8 | IPR8 | VPOS | ONB8 | OPR8 | VNEG | ONB7 | OPR7 | VNEG | VNEG | VNEG | A |
| B | VNEG | VNEG | VNEG | IPB12 | INR12 | VPOS | IPB11 | INR11 | VNEG | IPB10 | INR10 | VPOS | IPB9 | INR9 | VNEG | IPB8 | INR8 | VPOS | OPB8 | ONR8 | VNEG | OPB7 | ONR7 | VNEG | VNEG | VNEG | B |
| C | VNEG | VNEG | VNEG | ING12 | IPG12 | VPOS | ING11 | IPG11 | VNEG | ING10 | IPG10 | VPOS | ING9 | IPG9 | VNEG | ING8 | IPG8 | VPOS | ONG8 | OPG8 | VNEG | ONG7 | OPG7 | VNEG | VNEG | VNEG | C |
| D | IPR13 | INR13 | IPG13 | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | V8 | H8 | VPOS | V7 | H7 | VNEG | VNEG | VNEG | D |
| E | INB13 | IPB13 | ING13 | VPOS | VPOS | DGND | VDD | A0 | A1 | A2 | A3 | SER/PAR | SERIN | $\overline{CLK}$ | $\overline{CS}$ | SEROUT | VDD | DGND | VPOS | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | E |
| F | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | F |
| G | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | V6 | ONG6 | OPB6 | ONB6 | G |
| H | IPR14 | INR14 | IPG14 | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | H6 | OPG6 | ONR6 | OPR6 | H |
| J | INB14 | IPB14 | ING14 | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | J |
| K | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | V5 | ONG5 | OPB5 | ONB5 | K |
| L | IPR15 | INR15 | IPG15 | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | H5 | OPG5 | ONR5 | OPR5 | L |
| M | INB15 | IPB15 | ING15 | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | M |
| N | VPOS | VPOS | VPOS | VPOS | VOCM_CMENCON | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | V4 | ONG4 | OPB4 | ONB4 | N |
| P | VPOS | VPOS | VPOS | VPOS | VBLK | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | H4 | OPG4 | ONR4 | OPR4 | P |
| R | IPR7 | INR7 | IPG7 | VPOS | VOCM_CMENCOFF | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | R |
| T | INB7 | IPB7 | ING7 | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | V3 | ONG3 | OPB3 | ONB3 | T |
| U | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | H3 | OPG3 | ONR3 | OPR3 | U |
| V | IPR6 | INR6 | IPG6 | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | V |
| W | INB6 | IPB6 | ING6 | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VNEG | VPOS | VPOS | V2 | ONG2 | OPB2 | ONB2 | W |
| Y | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | H2 | OPG2 | ONR2 | OPR2 | Y |
| AA | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | AA |
| AB | IPR5 | INR5 | IPG5 | VPOS | VPOS | DGND | VDD | D0 | D1 | D2 | D3 | D4 | CMENC | $\overline{WE}$ | $\overline{UPDATE}$ | $\overline{RST}$ | VDD | DGND | VPOS | VPOS | VPOS | VPOS | VPOS | VNEG | VNEG | VNEG | AB |
| AC | INB5 | IPB5 | ING5 | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | VPOS | H0 | V0 | VPOS | H1 | V1 | VNEG | VNEG | VNEG | AC |
| AD | VNEG | VNEG | VNEG | IPG4 | ING4 | VNEG | IPG3 | ING3 | VPOS | IPG2 | ING2 | VNEG | IPG1 | ING1 | VPOS | IPG0 | ING0 | VNEG | OPG0 | ONG0 | VPOS | OPG1 | ONG1 | VNEG | VNEG | VNEG | AD |
| AE | VNEG | VNEG | VNEG | INR4 | IPB4 | VNEG | INR3 | IPB3 | VPOS | INR2 | IPB2 | VNEG | INR1 | IPB1 | VPOS | INR0 | IPB0 | VNEG | ONR0 | OPB0 | VPOS | ONR1 | OPB1 | VNEG | VNEG | VNEG | AE |
| AF | VNEG | VNEG | VNEG | IPR4 | INB4 | VNEG | IPR3 | INB3 | VPOS | IPR2 | INB2 | VNEG | IPR1 | INB1 | VPOS | IPR0 | INB0 | VNEG | OPR0 | ONB0 | VPOS | OPR1 | ONB1 | VNEG | VNEG | VNEG | AF |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |

06478-006

*Figure 6. Package Top View*

**Table 14. Ball Grid Description**

| Ball No. | Mnemonic | Description |
|---|---|---|
| A1 | VNEG | Negative Analog Power Supply. |
| A2 | VNEG | Negative Analog Power Supply. |
| A3 | VNEG | Negative Analog Power Supply. |
| A4 | INB12 | Input Number 12, Negative Phase. |
| A5 | IPR12 | Input Number 12, Positive Phase. |
| A6 | VPOS | Positive Analog Power Supply. |
| A7 | INB11 | Input Number 11, Negative Phase. |
| A8 | IPR11 | Input Number 11, Positive Phase. |
| A9 | VNEG | Negative Analog Power Supply. |
| A10 | INB10 | Input Number 10, Negative Phase. |
| A11 | IPR10 | Input Number 10, Positive Phase. |
| A12 | VPOS | Positive Analog Power Supply. |
| A13 | INB9 | Input Number 9, Negative Phase. |
| A14 | IPR9 | Input Number 9, Positive Phase. |
| A15 | VNEG | Negative Analog Power Supply. |
| A16 | INB8 | Input Number 8, Negative Phase. |
| A17 | IPR8 | Input Number 8, Positive Phase. |
| A18 | VPOS | Positive Analog Power Supply. |
| A19 | ONB8 | Output Number 8, Negative Phase. |
| A20 | OPR8 | Output Number 8, Positive Phase. |
| A21 | VNEG | Negative Analog Power Supply. |
| A22 | ONB7 | Output Number 7, Negative Phase. |
| A23 | OPR7 | Output Number 7, Positive Phase. |
| A24 | VNEG | Negative Analog Power Supply. |
| A25 | VNEG | Negative Analog Power Supply. |
| A26 | VNEG | Negative Analog Power Supply. |
| B1 | VNEG | Negative Analog Power Supply. |
| B2 | VNEG | Negative Analog Power Supply. |
| B3 | VNEG | Negative Analog Power Supply. |
| B4 | IPB12 | Input Number 12, Positive Phase. |
| B5 | INR12 | Input Number 12, Negative Phase. |
| B6 | VPOS | Positive Analog Power Supply. |
| B7 | IPB11 | Input Number 11, Positive Phase. |
| B8 | INR11 | Input Number 11, Negative Phase. |
| B9 | VNEG | Negative Analog Power Supply. |
| B10 | IPB10 | Input Number 10, Positive Phase. |
| B11 | INR10 | Input Number 10, Negative Phase. |
| B12 | VPOS | Positive Analog Power Supply. |
| B13 | IPB9 | Input Number 9, Positive Phase. |
| B14 | INR9 | Input Number 9, Negative Phase. |
| B15 | VNEG | Negative Analog Power Supply. |
| B16 | IPB8 | Input Number 8, Positive Phase. |
| B17 | INR8 | Input Number 8, Negative Phase. |
| B18 | VPOS | Positive Analog Power Supply. |
| B19 | OPB8 | Output Number 8, Positive Phase. |
| B20 | ONR8 | Output Number 8, Negative Phase. |
| B21 | VNEG | Negative Analog Power Supply. |
| B22 | OPB7 | Output Number 7, Positive Phase. |
| B23 | ONR7 | Output Number 7, Negative Phase. |
| B24 | VNEG | Negative Analog Power Supply. |
| B25 | VNEG | Negative Analog Power Supply. |
| B26 | VNEG | Negative Analog Power Supply. |
| C1 | VNEG | Negative Analog Power Supply. |
| C2 | VNEG | Negative Analog Power Supply. |
| C3 | VNEG | Negative Analog Power Supply. |
| C4 | ING12 | Input Number 12, Negative Phase. |
| C5 | IPG12 | Input Number 12, Positive Phase. |
| C6 | VPOS | Positive Analog Power Supply. |
| C7 | ING11 | Input Number 11, Negative Phase. |
| C8 | IPG11 | Input Number 11, Positive Phase. |
| C9 | VNEG | Negative Analog Power Supply. |
| C10 | ING10 | Input Number 10, Negative Phase. |
| C11 | IPG10 | Input Number 10, Positive Phase. |
| C12 | VPOS | Positive Analog Power Supply. |
| C13 | ING9 | Input Number 9, Negative Phase. |
| C14 | IPG9 | Input Number 9, Positive Phase. |
| C15 | VNEG | Negative Analog Power Supply. |
| C16 | ING8 | Input Number 8, Negative Phase. |
| C17 | IPG8 | Input Number 8, Positive Phase. |
| C18 | VPOS | Positive Analog Power Supply. |
| C19 | ONG8 | Output Number 8, Negative Phase. |
| C20 | OPG8 | Output Number 8, Positive Phase. |
| C21 | VNEG | Negative Analog Power Supply. |
| C22 | ONG7 | Output Number 7, Negative Phase. |
| C23 | OPG7 | Output Number 7, Positive Phase. |
| C24 | VNEG | Negative Analog Power Supply. |
| C25 | VNEG | Negative Analog Power Supply. |
| C26 | VNEG | Negative Analog Power Supply. |
| D1 | IPR13 | Input Number 13, Positive Phase. |
| D2 | INR13 | Input Number 13, Negative Phase. |
| D3 | IPG13 | Input Number 13, Positive Phase. |
| D4 | VPOS | Positive Analog Power Supply. |
| D5 | VPOS | Positive Analog Power Supply. |
| D6 | VPOS | Positive Analog Power Supply. |
| D7 | VPOS | Positive Analog Power Supply. |
| D8 | VPOS | Positive Analog Power Supply. |
| D9 | VPOS | Positive Analog Power Supply. |
| D10 | VPOS | Positive Analog Power Supply. |
| D11 | VPOS | Positive Analog Power Supply. |
| D12 | VPOS | Positive Analog Power Supply. |
| D13 | VPOS | Positive Analog Power Supply. |
| D14 | VPOS | Positive Analog Power Supply. |
| D15 | VPOS | Positive Analog Power Supply. |
| D16 | VPOS | Positive Analog Power Supply. |
| D17 | VPOS | Positive Analog Power Supply. |
| D18 | VPOS | Positive Analog Power Supply. |
| D19 | V8 | Output Number 8, V Sync. |
| D20 | H8 | Output Number 8, H Sync. |
| D21 | VPOS | Positive Analog Power Supply. |
| D22 | V7 | Output Number 7, V Sync. |
| D23 | H7 | Output Number 7, H Sync. |
| D24 | VNEG | Negative Analog Power Supply. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| D25 | VNEG | Negative Analog Power Supply. |
| D26 | VNEG | Negative Analog Power Supply. |
| E1 | INB13 | Input Number 13, Negative Phase. |
| E2 | IPB13 | Input Number 13, Positive Phase. |
| E3 | ING13 | Input Number 13, Negative Phase. |
| E4 | VPOS | Positive Analog Power Supply. |
| E5 | VPOS | Positive Analog Power Supply. |
| E6 | DGND | Digital Power Supply. |
| E7 | VDD | Digital Power Supply. |
| E8 | A0 | Control Pin 0, Output Address Bit 0. |
| E9 | A1 | Control Pin 1, Output Address Bit 1. |
| E10 | A2 | Control Pin 2, Output Address Bit 2. |
| E11 | A3 | Control Pin 3, Output Address Bit 3. |
| E12 | $\overline{\text{SER}}$/PAR | Control Pin: Serial Parallel Select Mode. |
| E13 | SERIN | Control Pin: Serial Data In. |
| E14 | $\overline{\text{CLK}}$ | Control Pin: Serial Data Clock. |
| E15 | $\overline{\text{CS}}$ | Control Pin: Chip Select. |
| E16 | SEROUT | Control Pin: Serial Data Out. |
| E17 | VDD | Digital Power Supply. |
| E18 | DGND | Digital Power Supply. |
| E19 | VPOS | Positive Analog Power Supply. |
| E20 | VPOS | Positive Analog Power Supply. |
| E21 | VPOS | Positive Analog Power Supply. |
| E22 | VPOS | Positive Analog Power Supply. |
| E23 | VPOS | Positive Analog Power Supply. |
| E24 | VNEG | Negative Analog Power Supply. |
| E25 | VNEG | Negative Analog Power Supply. |
| E26 | VNEG | Negative Analog Power Supply. |
| F1 | VPOS | Positive Analog Power Supply. |
| F2 | VPOS | Positive Analog Power Supply. |
| F3 | VPOS | Positive Analog Power Supply. |
| F4 | VPOS | Positive Analog Power Supply. |
| F5 | VPOS | Positive Analog Power Supply. |
| F6 | VPOS | Positive Analog Power Supply. |
| F7 | VPOS | Positive Analog Power Supply. |
| F8 | VPOS | Positive Analog Power Supply. |
| F9 | VPOS | Positive Analog Power Supply. |
| F10 | VPOS | Positive Analog Power Supply. |
| F11 | VPOS | Positive Analog Power Supply. |
| F12 | VPOS | Positive Analog Power Supply. |
| F13 | VPOS | Positive Analog Power Supply. |
| F14 | VPOS | Positive Analog Power Supply. |
| F15 | VPOS | Positive Analog Power Supply. |
| F16 | VPOS | Positive Analog Power Supply. |
| F17 | VPOS | Positive Analog Power Supply. |
| F18 | VPOS | Positive Analog Power Supply. |
| F19 | VPOS | Positive Analog Power Supply. |
| F20 | VPOS | Positive Analog Power Supply. |
| F21 | VPOS | Positive Analog Power Supply. |
| F22 | VPOS | Positive Analog Power Supply. |
| F23 | VPOS | Positive Analog Power Supply. |
| F24 | VPOS | Positive Analog Power Supply. |
| F25 | VPOS | Positive Analog Power Supply. |
| F26 | VPOS | Positive Analog Power Supply. |
| G1 | VPOS | Positive Analog Power Supply. |
| G2 | VPOS | Positive Analog Power Supply. |
| G3 | VPOS | Positive Analog Power Supply. |
| G4 | VPOS | Positive Analog Power Supply. |
| G5 | VPOS | Positive Analog Power Supply. |
| G6 | VPOS | Positive Analog Power Supply. |
| G7 | VPOS | Positive Analog Power Supply. |
| G8 | VPOS | Positive Analog Power Supply. |
| G9 | VPOS | Positive Analog Power Supply. |
| G10 | VPOS | Positive Analog Power Supply. |
| G11 | VPOS | Positive Analog Power Supply. |
| G12 | VPOS | Positive Analog Power Supply. |
| G13 | VPOS | Positive Analog Power Supply. |
| G14 | VPOS | Positive Analog Power Supply. |
| G15 | VPOS | Positive Analog Power Supply. |
| G16 | VPOS | Positive Analog Power Supply. |
| G17 | VPOS | Positive Analog Power Supply. |
| G18 | VPOS | Positive Analog Power Supply. |
| G19 | VPOS | Positive Analog Power Supply. |
| G20 | VPOS | Positive Analog Power Supply. |
| G21 | VPOS | Positive Analog Power Supply. |
| G22 | VPOS | Positive Analog Power Supply. |
| G23 | V6 | Output Number 6, V Sync. |
| G24 | ONG6 | Output Number 6, Negative Phase. |
| G25 | OPB6 | Output Number 6, Positive Phase. |
| G26 | ONB6 | Output Number 6, Negative Phase. |
| H1 | IPR14 | Input Number 14, Positive Phase. |
| H2 | INR14 | Input Number 14, Negative Phase. |
| H3 | IPG14 | Input Number 14, Positive Phase. |
| H4 | VPOS | Positive Analog Power Supply. |
| H5 | VPOS | Positive Analog Power Supply. |
| H6 | VPOS | Positive Analog Power Supply. |
| H7 | VPOS | Positive Analog Power Supply. |
| H8 | VNEG | Negative Analog Power Supply. |
| H9 | VNEG | Negative Analog Power Supply. |
| H10 | VNEG | Negative Analog Power Supply. |
| H11 | VNEG | Negative Analog Power Supply. |
| H12 | VNEG | Negative Analog Power Supply. |
| H13 | VNEG | Negative Analog Power Supply. |
| H14 | VNEG | Negative Analog Power Supply. |
| H15 | VNEG | Negative Analog Power Supply. |
| H16 | VNEG | Negative Analog Power Supply. |
| H17 | VNEG | Negative Analog Power Supply. |
| H18 | VNEG | Negative Analog Power Supply. |
| H19 | VNEG | Negative Analog Power Supply. |
| H20 | VNEG | Negative Analog Power Supply. |
| H21 | VPOS | Positive Analog Power Supply. |
| H22 | VPOS | Positive Analog Power Supply. |
| H23 | H6 | Output Number 6, H Sync. |
| H24 | OPG6 | Output Number 6, Positive Phase. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| H25 | ONR6 | Output Number 6, Negative Phase. |
| H26 | OPR6 | Output Number 6, Positive Phase. |
| J1 | INB14 | Input Number 14, Negative Phase. |
| J2 | IPB14 | Input Number 14, Positive Phase. |
| J3 | ING14 | Input Number 14, Negative Phase. |
| J4 | VPOS | Positive Analog Power Supply. |
| J5 | VPOS | Positive Analog Power Supply. |
| J6 | VPOS | Positive Analog Power Supply. |
| J7 | VPOS | Positive Analog Power Supply. |
| J8 | VNEG | Negative Analog Power Supply. |
| J9 | VNEG | Negative Analog Power Supply. |
| J10 | VNEG | Negative Analog Power Supply. |
| J11 | VNEG | Negative Analog Power Supply. |
| J12 | VNEG | Negative Analog Power Supply. |
| J13 | VNEG | Negative Analog Power Supply. |
| J14 | VNEG | Negative Analog Power Supply. |
| J15 | VNEG | Negative Analog Power Supply. |
| J16 | VNEG | Negative Analog Power Supply. |
| J17 | VNEG | Negative Analog Power Supply. |
| J18 | VNEG | Negative Analog Power Supply. |
| J19 | VNEG | Negative Analog Power Supply. |
| J20 | VNEG | Negative Analog Power Supply. |
| J21 | VPOS | Positive Analog Power Supply. |
| J22 | VPOS | Positive Analog Power Supply. |
| J23 | VPOS | Positive Analog Power Supply. |
| J24 | VNEG | Negative Analog Power Supply. |
| J25 | VNEG | Negative Analog Power Supply. |
| J26 | VNEG | Negative Analog Power Supply. |
| K1 | VNEG | Negative Analog Power Supply. |
| K2 | VNEG | Negative Analog Power Supply. |
| K3 | VNEG | Negative Analog Power Supply. |
| K4 | VPOS | Positive Analog Power Supply. |
| K5 | VPOS | Positive Analog Power Supply. |
| K6 | VPOS | Positive Analog Power Supply. |
| K7 | VPOS | Positive Analog Power Supply. |
| K8 | VNEG | Negative Analog Power Supply. |
| K9 | VNEG | Negative Analog Power Supply. |
| K10 | VNEG | Negative Analog Power Supply. |
| K11 | VNEG | Negative Analog Power Supply. |
| K12 | VNEG | Negative Analog Power Supply. |
| K13 | VNEG | Negative Analog Power Supply. |
| K14 | VNEG | Negative Analog Power Supply. |
| K15 | VNEG | Negative Analog Power Supply. |
| K16 | VNEG | Negative Analog Power Supply. |
| K17 | VNEG | Negative Analog Power Supply. |
| K18 | VNEG | Negative Analog Power Supply. |
| K19 | VNEG | Negative Analog Power Supply. |
| K20 | VNEG | Negative Analog Power Supply. |
| K21 | VPOS | Positive Analog Power Supply. |
| K22 | VPOS | Positive Analog Power Supply. |
| K23 | V5 | Output Number 5, V Sync. |
| K24 | ONG5 | Output Number 5, Negative Phase. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| K25 | OPB5 | Output Number 5, Positive Phase. |
| K26 | ONB5 | Output Number 5, Negative Phase. |
| L1 | IPR15 | Input Number 15, Positive Phase. |
| L2 | INR15 | Input Number 15, Negative Phase. |
| L3 | IPG15 | Input Number 15, Positive Phase. |
| L4 | VPOS | Positive Analog Power Supply. |
| L5 | VPOS | Positive Analog Power Supply. |
| L6 | VPOS | Positive Analog Power Supply. |
| L7 | VPOS | Positive Analog Power Supply. |
| L8 | VNEG | Negative Analog Power Supply. |
| L9 | VNEG | Negative Analog Power Supply. |
| L10 | VNEG | Negative Analog Power Supply. |
| L11 | VNEG | Negative Analog Power Supply. |
| L12 | VNEG | Negative Analog Power Supply. |
| L13 | VNEG | Negative Analog Power Supply. |
| L14 | VNEG | Negative Analog Power Supply. |
| L15 | VNEG | Negative Analog Power Supply. |
| L16 | VNEG | Negative Analog Power Supply. |
| L17 | VNEG | Negative Analog Power Supply. |
| L18 | VNEG | Negative Analog Power Supply. |
| L19 | VNEG | Negative Analog Power Supply. |
| L20 | VNEG | Negative Analog Power Supply. |
| L21 | VPOS | Positive Analog Power Supply. |
| L22 | VPOS | Positive Analog Power Supply. |
| L23 | H5 | Output Number 5, H Sync. |
| L24 | OPG5 | Output Number 5, Positive Phase. |
| L25 | ONR5 | Output Number 5, Negative Phase. |
| L26 | OPR5 | Output Number 5, Positive Phase. |
| M1 | INB15 | Input Number 15, Negative Phase. |
| M2 | IPB15 | Input Number 15, Positive Phase. |
| M3 | ING15 | Input Number 15, Negative Phase. |
| M4 | VPOS | Positive Analog Power Supply. |
| M5 | VPOS | Positive Analog Power Supply. |
| M6 | VPOS | Positive Analog Power Supply. |
| M7 | VPOS | Positive Analog Power Supply. |
| M8 | VNEG | Negative Analog Power Supply. |
| M9 | VNEG | Negative Analog Power Supply. |
| M10 | VNEG | Negative Analog Power Supply. |
| M11 | VNEG | Negative Analog Power Supply. |
| M12 | VNEG | Negative Analog Power Supply. |
| M13 | VNEG | Negative Analog Power Supply. |
| M14 | VNEG | Negative Analog Power Supply. |
| M15 | VNEG | Negative Analog Power Supply. |
| M16 | VNEG | Negative Analog Power Supply. |
| M17 | VNEG | Negative Analog Power Supply. |
| M18 | VNEG | Negative Analog Power Supply. |
| M19 | VNEG | Negative Analog Power Supply. |
| M20 | VNEG | Negative Analog Power Supply. |
| M21 | VPOS | Positive Analog Power Supply. |
| M22 | VPOS | Positive Analog Power Supply. |
| M23 | VPOS | Positive Analog Power Supply. |
| M24 | VPOS | Positive Analog Power Supply. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| M25 | VPOS | Positive Analog Power Supply. |
| M26 | VPOS | Positive Analog Power Supply. |
| N1 | VPOS | Positive Analog Power Supply. |
| N2 | VPOS | Positive Analog Power Supply. |
| N3 | VPOS | Positive Analog Power Supply. |
| N4 | VPOS | Positive Analog Power Supply. |
| N5 | VOCM_ CMENCON | Output CM Reference with CM Encoding On. |
| N6 | VPOS | Positive Analog Power Supply. |
| N7 | VPOS | Positive Analog Power Supply. |
| N8 | VNEG | Negative Analog Power Supply. |
| N9 | VNEG | Negative Analog Power Supply. |
| N10 | VNEG | Negative Analog Power Supply. |
| N11 | VNEG | Negative Analog Power Supply. |
| N12 | VNEG | Negative Analog Power Supply. |
| N13 | VNEG | Negative Analog Power Supply. |
| N14 | VNEG | Negative Analog Power Supply. |
| N15 | VNEG | Negative Analog Power Supply. |
| N16 | VNEG | Negative Analog Power Supply. |
| N17 | VNEG | Negative Analog Power Supply. |
| N18 | VNEG | Negative Analog Power Supply. |
| N19 | VNEG | Negative Analog Power Supply. |
| N20 | VNEG | Negative Analog Power Supply. |
| N21 | VPOS | Positive Analog Power Supply. |
| N22 | VPOS | Positive Analog Power Supply. |
| N23 | V4 | Output Number 4, V Sync. |
| N24 | ONG4 | Output Number 4, Negative Phase. |
| N25 | OPB4 | Output Number 4, Positive Phase. |
| N26 | ONB4 | Output Number 4, Negative Phase. |
| P1 | VPOS | Positive Analog Power Supply. |
| P2 | VPOS | Positive Analog Power Supply. |
| P3 | VPOS | Positive Analog Power Supply. |
| P4 | VPOS | Positive Analog Power Supply. |
| P5 | VBLK | Output Blank Level. |
| P6 | VPOS | Positive Analog Power Supply. |
| P7 | VPOS | Positive Analog Power Supply. |
| P8 | VNEG | Negative Analog Power Supply. |
| P9 | VNEG | Negative Analog Power Supply. |
| P10 | VNEG | Negative Analog Power Supply. |
| P11 | VNEG | Negative Analog Power Supply. |
| P12 | VNEG | Negative Analog Power Supply. |
| P13 | VNEG | Negative Analog Power Supply. |
| P14 | VNEG | Negative Analog Power Supply. |
| P15 | VNEG | Negative Analog Power Supply. |
| P16 | VNEG | Negative Analog Power Supply. |
| P17 | VNEG | Negative Analog Power Supply. |
| P18 | VNEG | Negative Analog Power Supply. |
| P19 | VNEG | Negative Analog Power Supply. |
| P20 | VNEG | Negative Analog Power Supply. |
| P21 | VPOS | Positive Analog Power Supply. |
| P22 | VPOS | Positive Analog Power Supply. |
| P23 | H4 | Output Number 4, H Sync. |
| P24 | OPG4 | Output Number 4, Positive Phase. |
| P25 | ONR4 | Output Number 4, Negative Phase. |
| P26 | OPR4 | Output Number 4, Positive Phase. |
| R1 | IPR7 | Input Number 7, Positive Phase. |
| R2 | INR7 | Input Number 7, Negative Phase. |
| R3 | IPG7 | Input Number 7, Positive Phase. |
| R4 | VPOS | Positive Analog Power Supply. |
| R5 | VOCM_ CMENCOFF | Output Reference with CM Encoding Off. |
| R6 | VPOS | Positive Analog Power Supply. |
| R7 | VPOS | Positive Analog Power Supply. |
| R8 | VNEG | Negative Analog Power Supply. |
| R9 | VNEG | Negative Analog Power Supply. |
| R10 | VNEG | Negative Analog Power Supply. |
| R11 | VNEG | Negative Analog Power Supply. |
| R12 | VNEG | Negative Analog Power Supply. |
| R13 | VNEG | Negative Analog Power Supply. |
| R14 | VNEG | Negative Analog Power Supply. |
| R15 | VNEG | Negative Analog Power Supply. |
| R16 | VNEG | Negative Analog Power Supply. |
| R17 | VNEG | Negative Analog Power Supply. |
| R18 | VNEG | Negative Analog Power Supply. |
| R19 | VNEG | Negative Analog Power Supply. |
| R20 | VNEG | Negative Analog Power Supply. |
| R21 | VPOS | Positive Analog Power Supply. |
| R22 | VPOS | Positive Analog Power Supply. |
| R23 | VPOS | Positive Analog Power Supply. |
| R24 | VNEG | Negative Analog Power Supply. |
| R25 | VNEG | Negative Analog Power Supply. |
| R26 | VNEG | Negative Analog Power Supply. |
| T1 | INB7 | Input Number 7, Negative Phase. |
| T2 | IPB7 | Input Number 7, Positive Phase. |
| T3 | ING7 | Input Number 7, Negative Phase. |
| T4 | VPOS | Positive Analog Power Supply. |
| T5 | VPOS | Positive Analog Power Supply. |
| T6 | VPOS | Positive Analog Power Supply. |
| T7 | VPOS | Positive Analog Power Supply. |
| T8 | VNEG | Negative Analog Power Supply. |
| T9 | VNEG | Negative Analog Power Supply. |
| T10 | VNEG | Negative Analog Power Supply. |
| T11 | VNEG | Negative Analog Power Supply. |
| T12 | VNEG | Negative Analog Power Supply. |
| T13 | VNEG | Negative Analog Power Supply. |
| T14 | VNEG | Negative Analog Power Supply. |
| T15 | VNEG | Negative Analog Power Supply. |
| T16 | VNEG | Negative Analog Power Supply. |
| T17 | VNEG | Negative Analog Power Supply. |
| T18 | VNEG | Negative Analog Power Supply. |
| T19 | VNEG | Negative Analog Power Supply. |
| T20 | VNEG | Negative Analog Power Supply. |
| T21 | VPOS | Positive Analog Power Supply. |
| T22 | VPOS | Positive Analog Power Supply. |
| T23 | V3 | Output Number 3, V Sync. |
| T24 | ONG3 | Output Number 3, Negative Phase. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| T25 | OPB3 | Output Number 3, Positive Phase. |
| T26 | ONB3 | Output Number 3, Negative Phase. |
| U1 | VNEG | Negative Analog Power Supply. |
| U2 | VNEG | Negative Analog Power Supply. |
| U3 | VNEG | Negative Analog Power Supply. |
| U4 | VPOS | Positive Analog Power Supply. |
| U5 | VPOS | Positive Analog Power Supply. |
| U6 | VPOS | Positive Analog Power Supply. |
| U7 | VPOS | Positive Analog Power Supply. |
| U8 | VNEG | Negative Analog Power Supply. |
| U9 | VNEG | Negative Analog Power Supply. |
| U10 | VNEG | Negative Analog Power Supply. |
| U11 | VNEG | Negative Analog Power Supply. |
| U12 | VNEG | Negative Analog Power Supply. |
| U13 | VNEG | Negative Analog Power Supply. |
| U14 | VNEG | Negative Analog Power Supply. |
| U15 | VNEG | Negative Analog Power Supply. |
| U16 | VNEG | Negative Analog Power Supply. |
| U17 | VNEG | Negative Analog Power Supply. |
| U18 | VNEG | Negative Analog Power Supply. |
| U19 | VNEG | Negative Analog Power Supply. |
| U20 | VNEG | Negative Analog Power Supply. |
| U21 | VPOS | Positive Analog Power Supply. |
| U22 | VPOS | Positive Analog Power Supply. |
| U23 | H3 | Output Number 3, H Sync. |
| U24 | OPG3 | Output Number 3, Positive Phase. |
| U25 | ONR3 | Output Number 3, Negative Phase. |
| U26 | OPR3 | Output Number 3, Positive Phase. |
| V1 | IPR6 | Input Number 6, Positive Phase. |
| V2 | INR6 | Input Number 6, Negative Phase. |
| V3 | IPG6 | Input Number 6, Positive Phase. |
| V4 | VPOS | Positive Analog Power Supply. |
| V5 | VPOS | Positive Analog Power Supply. |
| V6 | VPOS | Positive Analog Power Supply. |
| V7 | VPOS | Positive Analog Power Supply. |
| V8 | VNEG | Negative Analog Power Supply. |
| V9 | VNEG | Negative Analog Power Supply. |
| V10 | VNEG | Negative Analog Power Supply. |
| V11 | VNEG | Negative Analog Power Supply. |
| V12 | VNEG | Negative Analog Power Supply. |
| V13 | VNEG | Negative Analog Power Supply. |
| V14 | VNEG | Negative Analog Power Supply. |
| V15 | VNEG | Negative Analog Power Supply. |
| V16 | VNEG | Negative Analog Power Supply. |
| V17 | VNEG | Negative Analog Power Supply. |
| V18 | VNEG | Negative Analog Power Supply. |
| V19 | VNEG | Negative Analog Power Supply. |
| V20 | VNEG | Negative Analog Power Supply. |
| V21 | VPOS | Positive Analog Power Supply. |
| V22 | VPOS | Positive Analog Power Supply. |
| V23 | VPOS | Positive Analog Power Supply. |
| V24 | VPOS | Positive Analog Power Supply. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| V25 | VPOS | Positive Analog Power Supply. |
| V26 | VPOS | Positive Analog Power Supply. |
| W1 | INB6 | Input Number 6, Negative Phase. |
| W2 | IPB6 | Input Number 6, Positive Phase. |
| W3 | ING6 | Input Number 6, Negative Phase. |
| W4 | VPOS | Positive Analog Power Supply. |
| W5 | VPOS | Positive Analog Power Supply. |
| W6 | VPOS | Positive Analog Power Supply. |
| W7 | VPOS | Positive Analog Power Supply. |
| W8 | VNEG | Negative Analog Power Supply. |
| W9 | VNEG | Negative Analog Power Supply. |
| W10 | VNEG | Negative Analog Power Supply. |
| W11 | VNEG | Negative Analog Power Supply. |
| W12 | VNEG | Negative Analog Power Supply. |
| W13 | VNEG | Negative Analog Power Supply. |
| W14 | VNEG | Negative Analog Power Supply. |
| W15 | VNEG | Negative Analog Power Supply. |
| W16 | VNEG | Negative Analog Power Supply. |
| W17 | VNEG | Negative Analog Power Supply. |
| W18 | VNEG | Negative Analog Power Supply. |
| W19 | VNEG | Negative Analog Power Supply. |
| W20 | VNEG | Negative Analog Power Supply. |
| W21 | VPOS | Positive Analog Power Supply. |
| W22 | VPOS | Positive Analog Power Supply. |
| W23 | V2 | Output Number 2, V Sync. |
| W24 | ONG2 | Output Number 2, Negative Phase. |
| W25 | OPB2 | Output Number 2, Positive Phase. |
| W26 | ONB2 | Output Number 2, Negative Phase. |
| Y1 | VPOS | Positive Analog Power Supply. |
| Y2 | VPOS | Positive Analog Power Supply. |
| Y3 | VPOS | Positive Analog Power Supply. |
| Y4 | VPOS | Positive Analog Power Supply. |
| Y5 | VPOS | Positive Analog Power Supply. |
| Y6 | VPOS | Positive Analog Power Supply. |
| Y7 | VPOS | Positive Analog Power Supply. |
| Y8 | VPOS | Positive Analog Power Supply. |
| Y9 | VPOS | Positive Analog Power Supply. |
| Y10 | VPOS | Positive Analog Power Supply. |
| Y11 | VPOS | Positive Analog Power Supply. |
| Y12 | VPOS | Positive Analog Power Supply. |
| Y13 | VPOS | Positive Analog Power Supply. |
| Y14 | VPOS | Positive Analog Power Supply. |
| Y15 | VPOS | Positive Analog Power Supply. |
| Y16 | VPOS | Positive Analog Power Supply. |
| Y17 | VPOS | Positive Analog Power Supply. |
| Y18 | VPOS | Positive Analog Power Supply. |
| Y19 | VPOS | Positive Analog Power Supply. |
| Y20 | VPOS | Positive Analog Power Supply. |
| Y21 | VPOS | Positive Analog Power Supply. |
| Y22 | VPOS | Positive Analog Power Supply. |
| Y23 | H2 | Output Number 2, H Sync. |
| Y24 | OPG2 | Output Number 2, Positive Phase. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| Y25 | ONR2 | Output Number 2, Negative Phase. |
| Y26 | OPR2 | Output Number 2, Positive Phase. |
| AA1 | VPOS | Positive Analog Power Supply. |
| AA2 | VPOS | Positive Analog Power Supply. |
| AA3 | VPOS | Positive Analog Power Supply. |
| AA4 | VPOS | Positive Analog Power Supply. |
| AA5 | VPOS | Positive Analog Power Supply. |
| AA6 | VPOS | Positive Analog Power Supply. |
| AA7 | VPOS | Positive Analog Power Supply. |
| AA8 | VPOS | Positive Analog Power Supply. |
| AA9 | VPOS | Positive Analog Power Supply. |
| AA10 | VPOS | Positive Analog Power Supply. |
| AA11 | VPOS | Positive Analog Power Supply. |
| AA12 | VPOS | Positive Analog Power Supply. |
| AA13 | VPOS | Positive Analog Power Supply. |
| AA14 | VPOS | Positive Analog Power Supply. |
| AA15 | VPOS | Positive Analog Power Supply. |
| AA16 | VPOS | Positive Analog Power Supply. |
| AA17 | VPOS | Positive Analog Power Supply. |
| AA18 | VPOS | Positive Analog Power Supply. |
| AA19 | VPOS | Positive Analog Power Supply. |
| AA20 | VPOS | Positive Analog Power Supply. |
| AA21 | VPOS | Positive Analog Power Supply. |
| AA22 | VPOS | Positive Analog Power Supply. |
| AA23 | VPOS | Positive Analog Power Supply. |
| AA24 | VNEG | Negative Analog Power Supply. |
| AA25 | VNEG | Negative Analog Power Supply. |
| AA26 | VNEG | Negative Analog Power Supply. |
| AB1 | IPR5 | Input Number 5, Positive Phase. |
| AB2 | INR5 | Input Number 5, Negative Phase. |
| AB3 | IPG5 | Input Number 5, Positive Phase. |
| AB4 | VPOS | Positive Analog Power Supply. |
| AB5 | VPOS | Positive Analog Power Supply. |
| AB6 | DGND | Digital Power Supply. |
| AB7 | VDD | Digital Power Supply. |
| AB8 | D0 | Control Pin, Input Address Bit 0. |
| AB9 | D1 | Control Pin, Input Address Bit 1. |
| AB10 | D2 | Control Pin, Input Address Bit 2. |
| AB11 | D3 | Control Pin, Input Address Bit 3. |
| AB12 | D4 | Control Pin, Input Address Bit 4. |
| AB13 | CMENC | Control Pin, Pass/Stop CM Encoding. |
| AB14 | $\overline{WE}$ | Control Pin, 1st Rank Write Strobe. |
| AB15 | $\overline{UPDATE}$ | Control Pin, 2nd Rank Write Strobe. |
| AB16 | $\overline{RST}$ | Control Pin, 2nd Rank Data Reset. |
| AB17 | VDD | Digital Power Supply. |
| AB18 | DGND | Digital Power Supply. |
| AB19 | VPOS | Positive Analog Power Supply. |
| AB20 | VPOS | Positive Analog Power Supply. |
| AB21 | VPOS | Positive Analog Power Supply. |
| AB22 | VPOS | Positive Analog Power Supply. |
| AB23 | VPOS | Positive Analog Power Supply. |
| AB24 | VNEG | Negative Analog Power Supply. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| AB25 | VNEG | Negative Analog Power Supply. |
| AB26 | VNEG | Negative Analog Power Supply. |
| AC1 | INB5 | Input Number 5, Negative Phase. |
| AC2 | IPB5 | Input Number 5, Positive Phase. |
| AC3 | ING5 | Input Number 5, Negative Phase. |
| AC4 | VPOS | Positive Analog Power Supply. |
| AC5 | VPOS | Positive Analog Power Supply. |
| AC6 | VPOS | Positive Analog Power Supply. |
| AC7 | VPOS | Positive Analog Power Supply. |
| AC8 | VPOS | Positive Analog Power Supply. |
| AC9 | VPOS | Positive Analog Power Supply. |
| AC10 | VPOS | Positive Analog Power Supply. |
| AC11 | VPOS | Positive Analog Power Supply. |
| AC12 | VPOS | Positive Analog Power Supply. |
| AC13 | VPOS | Positive Analog Power Supply. |
| AC14 | VPOS | Positive Analog Power Supply. |
| AC15 | VPOS | Positive Analog Power Supply. |
| AC16 | VPOS | Positive Analog Power Supply. |
| AC17 | VPOS | Positive Analog Power Supply. |
| AC18 | VPOS | Positive Analog Power Supply. |
| AC19 | H0 | Output Number 1, H Sync. |
| AC20 | V0 | Output Number 0, V Sync. |
| AC21 | VPOS | Positive Analog Power Supply. |
| AC22 | H1 | Output Number 1, H Sync. |
| AC23 | V1 | Output Number 1, V Sync. |
| AC24 | VNEG | Negative Analog Power Supply. |
| AC25 | VNEG | Negative Analog Power Supply. |
| AC26 | VNEG | Negative Analog Power Supply. |
| AD1 | VNEG | Negative Analog Power Supply. |
| AD2 | VNEG | Negative Analog Power Supply. |
| AD3 | VNEG | Negative Analog Power Supply. |
| AD4 | IPG4 | Input Number 4, Positive Phase. |
| AD5 | ING4 | Input Number 4, Negative Phase. |
| AD6 | VNEG | Negative Analog Power Supply. |
| AD7 | IPG3 | Input Number 3, Positive Phase. |
| AD8 | ING3 | Input Number 3, Negative Phase. |
| AD9 | VPOS | Positive Analog Power Supply. |
| AD10 | IPG2 | Input Number 2, Positive Phase. |
| AD11 | ING2 | Input Number 2, Negative Phase. |
| AD12 | VNEG | Negative Analog Power Supply. |
| AD13 | IPG1 | Input Number 1, Positive Phase. |
| AD14 | ING1 | Input Number 1, Negative Phase. |
| AD15 | VPOS | Positive Analog Power Supply. |
| AD16 | IPG0 | Input Number 0, Positive Phase. |
| AD17 | ING0 | Input Number 0, Negative Phase. |
| AD18 | VNEG | Negative Analog Power Supply. |
| AD19 | OPG0 | Output Number 0, Positive Phase. |
| AD20 | ONG0 | Output Number 0, Negative Phase. |
| AD21 | VPOS | Positive Analog Power Supply. |
| AD22 | OPG1 | Output Number 1, Positive Phase. |
| AD23 | ONG1 | Output Number 1, Negative Phase. |
| AD24 | VNEG | Negative Analog Power Supply. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| AD25 | VNEG | Negative Analog Power Supply. |
| AD26 | VNEG | Negative Analog Power Supply. |
| AE1 | VNEG | Negative Analog Power Supply. |
| AE2 | VNEG | Negative Analog Power Supply. |
| AE3 | VNEG | Negative Analog Power Supply. |
| AE4 | INR4 | Input Number 4, Negative Phase. |
| AE5 | IPB4 | Input Number 4, Positive Phase. |
| AE6 | VNEG | Negative Analog Power Supply. |
| AE7 | INR3 | Input Number 3, Negative Phase. |
| AE8 | IPB3 | Input Number 3, Positive Phase. |
| AE9 | VPOS | Positive Analog Power Supply. |
| AE10 | INR2 | Input Number 2, Negative Phase. |
| AE11 | IPB2 | Input Number 2, Positive Phase. |
| AE12 | VNEG | Negative Analog Power Supply. |
| AE13 | INR1 | Input Number 1, Negative Phase. |
| AE14 | IPB1 | Input Number 1, Positive Phase. |
| AE15 | VPOS | Positive Analog Power Supply. |
| AE16 | INR0 | Input Number 0, Negative Phase. |
| AE17 | IPB0 | Input Number 0, Positive Phase. |
| AE18 | VNEG | Negative Analog Power Supply. |
| AE19 | ONR0 | Output Number 0, Negative Phase. |
| AE20 | OPB0 | Output Number 0, Positive Phase. |
| AE21 | VPOS | Positive Analog Power Supply. |
| AE22 | ONR1 | Output Number 1, Negative Phase. |
| AE23 | OPB1 | Output Number 1, Positive Phase. |
| AE24 | VNEG | Negative Analog Power Supply. |
| AE25 | VNEG | Negative Analog Power Supply. |

| Ball No. | Mnemonic | Description |
|---|---|---|
| AE26 | VNEG | Negative Analog Power Supply. |
| AF1 | VNEG | Negative Analog Power Supply. |
| AF2 | VNEG | Negative Analog Power Supply. |
| AF3 | VNEG | Negative Analog Power Supply. |
| AF4 | IPR4 | Input Number 4, Positive Phase. |
| AF5 | INB4 | Input Number 4, Negative Phase. |
| AF6 | VNEG | Negative Analog Power Supply. |
| AF7 | IPR3 | Input Number 3, Positive Phase. |
| AF8 | INB3 | Input Number 3, Negative Phase. |
| AF9 | VPOS | Positive Analog Power Supply. |
| AF10 | IPR2 | Input Number 2, Positive Phase. |
| AF11 | INB2 | Input Number 2, Negative Phase. |
| AF12 | VNEG | Negative Analog Power Supply. |
| AF13 | IPR1 | Input Number 1, Positive Phase. |
| AF14 | INB1 | Input Number 1, Negative Phase. |
| AF15 | VPOS | Positive Analog Power Supply. |
| AF16 | IPR0 | Input Number 0, Positive Phase. |
| AF17 | INB0 | Input Number 0, Negative Phase. |
| AF18 | VNEG | Negative Analog Power Supply. |
| AF19 | OPR0 | Output Number 0, Positive Phase. |
| AF20 | ONB0 | Output Number 0, Negative Phase. |
| AF21 | VPOS | Positive Analog Power Supply. |
| AF22 | OPR1 | Output Number 1, Positive Phase. |
| AF23 | ONB1 | Output Number 1, Negative Phase. |
| AF24 | VNEG | Negative Analog Power Supply. |
| AF25 | VNEG | Negative Analog Power Supply. |
| AF26 | VNEG | Negative Analog Power Supply. |

## TRUTH TABLE AND LOGIC DIAGRAM

**Table 15. Operation Truth Table**

| $\overline{WE}$ | $\overline{UPDATE}$ | $\overline{CLK}$ | SERIN | SEROUT | $\overline{RST}$ | $\overline{SER}$/PAR | $\overline{CS}$ | $\overline{CMENC}$ | Operation/Comment |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | 0 | X | X | X | Asynchronous reset. All outputs are disabled. Contents of 45-bit shift register are unchanged. |
| 0 | 1 | 1 | X | X | 1 | 0 | 0 | X | Broadcast. The data on D0 through D4 is loaded into all locations of the 45-bit shift register. Data is not applied to switch array. |
| 1 | 1 | ↴ | $SERIN_i$ | $SERIN_{i-45}$ | 1 | 0 | 0 | X | Serial mode. The data on the SERIN line is loaded into the 45-bit shift register. The first bit clocked into the shift register appears at SEROUT 45 clock cycles later. Data is not applied to switch array. |
| 0 | 1 | 1 | X | X | 1 | 1 | X | X | Parallel mode. The data on parallel lines D0 through D4 is loaded into the shift register location addressed by A0 through A3. Data is not applied to switch array. Chip select feature is not applicable. |
| 1 | 0 | 1 | X | X | 1 | X | 0 | X | Switch array update. Data in the 45-bit shift register is transferred to the parallel latches and applied to the switch array. |
| 1 | X | X | X | X | 1 | 1 | 0 | X | No change in logic. |

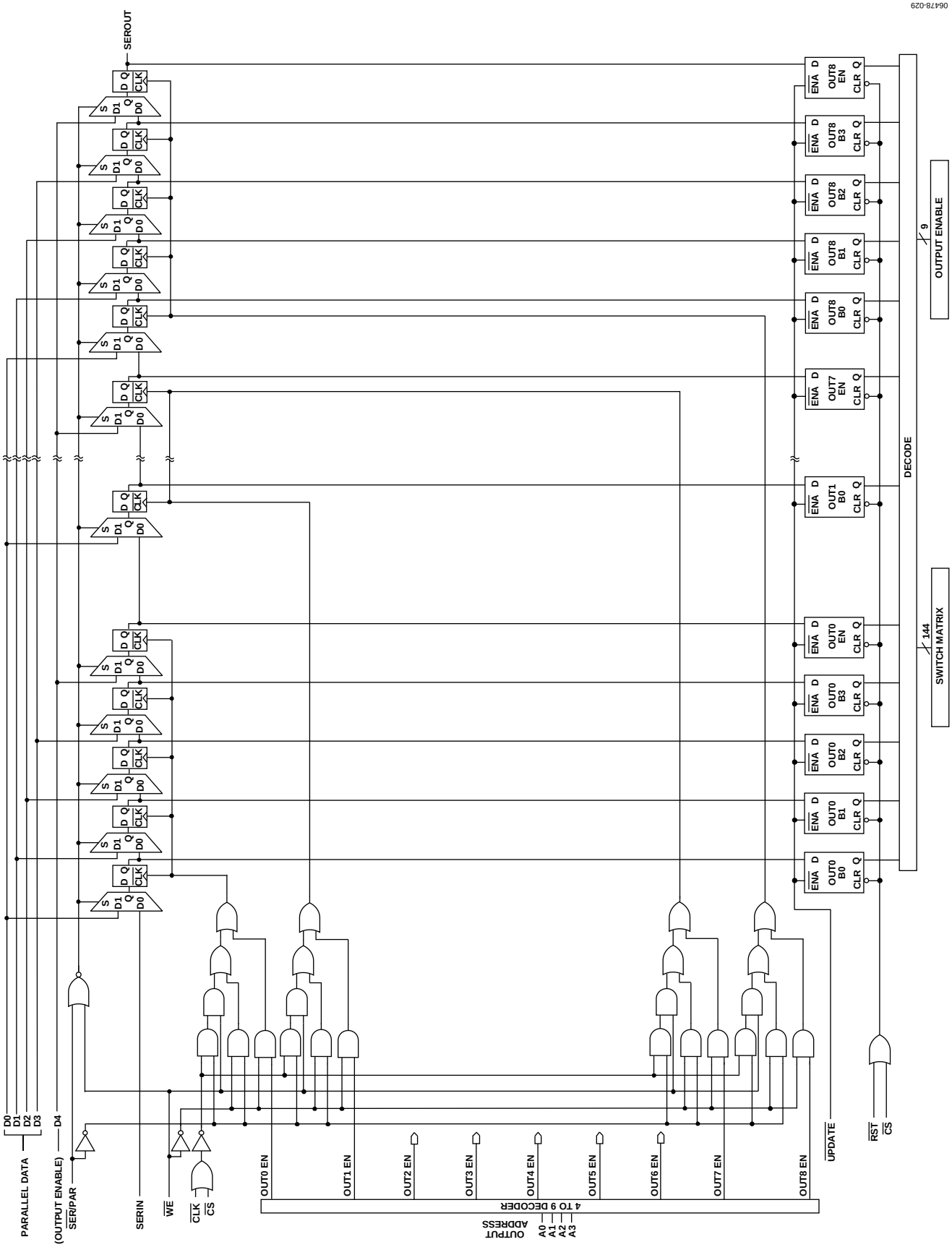



*Figure 7. Logic Diagram*

# EQUIVALENT CIRCUITS

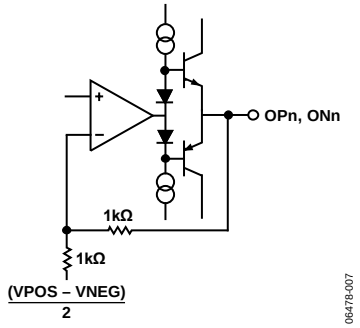



Figure 8. Enabled Output (see also ESD Protection Map , Figure 19)

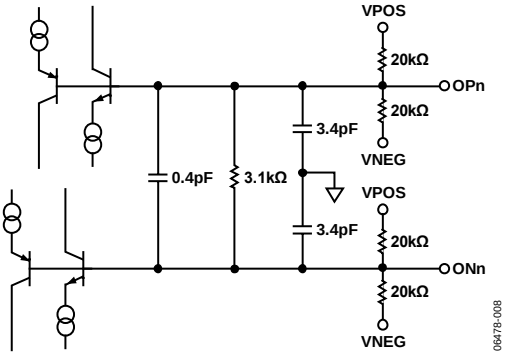



Figure 9. Disabled Output (see also ESD Protection Map, Figure 19)

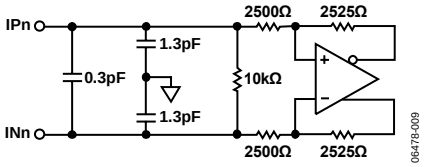



Figure 10. Receiver, Differential (see also ESD Protection Map, Figure 19)

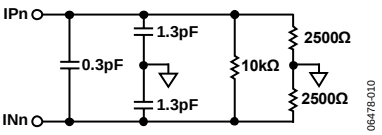



Figure 11. Receiver Simplified Equivalent Circuit When Driving Differentially

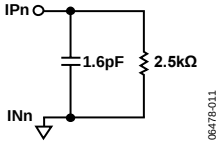



Figure 12. Receiver Simplified Equivalent Circuit When Driving Single-Ended

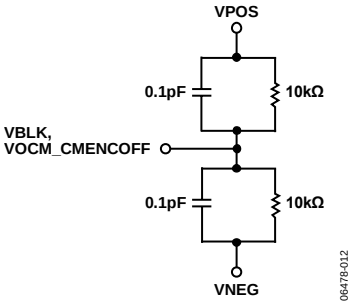



Figure 13. VBLK and VOCM_CMENCOFF Inputs (see also ESD Protection Map, Figure 19)

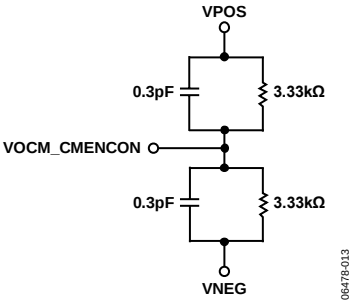



Figure 14. VOCM_CMENCON Input (see also ESD Protection Map, Figure 19)

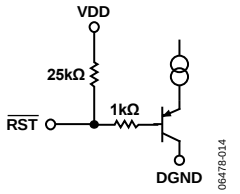



Figure 15. $\overline{RST}$ Input (see also ESD Protection Map, Figure 19)

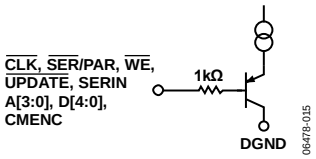



Figure 16. Logic Input (see also ESD Protection Map, Figure 19)

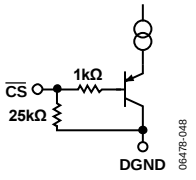



Figure 17. $\overline{CS}$ Input (see also ESD Protection Map, Figure 19)

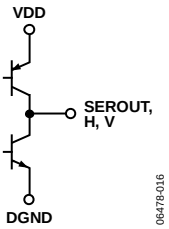



Figure 18. SEROUT, H, V Logic Outputs
(see also ESD Protection Map, Figure 19)

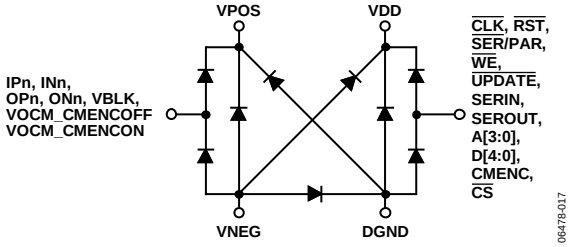



Figure 19. ESD Protection Map

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_S$ = ±2.5 V at $T_A$ = 25°C, G = +2, $R_L$ = 100 Ω (each output), VBLK = 0 V, output CM voltage = 0 V, differential I/O mode, unless otherwise noted.

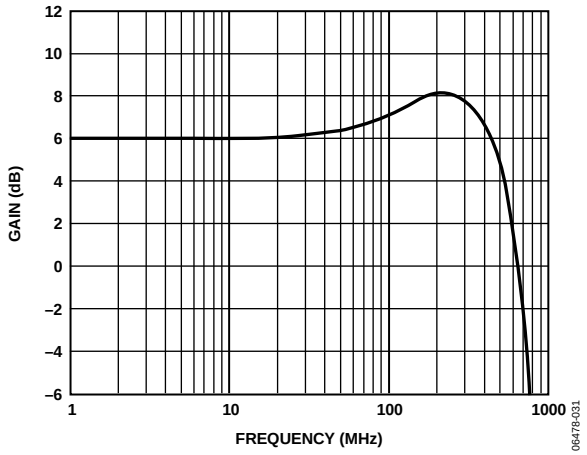



Figure 20. Small Signal Frequency Response, 200 mV p-p

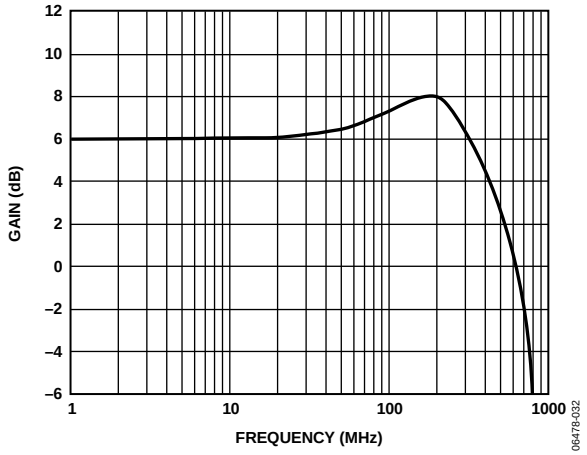



Figure 21. Large Signal Frequency Response, 2 V p-p

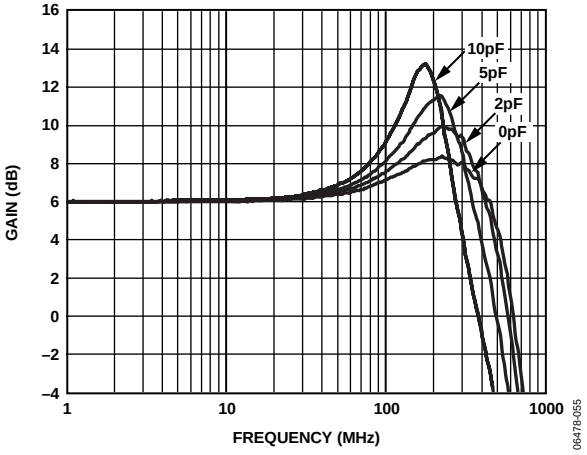



Figure 22. Small Signal Frequency Response with Capacitive Loads

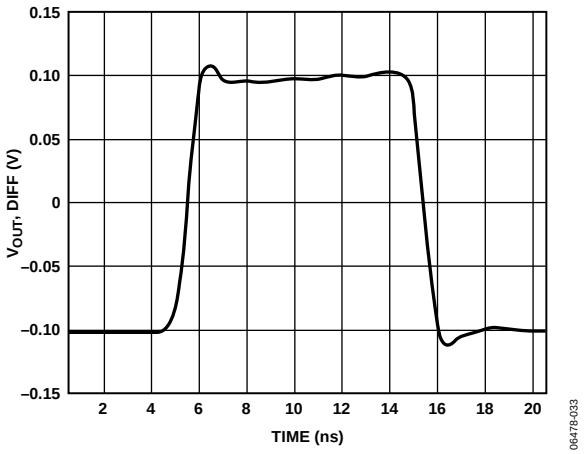



Figure 23. Small Signal Pulse Response, 200 mV p-p

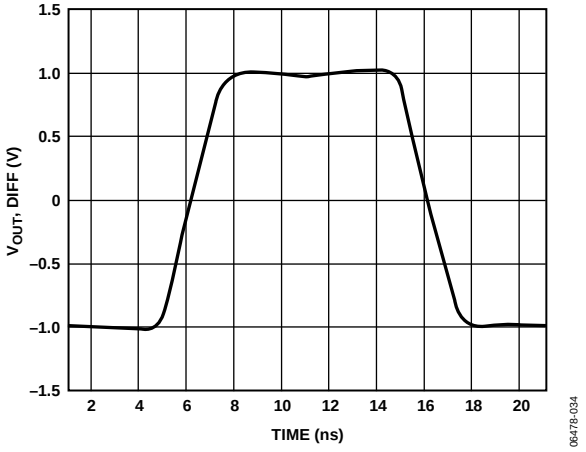



Figure 24. Large Signal Pulse Response, 2 V p-p

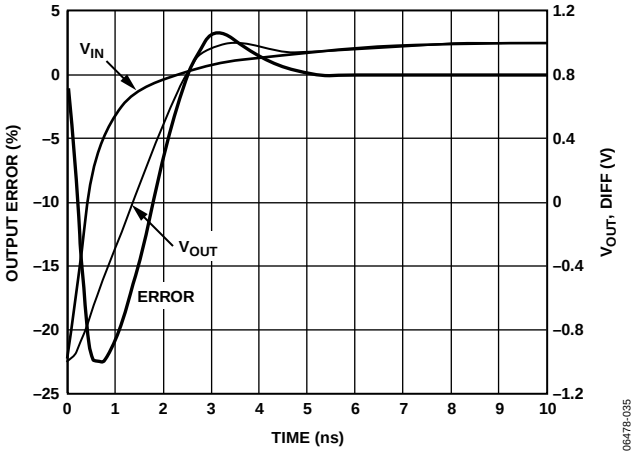



Figure 25. Settling Time

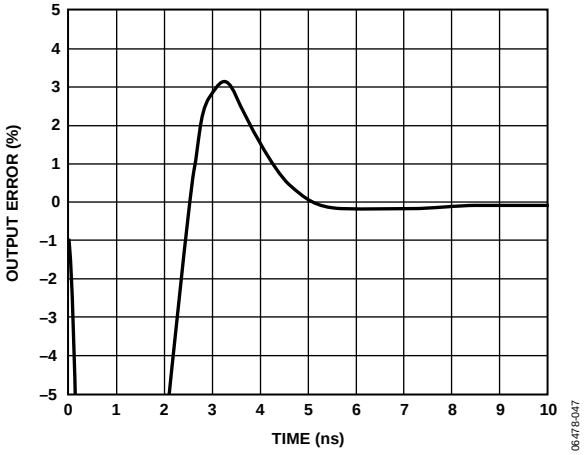



Figure 26. Settling Time, 1% Zoom

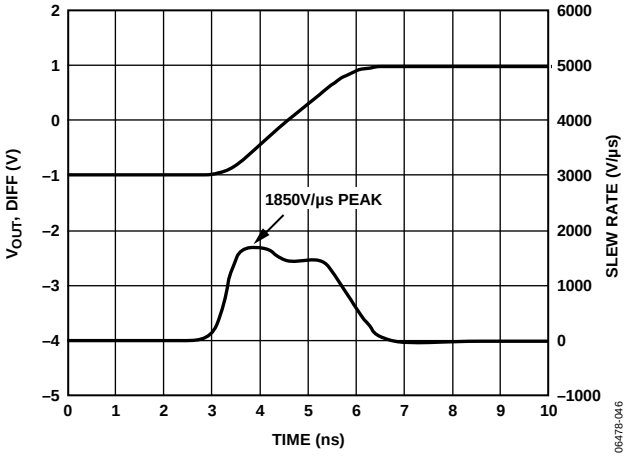



Figure 27. Large Signal Rising Edge Slew Rate

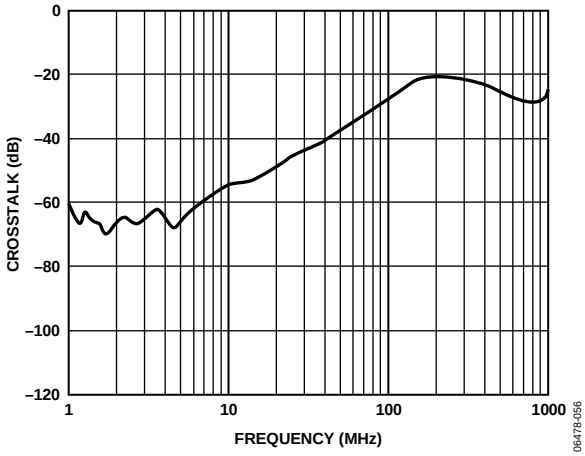



Figure 28. Crosstalk, All Hostile, Single-Ended

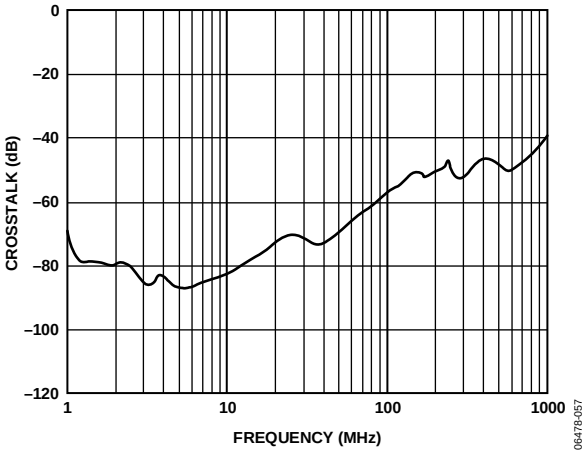



Figure 29. Crosstalk, All Hostile

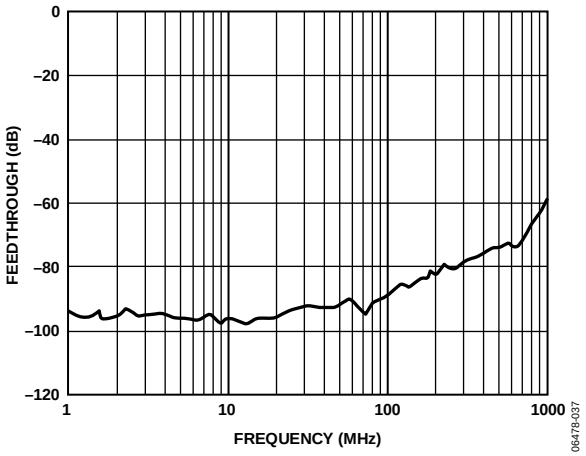



Figure 30. Crosstalk, Off Isolation

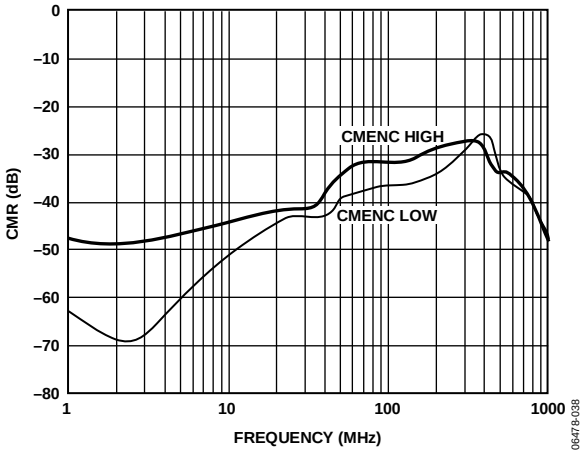



Figure 31. Common-Mode Rejection

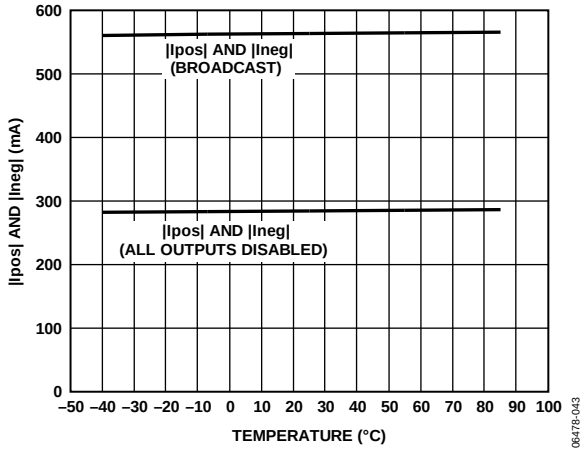



Figure 32. Quiescent Supply Currents vs. Temperature

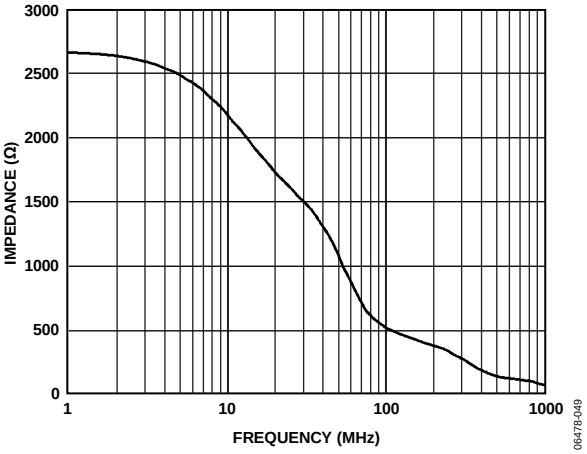



Figure 33. Output Impedance, Disabled

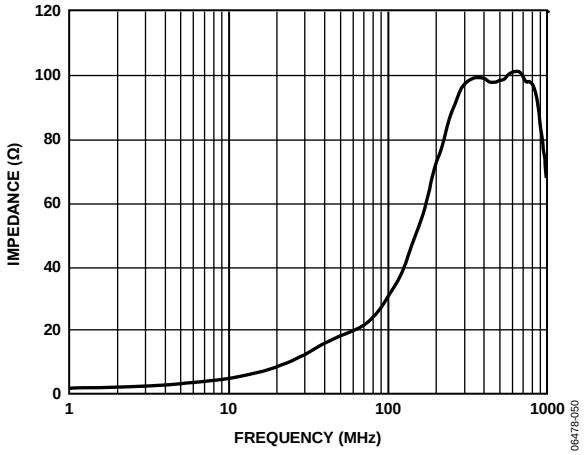



Figure 34. Output Impedance, Enabled

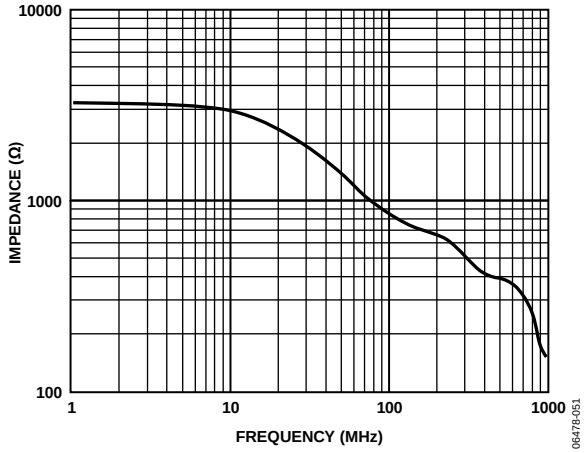



Figure 35. Input Impedance

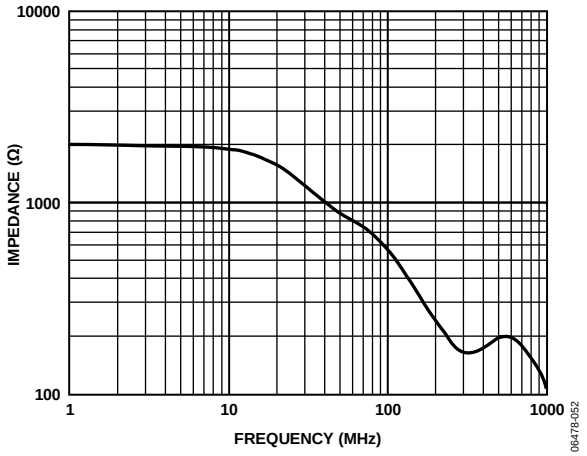



Figure 36. Input Impedance, Single-Ended

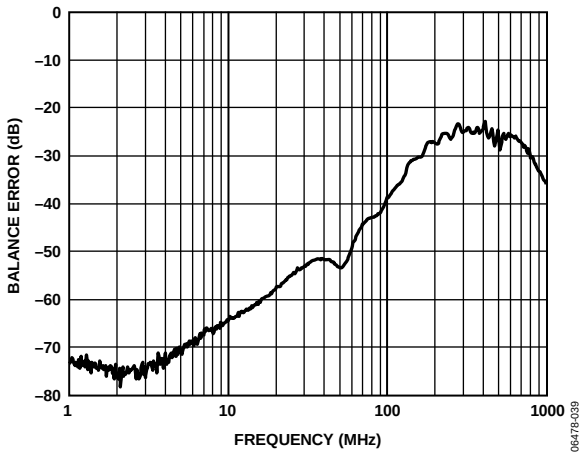



Figure 37. Output Balance Error

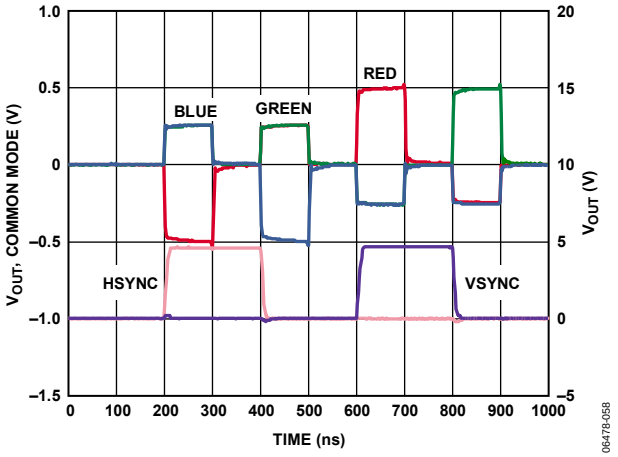



Figure 38. Common-Mode Pulse Response

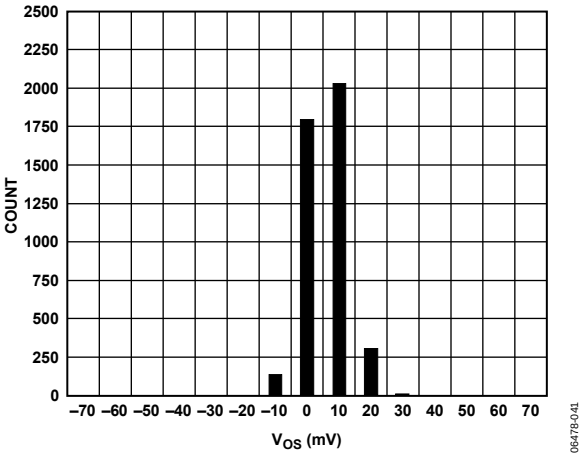



Figure 41. $V_{OS}$ Distribution

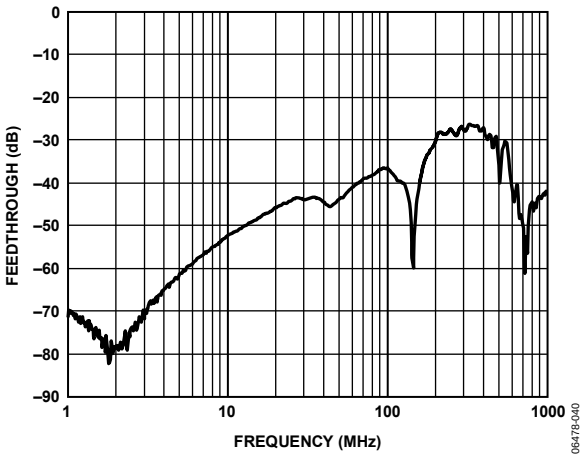



Figure 39. Common-Mode Isolation, CMENC Low

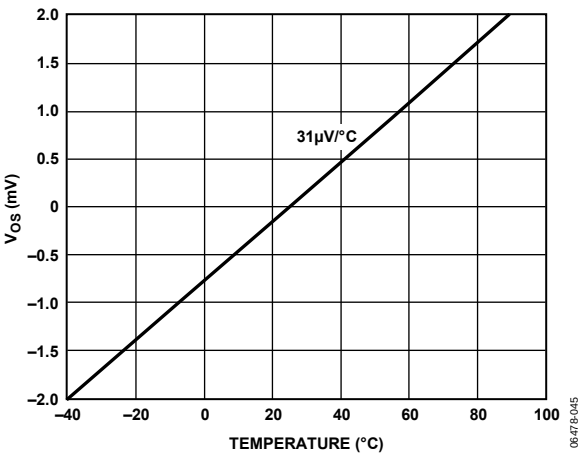



Figure 42. $V_{OS}$ Drift, RTO

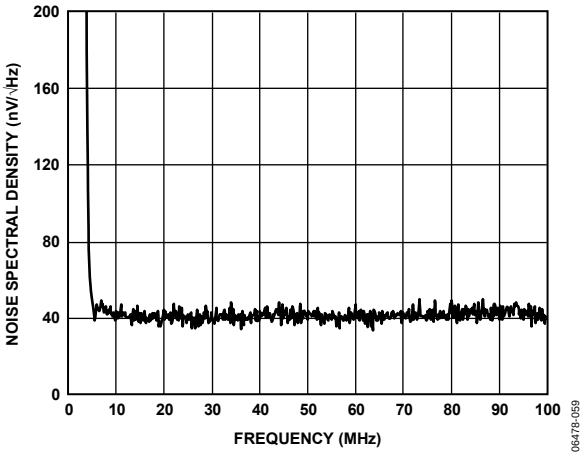



Figure 40. Noise Spectral Density

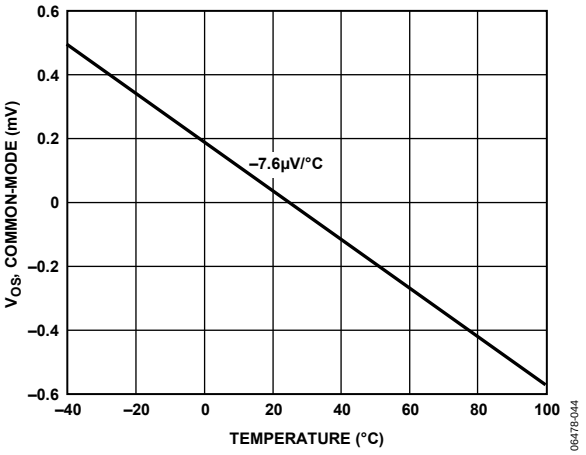



Figure 43. $V_{OS}$ Drift, Common Mode, RTO

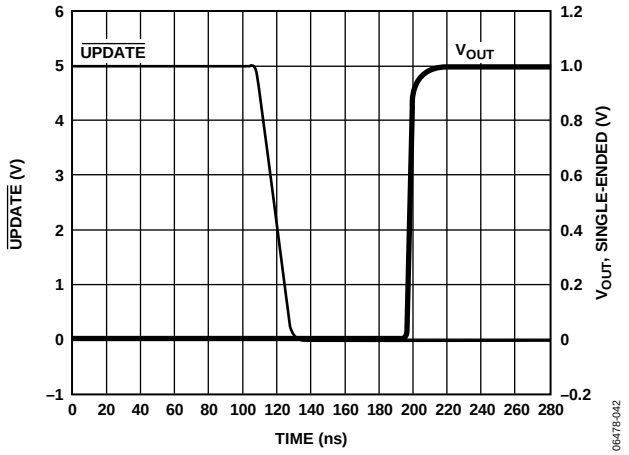



*Figure 44. Enable Time*

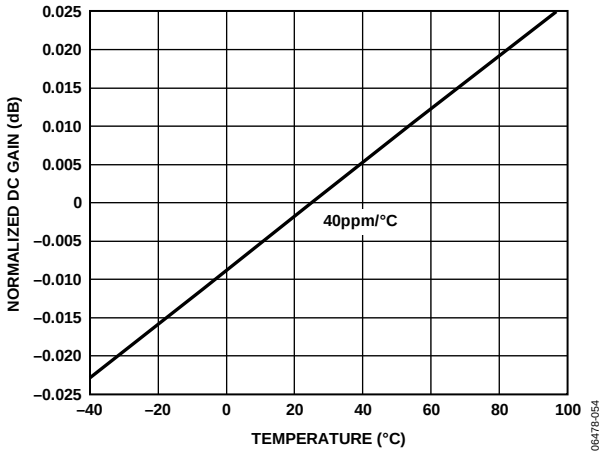



*Figure 45. Normalized DC Gain vs. Temperature*

# THEORY OF OPERATION

The AD8175 is a non-blocking crosspoint with 16 differential RGB input channels and nine differential RGB output channels. Although the AD8175 is primarily meant for differential-in, differential-out middle-of-CAT5-run applications, each differential RGB output channel is complemented by H and V syncs for use in end-of-CAT5-run, single-ended output applications.

Processing of common-mode (CM) voltage levels is achieved by placing the AD8175 in either of its two operation modes. In the first operation mode (CMENC low), the input CM of each RGB differential pair (possibly present either in the form of sync-on CM signaling or noise) is removed through the switch, and the output CM is set to a global reference voltage via the VOCM_CMENCOFF analog input. Therefore, the AD8175 can behave as a differential-in, differential-out switch. If sync-on CM signaling is present at the differential RGB inputs, then the H and V outputs represent decoded syncs. In the second operation mode, input sync-on CM signaling is propagated through the switch. Note that in this mode, as in the previous one, the overall input CM is blocked through the switch. In this mode, the overall output CM is set to a global reference voltage via the VOCM_CMENCON analog input.

In either operation mode, input pin VBLK defines the black level of the positive output phase. The combination of VBLK and VOCM_CMENCOFF allows the user to position the positive and negative output phases anywhere in the allowable output voltage range.

The switch is organized into nine 16:1 RBG multiplexers, with each being responsible for connecting an RGB input channel to its respective RGB output channel. Decoding logic selects a single input (or none) in each multiplexer and connects it to its respective output. Feedback around each multiplexer realizes a closed-loop differential-in, differential-out gain of +2. A second loop realizes a closed-loop common-mode-in gain of +1.

Each differential RGB input channel is buffered by a differential receiver, which is capable of accepting input CM voltages extending all the way to either supply rail. In addition to passing differential information, each receiver processes and routes input CM voltages. Excess closed-loop receiver bandwidth reduces the receiver's effect on the overall device bandwidth.

The output stage is designed for fast slew rate and settling time while driving a series-terminated CAT5 cable. Unlike competing multiplexer designs, the small signal bandwidth closely approaches the large signal bandwidth.

The outputs of the AD8175 can be disabled to minimize on-chip power dissipation. When disabled, there is a feedback network of approximately 2.7 kΩ between the differential outputs. This high impedance allows multiple ICs to be bussed together without additional buffering. Care must be taken to reduce output capacitance, which can result in overshoot and frequency-domain peaking. A series of internal amplifiers drive internal nodes such that wideband high impedance is presented at the disabled output, even while the output bus experiences fast signal swings. When the outputs are disabled and driven externally, the voltage applied to them should not exceed the valid output swing range for the AD8175 in order to keep these internal amplifiers in their linear range of operation. Applying excessive differential voltages to the disabled outputs can cause damage to the AD8175 and should be avoided (see the Absolute Maximum Ratings section of this data sheet for guidelines).

The connectivity of the AD8175 is controlled by a flexible TTL-compatible logic interface. Either parallel or serial loading into a first rank of latches preprograms each output. A global update signal moves the programming data into the second rank of latches, simultaneously updating all outputs. In serial mode, a serial-out pin allows devices to be daisy-chained together for a single-pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs. This power-on reset clears the second rank of latches, but does not clear the first rank of latches. A broadcast parallel programming feature is available in parallel mode to quickly clear the first rank. In serial mode, preprogramming individual inputs is not possible and the entire shift register needs to be flushed. A global chip-select pin gates the input clock and the global update signal to the second rank of buffers.

The AD8175 can operate on a single +5 V supply, powering both the signal path (with the VPOS/VNEG supply pins) and the control logic interface (with the VDD/DGND supply pins). Split supply operation is possible with ±2.5 V supplies in order to easily interface to ground-referenced video signals. In this case, a flexible logic interface allows the control logic supplies (VDD/DGND) to be run off +5 V/0 V to +3.3 V/0 V while the analog core remains on split supplies. Additional flexibility in the analog output common-mode level (VOCM_CMENCOFF) and output black level (VBLK) facilitates operation with unequally split supplies. If +3 V/−2 V supplies to +2 V/−3 V supplies are desired, the output CM can still be set to 0 V for ground-referenced video signals.

# APPLICATIONS

## OPERATING MODES

Depending on the state of the CMENC logic input, the AD8175 can be set in either of two differential-in, differential-out operating modes. An additional application is possible by tapping the outputs single-ended and making use of the decoded H and V outputs.

### *Middle-of-CAT5-Run Application, CM Encoding Turned Off*

In this application, the AD8175 is placed somewhere in the middle of a CAT5 run. By tying CMENC low, the CM of each RGB differential pair is removed through the device (or turned off), while the overall CM at the output is defined by the reference value VOCM_CMENCOFF. In this mode of operation, CM noise is removed, while the intended differential RGB signals are buffered and passed to the outputs. The AD8175 is placed in this operation mode when used in a sync-on color scheme. Figure 46 shows the voltage levels and CM handling for a single input channel connected to a single output channel in a middle-of-CAT5-run application with CM encoding turned off.

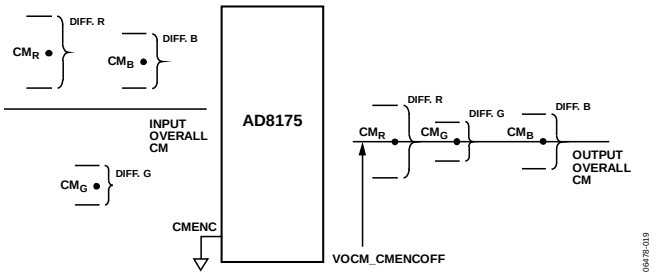



*Figure 46. AD8175 in a Middle-of-CAT5-Run Application, CM Encoding Off (Note that in this application, the H and V outputs, though asserted, are not used)*

Inputs VBLK and VOCM_CMENCOFF allow the user complete flexibility in defining the output CM level and the amount of overlap between the positive and negative phases, thus maximizing output headroom usage. Whenever VBLK differs from VOCM_CMENCOFF by more than approximately ±100 mV, a differential voltage $\Delta_{diff}$ is added at the outputs according to the expression $\Delta_{diff}$ = VBLK − VOCM_CMENCOFF. Conversely, whenever the difference between VBLK and VOCM_CMENCOFF is less than approximately ±100 mV, no differential voltage is added at the outputs.

As a first example, refer to Figure 47. The positive phase of a differential output is shown by the solid line, while the negative phase is shown by the dashed line. The input to the crosspoint is a positive differential pulse with a low level of 0 V and a high level of 0.7 V. The positive and negative outputs are shown with VOCM_CMENCOFF and VBLK both set to 0 V. (Note that both pulses have been slightly shifted off the 0 V line for clarity.)

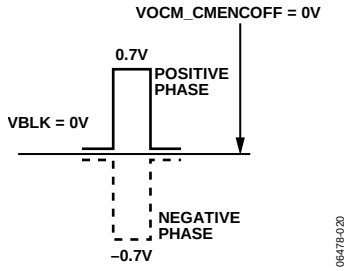



*Figure 47. Output for 0 V to 0.7 V Input Differential Pulse, VBLK = 0 V, VOCM_CMENCOFF = 0 V*

As a second example, refer to Figure 48. VCOM_CMENCOFF is set to 0.35 V, while VBLK is set to −0.35 V. The input is still a differential pulse with a low level of 0 V and a high level of 0.7 V. Note how the positive phase and the negative phase are now shifted with respect to each other by an amount equal to VBLK − VOCM_CMENCOFF or −0.35 V − 0.35 V = −0.7 V. Since the negative output phase spans the same voltage range as the positive output phase, the usable voltage range for single-ended applications is effectively doubled over the previous example. (Note that the output pulses have been slightly shifted with respect to each other for clarity.)

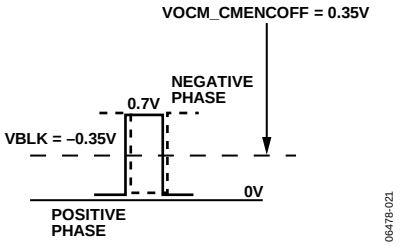



*Figure 48. Output for 0 V to 0.7 V Input Differential Pulse, VBLK = −0.35 V, VOCM_CMENCOFF = 0.35 V*

### *Middle-of-CAT5-Run Application, CM Encoding Turned On*

In this application, the AD8175 is also placed somewhere in the middle of a CAT5 run, although the common-mode handling is different. By tying CMENC high, the CM of each RGB input is passed through the part, while at the same time, the overall output CM is stripped and set equal to the voltage applied at the VOCM_CMENCON pin. The AD8175 is placed in this operation mode when used with a sync-on CM scheme. Although asserted, the H and V outputs are not used in this application. Figure 49 shows the voltage levels and CM handling for a single input channel connected to a single output channel in a middle-of-CAT5-run application with CM encoding turned on.

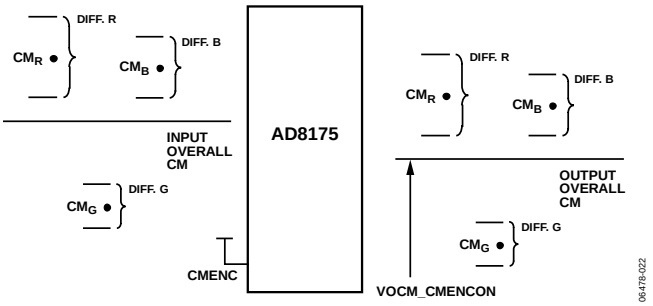



*Figure 49. AD8175 in Middle-of-CAT5-Run Application, CM Encoding On (Note that in this application, the H and V outputs, though asserted, are not used)*

In this operation mode, the difference $\Delta_{diff}$ = VBLK − VOCM_CMENCOFF still adds an output differential voltage, as described in the previous section.

### *End-of-CAT5-Run, CM Encoding Turned Off*

In this application, each AD8175 output is tapped single-ended at the positive phase and followed by a fast buffer to drive a monitor at the end of a CAT5 run (a suitable choice is the AD8003 set up in a noninverting configuration with gain of +4). The H and V outputs can then be used to drive the monitor's sync inputs directly. The relationship between the incoming sync-on CM signaling and the H and V syncs is defined according to Table 16.

**Table 16. H and V Sync Truth Table ($V_{POS}/V_{NEG}$ = ±2.5 V)**

| $CM_R$ | $CM_G$ | $CM_B$ | H | V |
|---|---|---|---|---|
| 0.5 | 0 | 0 | Low | High |
| 0 | 0.5 | −0.5 | Low | Low |
| −0.5 | 0.5 | 0 | High | Low |
| 0 | −0.5 | 0.5 | High | High |

The following two statements are equivalent to the truth table (Table 16) in producing H and V for all allowable CM inputs:

1. H sync is high when the CM of Blue is larger than the CM of Red.
2. V sync is high when the combined CM of Red and Blue is larger then the CM of Green.

## PROGRAMMING

The AD8175 has two options for changing the programming of the crosspoint matrix. In the first option, a serial word of 45 bits can be provided that updates the entire matrix each time. The second option allows for changing a single output's programming via a parallel interface. The serial option requires fewer signals, but more time (clock cycles) for changing the programming; the parallel programming technique requires more signals, but allows for changing a single output at a time, therefore requiring fewer clock cycles.

### *Serial Programming Description*

The serial programming mode uses the device pins $\overline{CS}$, $\overline{CLK}$, SERIN, $\overline{UPDATE}$, and $\overline{SER}$/PAR. The first step is to enable the $\overline{CLK}$ on by pulling $\overline{CS}$ low. Next, $\overline{SER}$/PAR is pulled low to enable the serial programming mode. The parallel clock $\overline{WE}$ should be held high during the entire serial programming operation.

The $\overline{UPDATE}$ signal should be high during the time that data is shifted into the device's serial port. Although the data still shifts in when $\overline{UPDATE}$ is low, the transparent, asynchronous latches allow the shifting data to reach the matrix. This causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at SERIN is clocked in at every falling edge of $\overline{CLK}$. A total of 45 bits must be shifted in to complete the programming. A total of five bits must be supplied for each of the nine RGB output channels—an output enable bit (D4) and four bits (D3 to D0), which determine the input channel. If D4 is low (output disabled), the four associated bits (D3 to D0) do not matter, because no input will be switched to that output.

The most-significant-output-address data is shifted in first, with the enable bit (D4) shifted in first, followed by the input address (D3 to D0) entered sequentially with D3 first and D0 last. Each remaining output is programmed sequentially, until the least-significant-output-address data is shifted in. At this point, $\overline{UPDATE}$ can be taken low, which causes the programming of the device according to the data that was just shifted in. The $\overline{UPDATE}$ latches are asynchronous and when $\overline{UPDATE}$ is low, they are transparent.

If more than one AD8175 device is to be serially programmed in a system, the SEROUT signal from one device can be connected to the SERIN of the next device to form a serial chain. All of the CLK, UPDATE, and SER/PAR pins should be connected in parallel and operated as described above. The serial data is input to the SERIN pin of the first device of the chain, and it will ripple through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence is 45 bits times the number of devices in the chain. CS gates the CLK and UPDATE signals, so that when CS is held high, both CLK and UPDATE are held in their inactive high state, while when CS is held low, both CLK and UPDATE function normally.

### *Parallel Programming Description*

When using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows the modification of a single output or more at a time. Since this takes only one WE/UPDATE cycle, significant time savings can be realized by using parallel programming.

One important consideration in using parallel programming is that the RST signal does not reset all registers in the AD8175. When taken low, the RST signal only sets each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs are not active at the same time.

After initial power-up, the internal registers in the device generally have random data, even though the RST signal has been asserted. If parallel programming is used to program one output, then that output will be properly programmed, but the rest of the device will have a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up. This ensures that the programming matrix is always in a known state. From then on, parallel programming can be used to modify a single output or more at a time.

In similar fashion, if UPDATE is taken low after initial power-up, the random power-up data in the shift register will be programmed into the matrix. Therefore, in order to prevent the crosspoint from being programmed into an unknown state, do not apply a logic level to UPDATE after power is initially applied. Programming the full shift register once to a desired state, by either serial or parallel programming after initial power-up, eliminates the possibility of programming the matrix to an unknown state.

The Chip select (CS) feature is not applicable in parallel programming mode; in other words, it is possible to program the AD8175 in parallel mode when the part is deselected. Refer to the logic diagram shown in Figure 7, which shows that the CS feature gates the serial clock and has no bearing on parallel mode programming. Shared WE lines should therefore not be used in parallel programming mode. To change an output's programming via parallel programming, SER/PAR, UPDATE, and CLK should all be taken high. The parallel clock, WE, should start in the high state. The 4-bit address of the output to be programmed should be put on A3 to A0. Data Bit D3 to Data Bit D0 should contain the information that identifies the input that gets programmed to the output that is addressed. Data Bit D4 determines the enabled state of the output. If D4 is low (output disabled), then the data on D3 to D0 does not matter.

After the desired address and data signals have been established, they can be latched into the shift register by a high-to-low transition of the WE signal. The matrix is not programmed, however, until the UPDATE signal is taken low. It is thus possible to latch in new data for several or all of the outputs first via successive negative transitions of WE while UPDATE is held high, and then have all the new data take effect when UPDATE goes low. This is the technique that should be used when programming the device for the first time after power-up when using parallel programming.

### *Reset*

When powering up the AD8175, it is usually desirable to have the outputs come up in the disabled state. The RST pin, when taken low, causes all outputs to be in the disabled state. However, the RST signal does not reset all registers in the AD8175. This is important when operating in the parallel programming mode. Refer to the Serial Programming Description section for information about programming internal registers after power-up. Serial programming programs the entire matrix each time, so no special considerations apply.

Since the data in the shift register is random after power-up, it should not be used to program the matrix, or the matrix can enter unknown states. To prevent this, do not apply a logic low signal to UPDATE initially after power-up. The shift register should first be loaded with the desired data, and only then can the UPDATE be taken low to program the device.

The RST pin has a 20 kΩ pull-up resistor to VDD that can be used to create a simple power-up reset circuit. A capacitor from RST to ground holds RST low for some time while the rest of the device stabilizes. The low condition causes all the outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thus allowing full programming capability of the device.

### *Broadcast*

The AD8175 logic interface has a broadcast mode, in which all first rank latches can be simultaneously parallel-programmed to the same data in one write-cycle. This is especially useful in clearing random first rank data after power-up. To access the broadcast mode, the part is parallel-programmed using the device pins WE, A0 to A3, D0 to D4 and UPDATE. The only

difference is that the $\overline{SER}$/PAR pin is held low, as if serial programming were taking place. By holding $\overline{CLK}$ high, no serial clocking will occur, and instead, the $\overline{WE}$ can be used to clock all first rank latches in the chip at once.

## DIFFERENTIAL AND SINGLE-ENDED OPERATION

Although the AD8175 has fully differential inputs and outputs, it can also be operated in a single-ended fashion. Single-ended and differential configurations are discussed below, along with implications on gain, impedances, and terminations.

### *Differential Input*

Each differential input to the AD8175 is applied to a differential receiver. These receivers allow the user to drive the inputs with an uncertain common-mode voltage, such as from a remote source over twisted pair. The receivers respond only to the differences in input voltages and restore an internal common-mode suitable for the internal signal path. Noise or crosstalk, which affect each receiver's inputs equally, are rejected by the input stage, as specified by its common-mode rejection ratio (CMRR).

Furthermore, the overall common-mode voltage of all three differential pairs comprising an RGB channel is processed and rejected by a separate circuit block. For example, a static discharge or a resistive voltage drop in a middle-of-CAT5-run with sync-on CM signaling coupling into all three pairs in an RGB channel are rejected at the output of the AD8175, while the sync-on CM signals are allowed through the switch.

The circuit configuration used by the differential input receivers is similar to that of several Analog Devices general-purpose differential amplifiers, such as the AD8131. The topology is that of a voltage-feedback amplifier with internal gain resistors. The input differential impedance for each receiver is 5 kΩ in parallel with 10 kΩ or 3.33 kΩ, as shown in Figure 50.

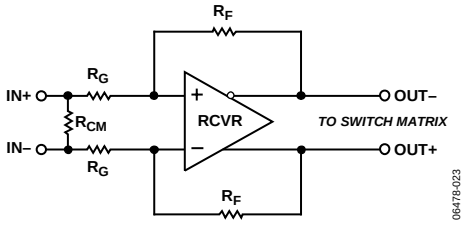



*Figure 50. Input Receiver Equivalent Circuit*

This impedance creates a small differential termination error if the user does not account for the 3.33 kΩ parallel element. However, this error is less than 1% in most cases. Additionally, the source impedance driving the AD8175 appears in parallel with the internal gain-setting resistors, such that there may be a gain error for some values of source resistance. The AD8175 is adjusted such that its gain is correct when driven by a back-terminated CAT5 cable (25 Ω effective impedance to ground at each input pin, or 100 Ω differential source impedance across pairs of input pins). If a different source impedance is presented, the differential gain of the AD8175 can be calculated as

$$G_{dm} = \frac{2.525\ \text{k}\Omega}{2.5\ \text{k}\Omega + R_S}$$

where $R_S$ is the effective impedance to ground at each input pin.

When operating with a differential input, care must be taken to keep the common-mode, or average, of the input voltages within the linear operating range of the AD8175 receiver. For the AD8175 receiver, this common-mode range can extend rail-to-rail, provided the differential signal swing is small enough to avoid forward biasing the ESD diodes (it is safest to keep the common-mode plus differential signal excursions within the supply voltages of the part).

The input voltage of the AD8175 is linear for ±1 V of differential input voltage difference (this limitation is primarily due to ability of the output to swing close to the rails, since the differential gain through the part is +2). Beyond this level, the signal path will saturate and limit the signal swing. This is not a desired operation, as the supply current will increase and the signal path will be slow to recover from clipping. The absolute maximum allowed differential input signal is limited by long-term reliability of the input stage. The limits in the Absolute Maximum Ratings section of the data sheet should be observed in order to avoid degrading device performance permanently.

#### AC Coupling of Inputs

It is possible to ac-couple the inputs of the AD8175 receiver, so that bias current does not need to be supplied externally. A capacitor in series with the inputs to the AD8175 creates a high-pass filter with the input impedance of the device. This capacitor needs to be sized large enough so that the corner frequency includes all frequencies of interest.

### *Single-Ended Input*

The AD8175 input receiver can be driven single-endedly (unbalanced). Single-ended inputs apply a component of common-mode signal to the receiver inputs, which is then rejected by the receiver (see the Specifications section for common-mode-to-differential-mode ratio of the part).

The single-ended input resistance $R_{IN}$ differs from the differential input impedance, and is equal to

$$R_{IN} = \frac{R_G}{1 - \dfrac{R_F}{2 \times (R_G + R_F)}}$$

with $R_G$ and $R_F$ as shown in Figure 50.

Note that this value is smaller than the differential input resistance, but it is larger than $R_G$. The difference is due to the component of common-mode level applied to the receiver by single-ended inputs. A second, smaller component of input resistance ($R_{CM}$, also shown in Figure 50) is present across the inputs in both single-ended and differential operation.

In single-ended operation, an input is driven, while the undriven input is often tied to midsupply or ground. Since

signal-frequency current flows at the undriven input, such input should be treated as a signal line in the board design. For example, in order to achieve best dynamic performance, the undriven input should be terminated with an impedance matching that seen by the part at the driven input.

### *Differential Output*

#### Benefits of Differential Operation

The AD8175 has a fully-differential switch core with differential outputs. The two output voltages move in opposite directions, with a differential feedback loop maintaining a fixed output stage differential gain of +2. This differential output stage provides improved crosstalk cancellation due to parasitic coupling from one output to another being equal and out of phase. Additionally, if the output of the device is utilized in a differential design, then noise, crosstalk, and offset voltages generated on-chip that are coupled equally into both outputs are reduced by the common-mode rejection ratio of the next device in the signal chain. By utilizing the AD8175 outputs in a differential application, the best possible noise and offset specifications can be realized.

#### Common-Mode Gain

The common-mode, or average voltage of pairs of output signals, is set by the voltage on the VOCM_CMENCOFF pin when common-mode encoding is off (CMENC is logic low), or by the voltage on the VOCM_CMENCON pin when common-mode encoding is on (CMENC is logic high). Note that in the latter case, VCOM_CMENCON sets the overall common-mode of RGB triplets of differential outputs, while the individual common-mode of each RGB output is free to change. VCOM_CMENCON and VCOM_CMENCOFF are typically set to midsupply (often ground), but can be moved approximately ±0.5 V in order to accommodate cases where the desired output common-mode voltage may not be midsupply (as in the case of unequal split supplies). Adjusting the output common-mode voltage beyond ±0.5 V can limit differential swing internally below the specifications on the data sheet. The overall common-mode of the output voltages follows the voltage applied to VOCM_CMENCON or VCOM_CMENCOFF, implying a gain of +1. Likewise, sync-on common-mode signaling is carried through the AD8175 (CMENC must be in its high state), implying a gain of +1 for this path as well.

The common-mode reference pins are analog signal inputs, common to all output stages on the device. They require only small amounts of bias current, but noise appearing on these pins is buffered to all the output stages. As such, they should be connected to low noise, low impedance voltage references to avoid being sources of noise, offset, and crosstalk in the signal path.

#### Termination

The AD8175 is designed to drive 100 Ω terminated to ground on each output (or an effective 200 Ω differential) while meeting data sheet specifications over the specified operating temperature range, if care is taken to observe the maximum power derating curves.

Termination at the load end is recommended to shorten settling time and for best signal integrity. In differential signal paths, it is often desirable to series-terminate the outputs, with a resistor in series with each output. A side effect of termination is an attenuation of the output signal by a factor of two. In this case, gain is usually necessary somewhere else in the signal path to restore the signal level.

Whenever a differential output is used single-ended, it is desirable to terminate the used single-ended output with a series resistor, as well as to place a resistor on the unused output to match the load seen by the used output.

When disabled, the outputs float to midsupply. A small current is required to drive the outputs away from their midsupply state. This current is easily provided by an AD8175 output (in its enabled state) bussed together with the disabled output. Exceeding the allowed output voltage range may saturate internal nodes in the disabled output, and consequently an increase in disabled output current may be observed.

### *Single-Ended Output*

#### Usage

The AD8175 output pairs can be used single-ended, taking only one output and not using the second. This is often desired to reduce the routing complexity in the design, or because a single-ended load is being driven directly. This mode of operation produces good results, but has some shortcomings when compared to taking the output differentially. When observing the single-ended output, noise that is common to both outputs appears in the output signal.

When observing the output single-ended, the distribution of offset voltages will appear greater. In the differential case, the difference between the outputs when the difference between the inputs is zero is a small differential offset. This offset is created from mismatches in devices in the signal path. In the single-ended case, this differential offset is still observed, but an additional offset component is also relevant. This additional component is the common-mode offset, which is the difference between the average of the outputs and the output common-mode reference. This offset is created by mismatches that affect the signal path in a common-mode manner. A differential receiver rejects this common-mode offset voltage, but in the single-ended case, this offset is observed with respect to the signal ground. The single-ended output sums half the differential offset voltage and all of the common-mode offset voltage for a net increase in observed offset.

#### Single-Ended Gain

The AD8175 operates as a closed-loop differential amplifier. The primary control loop forces the difference between the output terminals to be a ratio of the difference between the

input terminals. One output increases in voltage, while the other decreases an equal amount to make the total output voltage difference correct. The average of these output voltages is forced to the voltage on the common-mode reference terminal (VOCM_CMENCOFF or VOCM_CMENCON) by a second control loop. If only one output terminal is observed with respect to the common-mode reference terminal, only half of the difference voltage will be observed. This implies that when using only one output of the device, half of the differential gain is observed. An AD8175 taken with single-ended output appears to have a gain of +1.

It is important to note that all considerations applying to the used output phase regarding output voltage headroom, apply unchanged to the complement output phase even if this is not actually used.

**Termination**

When operating the AD8175 with a single-ended output, the preferred output termination scheme is to refer the load to the output common-mode. A series-termination can be used, at an additional cost of one half the signal gain.

In single-ended output operation, the complementary phase of the output is not used, and may or may not be terminated locally. Although the unused output can be floated to reduce power dissipation, there are several reasons for terminating the unused output with a load resistance matched to the load on the signal output.

One component of crosstalk is magnetic coupling by mutual inductance between output package traces and bond wires that carry load current. In a differential design, there is coupling from one pair of outputs to other adjacent pairs of outputs. The differential nature of the output signal simultaneously drives the coupling field in one direction for one phase of the output, and in an opposite direction for the other phase of the output. These magnetic fields do not couple equally into adjacent output pairs due to different proximities, but they do destructively cancel the crosstalk to some extent. If the load current in each output is equal, this cancellation will be greater and less adjacent crosstalk will be observed (regardless of whether the second output is actually being used).

A second benefit of balancing the output loads in a differential pair is to reduce fluctuations in current requirements from the power supply. In single-ended loads, the load currents alternate from the positive supply to the negative supply. This creates a parasitic signal voltage in the supply pins due to the finite resistance and inductance of the supplies. This supply fluctuation appears as crosstalk in all outputs, attenuated by the power supply rejection ratio (PSRR) of the device. At low frequencies, this is a negligible component of crosstalk, but PSRR falls off as frequency increases. With differential, balanced loads, as one output draws current from the positive supply, the other output draws current from the negative supply. When the phase alternates, the first output draws current from the negative supply and the second from the positive supply. The effect is that a more constant current is drawn from each supply, such that the crosstalk-inducing supply fluctuation is minimized.

A third benefit of driving balanced loads can be seen if one considers that the output pulse response changes as load changes. The differential signal control loop in the AD8175 forces the difference of the outputs to be a fixed ratio to the difference of the inputs. If the two output responses are different due to loading, this creates a difference that the control loop sees as signal response error, and it will attempt to correct this error. This distorts the output signal from the ideal response compared to the case when the two outputs are balanced.

***Decoupling***

The signal path of the AD8175 is based on high open-loop gain amplifiers with negative feedback. Dominant-pole compensation is used on-chip to stabilize these amplifiers over the range of expected applied swing and load conditions. To guarantee this designed stability, proper supply decoupling is necessary with respect to both the differential control loops and the common-mode control loops of the signal path. Signal-generated currents must return to their sources through low impedance paths at all frequencies in which there is still loop gain (up to 700 MHz at a minimum).

The signal path compensation capacitors in the AD8175 are connected to the VNEG supply. At high frequencies, this limits the power supply rejection ratio (PSRR) from the VNEG supply to a lower value than that from the VPOS supply. If given a choice, an application board should be designed such that the VNEG power is supplied from a low inductance plane, subject to a least amount of noise.

VOCM_CMENCON and VOCM_CMENCOFF are high speed common-mode control loops of all output drivers. In the single-ended output sense, there is no rejection from noise on these inputs to the outputs. For this reason, care must be taken to produce low noise sources over the entire range of frequencies of interest. This is not only important to single-ended operation, but to differential operation, as there is a common-mode-to-differential gain conversion that becomes greater at higher frequencies.

VOCM_CMENCON and VOCM_CMENCOFF are internally buffered to prevent transient currents from flowing into or out of these inputs and becoming sources of crosstalk, by acting on their respective source impedances.

### *Power Dissipation*

#### Calculation of Power Dissipation

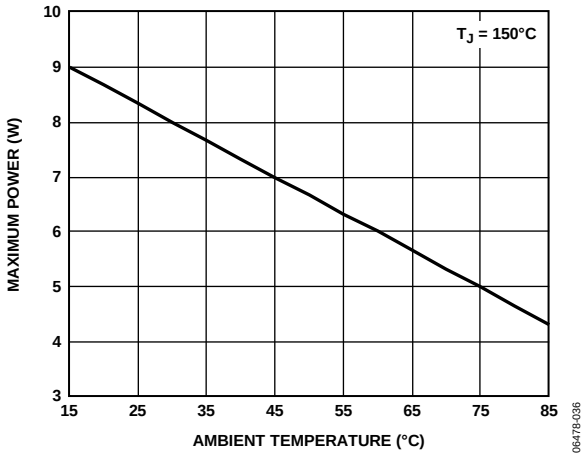



*Figure 51. Maximum Die Power Dissipation vs. Ambient Temperature*

The curve in Figure 51 was calculated from

$$P_{D,MAX} = \frac{T_{JUNCTION,MAX} - T_{AMBIENT}}{\theta_{JA}} \quad (1)$$

As an example, if the AD8175 is enclosed in an environment at 45 C ($T_A$), the total on-chip dissipation under all load and supply conditions must not be allowed to exceed 7.0 W.

When calculating on-chip power dissipation, it is necessary to include the power dissipated in the output devices due to current flowing in the loads. For a sinusoidal output about ground and symmetrical split supplies, the on-chip power dissipation due the load can be approximated by

$$P_{D,OUTPUT} = \left(V_{POS} - V_{OUTPUT,RMS}\right) \times I_{OUTPUT,RMS} \quad (2)$$

For nonsinusoidal output, the power dissipation should be calculated by integrating the on-chip voltage drop across the output devices multiplied by the load current over one period.

The user can subtract the quiescent current for the Class AB output stage when calculating the loaded power dissipation. For each output stage driving a load, subtract a quiescent power, according to

$$P_{DQ,OUTPUT} = (V_{POS} - V_{NEG}) \times I_{OUTPUT,QUIESCENT} \quad (3)$$

where $I_{OUTPUT, QUIESCENT}$ = 1.65 mA for each single-ended output pin for the AD8175.

For each disabled RGB output channel, the quiescent power supply current in VPOS and VNEG drops by approximately 34 mA.

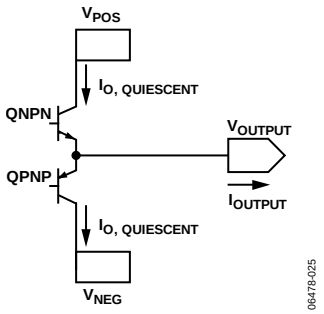



*Figure 52. Simplified Output Stage*

#### Example

For the AD8175, with an ambient temperature of 85°C, all nine RGB output channels driving 1 $V_{rms}$ into 100 Ω loads, and power supplies at ±2.5 V, follow these steps:

1. Calculate power dissipation of AD8175 using data sheet quiescent currents. Neglecting $V_{DD}$ current, as it is insignificant.

$$P_{D,QUIESCENT} = \left(V_{POS} \times I_{VPOS}\right) + \left(V_{NEG} \times I_{VNEG}\right) \quad (4)$$

$$P_{D,QUIESCENT} = \left(2.5\text{ V} \times 600\text{ mA}\right) + \left(2.5\text{ V} \times 600\text{ mA}\right) = 3\text{ W}$$

2. Calculate power dissipation from loads. For a differential output and ground-referenced load, the output power is symmetrical in each output phase.

$$P_{D,OUTPUT} = \left(V_{POS} - V_{OUTPUT,RMS}\right) \times I_{OUTPUT,RMS} \quad (5)$$

$$P_{D,OUTPUT} = (2.5\text{ V} - 1\text{ V}) \times (1\text{ V}/100\ \Omega) = 15\text{ mW}$$

There are 27 output pairs, or 54 output currents.

$$nP_{D,OUTPUT} = 54 \times 15\text{ mW} = 0.81\text{ W}$$

3. Subtract quiescent output stage current for number of loads (54 in this example). The output stage is either standing or driving a load, but the current only needs to be counted once (valid for output voltages > 0.5 V).

$$P_{DQ,OUTPUT} = \left(V_{POS} - V_{NEG}\right) \times I_{OUTPUT,QUIESCENT} \quad (6)$$

$$P_{DQ,OUTPUT} = \left(2.5\text{ V} - (-2.5\text{ V})\right) \times 1.65\text{ mA} = 8.25\text{ mW}$$

There are 27 output pairs, or 54 output currents.

$$nP_{DQ,OUTPUT} = 54 \times 8.25\text{ mW} = 0.45\text{ W}$$

4. Verify that the power dissipation does not exceed the maximum allowed value.

$$P_{D,ON-CHIP} = P_{D,QUIESCENT} + nP_{D,OUTPUT} - nP_{DQ,OUTPUT} \quad (7)$$

$$P_{D,ON-CHIP} = 3\text{ W} + 0.81\text{ W} - 0.45\text{ W} = 3.36\text{ W}$$

From Figure 51 or Equation 1, this power dissipation is below the maximum allowed dissipation for all ambient temperatures up to and including 85°C.

In a general case, the power delivered by the digital supply and dissipated into the digital output devices has to be taken into account following a similar derivation. However, since the loads driven by the H and V outputs is high and since the voltage at these outputs typically sits close to either rail, the correction to the on-chip power estimate is small. Furthermore, the H and V outputs are active only briefly during sync generation and returned to digital ground thereafter.

**Short-Circuit Output Conditions**

Although there is short-circuit current protection on the AD8175 outputs, the output current can reach values of 80 mA into a grounded output. Any sustained operation with too many shorted outputs can exceed the maximum die temperature and can result in device failure (see the Absolute Maximum Ratings section).

### *Crosstalk*

Many systems (such KVM switches) that handle numerous analog signal channels have strict requirements for keeping the various signals from influencing any of the other signals in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in close proximity in a system, as is undoubtedly the case in a system that uses the AD8175, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required in order to specify a system that uses one or more crosspoint devices.

**Types of Crosstalk**

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field, and the sharing of common impedances. This section explains these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (for example, free space) and couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities, so the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk. The fact that the AD8175 is a fully-differential design means that many sources of crosstalk either destructively cancel, or are common-mode to the signal and can be rejected by a differential receiver.

**Areas of Crosstalk**

A practical AD8175 circuit must be mounted to an actual circuit board in order to connect it to power supplies and measurement equipment. Great care has been taken to create an evaluation board (available upon request) that adds minimum crosstalk to the intrinsic device. This, however, raises the issue that a system's crosstalk is a combination of the intrinsic crosstalk of the devices in addition to the circuit board to which they are mounted. It is important to try to separate these two areas when attempting to minimize the effect of crosstalk.

In addition, crosstalk can occur among the inputs to a crosspoint and among the outputs. It can also occur from input to output. Techniques are discussed in the following sections for diagnosing which part of a system is contributing to crosstalk.

**Measuring Crosstalk**

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by

$$|XT| = 20\log_{10}\left(\frac{A_{SEL}(s)}{A_{TEST}(s)}\right) \quad (8)$$

where:
$s = j\omega$, the Laplace transform variable
$A_{SEL}(s)$ is the amplitude of the crosstalk induced signal in the selected channel.
$A_{TEST}(s)$ is the amplitude of the test signal.

It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). In addition, the crosstalk signal has a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the triple 16×9 matrix of the AD8175, we can look at the number of crosstalk terms that can be considered for a single channel, for

example, input channel INPUT0. INPUT0 is programmed to connect to one of the AD8175 outputs where the measurement can be made.

First, the crosstalk terms associated with driving a test signal into each of the other 15 input channels can be measured one at a time, while applying no signal to INPUT0. Then, the crosstalk terms associated with driving a parallel test signal into all 15 other inputs can be measured two at a time in all possible combinations, then three at a time, and so on, until, finally, there is only one way to drive a test signal into all 15 other input channels in parallel.

Each of these cases is legitimately different from the others and might yield a unique value, depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other outputs (not used for measurement) are taken into consideration, the numbers rather quickly grow to astronomical proportions. If a larger crosspoint array of multiple AD8175s is constructed, the numbers grow larger still.

Obviously, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all hostile crosstalk; this means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this yields the worst crosstalk number, but this is not always the case, due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements are generally higher than those of more distant channels, so they can serve as a worst-case measure for any other one-channel or two-channel crosstalk measurements.

**Input and Output Crosstalk**

Capacitive coupling is voltage-driven (dV/dt), but is generally a constant ratio. Capacitive crosstalk is proportional to input or output voltage, but this ratio is not reduced by simply reducing signal swings. Attenuation factors must be changed by changing impedances (lowering mutual capacitance), or destructive canceling must be utilized by summing equal and out of phase components. For high input impedance devices such as the AD8175, capacitances generally dominate input-generated crosstalk.

Inductive coupling is proportional to current (dI/dt), and often scales as a constant ratio with signal voltage, but also shows a dependence on impedances (load current). Inductive coupling can also be reduced by constructive canceling of equal and out of phase fields. In the case of driving low impedance video loads, output inductances contribute highly to output crosstalk.

The flexible programming capability of the AD8175 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input channel (INPUT7 roughly in the middle for this example) can be programmed to drive OUTPUT4 (exactly in the middle). The inputs to INPUT7 are just terminated to ground (via 50 Ω or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically provided by a distribution amplifier), with all other outputs except OUTPUT4 disabled. Since grounded INPUT7 is programmed to drive OUTPUT4, no signal should be present. Any signal that is present can be attributed to the other 15 hostile input signals, because no other outputs are driven (they are all disabled). Thus, this method measures the all-hostile input contribution to crosstalk into INPUT7. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (INPUT0, for example) and all outputs other than a given output (OUTPUT4 in the middle) are programmed to connect to INPUT0. OUTPUT4 is programmed to connect to INPUT15 (far away from INPUT0), which is terminated to ground. Thus, OUTPUT4 should not have a signal present since it is listening to a quiet input. Any signal measured at the OUTPUT4 can be attributed to the output crosstalk of the other eight hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

**Effect of Impedances on Crosstalk**

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the PC board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}\left[(R_S C_M) \times s\right] \quad (9)$$

where:
$R_S$ is the source resistance.
$C_M$ is the mutual capacitance between the test signal circuit and the selected circuit.
$s$ is the Laplace transform variable.

From Equation 9, it can be observed that this crosstalk mechanism has a high-pass nature; it can also be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is

driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8175 is specified with excellent settling time when driving a properly terminated CAT5, the crosstalk is higher than the minimum obtainable due to the high output currents. These currents induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8175.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer with a mutual inductance between the windings that drives a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}\left(M_{XY} \times \frac{s}{R_L}\right) \quad (10)$$

where:
$M_{XY}$ is the mutual inductance of Output X to Output Y.
$R_L$ is the load resistance on the measured output.

This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing $R_L$. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

**PCB Layout**

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing, and supply bypassing.

The packaging of the AD8175 is designed to help keep the crosstalk to a minimum. On the BGA substrate, each pair is carefully routed to predominately couple to each other, with shielding traces separating adjacent signal pairs. The ball grid array is arranged such that similar board routing can be achieved. Input and output differential pairs are grouped by channel rather than by color to allow for easy, convenient board routing.

The input and output signals have minimum crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The input and output signals surface at the input termination resistors and the output series back-termination resistors. To the extent possible, these signals should also be separated as soon as they emerge from the IC package.

**PCB Termination Layout**

As frequencies of operation increase, the importance of proper transmission line signal routing becomes more important. The bandwidth of the AD8175 is large enough that using high impedance routing does not provide a flat in-band frequency response for practical signal trace lengths. It is necessary for the user to choose a characteristic impedance suitable for the application and properly terminate the input and output signals of the AD8175. Traditionally, video applications have used 75 Ω single-ended environments. RF applications are generally 50 Ω single-ended (and board manufacturers have the most experience with this application). CAT-5 cabling is usually driven as differential pairs of 100 Ω differential impedance.

For flexibility, the AD8175 does not contain on-chip termination resistors. This flexibility in application comes with some board layout challenges. The distance between the termination of the input transmission line and the AD8175 die is a high impedance stub, and causes reflections of the input signal. With some simplification, it can be shown that these reflections cause peaking of the input at regular intervals in frequency, dependent on the propagation speed ($V_P$) of the signal in the chosen board material and the distance (d) between the termination resistor and the AD8175. If the distance is great enough, these peaks can occur in-band. In fact, practical experience shows that these peaks are not high-Q, and should be pushed out to three or four times the desired bandwidth in order to not have an effect on the signal. For a board designer using FR4 ($V_P = 144 \times 10^6$ m/s), this means the AD8175 should be no more than 1.5 cm after the termination resistors, and preferably should be placed even closer. The BGA substrate routing inside the AD8175 is approximately 1 cm in length and adds to the stub length, so 1.5 cm PCB routing equates to $d = 2.5 \times 10^{-2}$ m in the calculations.

$$f_{PEAK} = \frac{(2n+1)V_P}{4d} \quad (11)$$

where $n$ = {0, 1, 2, 3, ...}.

In some cases, it is difficult to place the termination close to the AD8175 due to space constraints, differential routing, and large resistor footprints. A preferable solution in this case is to maintain a controlled transmission line past the AD8175 inputs and terminate the end of the line. This is known as fly-by termination. The input impedance of the AD8175 is large enough and stub length inside the package is small enough that this works well in practice. Implementation of fly-by input termination often includes bringing the signal in on one routing layer, then passing through a filled via under the AD8175 input ball, then back out to termination on another signal layer. In this case, care must be taken to tie the reference ground planes together near the signal via if the signal layers are referenced to different ground planes.

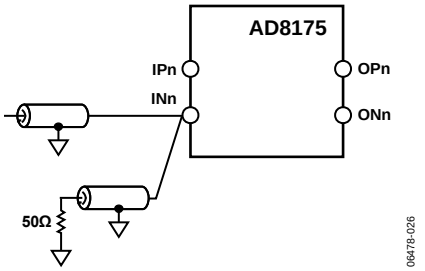



*Figure 53. Fly-By Input Termination (Grounds for the two transmission lines shown must be tied together close to the INn pin)*

If multiple AD8175s are to be driven in parallel, a fly-by input termination scheme is very useful, but the distance from each AD8175 input to the driven input transmission line is a stub that should be minimized in length and parasitics using the discussed guidelines.

When driving the AD8175 single-endedly, the undriven input is often terminated with a resistance in order to balance the input stage. It can be seen that by terminating the undriven input with a resistor of one-half the characteristic impedance, the input stage will be perfectly balanced (25 Ω, for example, to balance the two parallel 50 Ω terminations on the driven input). However, due to the feedback in the input receiver, there is high speed signal current leaving the undriven input. In order to terminate this high speed signal, proper transmission line techniques should be used. One solution is to adjust the trace width to create a transmission line of half the characteristic impedance and terminate the far end with this resistance (25 Ω in a 50 Ω system). This is not often practical as trace widths become large. In most cases, the best practical solution is to place the half-characteristic impedance resistor as close as possible (preferably less than 1.5 cm away) and to reduce the parasitics of the stub (by removing the ground plane under the stub, for example). In either case, the designer must decide if the layout complexity created by a balanced, terminated solution is preferable to simply grounding the undriven input at the ball with no trace.

While the examples discussed so far are for input termination, the theory is similar for output back-termination. Taking the AD8175 as an ideal voltage source, any distance of routing between the AD8175 and a back-termination resistor will be an impedance mismatch that potentially creates reflections. For this reason, back-termination resistors should also be placed close to the AD8175. In practice, because back-termination resistors are series elements, they can be placed close to the AD8175 outputs.

Finally, the AD8175 pinout allows the user to bring the outputs out as surface traces to the back-termination resistors. The designer can avoid creating stubs and reflections by keeping the AD8175 output signal path on the surface of the board. A stub is created when a top-to-bottom via connection is made on the output signal path that is perpendicular to the signal flow.

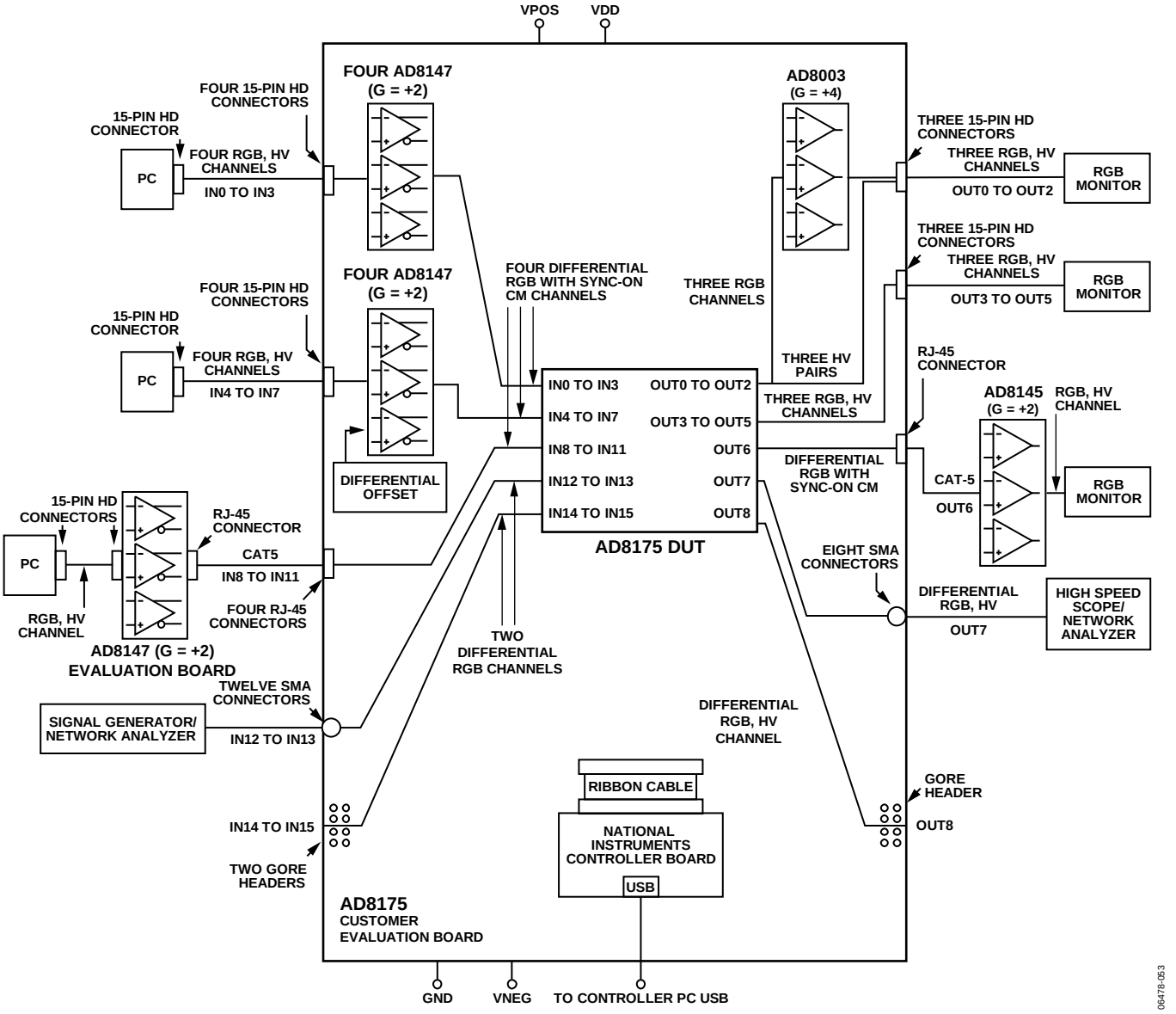
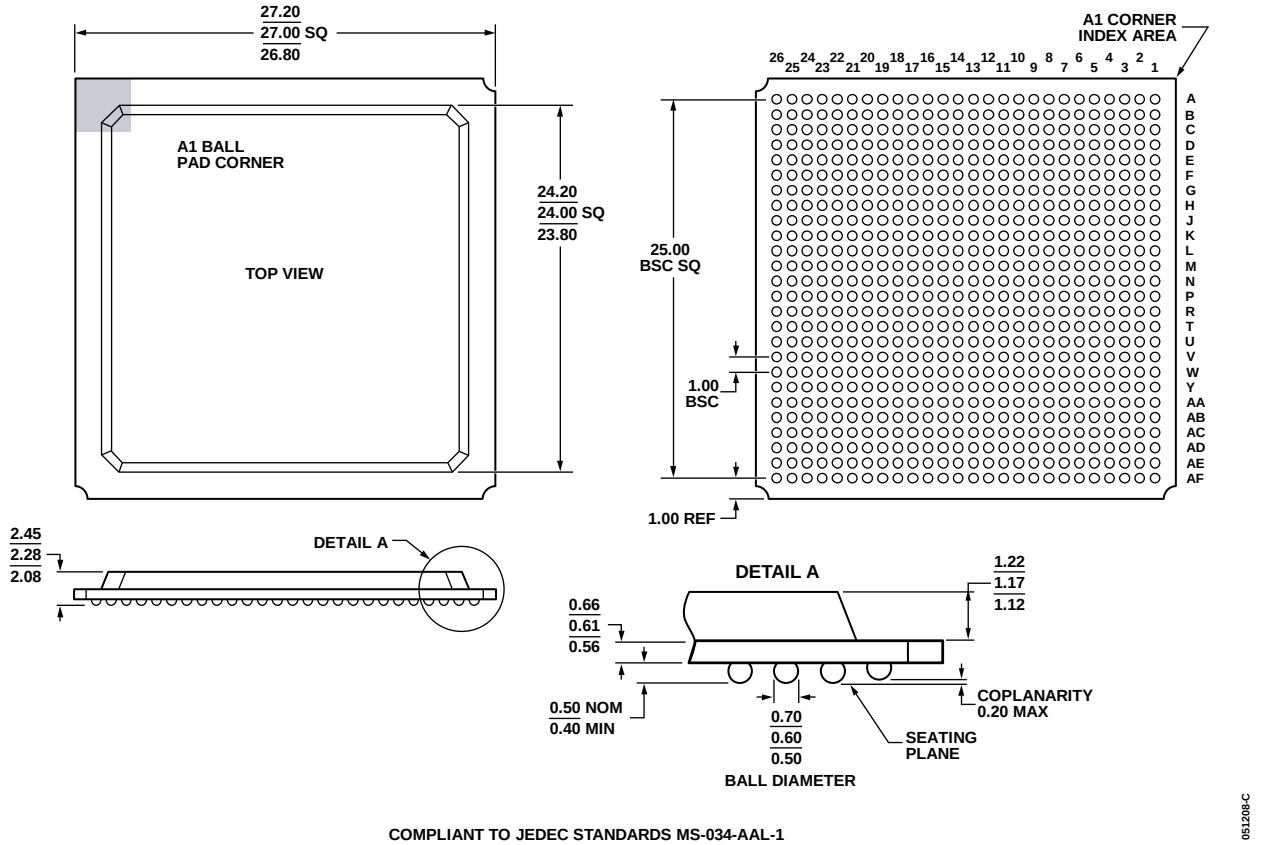



*Figure 54. Evaluation Board Block Diagram*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-034-AAL-1

*Figure 55. 676-Ball Plastic Ball Grid Array [PBGA]*
*(B-676)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD8175ABPZ | −40°C to +85°C | 676-Ball Plastic Ball Grid Array [PBGA] | B-676 |
| AD8175-EVALZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

## NOTES

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