

SBOS320D – SEPTEMBER 2004 – REVISED APRIL 2013

Dual, Wideband, Low-Power, Current Feedback Operational Amplifier

FEATURES

- **UNITY GAIN STABLE BANDWIDTH: 1500MHz**
- **HIGH GAIN OF 2V/V BANDWIDTH: 690MHz**
- **LOW SUPPLY CURRENT: 5.8mA/ch**
- **HIGH SLEW RATE: 1700V/μs**
- **HIGH FULL-POWER BANDWIDTH: 670MHz**
- **LOW DIFFERENTIAL GAIN/PHASE: 0.03%/0.015°**

APPLICATIONS

- **MEDICAL IMAGING**
- **WIDEBAND VIDEO LINE DRIVER**
- **DIFFERENTIAL RECEIVER**
- **ADC DRIVER**
- **HIGH-SPEED SIGNAL PROCESSING**
- **PULSE AMPLIFIER**
- **IMPROVED REPLACEMENT FOR OPA2658**

RELATED PRODUCTS

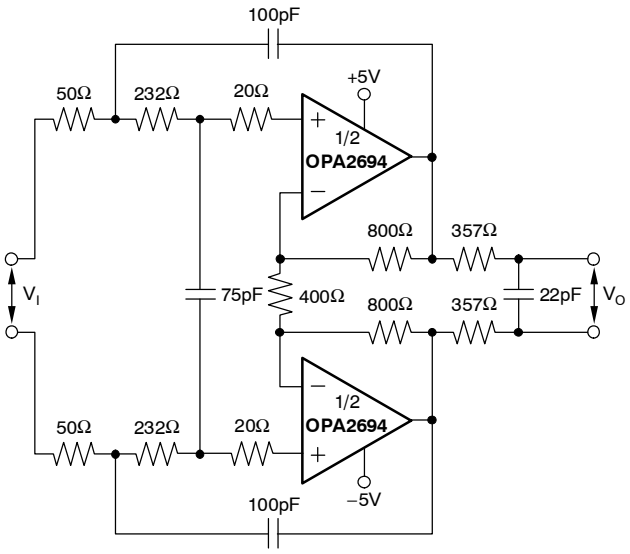
SINGLES	DUALS	TRIPLES	QUADS	FEATURES
OPA694	—	—	—	
OPA683	OPA2683	—	—	Low-Power, CFB_{PLUS}
OPA684	OPA2684	OPA3684	OPA4684	Low-Power, CFB_{PLUS}
OPA691	OPA2691	OPA3691	—	High Output Current
OPA695	OPA2695	OPA3695	—	High Intercept

DESCRIPTION

The OPA2694 is a dual, ultra-wideband, low-power, current feedback operational amplifier f eaturing high slew rate and low differential gain/phase errors. An improved output stage provides ±70mA output drive with < 1.5V output voltage headroom. Low supply current with > 500MHz bandwidth meets the requirements of high density video routers. Being a current feedback design, the OPA2694 holds its bandwidth to very high gains—at a gain of 10, the OPA2694 will still provide > 200MHz bandwidth.

RF applications can use the OPA2694 as a low-power SAW pre-amplifier. Extremely high 3rd-order intercept is provided through 70MHz at much lower quiescent power than many typical RF amplifiers.

The OPA2694 is available in an industry-standard pinout in an SO-8 package.



Low-Power, Differential I/O, 3rd-Order Butterworth Active Filter

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Voltage Range	±V_S
Storage Temperature Range: D, DBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)	3000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	100V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

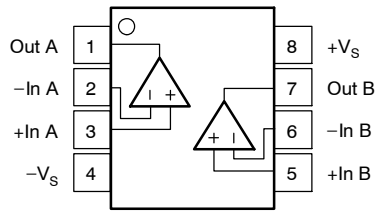
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2694	SO-8	D	–40°C to +85°C	OPA2694	OPA2694ID	Rails, 100
					OPA2694IDR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATION

TOP VIEW **SO-8**



ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.** At $R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2V/V, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2694ID TYP +25°C	OPA2694ID MIN/MAX OVER TEMPERATURE 0°C to 70°C(2)	OPA2694ID MIN/MAX OVER TEMPERATURE –40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)							
Small-Signal Bandwidth	G = +1, $V_O = 0.5V_{PP}$, $R_F = 430\Omega$	1500			MHz	typ	C
	G = +2, $V_O = 0.5V_{PP}$, $R_F = 390\Omega$	690	340	330	320	MHz	min	B
	G = +5, $V_O = 0.5V_{PP}$, $R_F = 330\Omega$	250	190	170	150	MHz	min	B
	G = +10, $V_O = 0.5V_{PP}$, $R_F = 180\Omega$	200	140	120	110	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +1, $V_O = 0.5V_{PP}$, $R_F = 430\Omega$	90			MHz	min	B
Peaking at a Gain of +1	$V_O \le 0.1V_{PP}$, $R_F = 430\Omega$	2			dB	typ	C
Large-Signal Bandwidth	G = +2, $V_O = 2V_{PP}$	670			MHz	typ	C
Slew Rate	G = +2, 2V Step	1700	1300	1275	1250	V/µs	min	B
Rise Time and Fall Time	G = +2, V_O = 0.2V Step	0.8			ns	typ	C
Settling Time to 0.01%	G = +2, V_O = 2V Step	20			ns	typ	C
to 0.1%	G = +2, V_O = 2V Step	13			ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, $V_O = 2V_{PP}$	—			—	—	—
2nd-Harmonic	$R_L = 100\Omega$	–85	–78	–72	–70	dBc	max	B
	$R_L \ge 500\Omega$	–92	–87	–85	–83	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–72	–68	–66	–65	dBc	max	B
	$R_L \ge 500\Omega$	–93	–87	–85	–83	dBc	max	B
Input Voltage Noise	f > 1MHz	2.1	2.5	2.9	3.1	nV/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	22	25	26	29	pA/√Hz	max	B
Non-inverting Input Current Noise	f > 1MHz	24	27	28	30	pA/√Hz	max	B
NTSC Differential Gain	$V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.03			%	max	C
	$V_O = 1.4V_{PP}$, $R_L = 37.5\Omega$	0.05			%	max	C
NTSC Differential Phase	G = +2, V_O – $1.4V_{PP}$, $R_L = 150\Omega$	0.015			°	typ	C
	V_O – $1.4V_{PP}$, $R_L = 37.5\Omega$	0.15			°	typ	C
Channel-to-Channel Crosstalk	f = 5MHz	63			dB	typ	C
DC PERFORMANCE(4)							
Open-Loop Transimpedance	V_O = 0V, $R_L = 100\Omega$	145	**88**	63	58	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±0.7	**±3.2**	±3.9	±4.3	mV	max	A
Average Input Offset Voltage Drift	V_{CM} = 0V	—		12	15	µV/°C	max	B
Channel to Channel ΔV_{IO}	V_{CM} = 0V	±0.5				mV	typ	C
Noninverting Input Bias Current	V_{CM} = 0V	±5	**±22**	±28	±33	µA	max	A
Average Input Bias Current Drift	V_{CM} = 0V	—		±100	±150	nA/°C	max	B
Channel to Channel ΔI_{BI}	V_{CM} = 0V	±5				µA	typ	C
Inverting Input Bias Current	V_{CM} = 0V	±4	**±20**	±28	±40	µA	max	A
Average Input Bias Current Drift	V_{CM} = 0V	—		±150	±200	nA/°C	max	B
Channel to Channel ΔI_{BN}	V_{CM} = 0V	±4				µA	typ	C
INPUT							
Common-Mode Input Voltage(5) (CMIR)		±2.5	**±2.3**	±2.2	±2.1	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	60	**54**	52	50	dB	min	A
Noninverting Input Impedance		280 ‖ 1.2				kΩ ‖ pF	typ	C
Inverting Input Resistance	Open-Loop	30				Ω	typ	C
OUTPUT							
Voltage Output Voltage	No Load	±4	**±3.8**	±3.7	±3.6	V	min	A
	$R_L = 100\Omega$	±3.4	**±3.1**	±3.1	±3.0	V	min	A
Output Current	V_O = 0V	±70	**±55**	±53	±45	mA	min	A
Short-Circuit Output Current	V_O = 0V	±200				mA	typ	C
Closed-Loop Output Impedance	G = +2, f =100kHz	0.02				Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C.** At R_F = 402Ω, R_L = 100Ω, and G = +2V/V, unless otherwise noted.

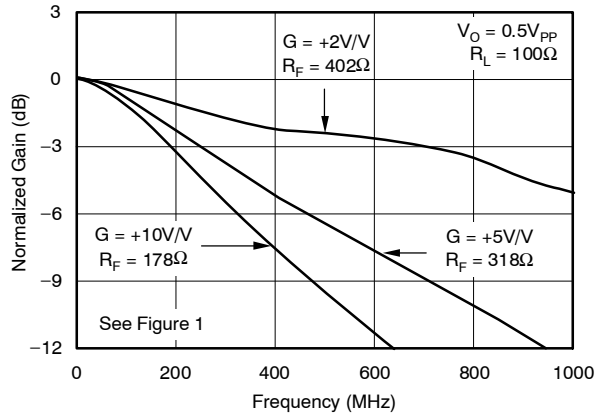
PARAMETER	CONDITIONS	OPA2694ID				UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)			
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range		—	**±6.3**	±6.3	±6.3	V	max	A
Minimum Operating Voltage Range		—	±3.5	±3.5	±3.5	mA	max	B
Maximum Quiescent Current	V_S = ±5V, Both Channels	11.6	**12.1**	12.5	12.7	mA	max	A
Minimum Quiescent Current	V_S = ±5V, Both Channels	11.6	**11.1**	10.5	9.9	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	58	**53**	51	49	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}	Junction-to-Ambient	—				—	—	—
D SO-8		125				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

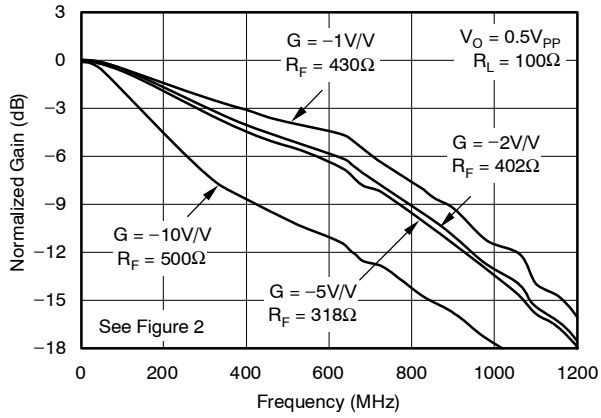
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2V/V, unless otherwise noted

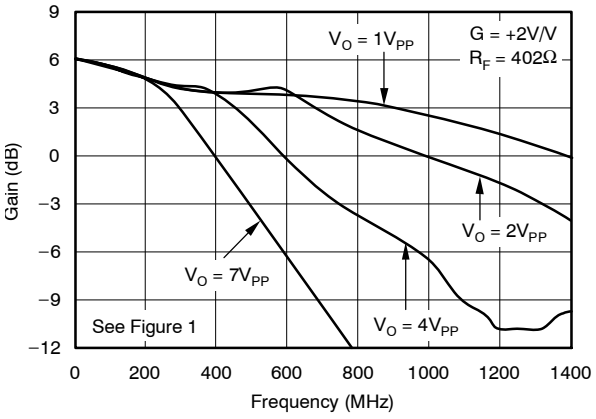
NONINVERTING SMALL–SIGNAL FREQUENCY RESPONSE



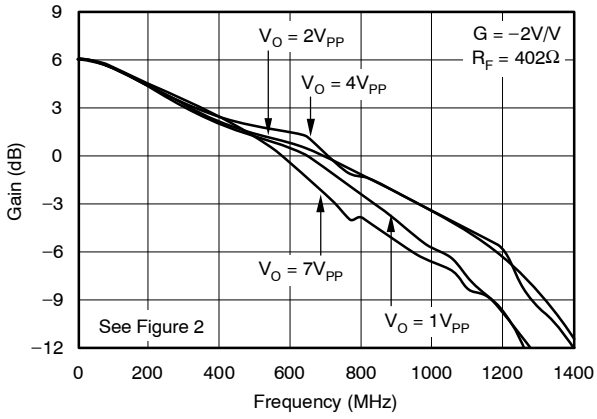
INVERTING SMALL–SIGNAL FREQUENCY RESPONSE



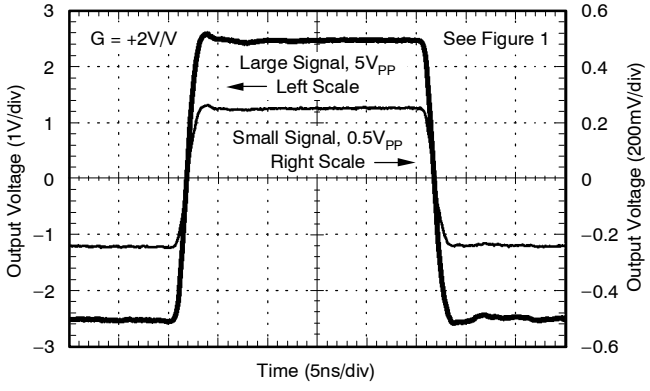
NONINVERTING LARGE–SIGNAL FREQUENCY RESPONSE



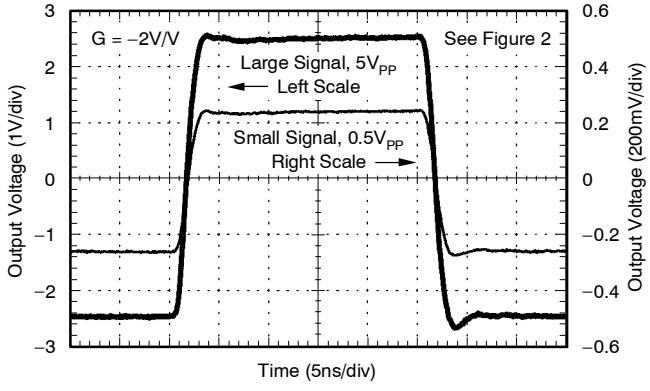
INVERTING LARGE–SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



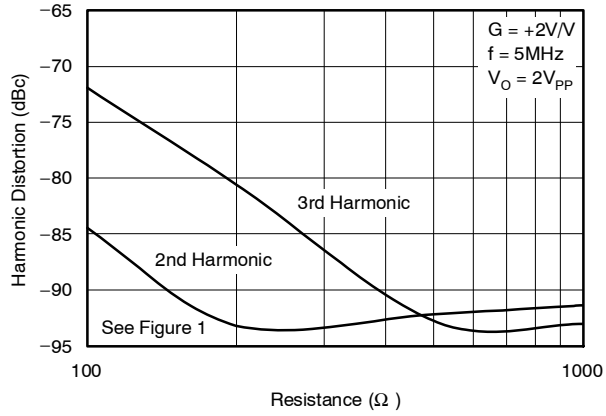
INVERTING PULSE RESPONSE



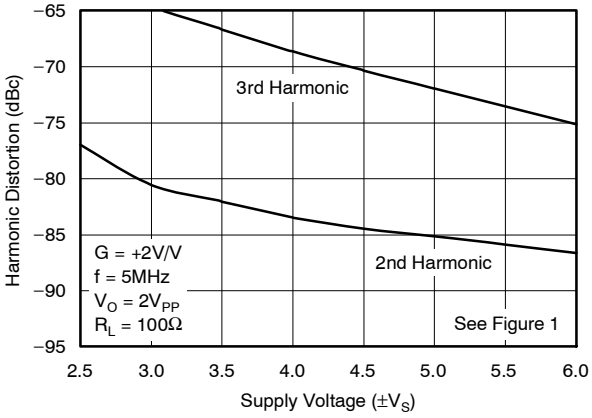
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2V/V, unless otherwise noted

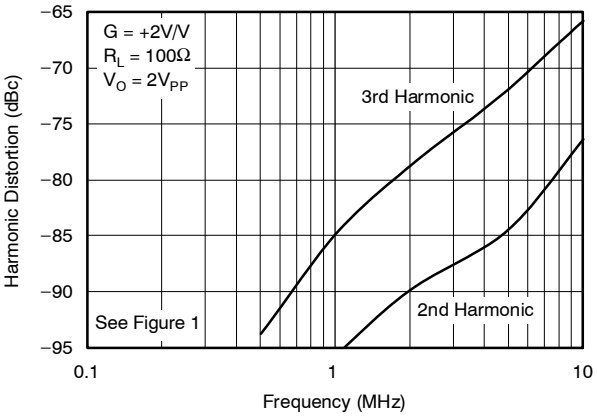
HARMONIC DISTORTION
vs LOAD RESISTANCE



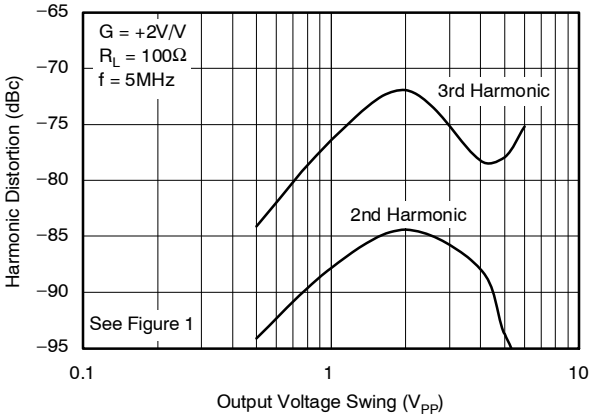
HARMONIC DISTORTION
vs SUPPLY VOLTAGE



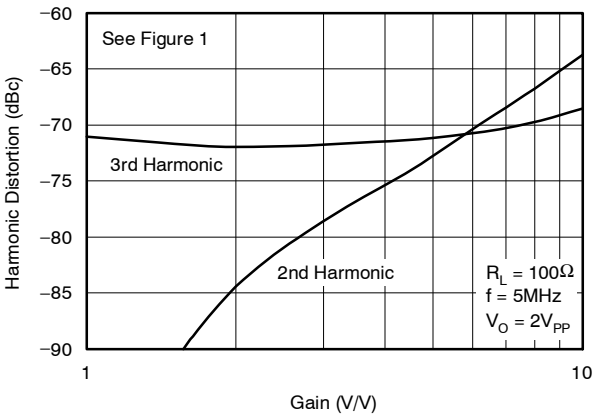
HARMONIC DISTORTION
vs FREQUENCY



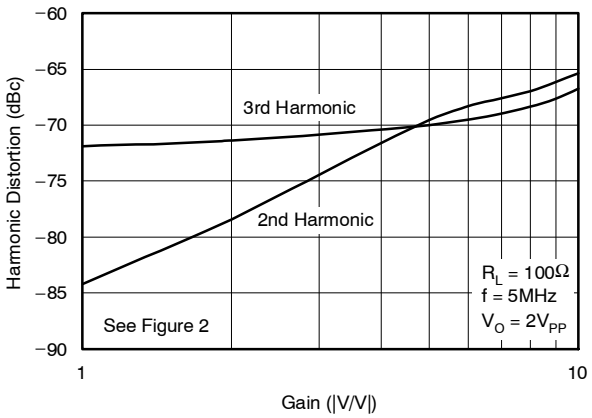
5MHz HARMONIC DISTORTION
vs OUTPUT VOLTAGE



HARMONIC DISTORTION
vs NONINVERTING GAIN



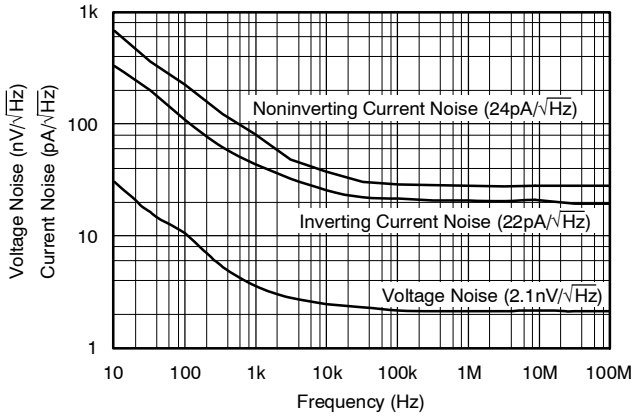
HARMONIC DISTORTION
vs INVERTING GAIN



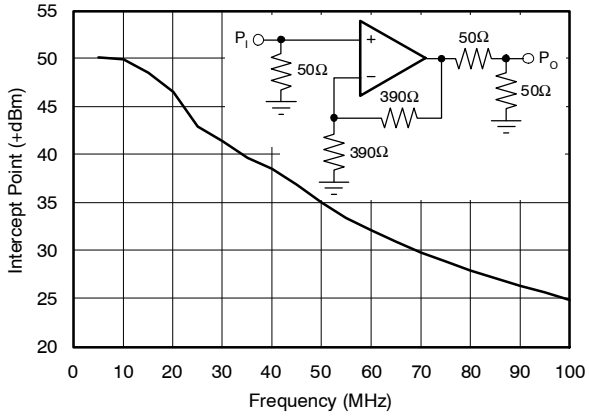
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2V/V, unless otherwise noted

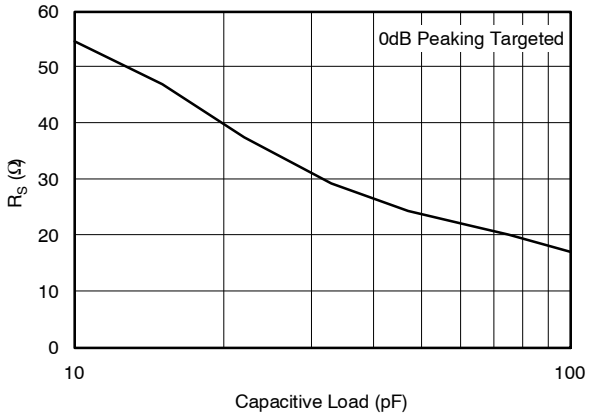
INPUT VOLTAGE AND CURRENT NOISE



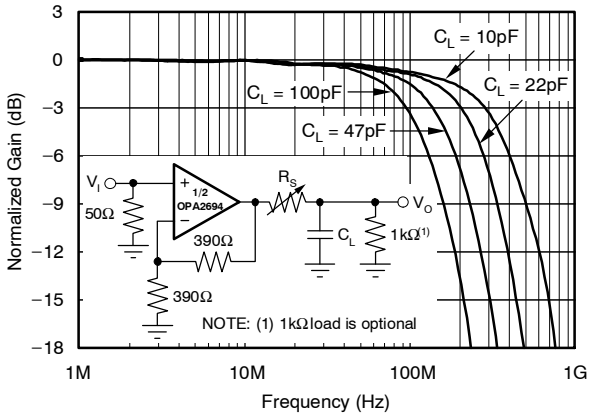
2–TONE, 3rd–ORDER INTERMODULATION INTERCEPT



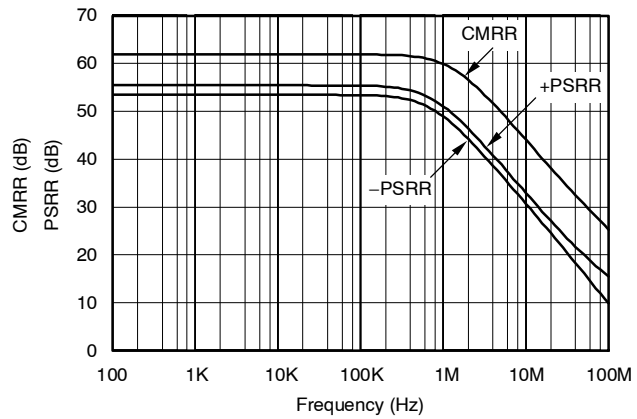
RECOMMENDED R_S vs CAPACITIVE LOAD



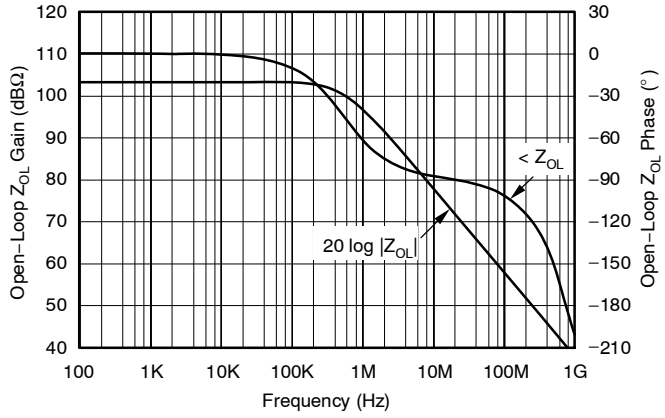
FREQUENCY RESPONSE vs CAPACITIVE LOAD



COMMON–MODE REJECTION RATIO AND POWER–SUPPLY REJECTION RATIO vs FREQUENCY



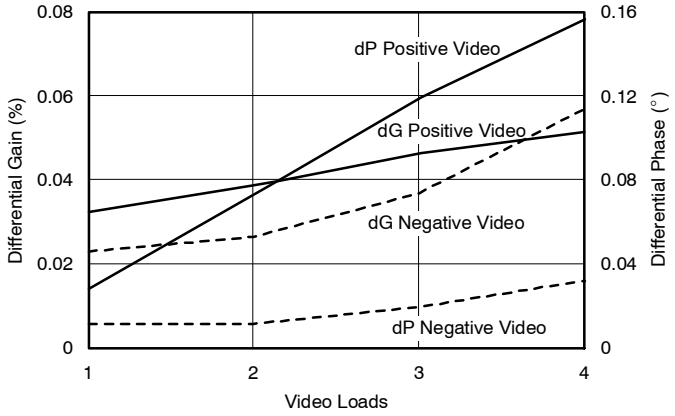
OPEN–LOOP Z_{OL} GAIN AND PHASE



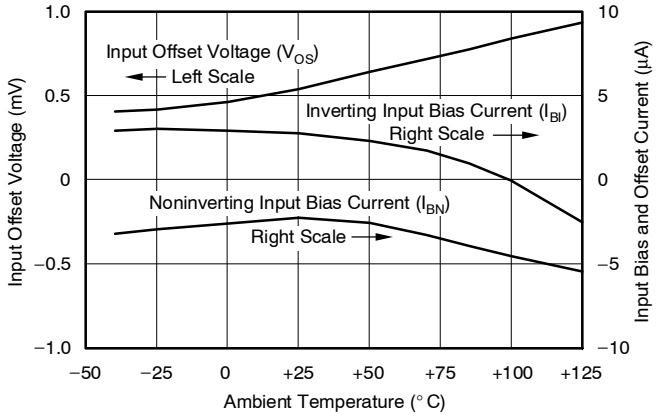
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2V/V, unless otherwise noted

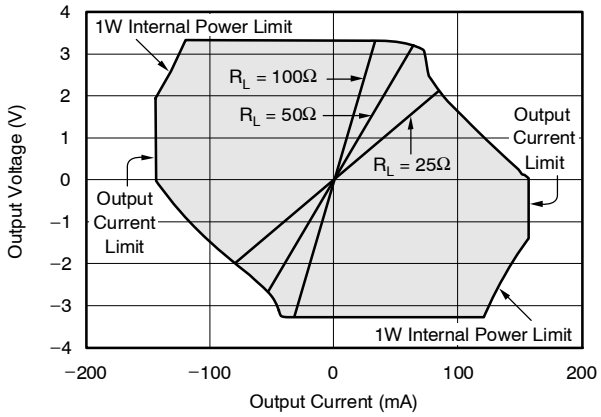
VIDEO DIFFERENTIAL GAIN/DIFFERNTIAL PHASE
(No Pulldown)



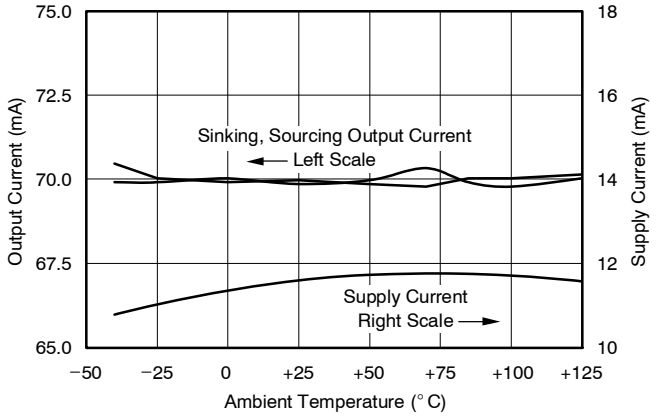
TYPICAL DC DRIFT
OVER TEMPERATURE



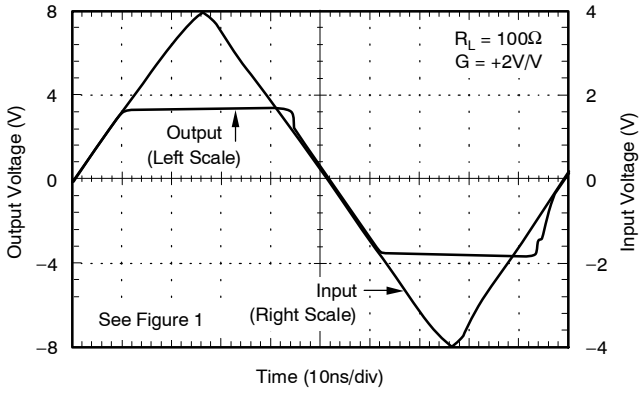
OUTPUT VOLTAGE
AND CURRENT LIMITATIONS



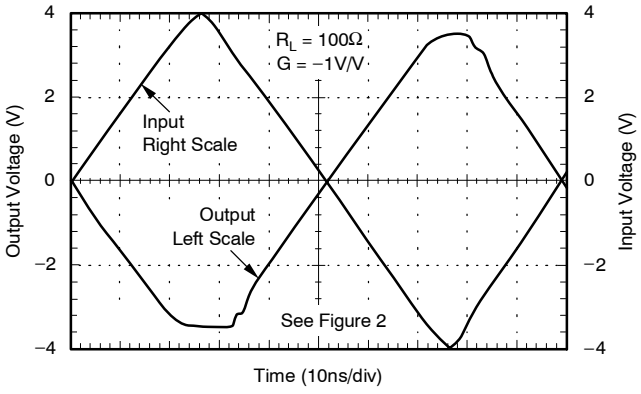
SUPPLY AND OUTPUT CURRENT
vs TEMPERATURE



NONINVERTING
OVERDRIVE RECOVERY

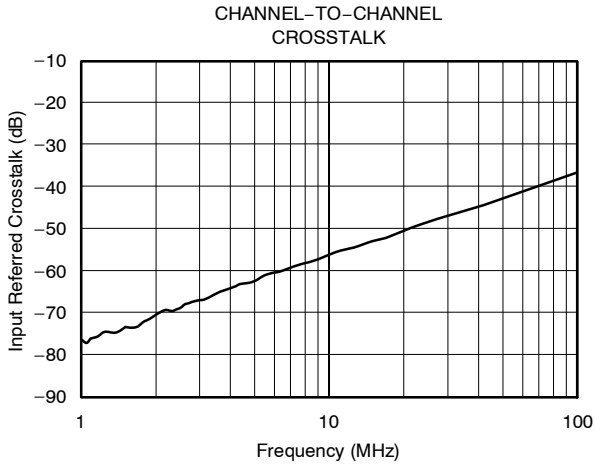


INVERTING
OVERDRIVE RECOVERY



TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

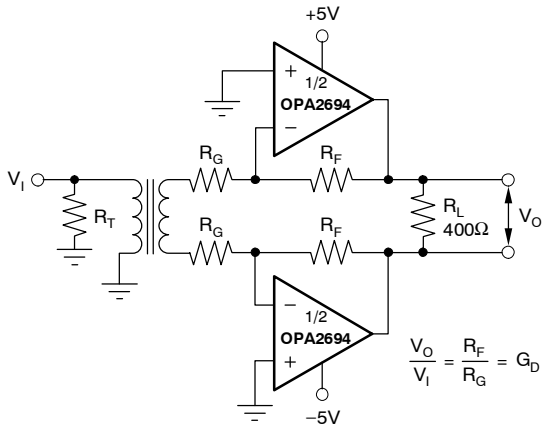
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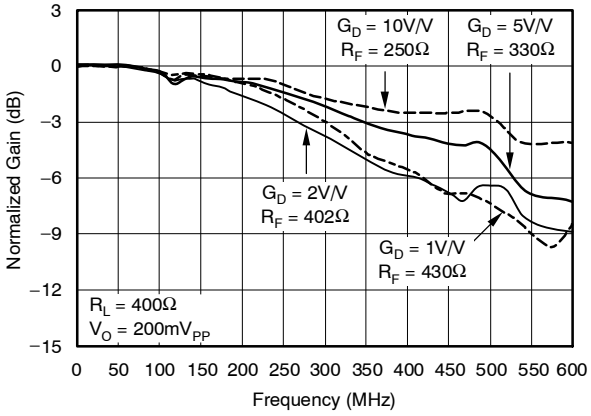
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2V/V, unless otherwise noted

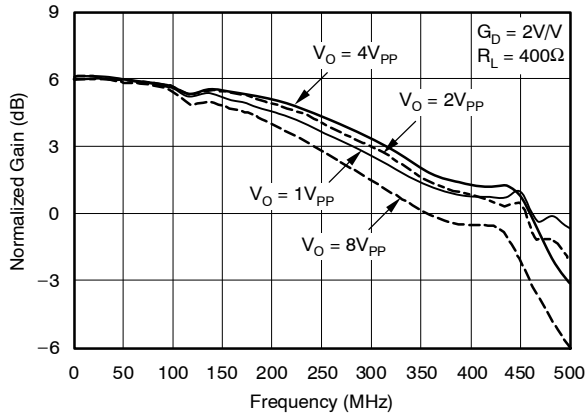
Differential Performance Test Circuit



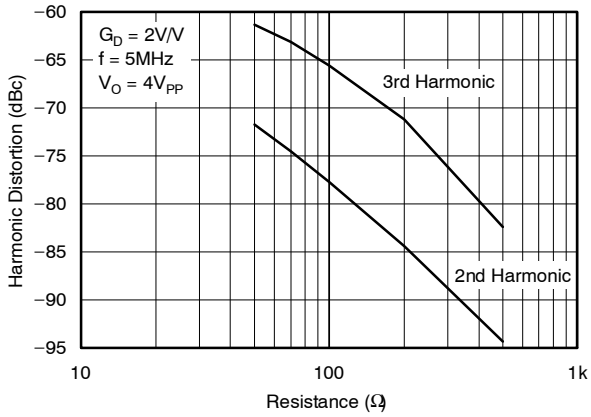
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



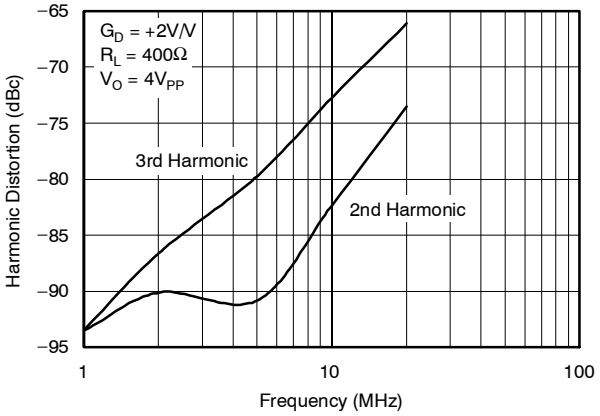
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



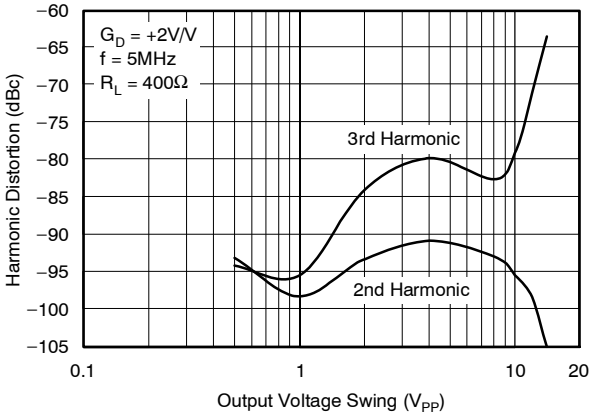
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATION INFORMATION

WIDEBAND CURRENT FEEDBACK OPERATION

The OPA2694 provides exceptional AC performance for a wideband, low-power, current-feedback operational amplifier. Requiring only 5.8mA/ch quiescent current, the OPA2694 offers a 690MHz bandwidth at a gain of +2, along with a 1700V/µs slew rate. An improved output stage provides ±70mA output drive, along with < 1.5V output voltage headroom. This combination of low power and high bandwidth can benefit high-resolution video applications.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristic tables and Typical Characteristic curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Charateristics are taken directly at the input and output pins, while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 804Ω = 89Ω. One optional component is included in Figure 1. In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical PCB layouts, this optional added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

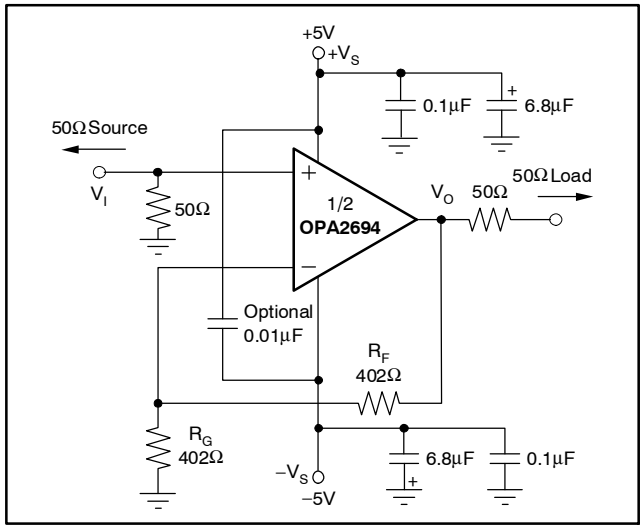


Figure 1. DC-Coupled, G = +2, Bipolar-Supply Specification and Test Circuit

Figure 2 shows the DC-coupled, gain of –2V/V, dual power-supply circuit used as the basis of the inverting Typical Characteristic curves. Inverting operation offers several performance benefits. Since there is no common-mode signal across the input stage, the slew rate for inverting operation is higher and the distortion performance is slightly improved. An additional input resistor, R_T, is included in Figure 2 to set the input impedance equal to 50Ω. The parallel combination of R_T and R_G sets the input impedance. Both the noninverting and inverting applications of Figure 1 and Figure 2 will benefit from optimizing the feedback resistor (R_F) value for bandwidth (see the discussion in *Setting Resistor Values to Optimize Bandwidth*). The typical design sequence is to select the R_F value for best bandwidth, set R_G for the gain, then set R_T for the desired input impedance. As the gain increases for the inverting configuration, a point will be reached where R_G will equal 50Ω, where R_T is removed and the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, R_F is simply increased, to increase gain. This will, however, quickly reduce the achievable bandwidth, as shown by the inverting gain of –10 frequency response in the Typical Characteristic curves. For gains > 10V/V (14dB at the matched load), noninverting operation is recommended to maintain broader bandwidth.

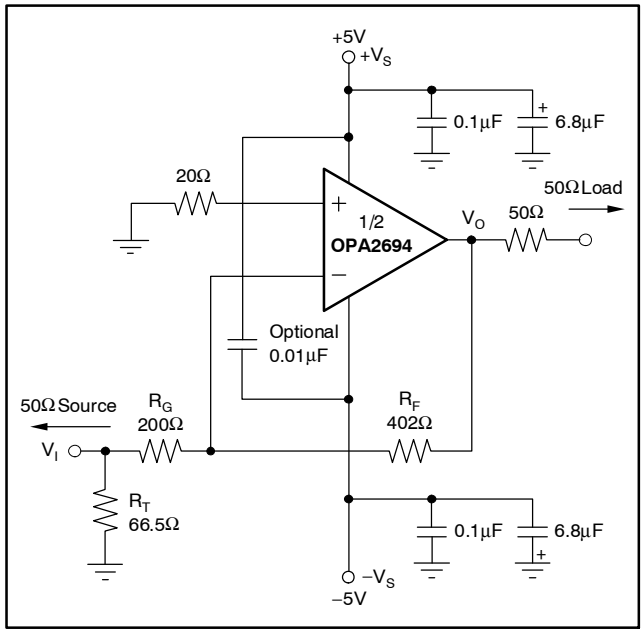


Figure 2. DC-Coupled, G = –2V/V, Bipolar-Supply Specification and Test Circuit

ADC DRIVER

Most modern, high-performance analog-to-digital converters (ADCs), such as Texas Instruments ADS522x series, require a low-noise, low-distortion driver. The OPA2694 combines low-voltage noise (2.1nV/$\sqrt{Hz}$) with low harmonic distortion. Figure 3 shows an example of a wideband, AC-coupled, 12-bit ADC driver.

One OPA2694 is used in the circuit of Figure 3 to form a differential driver for the ADS5220. The OPA2694 offers > 150MHz bandwidth at a differential gain of 5V/V, with a $2V_{PP}$ output swing. A 2nd-order RLC filter is used in order to limit the noise from the amplifier and provide some attenuation for higher-frequency harmonic distortion.

WIDEBAND INVERTING SUMMING AMPLIFIER

Since the signal bandwidth for a current-feedback op amp can be controlled independently of the noise gain (NG), which is normally the same as the noninverting signal gain), wideband inverting summing stages may be implemented using the OPA2694. The circuit in Figure 4 shows an example inverting summing amplifier, where the resistor values have been adjusted to maintain both maximum bandwidth and input impedance matching. If each RF signal is assumed to be driven from a 50Ω source, the NG for this circuit will be (1 + 100Ω/(100Ω/5)) = 6. The total feedback impedance (from V_O to the inverting error current) is the sum of R_F + (R_I • NG). where R_I is the impedance looking into the inverting input from the summing junction (see the *Setting Resistor Values to Optimize Performance* section). Using 100Ω feedback (to get a signal gain of −2 from each input to the output pin) requires an additional 30Ω in series with the inverting input to increase the feedback impedance. With this resistor added to the typical internal R_I = 30Ω, the total feedback impedance is 100Ω + (60Ω • 6) = 460Ω, which is equal to the required value to get a maximum bandwidth flat frequency response for NG = 6.

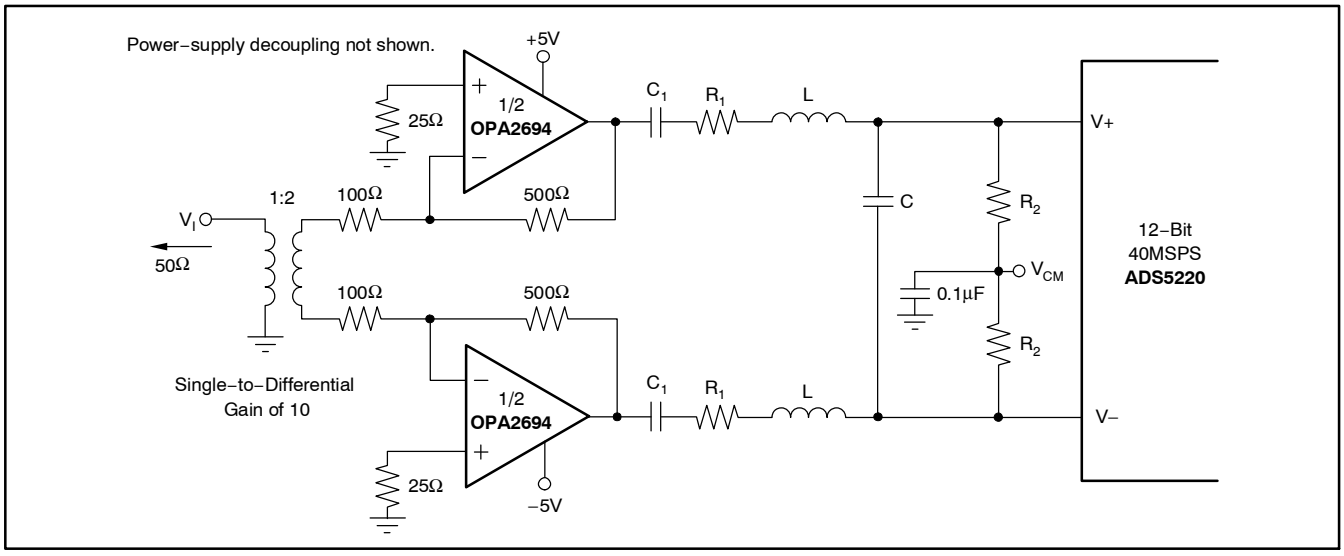


Figure 3. Wideband, AC-Coupled, Low-Power ADC Driver

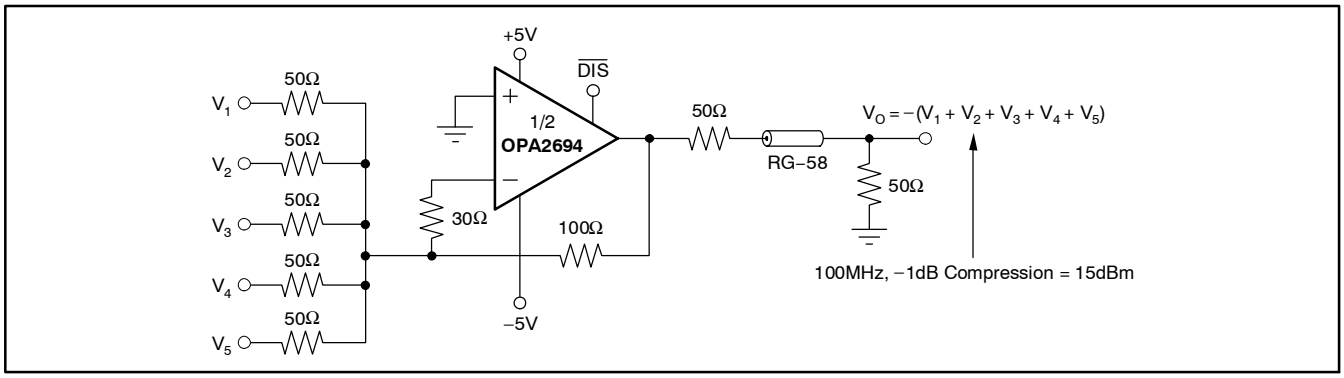


Figure 4. 200MHz RF Summing Amplifier

SAW FILTER BUFFER

One common requirement in an IF strip is to buffer the output of a mixer with enough gain to recover the insertion loss of a narrowband SAW filter. Figure 5 shows one possible configuration driving a SAW filter. The *2-Tone, 3rd-Order Intermodulation Intercept* plot is shown in the Typical Characteritics curves. Operating in the inverting mode at a voltage gain of –8V/V, this circuit provides a 50Ω input match using the gain set resistor, has the feedback optimized for maximum bandwidth (250MHz in this case), and drives through a 50Ω output resistor into the matching network at the input of the SAW filter. If the SAW filter gives a 12dB insertion loss, a net gain of 0dB to the 50Ω load at the output of the SAW (which could be the input impedance of the next IF amplifier or mixer) will be delivered in the passband of the SAW filter. Using the OPA2694 in this application will isolate the first mixer from the impedance of the SAW filter and provide very low two-tone, 3rd-order spurious levels in the SAW filter bandwidth.

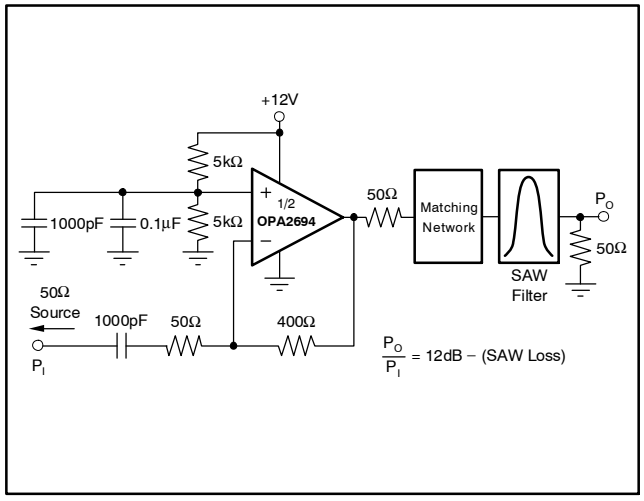


Figure 5. IF Amplifier Driving SAW Filter

DIFFERENTIAL INTERFACE APPLICATIONS

Dual op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either ADC input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA2694. Each has its advantages and disadvantages. Figure 6 shows a basic starting point for noninverting differential I/O applications.

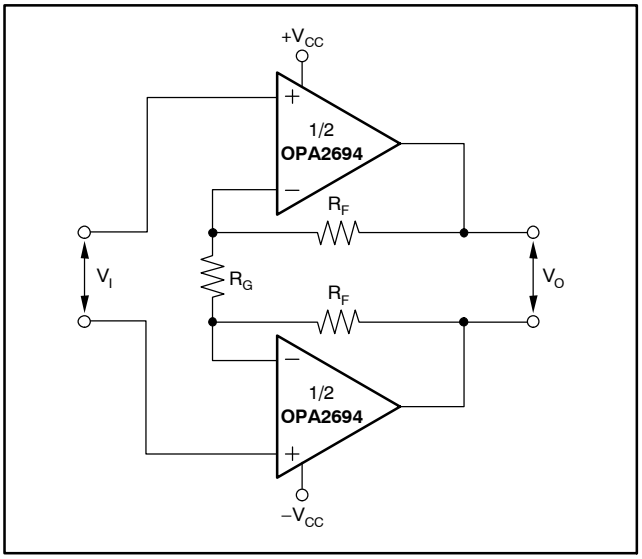


Figure 6. Noninverting Differential I/O Amplifier

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 6 is shown in Equation (1):

$$A_D = 1 + 2 \times \frac{R_F}{R_G} \quad (1)$$

The differential gain, however, may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be a reactive network providing a very isolated shaping to the differential frequency response. Since the inverting inputs of the OPA2694 are low-impedance closed-loop buffer outputs, the R_G element does not interact with the amplifier bandwidth. Wide ranges of resistor values and/or filter elements may be inserted here with minimal amplifier bandwidth interaction.

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 6. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1, since an equal DC voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject

common-mode signals very well, while a line driver application through a transformer also attenuates the common-mode signal through to the line.

Figure 7 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become part of the input resistance for the source. This provides a better noise performance than the noninverting configuration, but does limit the flexibility in setting the input impedance separately from the gain.

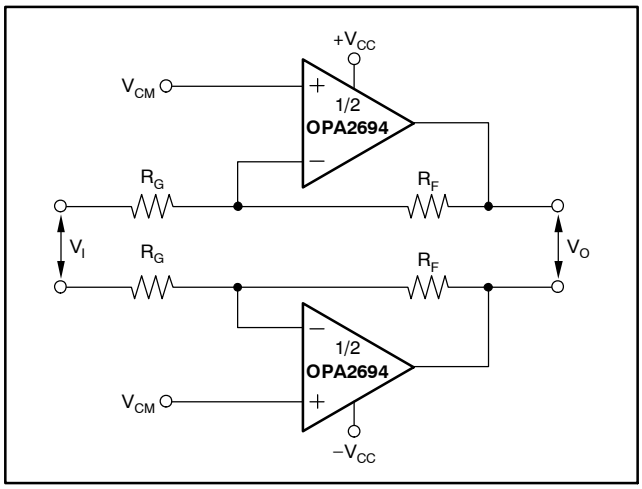


Figure 7. Inverting Differential I/O Amplifier

The two noninverting inputs provide an easy common-mode control input. This is particularly easy if the source is AC-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins, giving particularly easy common-mode control for single-supply operation. Once R_F is fixed, the input resistors can be adjusted to the desired gain, but will also be changing the input impedance as well. The high-frequency, common-mode gain for this circuit from input to output is the same as for the signal gain. Again, if the source includes an undesired common-mode signal, it can be rejected at the input using blocking caps (for low-frequency and DC common-mode) or a transformer coupling.

DC-COUPLED SINGLE-TO-DIFFERENTIAL CONVERSION

The previous differential output circuits were set up to receive a differential input as well. A simple way to provide a DC-coupled single-to-differential conversion using a dual op amp is shown in Figure 8. Here, the output of the first stage is simply inverted by the second to provide an inverting version of a single amplifier design. This approach works well for lower frequencies, but will start to depart from ideal differential outputs as the propagation delay and distortion of the inverting stage adds significantly to that present at the noninverting output pin.

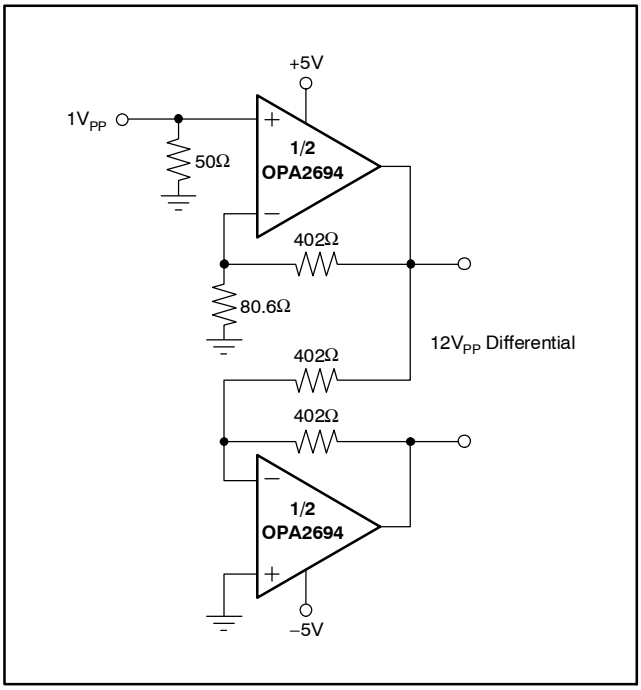


Figure 8. Single-to-Differential Conversion

The circuit of Figure 8 is set up for a single-ended gain of 6 to the output of the first amplifier, then an inverting gain of −1 through the second stage to provide a total differential gain of 12.

DIFFERENTIAL ACTIVE FILTER

The OPA2694 can provide a very capable gain block for low-noise active filters. The dual design lends itself very well to differential active filters. Where the filter topology is looking for a simple gain function to implement the filter, the noninverting configuration is preferred to isolate the filter elements from the gain elements in the design. Figure 9 shows an example of a very low power, 10MHz 3rd-order Butterworth low-pass, Sallen-Key filter. The example of Figure 9 designs the filter for a differential gain of 1 using the OPA2694. The resistor values have been adjusted slightly to account for the amplifier bandwidth effects.

While this circuit is bipolar (using ±5V supplies), it can easily be adapted to single-supply operation. This is typically done by providing a supply midpoint reference at the noninverting inputs, and then adding DC blocking caps at each input and in series with the amplifier gain resistor, R_G. This will add two real zeroes in the response, transforming the circuit into a bandpass.

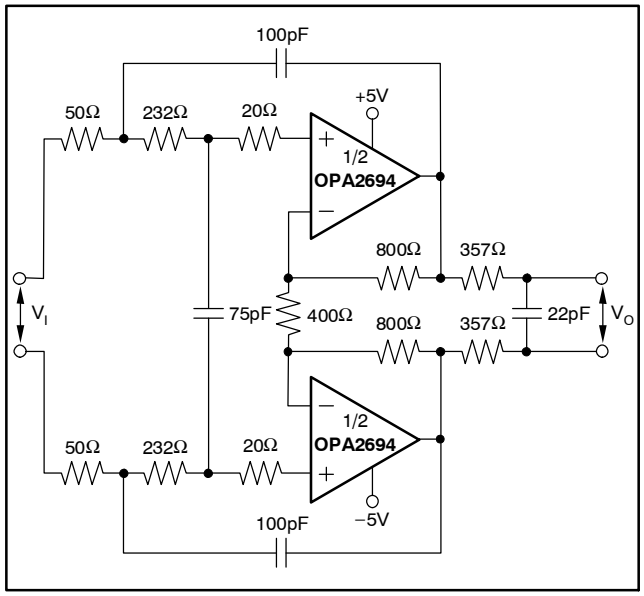


Figure 9. Low-Power, Differential I/O, 3rd-Order Butterworth Active Filter

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2694 in either of two possible configurations: inverting or noninverting. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2694ID	SO-8	DEM-OPA-SO-2B (noninverting)	SBOU030
OPA2694ID	SO-8	DEM-OPA-SO-2C (inverting)	SBOU029

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2694 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2694 is available through the TI web site (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dϕ characteristics. These models do not attempt to distinguish between package types in their small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp like the OPA2694 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This is shown in the Typical Characteristic curves; the small-signal bandwidth decreases only slightly with increasing gain. Those curves also show that the feedback resistor has been changed for each gain setting. The resistor ***values*** on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements while their ***ratios*** set the signal gain. Figure 10 shows the small-signal frequency response analysis circuit for the OPA2694.

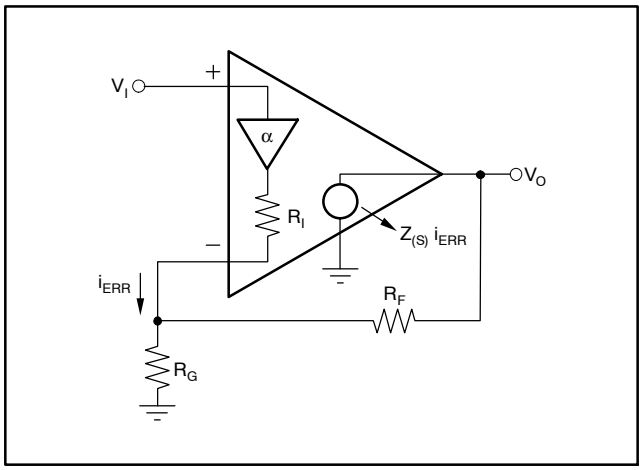


Figure 10. Recommended Feedback Resistor Versus Noise Gain

The key elements of this current-feedback op amp model are:

α → Buffer gain from the noninverting input to the inverting input

R_I → Buffer output impedance

i_{ERR} → Feedback error current signal

$Z_{(s)}$ → Frequency dependent open-loop transimpedance gain from i_{ERR} to V_O

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For a buffer gain $\alpha < 1.0$, the CMRR = $-20 \times \log(1-\alpha)$ dB.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. R_I for the OPA2694 is typically about 30Ω.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 10 gives Equation (2):

$$\frac{V_O}{V_I} = \frac{\alpha\left(1 + \frac{R_F}{R_G}\right)}{1 + \frac{R_F + R_I\left(1 + \frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1 + \frac{R_F + R_I\, NG}{Z_{(S)}}} \quad (2)$$

where:

$$NG = \left(1 + \frac{R_F}{R_G}\right)$$

This is written in a loop-gain analysis format, where the errors arising from a noninfinite open-loop gain are shown in the denominator. If $Z_{(S)}$ were infinite over all frequencies, the denominator of Equation (2) would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation (2) determines the frequency response. Equation (3) shows this as the loop-gain equation:

$$\frac{Z_{(S)}}{R_F + R_I\, NG} = \text{Loop Gain} \quad (3)$$

If $20 \times \log(R_F + NG \times R_I)$ were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, $Z_{(S)}$ rolls off to equal the denominator of Equation (3), at which point the loop gain reduces to 1 (and the curves intersect). This point of equality is where the amplifier closed-loop frequency response given by Equation (2) starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation (3) may be controlled somewhat separately from the desired signal gain (or NG).

The OPA2694 is internally compensated to give a maximally flat frequency response for R_F = 402Ω at NG = 2 on ±5V supplies. Evaluating the denominator of Equation (3) (which is the feedback transimpedance) gives an optimal target of 462Ω. As the signal gain changes, the contribution of the $NG \times R_I$ term in the feedback transimpedance will change, but the total can be held constant by adjusting R_F. Equation (4) gives an approximate equation for optimum R_F over signal gain:

$$R_F = 462\Omega - NG \cdot R_I \quad (4)$$

As the desired signal gain increases, this equation will eventually predict a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values will load both the buffer stage at the input and the output stage, if R_F gets too low, actually decreasing the bandwidth. Figure 11 shows the recommended R_F versus NG for ±5V operation. The values for R_F versus gain shown here are approximately equal to the values used to generate the Typical Characteristics. They differ in that the optimized values used in the Typical Characteristics are also correcting for board parasitics not considered in the simplified analysis leading to Equation (3). The values shown in Figure 11 give a good starting point for design where bandwidth optimization is desired.

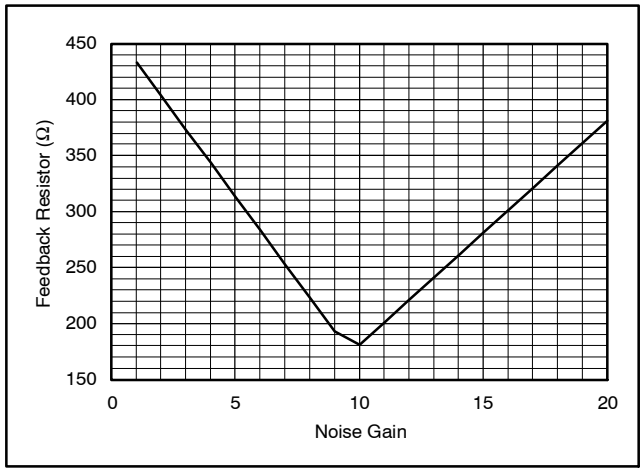


Figure 11. Feedback Resistor vs Noise Gain

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction will increase the feedback impedance (denominator of Equation (2)), decreasing the bandwidth. This approach to bandwidth control is used for the inverting summing circuit of Figure 4. The internal buffer output impedance for the OPA2694 is slightly influenced by the source impedance looking out of the noninverting input terminal. High source resistors will have the effect of increasing R_I, decreasing the bandwidth.

OUTPUT CURRENT AND VOLTAGE

The OPA2694 provides output voltage and current capabilities that are not usually found in wideband amplifiers. Under no-load conditions at 25°C, the output voltage typically swings closer than 1.2V to either supply rail; the +25°C swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±55mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or V–I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2694 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA2694 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.4V output swing capability, as shown in the Electrical Charateristics.

The minimum specified output voltage and current over-temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, the junction temperatures will increase, decreasing both V_{BE} (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2694 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds

a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2694. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2694 output pin (see the *Board Layout Guidelines* section).

DISTORTION PERFORMANCE

The OPA2694 provides good distortion performance into a 100Ω load on ±5V supplies. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1), this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1μF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2x rate, while the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the 2nd-harmonic increases by less than the expected 6dB, while the 3rd-harmonic increases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly.

NOISE PERFORMANCE

Wideband, current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2694 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (24pA/√Hz) is significantly lower than earlier solutions, while the input voltage noise (2.1nV/√Hz) is lower than most unity-gain stable, wideband, voltage-feedback op amps. This low input voltage noise was achieved at the price of higher noninverting input current noise (22pA/√Hz). As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 12 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

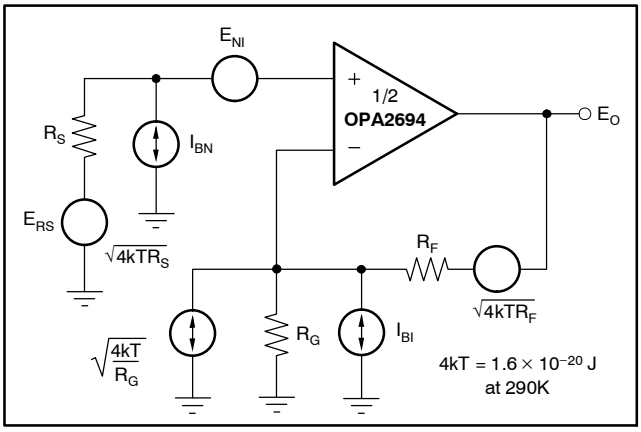


Figure 12. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation (5) shows the general form for the output noise voltage using the terms shown in Figure 12.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (5)$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 6.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (6)$$

Evaluating these two equations for the OPA2694 circuit and component values (see Figure 1) gives a total output spot noise voltage of 11.2nV/√Hz and a total equivalent input spot noise voltage of 5.6nV/√Hz. This total input-referred spot noise voltage is higher than the 2.1nV/√Hz specification for the op amp voltage noise

alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input-referred voltage noise given by Equation (5) will approach just the 2.1nV/$\sqrt{\text{Hz}}$ of the op amp itself. For example, going to a gain of +10 using R_F = 178Ω will give a total input-referred noise of 2.36nV/$\sqrt{\text{Hz}}$.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA2694 provides exceptional bandwidth in high gains, giving fast pulse settling, but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed, voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband, current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$\pm (NG \times V_{OS}) \pm (I_{BN} \times R_S/2 \times NG) \pm (I_{BI} \times R_F)$$

where NG = noninverting signal gain

$$= \pm (2 \times 3.2\text{mV}) \pm (22\mu\text{A} \times 25\Omega \times 2) \pm (402\Omega \times 20\mu\text{A})$$

$$= \pm 6.4\text{mV} + 1.1\text{mV} \pm 8.04\text{mV} = \pm 15.54\text{mV}$$

A fine-scale, output offset null, or DC operating point adjustment, is sometimes required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most simple adjustment techniques do not correct for temperature drift. It is possible to combine a lower speed, precision op amp with the OPA2694 to get the DC accuracy of the precision op amp along with the signal bandwidth of the OPA2694. Figure 13 shows a noninverting G = +10 circuit that holds an output offset voltage less than ±7.5mV over-temperature with > 150MHz signal bandwidth.

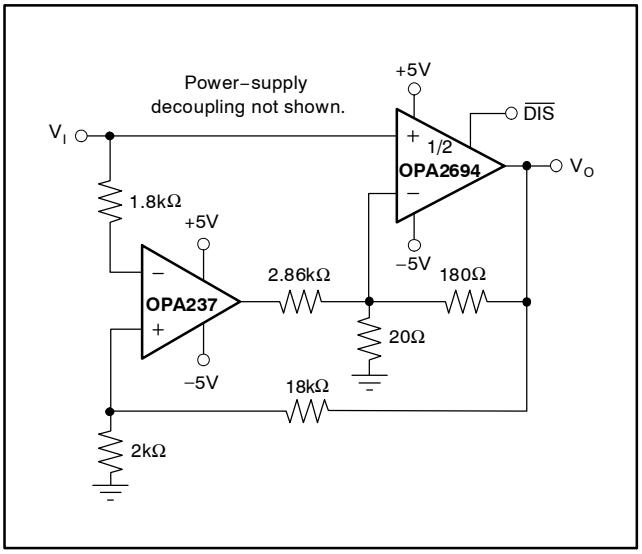


Figure 13. Wideband, DC-Connected Composite Circuit

This DC-coupled circuit provides very high signal bandwidth using the OPA2694. At lower frequencies, the output voltage is attenuated by the signal gain and compared to the original input voltage at the inputs of the OPA237 (this is a low-cost, precision voltage-feedback op amp with 1.5MHz gain bandwidth product). If these two do not agree (due to DC offsets introduced by the OPA2694), the OPA237 sums in a correction current through the 2.86kΩ inverting summing path. Several design considerations will allow this circuit to be optimized. First, the feedback to the OPA237 noninverting input must be precisely matched to the high-speed signal gain. Making the 2kΩ resistor to ground an adjustable resistor would allow the low- and high-frequency gains to be precisely matched. Second, the crossover frequency region where the OPA237 passes control to the OPA2694 must occur with exceptional phase linearity. These two issues reduce to designing for pole/zero cancellation in the overall transfer function. Using the 2.86kΩ resistor will nominally satisfy this requirement for the circuit in Figure 13. Perfect cancellation over process and temperature is not possible. However, this initial resistor setting and precise gain matching will minimize long-term pulse settling tails.

THERMAL ANALYSIS

Due to the high output power capability of the OPA2694, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2694ID (SO-8 package) in the circuit of Figure 1, with both amplifiers operating at the maximum specified ambient temperature of +85°C and driving a grounded 20Ω load to +2.5V DC:

$P_D = 10V \times 12.7mA + 2 \times [5^2/(4 \times (20\Omega \parallel 804\Omega))] = 768mW$

Maximum $T_J = +85°C + (0.45W \times (125°C/W)) = 180°C$

This absolute worst-case condition exceeds the specified maximum junction temperature. Remember, this is a worst-case internal power dissipation—use your actual signal and load to compute P_{DL}. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The *Output Voltage and Current Limitations* plot shown in the Typical Characteristics includes a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2694 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2694. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC-board trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value, as described previously. Increasing its value will reduce the bandwidth, while decreasing it will give a more peaked frequency response. The 402Ω feedback resistor used in the Electrical Characteristic tables at a gain of +2 on ±5V supplies is a good starting point for design. Note that a 430Ω feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load

and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S, since the OPA2694 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion, as shown in the Distortion versus Load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2694 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2694 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *Recommended R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2694 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2694 directly onto the board.

INPUT AND ESD PROTECTION

The OPA2694 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 14.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2694), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

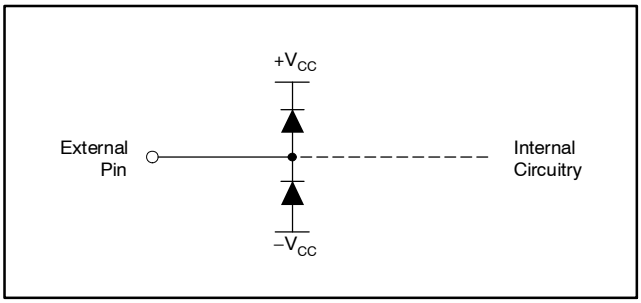


Figure 14. Internal ESD Protection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2694ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2694	Samples
OPA2694IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2694	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

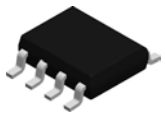
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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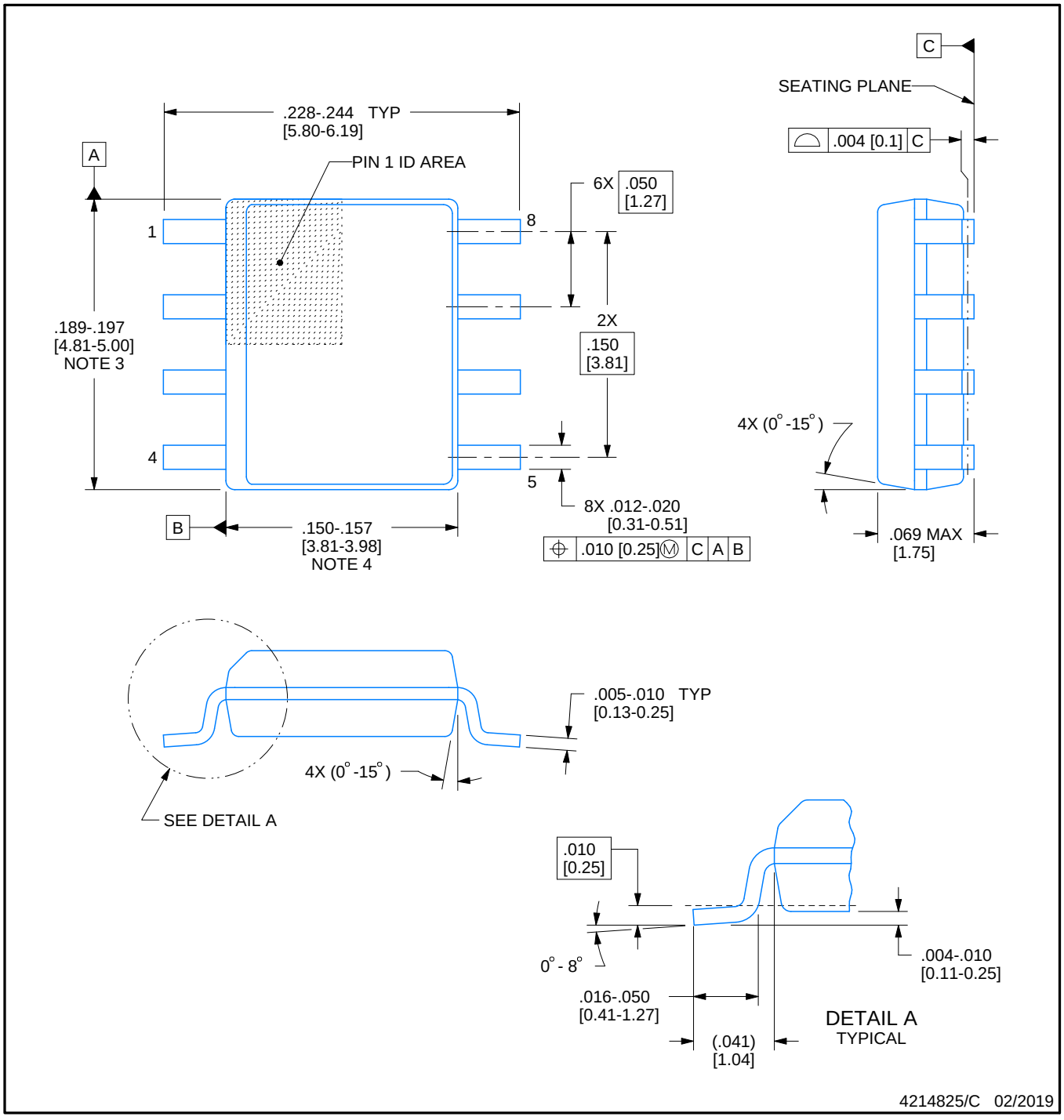


PACKAGE OUTLINE

D0008A

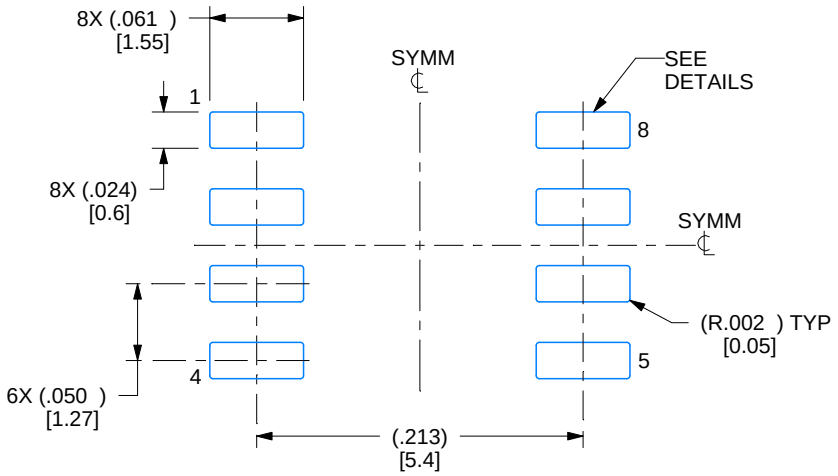
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

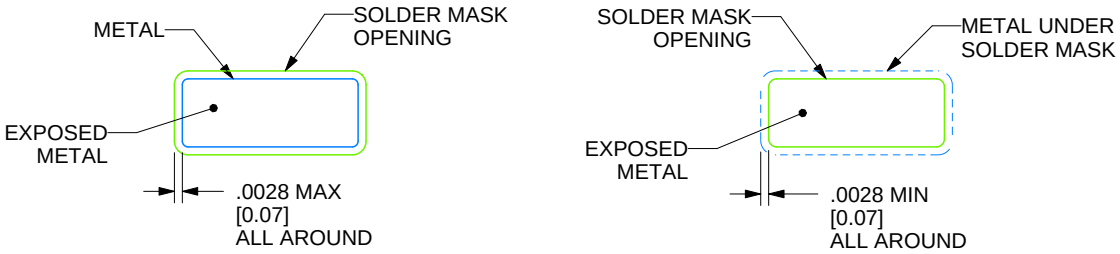


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

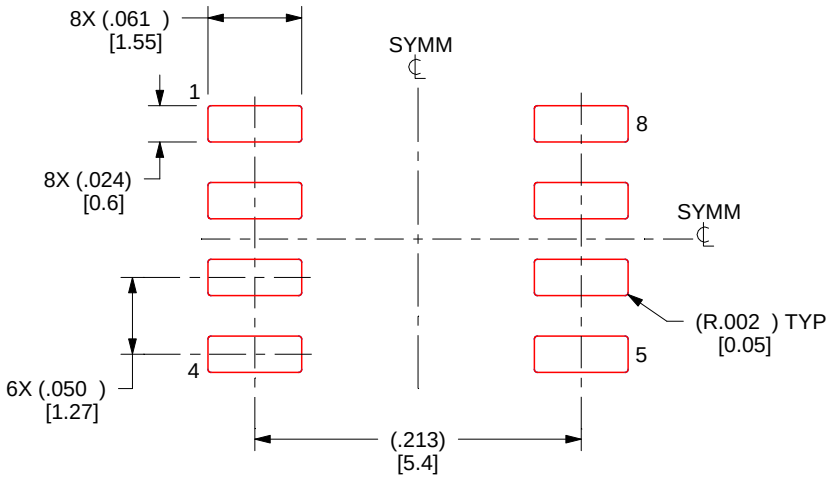
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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