TEXAS INSTRUMENTS

ADS5413EVM

User's Guide

January 2004 *Wireless Infrastructure Products*

SLWU012

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output voltage ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Overview

This user's guide document gives a general overview of the ADS5413 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

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1.1 Purpose

The ADS5413 EVM provides a platform for evaluating the ADS5413 analog-to-digital converter (ADC) under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Analog input to the ADC is provided via two external SMA connectors. The single-ended input the user provides is converted into a differential signal at the input of the device. One input uses a differential amplifier, while the other input is transformer coupled.

The EVM provides external SMA connectors for input of the ADC clock. The EVM allows the user to send a single-ended or differential clock to the ADC. Another SMA connector allows the user to send a second clock source to the output connector along with the digital data. This allows the user to provide the required setup and hold times of the output data with respect to the output clock. See the *Clock Inputs* section for proper configuration and operation.

Digital outputs from the EVM are via a 40-pin connector. The digital lines from the ADC are buffered before going to this connector. More information on these connectors can be found in the ADC output section.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the ADC core, output drivers, and external reference/differential amplifier supplies.

1.3 Power Requirements

The EVM can be powered directly with only a 3.3-V supply if using the ADC with 3.3-VDC output levels.

±5 V is required if using the differential amplifier input. 1.8 V is required for DRVDD if 1.8-V logic output levels are desired.

1.3.1 Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Under voltage may cause improper operation of some or all of the EVM components.

1.4 ADS5413 EVM Operational Procedure

The ADS5413EVM provides a flexible means of evaluating the ADS5413 in a number of modes of operation. A basic set-up procedure that can be used as a board confidence check is as follows:

1) Verify all jumper settings against the schematic jumper listed in Table 1−1 and Table 1−2.

Table 1−1. Two Pin Jumper List Table

Jumper	Function	Installed	Removed	Default
SJP1	Differential amplifier common-mode voltage input	Applies ADC common mode to differential amplifier	No connection	Removed
W4	External REFT feed	External	Internal	Removed
W9	External REFB feed	External	Internal	Removed

Table 1−2. Three Pin Jumper List Table

Jumper	Function	Location: Pins 1− 2	Location: Pins 2−3	Default
SJP2	Transformer and differential amplifier common-mode select	External common-mode voltage	ADC output common-mode voltage	2−3
W1	Reference select	External reference	Internal reference	2−3
W2	DRVDD voltage source	+3.3 Vdc	Voltage from J13	1−2
W5	Duty cycle select	Duty cycle adjust off	Duty cycle adjust on	1−2
W7	Power down select	Operate mode	Power-down mode	1−2

2) Connect supplies to the EVM as follows:

   a) 3.3-V core and output driver supply to J6 and return to J5.

3) Switch power supply on.

4) Use a function generator with 50-Ω output to input an 65-MHz, 0-V offset, 2-V_{p-p} amplitude differential sine-wave signal into J3 and the complementary signal into J4 to provide a true differential ADC input clock. The frequency of the clock must be within the specification for the device speed grade.

5) Use a function generator with 50-Ω output to input a 1.65-V offset, 3.3-V_{p-p} amplitude square-wave signal into J9 to be used as the buffered output clock. This signal must be the same frequency and synchronized with the ADC clock.

6) Use a frequency generator with 50-Ω output to input a 17-MHz, 0-V offset, 1-V_{p-p} amplitude sine-wave signal into J2. This provides a transformer coupled differential input signal to the ADC.

7) The digital pattern on the output connector J10 should now represent a sine wave and can be monitored using a logic analyzer.

Chapter 2

Circuit Description

This chapter discusses the circuit description of the ADS5413 EVM.

Topic **Page**

2.1 Schematic Diagram 2–2
2.2 Circuit Function 2–2

2.1 Schematic Diagram

The schematic diagram for the EVM is attached to the end of this document.

2.2 Circuit Function

The following paragraphs describe the function of individual circuits. See the relevant data sheet for device operating characteristics.

2.2.1 Analog Inputs

The ADC has either transformer-coupled inputs or differential amplifier inputs from a single-ended source. The inputs are provided via SMA connectors J1 and J2 on the EVM, which must be configured as follows:

1) For a 1:1 transformer coupled input to the ADC, a single-ended source is connected to J2. R36, R38, SJP1 must be removed, and R41 and R45 must be installed. The input is ac coupled and has a 50-Ω terminator. This is the default configuration for the EVM.

2) For a differential amplifier input to the ADC, a single ended source is connected to J1. R36, R38, and SJP1 must be installed, and R41 and R45 must be removed. The input has a 50-Ω terminator.

2.2.2 Clock Inputs

The EVM provides separate inputs for the ADC clock and output buffer clock. This allows the user to send a modified version of the ADC clock (inverted, delayed, etc…) with the output data to generate the required setup and hold times for the users interface.

2.2.2.1 True Differential ADC Clock

To provide a true differential clock, input a positive 65 MHz, 0-V offset, 0.5 V_{p-p} amplitude sine-wave signal into J3 and the complimentary signal into J4. This is the default configuration for the EVM

2.2.2.2 Single-Ended ADC Clock

To provide a single-ended ADC clock, simply connect a single-ended source to J3. No board modifications are required.

2.2.2.3 Transformer-Coupled Differential ADC Clock

To provide a transformer-coupled differential clock using a single-ended input source, configure the board as follows:

1) Install T2, R39, C31, and C32 and remove C25 and C40.

2) Connect the single-ended clock input to J12. The clock is ac-coupled and terminated with 50 Ω.

2.2.2.4 Buffer Clock

To provide a clock to the output buffer, apply a +3.3 V, 1.65-V offset signal input to J9. This input is terminated with a 50-Ω resistor to ground. This signal must be the same frequency and synchronized with the ADC clock

2.2.3 Control Inputs

The EVM has three discrete inputs to control the operation of the device.

2.2.3.1 Power Down

With jumper W7 installed between pins 2 and 3, the ADC is in power down mode. The device is in operate mode with jumper W7 installed between pins 1 and 2 or removed. (The device has a weak internal pulldown resistor on this pin).

2.2.3.2 External Reference

With jumper W1 installed between pins 2 and 3, the ADC is in internal reference mode. The device is in external reference mode with jumper W1 installed between pins 1 and 2. (The device has a weak internal pulldown resistor on this pin).

2.2.3.3 Duty Cycle Adjust Select

With jumper W5 installed between pins 2 and 3, the ADC is in the duty cycle adjust mode (DCS). The DCS is disabled with jumper W5 installed between pins 1 and 2. (The device has a weak internal pullup resistor on this pin).

2.2.4 Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a 3.3-V core supply (J6 and J5), 1.8-V/3.3-V digital driver supply (J13 and J14), and ±5-V differential amplifier and external reference generator supplies (J7, J8, and J11). The digital driver supply is only required if jumper W2 is between pins 2 and 3.

2.2.5 Outputs

The data outputs from the ADC are buffered using a SN74AVC16244 before going to header J10. The ADC and output buffer can provide 1.8-V or 3.3-V output levels. This is selected by the voltage placed on the digital driver power inputs (DRVDD). J10 is a standard 40-pin header on a 100-mil grid and allows easy connection to a logic analyzer.

Chapter 3

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM, lists the components used on the module, and shows the schematic.

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3–2 Parts List 3–8

3–3 Schematic 3–9

3.1 PCB Layout

The EVM is constructed on a 6-layer, 4.25-inch × 5.3-inch, 0.062-inch thick PCB using FR−4 material. The individual layers are shown in Figure 3−1 through Figure 3−6.

Figure 3−1. Top Layer 1

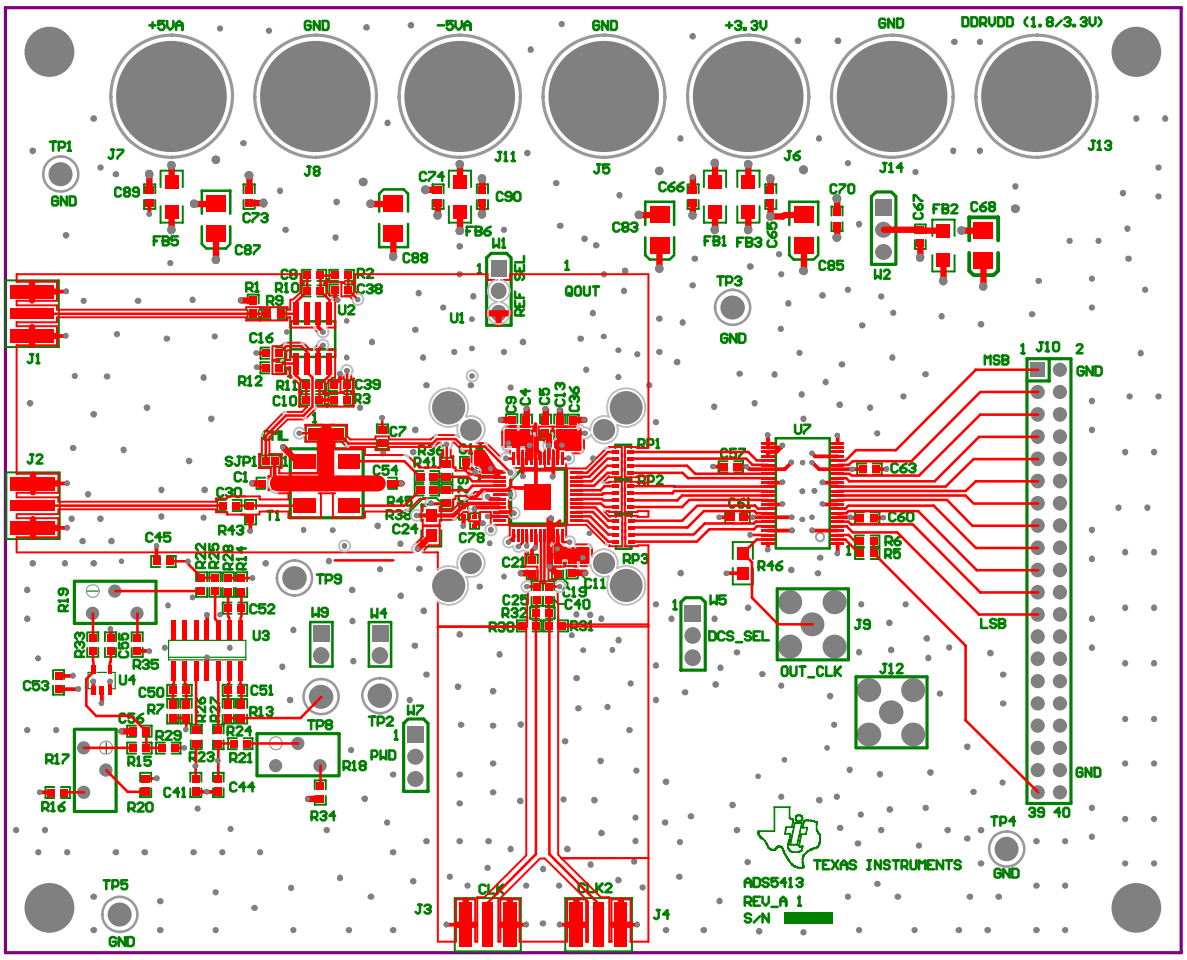


Figure 3−2. Layer 2, Ground Plane

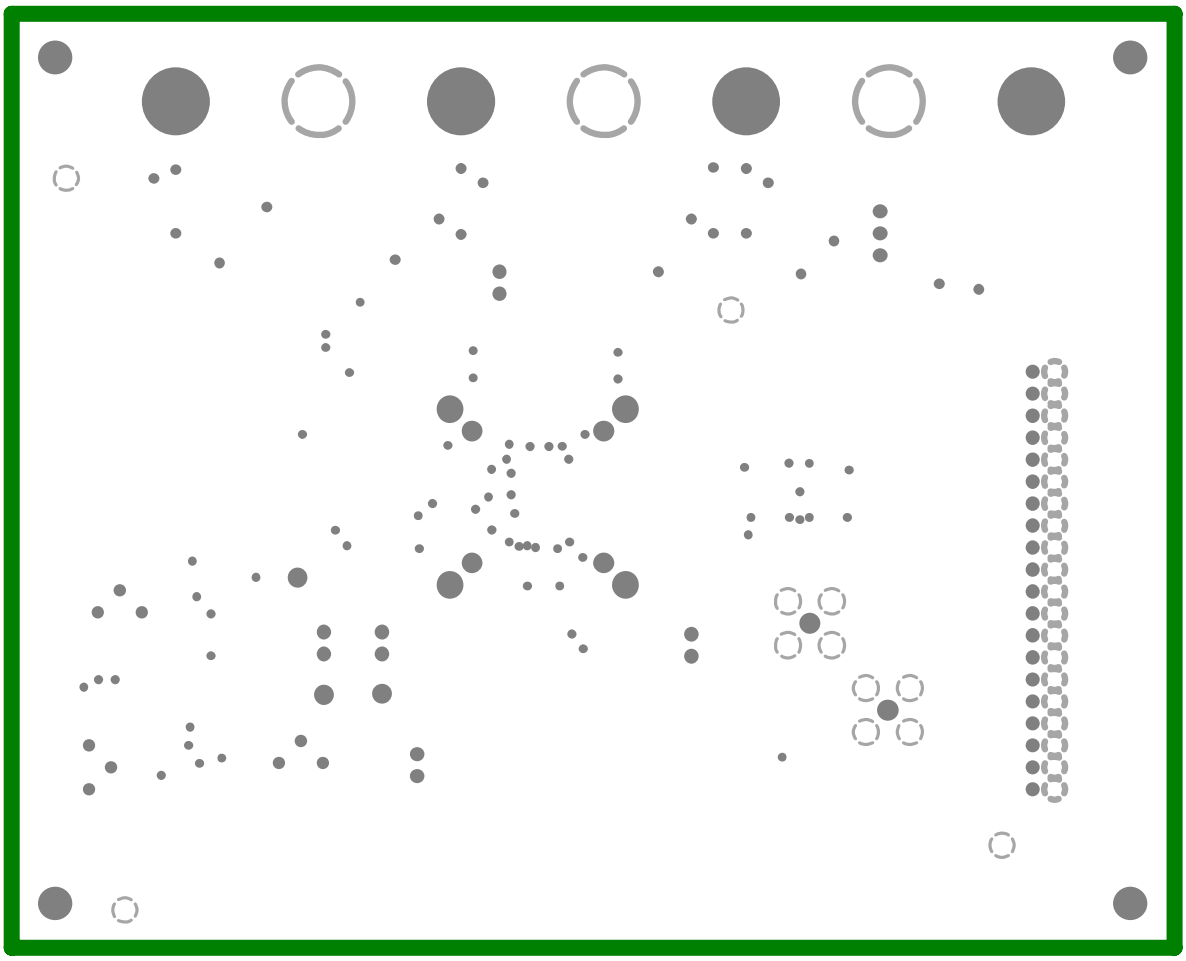


Figure 3−3. Layer 3, Power Plane

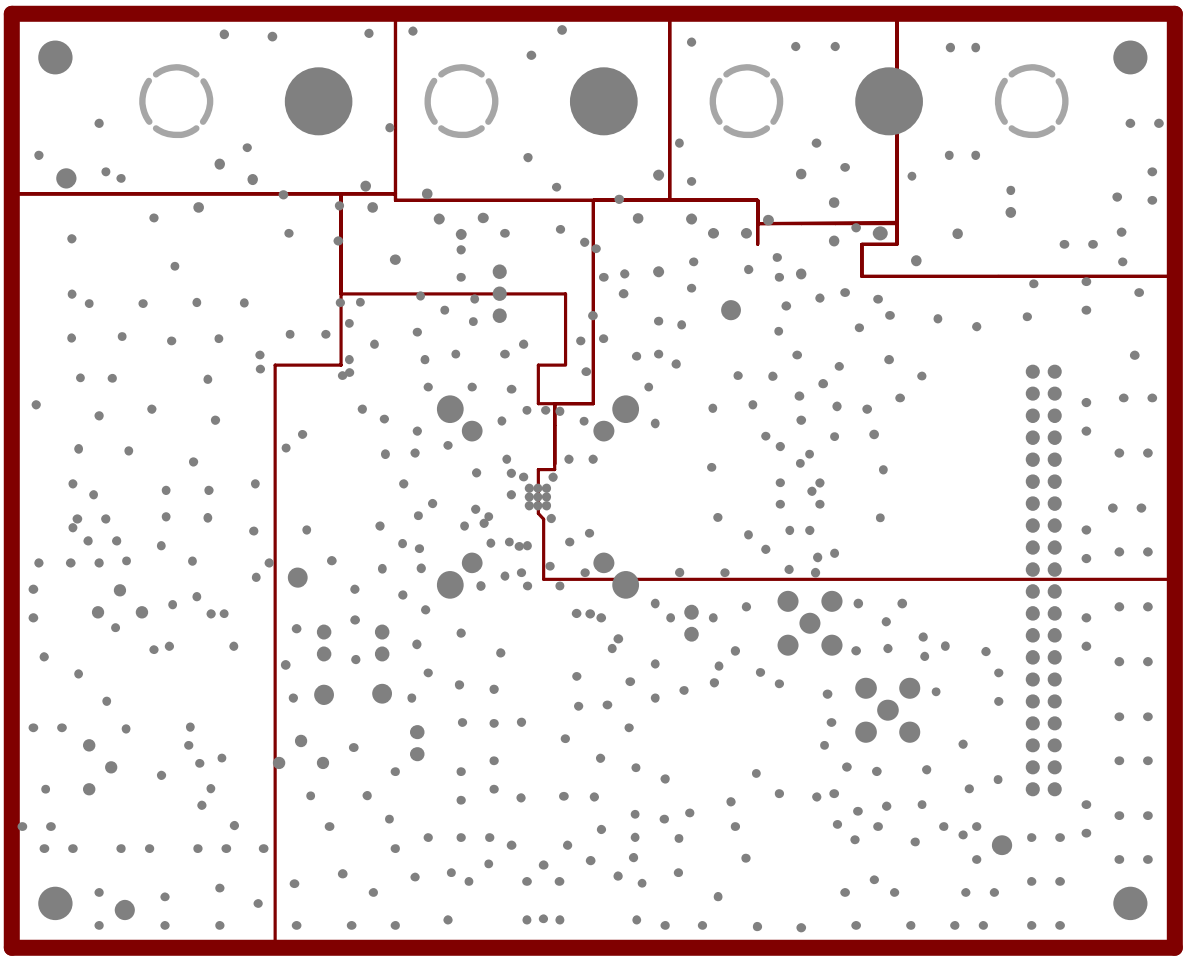


Figure 3−4. Layer 4, Power Plane

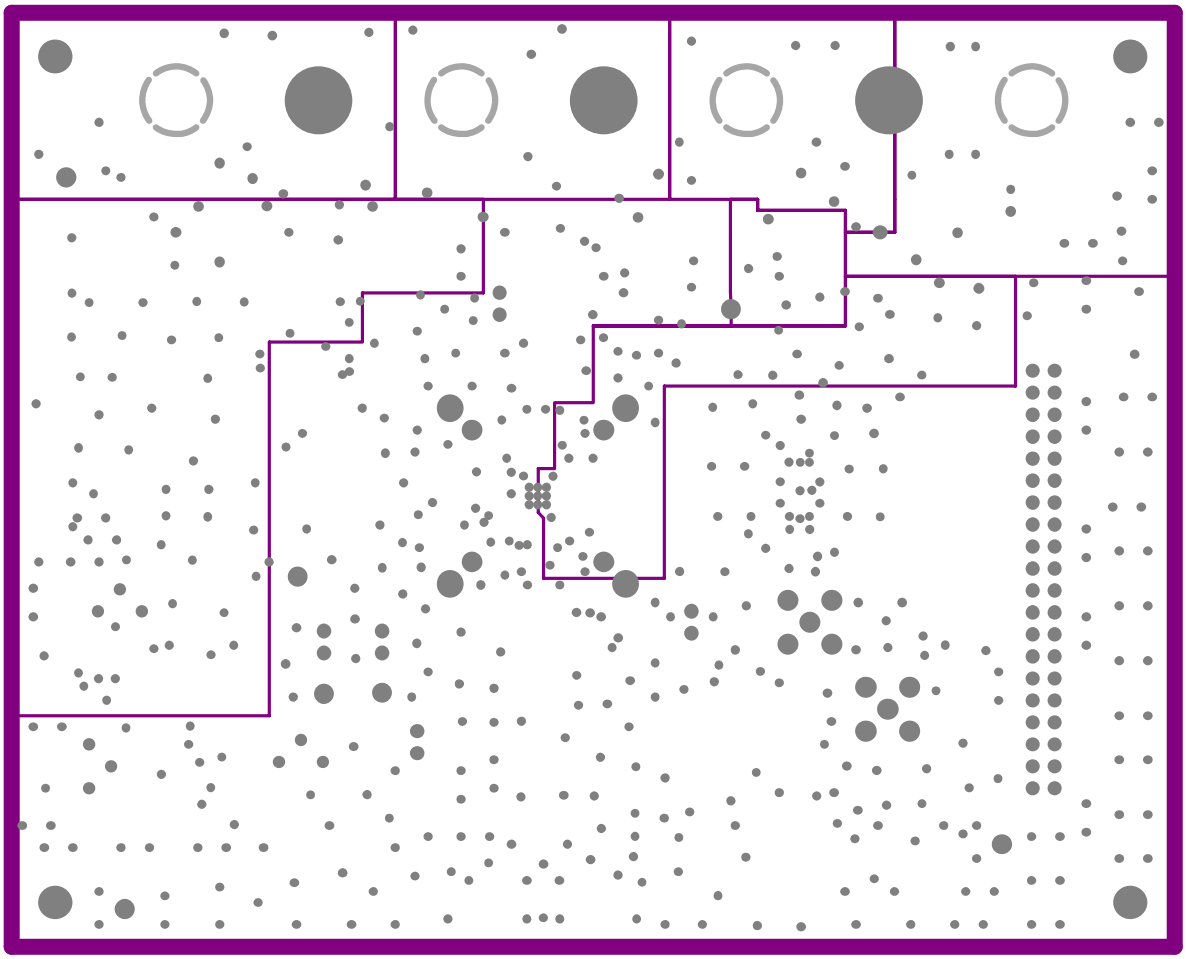


Figure 3−5. Layer 5, Ground Plane

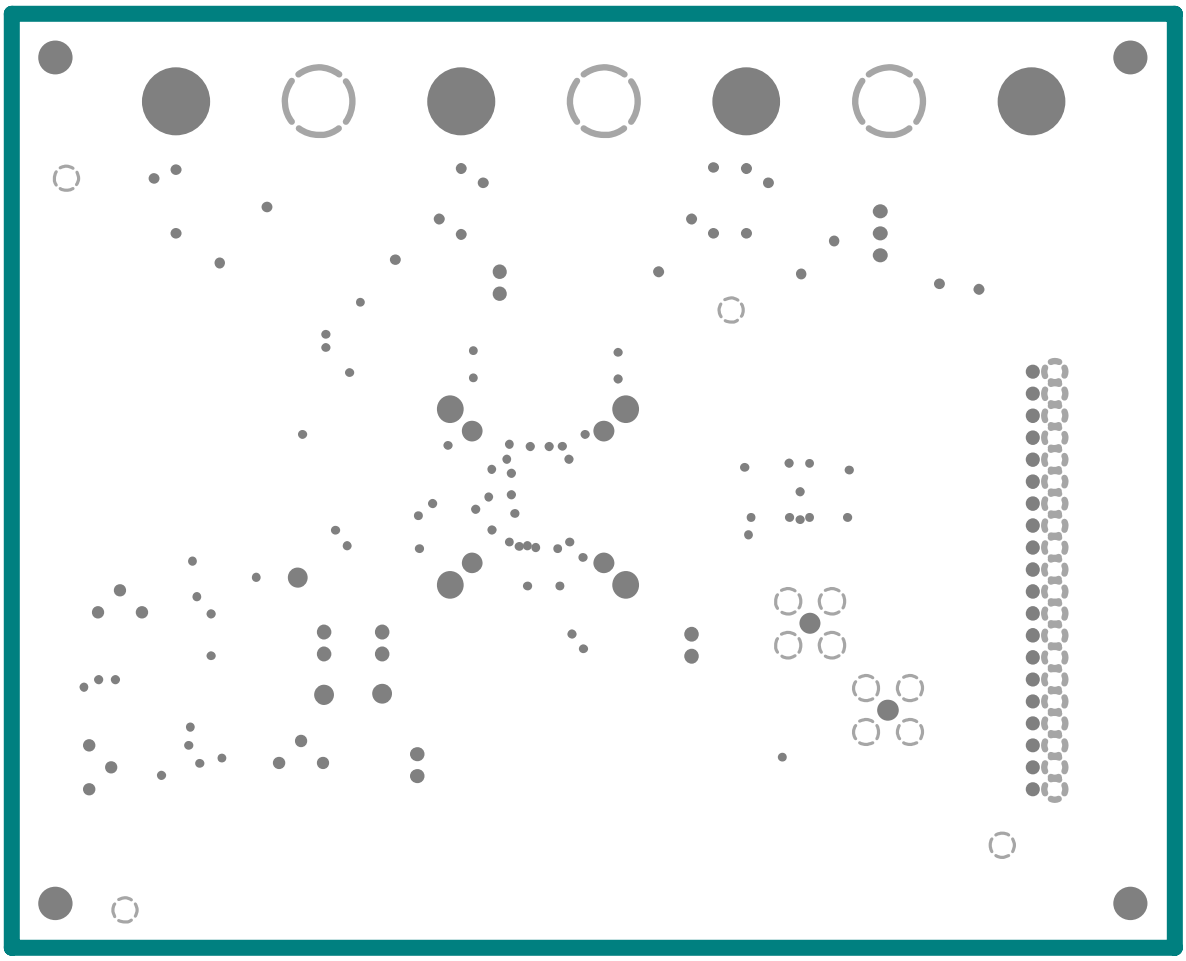
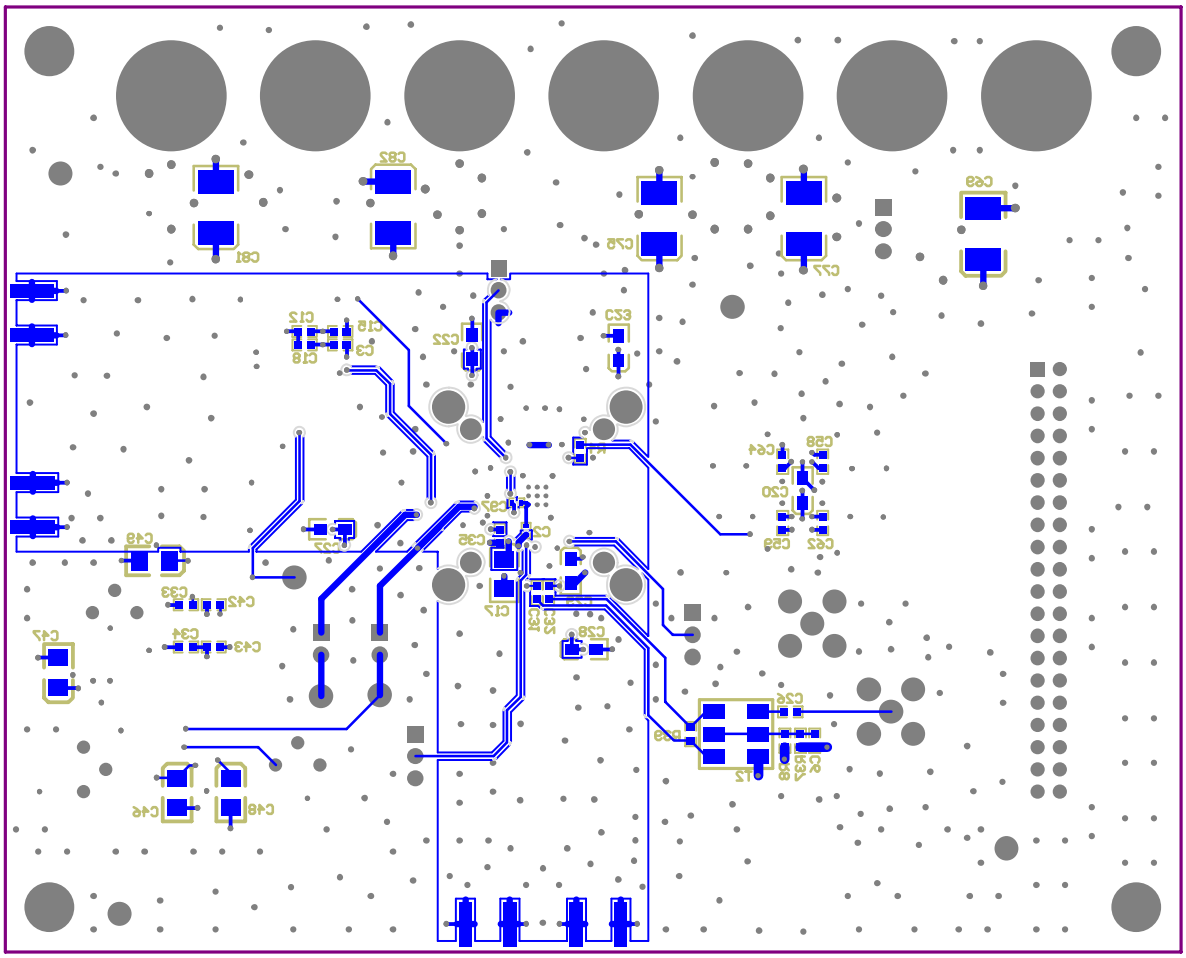


Figure 3−6. Layer 6, Bottom Layer



3.2 Parts List

Table 3−1 lists the parts used in constructing the EVM.

Table 3−1. Parts List

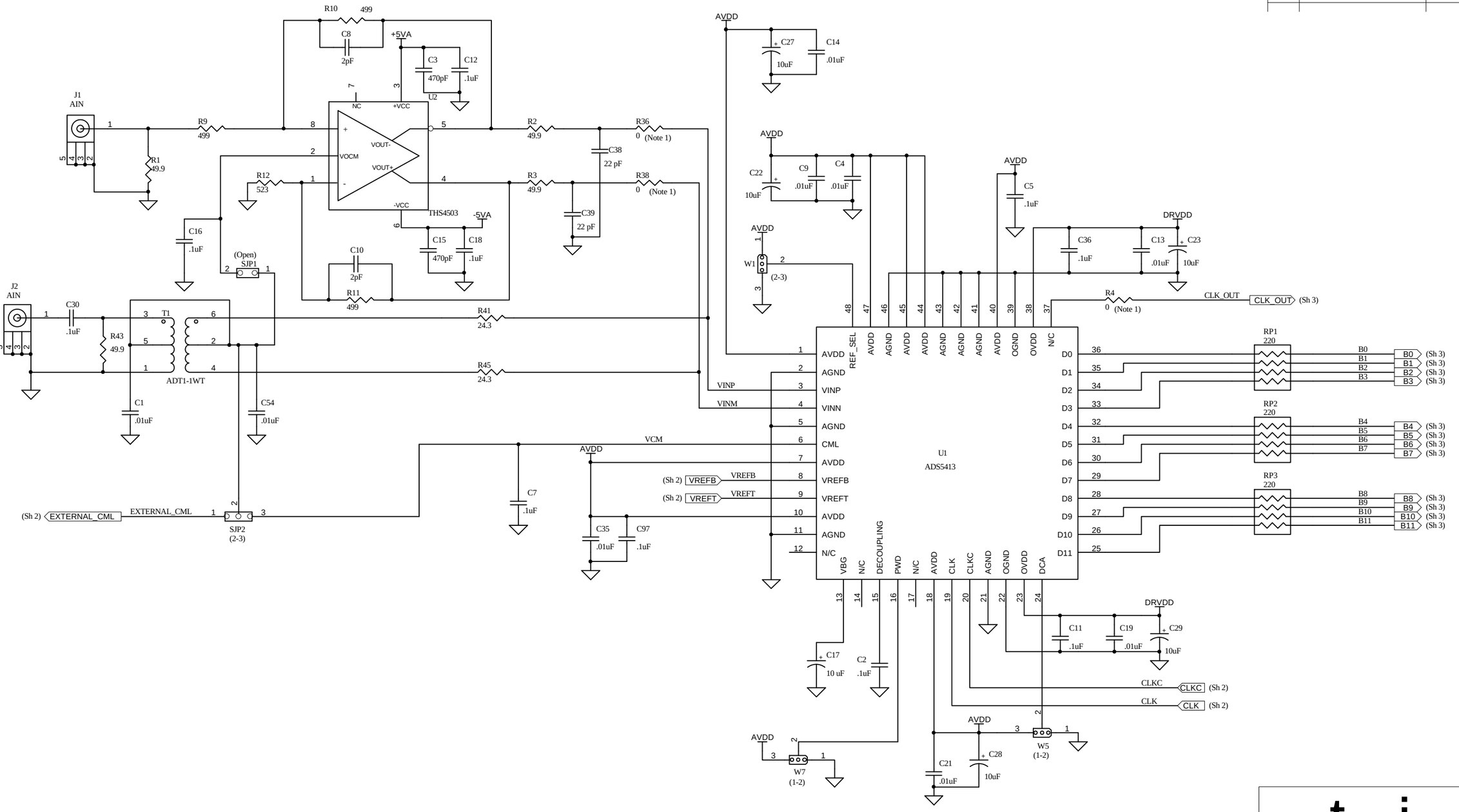
Value	Qty.	Part Number	Vendor	REF DES	Not Installed
CAPACITORS					
47 μF, 10 V, 10% tantalum capacitor	5	ECS−T3AD476R	SANYO	C69, C75, C77, C81, C82	
10 μF, 10 V, 10% capacitor	10	ECS−T1AX106R	Murata	C17, C46−C49, C68, C83, C85, C87, C88	
10 μF, 10 V, 10% capacitor	6	T491A106K010AS	KEMET	C20, C22, C23, C26, C28, C29	
0.1 μF, 16 V, 10% capacitor	1	ECJ−2VB1C104K	Panasonic	C24	
1 μF, 16 V, 10% capacitor	1	ECJ−1VB1C105K	Panasonic	C53	
0.1 μF, 16 V, 10% capacitor	28	ECJ−1VB1C104K	Panasonic	C5, C6, C7, C11, C12, C16, C18, C25, C30, C36, C40−C45, C58, C60, C62, C64, C65, C66, C67, C70, C73, C74, C89, C90	C31, C32
0.01 μF, 16 V,10% capacitor	11	ECJ−1VB1C103K	Panasonic	C1, C4, C9, C13, C14, C19, C21, C26, C35, C54, C55	
0.047 μF, 50 V, 5% capacitor	3	ECJ−1VC1H471J	Panasonic	C50, C51, C52	
470 pF, 50 V, 5% capacitor	8	ECJ−1VC1H471J	Panasonic	C3, C15, C33, C34, C57, C59, C61, C63	
2 pF, 50 V, .25% capacitor	2	ECU−V1HO20CCV	Panasonic	C8, C10	
22 pF, 50 V, 5% capacitor	2	ECU−1VC1H220J	Panasonic	C38, C39	
2.2 μF, 6.3 V, +80/−20% capacitor	1	ECJ−1VF0J225Z	Panasonic	C56	
0.1 μF,10 V, 10% capacitor	4	ECJ−0EB1A104K	Panasonic	C2, C97, C78, C79	
RESISTORS					
49.9-Ω resistor, 1/16 W, 1 %	1	ERJ−6ENF49R9V	Panasonic	R46	
0-Ω resistor, 1/16 W, 1 %	1	ERJ−3EKF0R00V	Panasonic	R5	R4, R6, R36, R38
24.3-Ω resistor, 1/16 W, 1%	2	ERJ−3EKF24R3V	Panasonic	R41, R45	
49.9-Ω resistor, 1/16 W, 1%	9	ERJ−3EKF49R9V	Panasonic	R1, R2, R3, R7, R13, R14, R30, R31, R43	R39
100-Ω resistor, 1/16 W, 1%	3	ERJ−3EKF1000V	Panasonic	R23, R24, R25	
499-Ω resistor, 1/16 W, 1%	4	ERJ−3EKF4990V	Panasonic	R9, R10, R11, R15	
523-Ω resistor, 1/16 W, 1%	1	ERJ−3EKF5230V	Panasonic	R12	
1-kΩ resistor, 1/16 W, 1%	0	ERJ−3EKF1001V	Panasonic		R8, R37
2-kΩ resistor, 1/16 W, 1%	4	ERJ−3EKF2001V	Panasonic	R26, R27, R28, R33	
2.55-kΩ resistor, 1/16 W, 1%	1	ERJ−3EKF2551V	Panasonic	R34	
2.87-kΩ resistor, 1/16 W, 1%	1	ERJ−3EKF2871V	Panasonic	R29	
4.99-kΩ resistor, 1/16 W, 1%	1	ERJ−3EKF4991V	Panasonic	R35	
5.62-kΩ resistor, 1/16 W, 1%	1	ERJ−3EKF5621V	Panasonic	R16	

Value	Qty.	Part Number	Vendor	REF DES	Not Installed
10-kΩ resistor, 1/16 W, 1%	3	ERJ−3EKF1002V	Panasonic	R20, R21, R22	
200-kΩ resistor, 1/16 W, 1%	0	ERJ−3EKF2000V	Panasonic		R32
1K POT	3	3296Y−102	BOURNS	R17, R18, R19	
220-Ω R-Pack	2	CTS_742	CTS	RP1, RP2, RP3	
CONNECTORS, JUMPERS, HEADERS, FERRITE BEADS, TRANSFORMERS, ICS					
Ferrite bead	5	EXC−ML32A680U	Panasonic	FB1, FB2, FB3, FB5, FB6	
Transformer	2	ADT1−1WT	Mini-Circuits	T1, T2	
SMA end small	4	16F3627	NEWARK	J1, J2, J3, J4	
SMA connectors	2	2262−0000−09	NEWARK	J9, J12	
Black test point	4	5000K−ND	Keystone	TP1, TP3, TP4, TP5	
RED test point	3	5001K−ND	Keystone	TP2, TP8, TP9	
2POS_header	2	TSW−150−07−L−S	Samtec	W4, W9	
3POS_header	4	TSW−150−07−L−S	Samtec	W1, W2, W5, W7	
40-pin IDC connector	1	TSW−120−07−L−D	Samtec	J10	
Red banana jacks	4	ST−351A	Allied	J6, J7, J11, J13	
Black banana jacks	3	ST351B	Allied	J5, J8, J14	
ADS5413	1	ADS5413IPHP	Texas Instruments	U1	
OPA4227UA	1	OPA4227UA	Texas Instruments	U3	
THS4503	1	THS4503ID	Texas Instruments	U2	
TPS79225	1	TPS79225DBVR	Texas Instruments	U4	
SN74AVC16244	1	SN74AVC16244DGG	Texas Instruments	U7	

3.3 Schematic

The following pages contain the schematic.

Revision History		
REV	ECN Number	Approved



Note 1. Part not installed

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Drawn By: Y. DEWONCK	SIZE:	DATE: 12-Jan-2004	REV: A
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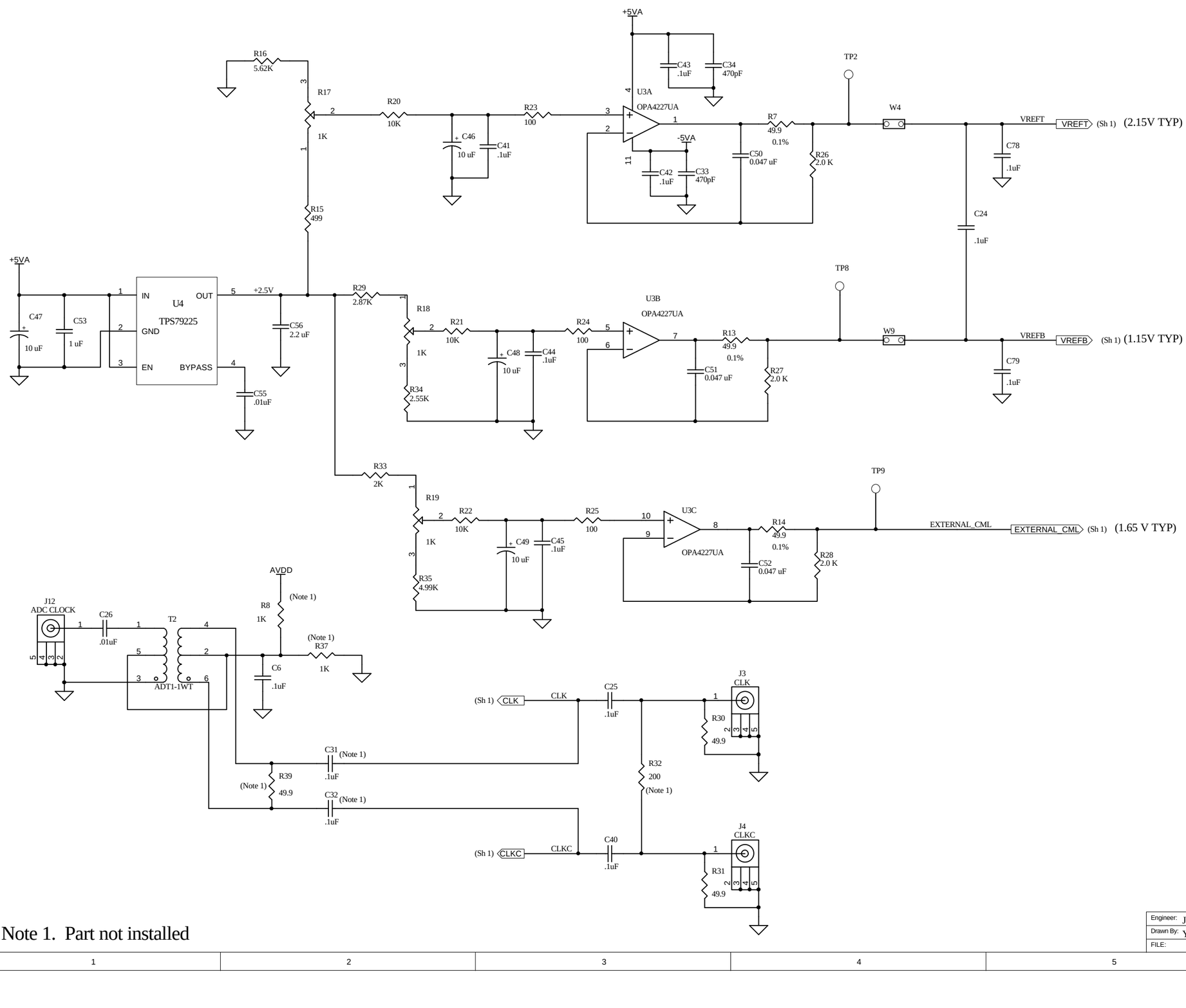
12500 TI Boulevard. Dallas, Texas 75243

Title: ADS5413



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Drawn By: Y. DEWONCK	Title: **ADS5413**
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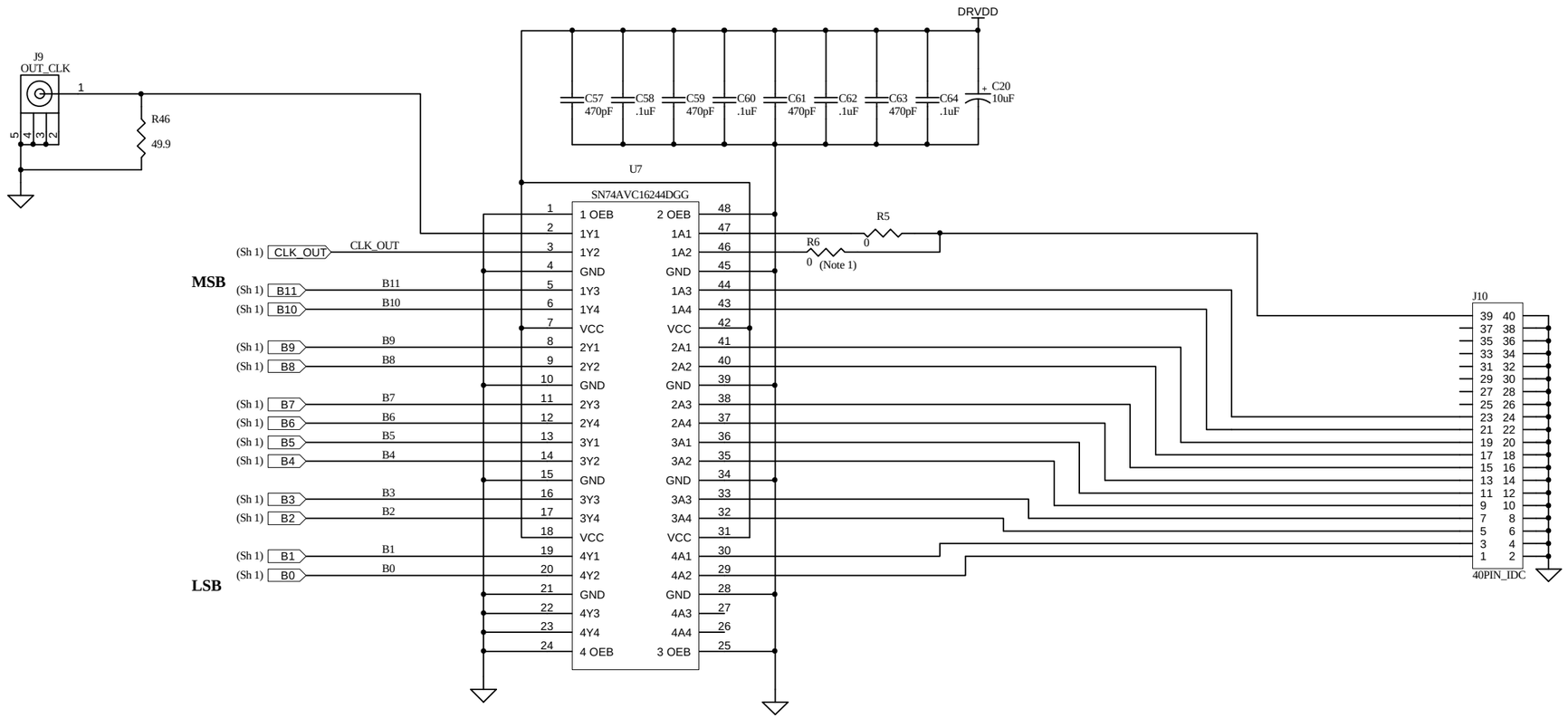

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	SIZE:
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	REV: A

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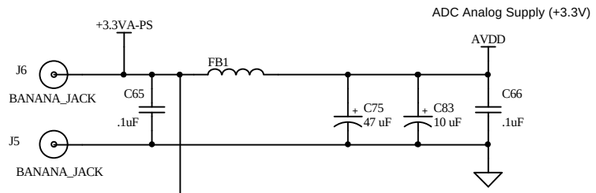
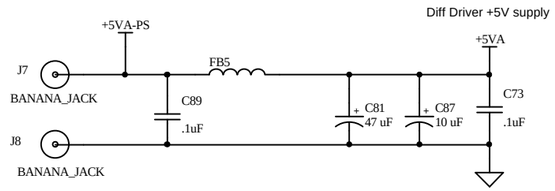
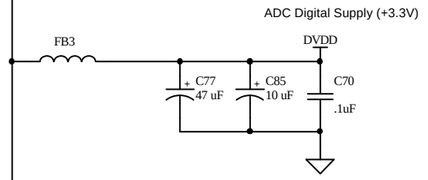
ADC Analog Supply (+3.3V)



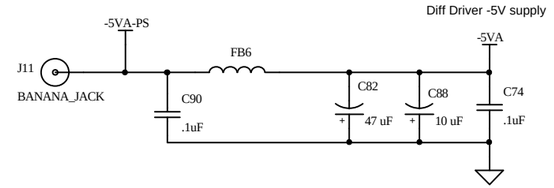
Diff Driver +5V supply

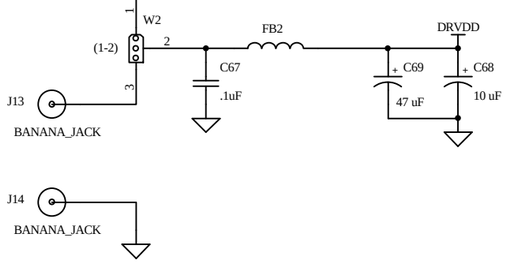


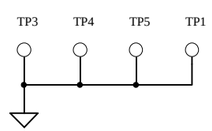
ADC Digital Supply (+3.3V)



Diff Driver -5V supply







Engineer: J. SETON			
Drawn By: Y. DEWONCK			
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DATE: 12-Jan-2004	SIZE:	SHEET: 4 OF: 4	

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