# NCP1547

# 1.5 A, 340 kHz, Buck Regulator with Synchronization Capability

The NCP1547 is a 1.5 A buck regulator IC operating at a fixed−frequency of 340 kHz. The device uses the V$^{2TM}$ control architecture to provide unmatched transient response, the best overall regulation and the simplest loop compensation for today's high−speed logic. The NCP1547 accommodates input voltages from 4.0 V to 40 V and contains synchronization circuitry.

The on−chip NPN transistor is capable of providing a minimum of 1.5 A of output current, and is biased by an external "boost" capacitor to ensure saturation, thus minimizing on−chip power dissipation. Protection circuitry includes thermal shutdown, cycle−by−cycle current limiting and frequency foldback.

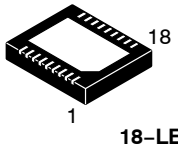
### Features

- V$^2$ Architecture Provides Ultra−Fast Transient Response, Improved Regulation and Simplified Design
- Wide Operating Range: 4 V to 40 V
- 2.0% Error Amp Reference Voltage Tolerance
- Switch Frequency Decrease of 4:1 in Short Circuit Conditions Reduces Short Circuit Power Dissipation
- BOOST Lead Allows "Bootstrapped" Operation to Maximize Efficiency
- Sync Function for Parallel Supply Operation or Noise Minimization
- Shutdown Lead Provides Power−Down Option
- 1.0 μA Quiescent Current During Power−Down
- Thermal Shutdown
- Soft−Start
- These are Pb−Free Devices

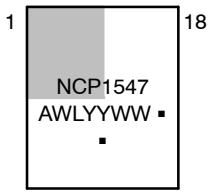
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**MARKING DIAGRAM**



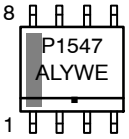

**18−LEAD DFN**
**MN SUFFIX**
**CASE 505**







**SOIC−8**
**D SUFFIX**
**CASE 751**




| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| E | = Automotive Grade |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP1547DG | SOIC−8 (Pb−Free) | 98 Units / Rail |
| NCP1547DR2G | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |
| NCP1547MNR2G | DFN18 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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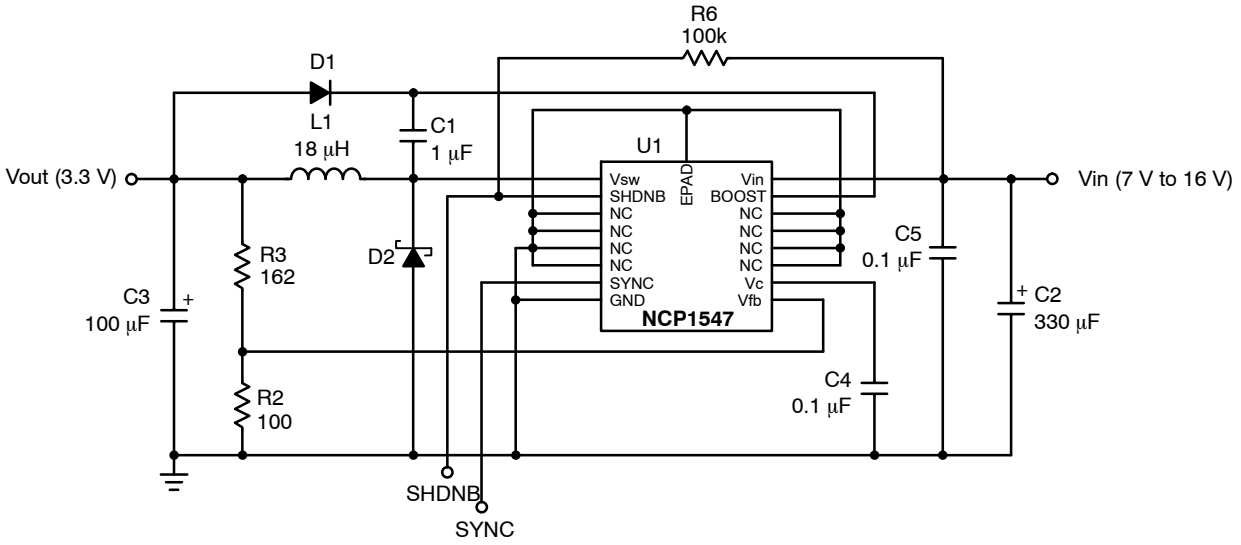



**Figure 1. Application Diagram, 4.5 V – 16 V to 3.3 V @ 1.0 A Converter**

**MAXIMUM RATINGS***

| Rating | | Value | Unit |
|---|---|---|---|
| Peak Transient Voltage (31 V Load Dump @ $V_{IN}$ = 14 V) | | 45 | V |
| Operating Junction Temperature Range, $T_J$ | | −40 to 150 | °C |
| Lead Temperature Soldering: | Reflow: (Note 1) | 260 peak (Note 2) | °C |
| Storage Temperature Range, $T_S$ | | −65 to +150 | °C |
| ESD | (Human Body Model)<br>(Machine Model)<br>(Charge Device Model) | 2.0<br>200<br>>1.0 | kV<br>V<br>kV |
| Package Thermal Resistance | 18−Lead DFN Junction−to−Ambient, $R_{\theta JA}$<br>SO−8 Junction−to−Ambient, $R_{\theta JA}$ (Note 3) | 35<br>100 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*The maximum package power dissipation must be observed.

1. 60 second maximum above 183°C.
2. −5°C/0°C allowable conditions.
3. 1 $in^2$, 1 oz copper area used for heatsinking.

**MAXIMUM RATINGS** (Voltages are with respect to GND)

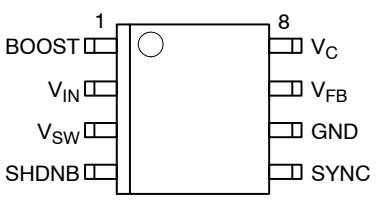
| Pin Name | $V_{Max}$ | $V_{MIN}$ | $I_{SOURCE}$ | $I_{SINK}$ |
|---|---|---|---|---|
| $V_{IN}$ (DC)* | 40 V | −0.3 V | N/A | 4.0 A |
| BOOST | 40 V | −0.3 V | N/A | 100 mA |
| $V_{SW}$ | 40 V | −0.6 V/−1.0 V, t < 50 ns | 4.0 A | 10 mA |
| $V_C$ | 7.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| SHDNB | 7.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| SYNC | 7.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| $V_{FB}$ | 7.0 V | −0.3 V | 1.0 mA | 1.0 mA |

*See table above for load dump.

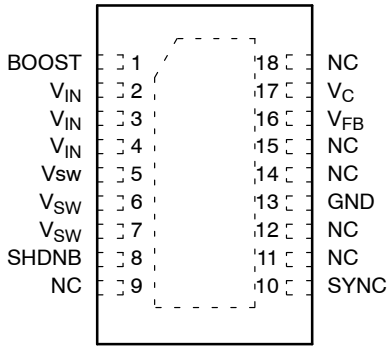
**PACKAGE PIN DESCRIPTION**

| SO−8 | DFN−18 | PIN SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | 1 | BOOST | The BOOST pin provides additional drive voltage to the on−chip NPN power transistor. The resulting decrease in switch on voltage increases efficiency. |
| 2 | 2−4 | $V_{IN}$ | This pin is the main power input to the IC. |
| 3 | 5−7 | $V_{SW}$ | This is the connection to the emitter of the on−chip NPN power transistor and serves as the switch output to the inductor. This pin may be subjected to negative voltages during switch off−time. A catch diode is required to clamp the pin voltage in normal operation. This node can stand −1.0 V for less than 50 ns during switch node flyback. |
| 4 | 8 | SHDNB | The shutdown pin is active low and TTL compatible. The IC goes into sleep mode, drawing less than 1.0 μA when the pin voltage is pulled below 1.0 V.<br>This pin should be pulled up to $V_{CC}$ with a resistor. |
| 5 | 10 | SYNC | This pin provides the synchronization input. |
| 6 | 13 | GND | Power return connection for the IC. |
| 7 | 16 | $V_{FB}$ | The FB pin provides input to the inverting input of the error amplifier. If $V_{FB}$ is lower than 0.29 V, the oscillator frequency is divided by four, and current limit folds back to about 1 A. These features protect the IC under severe overcurrent or short circuit conditions. |
| 8 | 17 | $V_C$ | The $V_C$ pin provides a connection point to the output of the error amplifier and input to the PWM comparator. Driving of this pin should be avoided because on−chip test circuitry becomes active whenever current exceeding 0.5 mA is forced into the IC. |
| − | 9, 11, 12, 14, 15, 18 | NC | No Connection |
| − | − | − | Exposed die attach pad. Internally connected to GND. External connection to GND is optional. |

**PIN CONNECTIONS**




**SO−8**




**18−Lead DFN**

**ELECTRICAL CHARACTERISTICS** (0°C < $T_J$ < 70°C, 4.5 V< $V_{IN}$ < 40 V; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Oscillator** | | | | | |
| Operating Frequency | – | 306 | 340 | 374 | kHz |
| Frequency Line Regulation | – | – | 0.05 | 0.15 | %/V |
| Maximum Duty Cycle | – | 85 | 90 | 95 | % |
| $V_{FB}$ Frequency Foldback Threshold | – | 0.29 | 0.32 | 0.36 | V |
| **PWM Comparator** | | | | | |
| Slope Compensation Voltage | Fix $V_{FB}$, $\Delta V_C/\Delta T_{ON}$ | 11 | 22 | 34 | mV/μs |
| Minimum Output Pulse Width | $V_{FB}$ to $V_{SW}$ | – | 100 | 200 | ns |
| **Power Switch** | | | | | |
| Current Limit | $V_{FB}$ > 0.36 V | 1.6 | 2.3 | 3.0 | A |
| Foldback Current | $V_{FB}$ < 0.29 V | 0.9 | 1.5 | 2.1 | A |
| Saturation Voltage | $I_{OUT}$ = 1.5 A, $V_{BOOST}$ = $V_{IN}$ + 2.5 V | 0.4 | 0.7 | 1.0 | V |
| Current Limit Delay | (Note 4) | – | 120 | 160 | ns |
| **Error Amplifier** | | | | | |
| Internal Reference Voltage | – | 1.244 | 1.270 | 1.296 | V |
| Reference PSRR | (Note 4) | – | 40 | – | dB |
| FB Input Bias Current | – | – | 0.02 | 0.1 | μA |
| Output Source Current | $V_C$ = 1.270 V, $V_{FB}$ = 1.0 V | 15 | 25 | 35 | μA |
| Output Sink Current | $V_C$ = 1.270 V, $V_{FB}$ = 2.0 V | 15 | 25 | 35 | μA |
| Output High Voltage | $V_{FB}$ = 1.0 V | 1.39 | 1.46 | 1.53 | V |
| Output Low Voltage | $V_{FB}$ = 2.0 V | 5.0 | 20 | 60 | mV |
| Unity Gain Bandwidth | (Note 4) | – | 500 | – | kHz |
| Open Loop Amplifier Gain | (Note 4) | – | 70 | – | dB |
| Amplifier Transconductance | (Note 4) | – | 6.4 | – | mA/V |
| **Sync** | | | | | |
| Sync Frequency Range | – | 377 | – | 710 | kHz |
| Sync Pin Bias Current | $V_{SYNC}$ = 5.0 V | – | 360 | 485 | μA |
| Sync Threshold Voltage | – | 0.9 | 1.5 | 1.9 | V |
| **Shutdown** | | | | | |
| Shutdown Threshold Voltage | – | 1.0 | 1.3 | 1.6 | V |
| **Thermal Shutdown** | | | | | |
| Overtemperature Trip Point | (Note 4) | 175 | 185 | 195 | °C |
| Thermal Shutdown Hysteresis | (Note 4) | – | 42 | – | °C |

4. Guaranteed by design, not 100% tested in production.

**ELECTRICAL CHARACTERISTICS (continued)** ($0°C < T_J < 70°C$, $4.5\ V < V_{IN} < 40\ V$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Quiescent Current | $I_{SW}$ = 0 A | – | 4.0 | 7.5 | mA |
| Shutdown Quiescent Current | $V_{SHDNB}$ = 0 V | – | 1.0 | 5.0 | μA |
| Boost Operating Current | $V_{BOOST} - V_{SW}$ = 2.5 V | 6.0 | 15 | 40 | mA/A |
| Minimum Boost Voltage | (Note 5) | – | – | 2.5 | V |
| Startup Voltage | – | 3.0 | 3.5 | 4.0 | V |
| Minimum Output Current | – | – | 7.0 | 12 | mA |

5. Guaranteed by design, not 100% tested in production.

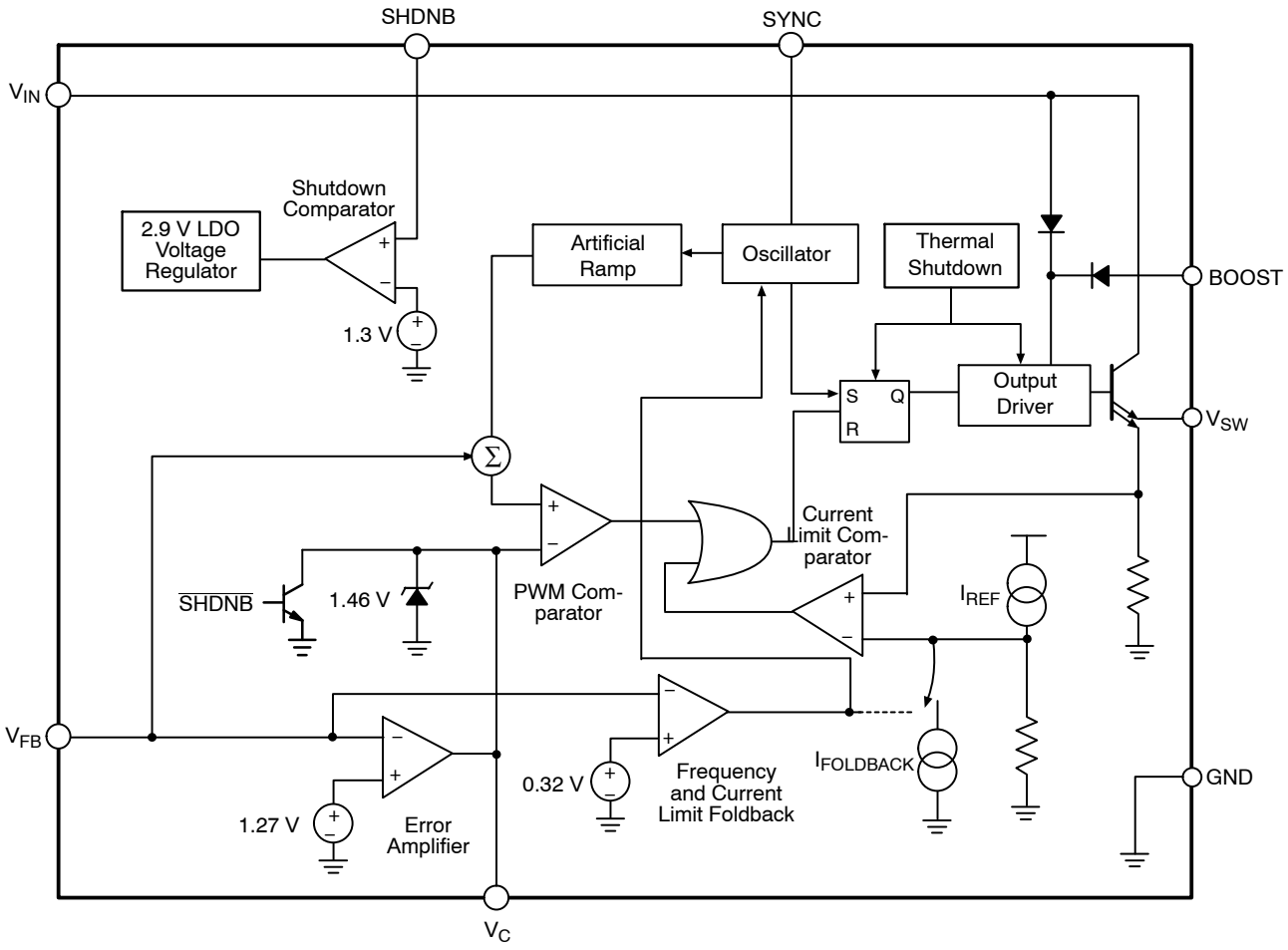



**Figure 2. Block Diagram**

## APPLICATIONS INFORMATION

### THEORY OF OPERATION

#### V² Control

The NCP1547 buck regulator provides a high level of integration and high operating frequencies allowing the layout of a switch−mode power supply in a very small board area. This device is based on the proprietary $V^2$ control architecture. $V^2$ control uses the output voltage and its ripple as the ramp signal, providing an ease of use not generally associated with voltage or current mode control. Improved line regulation, load regulation and very fast transient response are also major advantages.

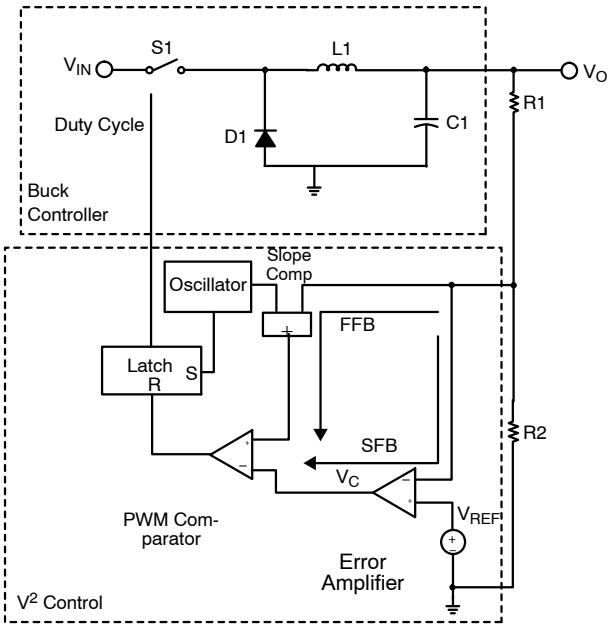



**Figure 3. Buck Converter with V² Control.**

As shown in Figure 3, there are two voltage feedback paths in $V^2$ control, namely FFB(Fast Feedback) and SFB(Slow Feedback). In FFB path, the feedback voltage connects directly to the PWM comparator. This feedback path carries the ramp signal as well as the output DC voltage. Artificial ramp derived from the oscillator is added to the feedback signal to improve stability. The other feedback path, SFB, connects the feedback voltage to the error amplifier whose output $V_C$ feeds to the other input of the PWM comparator. In a constant frequency mode, the oscillator signal sets the output latch and turns on the switch S1. This starts a new switch cycle. The ramp signal, composed of both artificial ramp and output ripple, eventually comes across the $V_C$ voltage, and consequently resets the latch to turn off the switch. The switch S1 will turn on again at the beginning of the next switch cycle. In a buck converter, the output ripple is determined by the ripple current of the inductor L1 and the ESR (equivalent series resistor) of the output capacitor C1.

The slope compensation signal is a fixed voltage ramp provided by the oscillator. Adding this signal eliminates subharmonic oscillation associated with the operation at duty cycle greater than 50%. The artificial ramp also ensures the proper PWM function when the output ripple voltage is inadequate. The slope compensation signal is properly sized to serve it purposes without sacrificing the transient response speed.

Under load and line transient, not only the ramp signal changes, but more significantly the DC component of the feedback voltage varies proportionally to the output voltage. FFB path connects both signals directly to the PWM comparator. This allows instant modulation of the duty cycle to counteract any output voltage deviations. The transient response time is independent of the error amplifier bandwidth. This eliminates the delay associated with error amplifier and greatly improves the transient response time. The error amplifier is used here to ensure excellent DC accuracy.

#### Error Amplifier

The NCP1547 has a transconductance error amplifier, whose non−inverting input is connected to an Internal Reference Voltage generated from the on−chip regulator. The inverting input connects to the $V_{FB}$ pin. The output of the error amplifier is made available at the $V_C$ pin. A typical frequency compensation requires only a 0.1 μF capacitor connected between the $V_C$ pin and ground, as shown in Figure 1. This capacitor and error amplifier's output resistance (approximately 8.0 MΩ) create a low frequency pole to limit the bandwidth. Since $V^2$ control does not require a high bandwidth error amplifier, the frequency compensation is greatly simplified.

The $V_C$ pin is clamped below Output High Voltage. This allows the regulator to recover quickly from over current or short circuit conditions.

#### Oscillator and Sync Feature

The on−chip oscillator is trimmed at the factory and requires no external components for frequency control. The high switching frequency allows smaller external components to be used, resulting in a board area and cost savings. The tight frequency tolerance simplifies magnetic components selection. The switching frequency is reduced to no more than 25% of the nominal value when the $V_{FB}$ pin voltage is below Frequency Foldback Threshold. In short circuit or over−load conditions, this reduces the power dissipation of the IC and external components.

The oscillator frequency varies with junction temperature, as seen in the following graph.

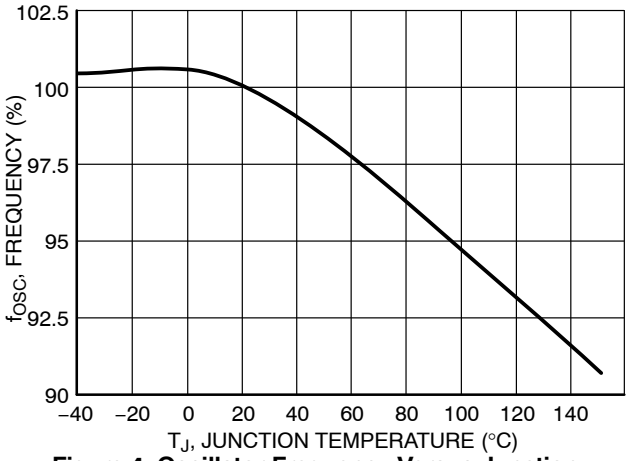



**Figure 4. Oscillator Frequency Versus Junction Temperature**

An external clock signal can sync the NCP1547 to a higher frequency. The SYNC pin equivalent input circuit is shown in Figure 5.

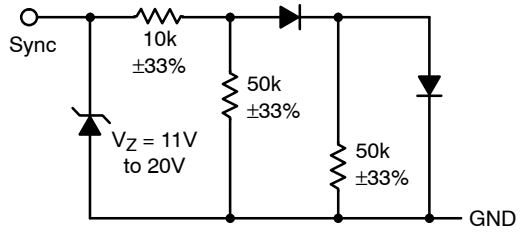



**Figure 5.**

The rising edge of the sync pulse turns on the power switch to start a new switching cycle, as shown in Figure 6. There is approximately 0.5 μs delay between the rising edge of the sync pulse and rising edge of the $V_{SW}$ pin voltage. The sync threshold is TTL logic compatible, and duty cycle of the sync pulses can vary from 10% to 90%. The frequency foldback feature is disabled during the sync mode.

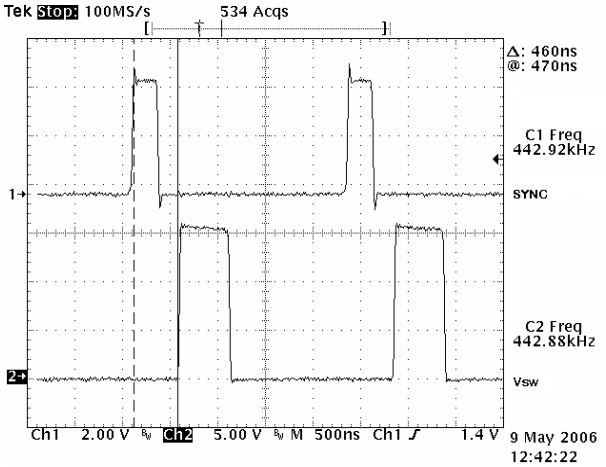



**Figure 6. A NCP1547 Buck Regulator is Synchronized to an External 443 kHz Pulse Signal**

**Power Switch and Current Limit**

The collector of the built−in NPN power switch is connected to the $V_{IN}$ pin, and the emitter to the $V_{SW}$ pin. When the switch turns on, the $V_{SW}$ voltage is equal to the $V_{IN}$ minus switch Saturation Voltage. In the buck regulator, the $V_{SW}$ voltage swings to one diode drop below ground when the power switch turns off, and the inductor current is commutated to the catch diode. Due to the presence of high pulsed current, the traces connecting the $V_{SW}$ pin, inductor and diode should be kept as short as possible to minimize the noise and radiation. For the same reason, the input capacitor should be placed close to the $V_{IN}$ pin and the anode of the diode.

The saturation voltage of the power switch is dependent on the switching current, as shown in Figure 7.

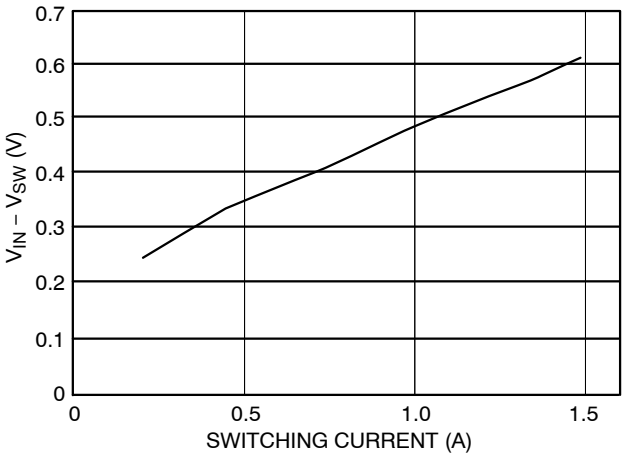



**Figure 7. The Saturation Voltage of the Power Switch Increases with the Conducting Current**

The NCP1547 contains pulse−by−pulse current limiting to protect the power switch and external components. When the peak of the switching current reaches the Current Limit, the power switch turns off after the Current Limit Delay. The switch will not turn on until the next switching cycle. The current limit threshold is independent of switching duty cycle. The maximum load current, given by the following formula under continuous conduction mode, is less than the Current Limit due to the ripple current.

$$I_{O(MAX)} = I_{LIM} - \frac{V_O(V_{IN} - V_O)}{2(L)(V_{IN})(f_S)}$$

where:

$f_S$ = switching frequency,
$I_{LIM}$ = current limit threshold,
$V_O$ = output voltage,
$V_{IN}$ = input voltage,
L = inductor value.

When the regulator runs under current limit, the subharmonic oscillation may cause low frequency

oscillation, as shown in Figure 8. Similar to current mode control, this oscillation occurs at the duty cycle greater than 50% and can be alleviated by using a larger inductor value. The current limit threshold is reduced to Foldback Current when the FB pin falls below Foldback Threshold. This feature protects the IC and external components under the power up or over−load conditions.

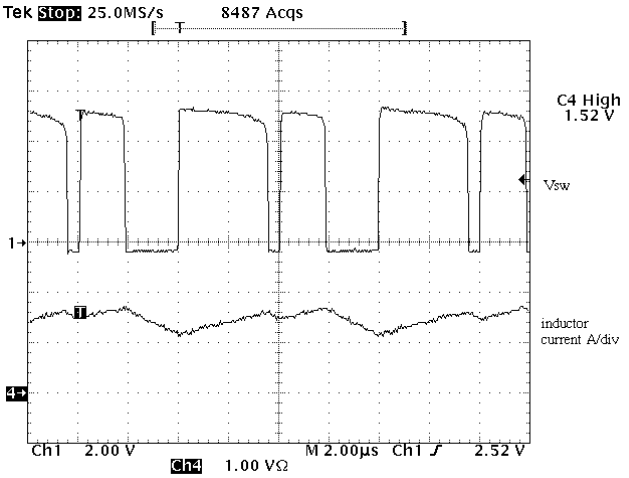



**Figure 8. The Regulator in Current Limit**

### BOOST Pin

The BOOST pin provides base driving current for the power switch. A voltage higher than $V_{IN}$ provides required headroom to turn on the power switch. This in turn reduces IC power dissipation and improves overall system efficiency. The BOOST pin can be connected to an external boost−strapping circuit which typically uses a 0.1 μF capacitor and a 1N914 or 1N4148 diode, as shown in Figure 1.

When the power switch is turned on, the voltage on the BOOST pin is equal to

$$V_{BOOST} = V_{IN} + V_O - V_F$$

where:

$V_F$ = diode forward voltage.

The anode of the diode can be connected to any DC voltage as well as the regulated output voltage (Figure 1). However, the maximum voltage on the BOOST pin shall not exceed 40 V.

As shown in Figure 9, the BOOST pin current includes a constant 7.0 mA pre−driver current and base current proportional to switch conducting current. A detailed discussion of this current is conducted in Thermal Consideration section. A 0.1 μF capacitor is usually adequate for maintaining the Boost pin voltage during the on time.

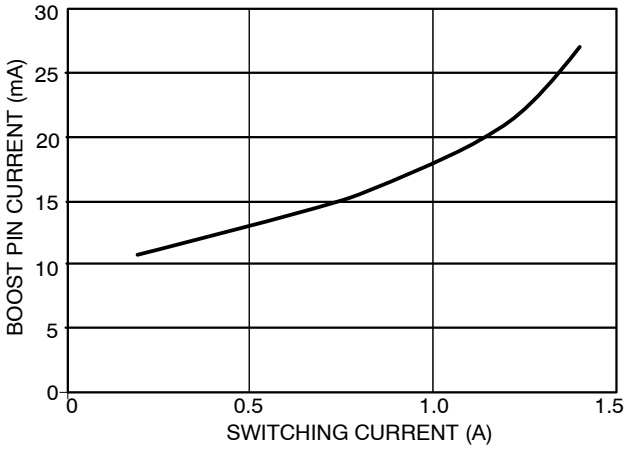



**Figure 9. The Boost Pin Current Includes 7.0 mA Pre−Driver Current and Base Current when the Switch is Turned On. The Beta Decline of the Power Switch Further Increases the Base Current at High Switching Current**

### Shutdown

The internal power switch will not turn on until the $V_{IN}$ pin rises above the Startup Voltage. This ensures no switching will occur until adequate supply voltage is provided to the IC. Refer to Figure 10 for the SHDNB (shutdown−bar) pin input circuit.

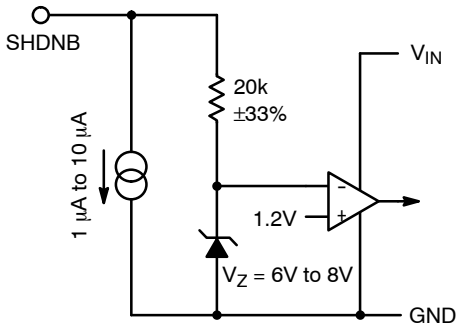



**Figure 10.**

The IC enters a sleep mode when the SHDNB pin is pulled below the Shutdown Threshold Voltage. In sleep mode, the power switch is kept open and the supply current reduces to Shutdown Quiescent Current (1 μA typically). This pin has an internal pull−down current. When not in use, pull this pin up to $V_{CC}$ with a resistor (See Figure 1). A 100 kΩ pullup resistor will ensure safe operation from below 9 V and during a 40 V load dump condition.

### Startup

During power up, the regulator tends to quickly charge up the output capacitors to reach voltage regulation. This gives rise to an excessive in−rush current which can be detrimental to the inductor, IC and catch diode. In $V^2$ control , the compensation capacitor provides Soft−Start with no need for extra pin or circuitry. During the power up, the Output Source Current of the error amplifier charges the compensation capacitor which forces $V_C$ pin and thus output voltage ramp up gradually. The Soft−Start duration can be calculated by

$$T_{SS} = \frac{V_C \times C_{COMP}}{I_{SOURCE}}$$

where:

$V_C$ = $V_C$ pin steady−state voltage, which is approximately equal to error amplifier's reference voltage.

$C_{COMP}$ = Compensation capacitor connected to the $V_C$ pin

$I_{SOURCE}$ = Output Source Current of the error amplifier.

Using a 0.1 μF $C_{COMP}$, the calculation shows a $T_{SS}$ over 5.0 ms which is adequate to avoid any current stresses. Figure 11 shows the gradual rise of the $V_C$, $V_O$ and envelope of the $V_{SW}$ during power up. There is no voltage over−shoot after the output voltage reaches the regulation. If the supply voltage rises slower than the $V_C$ pin, output voltage may over−shoot.

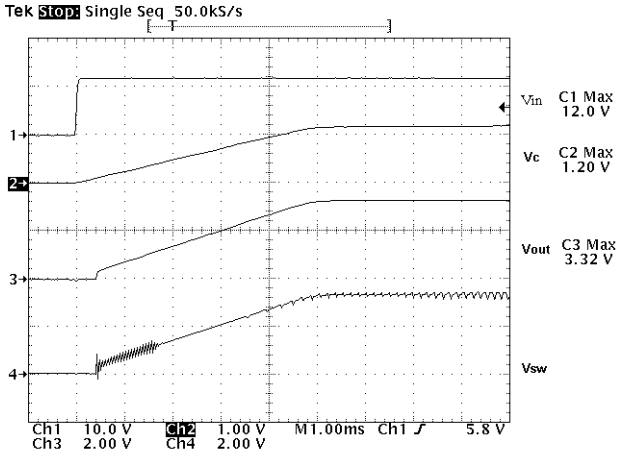



**Figure 11. The Power Up Transition of NCP1547 Regulator**

### Short Circuit

When the $V_{FB}$ pin voltage drops below Foldback Threshold, the regulator reduces the peak current limit by 40% and switching frequency to 1/4 of the nominal frequency. These features are designed to protect the IC and external components during over load or short circuit conditions. In those conditions, peak switching current is clamped to the current limit threshold. The reduced switching frequency significantly increases the ripple current, and thus lowers the DC current. The short circuit can cause the minimum duty cycle to be limited by Minimum Output Pulse Width. The foldback frequency reduces the minimum duty cycle by extending the switching cycle. This protects the IC from overheating, and also limits the power that can be transferred to the output. The current limit foldback effectively reduces the current stress on the inductor and diode. When the output is shorted, the DC current of the inductor and diode can approach the current limit threshold. Therefore, reducing the current limit by 40% can result in an equal percentage drop of the inductor and diode current. The short circuit waveforms are captured in Figure 12, and the benefit of the foldback frequency and current limit is self−evident.

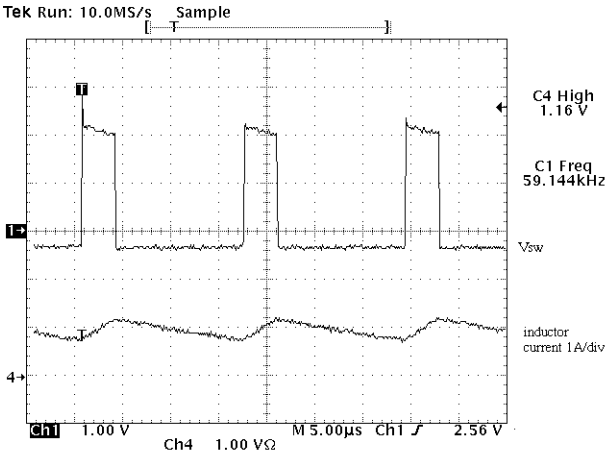



**Figure 12. In Short Circuit, the Foldback Current and Foldback Frequency Limit the Switching Current to Protect the IC, Inductor and Catch Diode**

### Thermal Considerations

A calculation of the power dissipation of the IC is always necessary prior to the adoption of the regulator. The current drawn by the IC includes quiescent current, pre−driver current, and power switch base current. The quiescent current drives the low power circuits in the IC, which include comparators, error amplifier and other logic blocks. Therefore, this current is independent of the switching current and generates power equal to

$$W_Q = V_{IN} \times I_Q$$

where:

$I_Q$ = quiescent current.

The pre−driver current is used to turn on/off the power switch and is approximately equal to 12 mA in worst case. During steady state operation, the IC draws this current from the Boost pin when the power switch is on and then receives it from the $V_{IN}$ pin when the switch is off. The pre−driver current always returns to the $V_{SW}$ pin. Since the pre−driver current goes out to the regulator's output even when the power switch is turned off, a minimum load is required to prevent overvoltage in light load conditions. If the Boost pin voltage is equal to $V_{IN} + V_O$ when the switch is on, the power dissipation due to pre−driver current can be calculated by

$$W_{DRV} = 12\ mA \times (V_{IN} - V_O + \frac{V_O^2}{V_{IN}})$$

The base current of a bipolar transistor is equal to collector current divided by beta of the device. Beta of 60 is used here to estimate the base current. The Boost pin provides the base current when the transistor needs to be on. The power dissipated by the IC due to this current is

$$W_{BASE} = \frac{V_O^2}{V_{IN}} \times \frac{I_S}{60}$$

where:

$I_S$ = DC switching current.

When the power switch turns on, the saturation voltage and conduction current contribute to the power loss of a non−ideal switch. The power loss can be quantified as

$$W_{SAT} = \frac{V_O}{V_{IN}} \times I_S \times V_{SAT}$$

where:

$V_{SAT}$ = saturation voltage of the power switch which is shown in Figure 7.

The switching loss occurs when the switch experiences both high current and voltage during each switch transition. This regulator has a 30 ns turn−off time and associated power loss is equal to

$$W_S = \frac{I_S \times V_{IN}}{2} \times 30\ ns \times f_S$$

The turn−on time is much shorter and thus turn−on loss is not considered here.

The total power dissipated by the IC is sum of all the above

$$W_{IC} = W_Q + W_{DRV} + W_{BASE} + W_{SAT} + W_S$$

The IC junction temperature can be calculated from the ambient temperature, IC power dissipation and thermal resistance of the package. The equation is shown as follows,

$$T_J = W_{IC} \times R_{\theta JA} + T_A$$

### Minimum Load Requirement

As pointed out in the previous section, a minimum load is required for this regulator due to the pre−driver current feeding the output. Placing a resistor equal to $V_O$ divided by 12 mA should prevent any voltage overshoot at light load conditions. Alternatively, the feedback resistors can be valued properly to consume 12 mA current.

## COMPONENT SELECTION

### Input Capacitor

In a buck converter, the input capacitor witnesses pulsed current with an amplitude equal to the load current. This pulsed current and the ESR of the input capacitors determine the $V_{IN}$ ripple voltage, which is shown in Figure 13. For $V_{IN}$ ripple, low ESR is a critical requirement for the input capacitor selection. The pulsed input current possesses a significant AC component, which is absorbed by the input capacitors. The RMS current of the input capacitor can be calculated using:

$$I_{RMS} = I_O \sqrt{D(1 - D)}$$

where:

D = switching duty cycle which is equal to $V_O/V_{IN}$.

$I_O$ = load current.

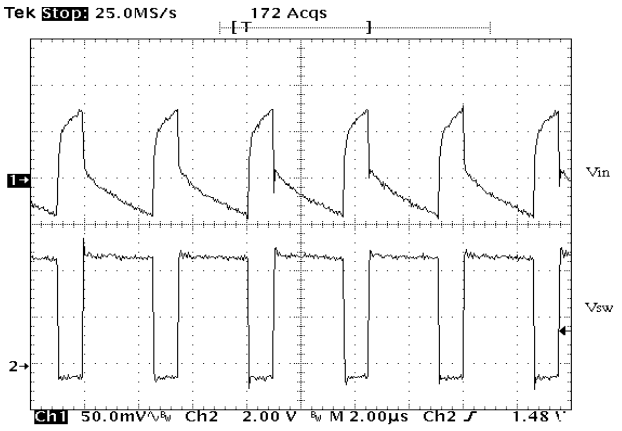



**Figure 13. Input Voltage Ripple in a Buck Converter**

To calculate the RMS current, multiply the load current with the constant given by Figure 14 at each duty cycle. It is a common practice to select the input capacitor with an RMS current rating more than half the maximum load current. If multiple capacitors are paralleled, the RMS current for each capacitor should be the total current divided by the number of capacitors.

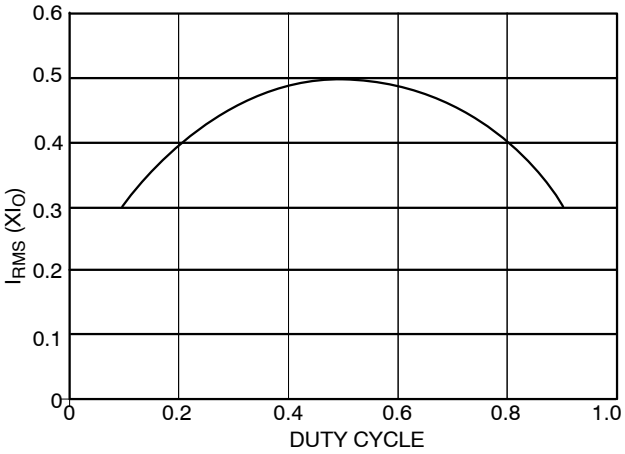



**Figure 14. Input Capacitor RMS Current can be Calculated by Multiplying Y Value with Maximum Load Current at any Duty Cycle**

Selecting the capacitor type is determined by each design's constraint and emphasis. The aluminum electrolytic capacitors are widely available at lowest cost. Their ESR and ESL (equivalent series inductor) are relatively high. Multiple capacitors are usually paralleled to achieve lower ESR. In addition, electrolytic capacitors usually need to be paralleled with a ceramic capacitor for filtering high frequency noises. The OS−CON are solid aluminum electrolytic capacitors, and therefore has a much lower ESR. Recently, the price of the OS−CON capacitors has dropped significantly so that it is now feasible to use

them for some low cost designs. Electrolytic capacitors are physically large, and not used in applications where the size, and especially height is the major concern.

Ceramic capacitors are now available in values over 10 μF. Since the ceramic capacitor has low ESR and ESL, a single ceramic capacitor can be adequate for both low frequency and high frequency noises. The disadvantage of ceramic capacitors are their high cost. Solid tantalum capacitors can have low ESR and small size. However, the reliability of the tantalum capacitor is always a concern in the application where the capacitor may experience surge current.

### Output Capacitor

In a buck converter, the requirements on the output capacitor are not as critical as those on the input capacitor. The current to the output capacitor comes from the inductor and thus is triangular. In most applications, this makes the RMS ripple current not an issue in selecting output capacitors.

The output ripple voltage is the sum of a triangular wave caused by ripple current flowing through ESR, and a square wave due to ESL. Capacitive reactance is assumed to be small compared to ESR and ESL. The peak to peak ripple current of the inductor is:

$$I_{P-P} = \frac{V_O(V_{IN} - V_O)}{(V_{IN})(L)(f_S)}$$

$V_{RIPPLE(ESR)}$, the output ripple due to the ESR, is equal to the product of $I_{P-P}$ and ESR. The voltage developed across the ESL is proportional to the di/dt of the output capacitor. It is realized that the di/dt of the output capacitor is the same as the di/dt of the inductor current. Therefore, when the switch turns on, the di/dt is equal to $(V_{IN} - V_O)/L$, and it becomes $V_O/L$ when the switch turns off. The total ripple voltage induced by ESL can then be derived from

$$V_{RIPPLE(ESL)} = ESL(\frac{V_O}{L}) + ESL(\frac{V_{IN} - V_O}{L}) = ESL(\frac{V_{IN}}{L})$$

The total output ripple is the sum of the $V_{RIPPLE(ESR)}$ and $V_{RIPPLE(ESL)}$.

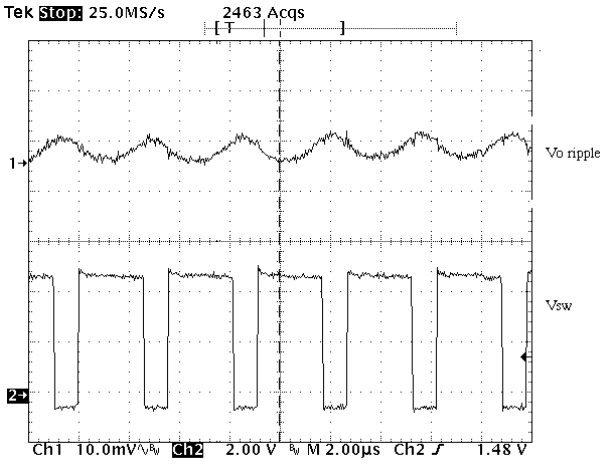



**Figure 15. The Output Voltage Ripple Using Two 10 μF Ceramic Capacitors in Parallel**

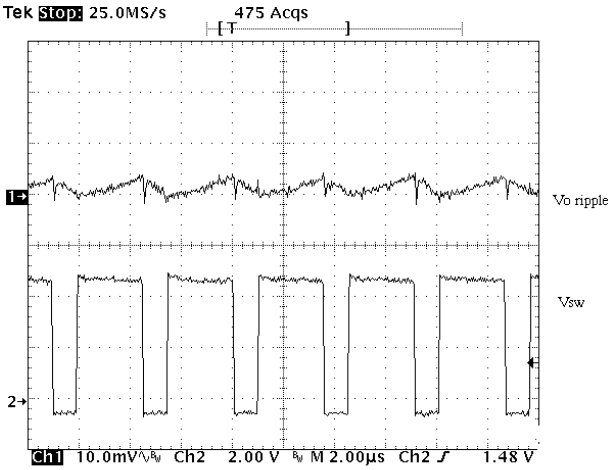



**Figure 16. The Output Voltage Ripple Using One 100 μF POSCAP Capacitor**

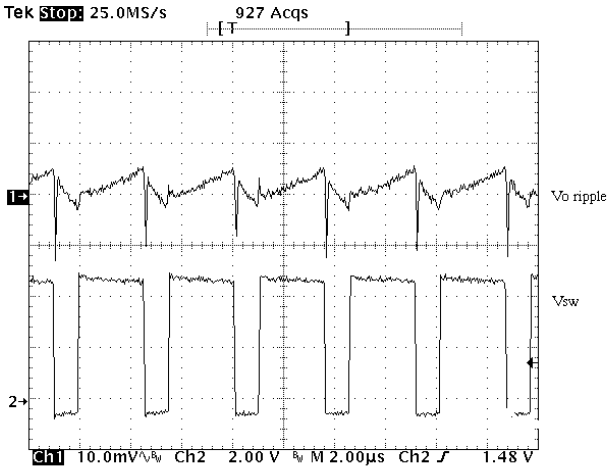



**Figure 17. The Output Voltage Ripple Using One 100 μF OS−CON**

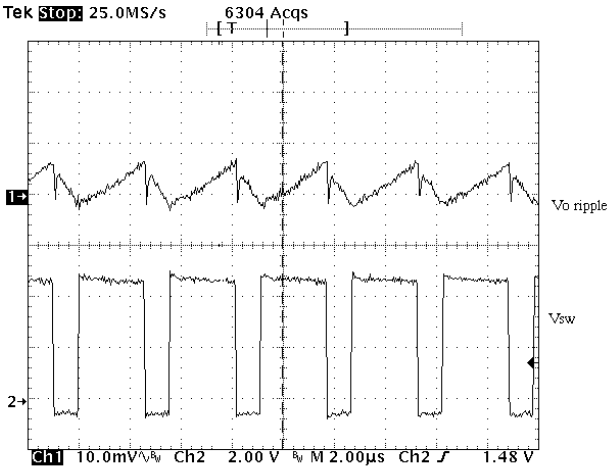



**Figure 18. The Output Voltage Ripple Using One 100 μF Tantalum Capacitor**

Figure 15 to Figure 18 show the output ripple of a 5.0 V to 3.3 V/500 mA regulator using 22 μH inductor and various capacitor types. At the switching frequency, the low ESR and ESL make the ceramic capacitors behave capacitively as shown in Figure 15. Additional paralleled ceramic capacitors will further reduce the ripple voltage, but inevitably increase the cost. “POSCAP”, manufactured by SANYO, is a solid electrolytic capacitor. The anode is sintered tantalum and the cathode is a highly conductive polymerized organic semiconductor. TPC series, featuring low ESR and low profile, is used in the measurement of Figure 16. It is shown that POSCAP presents a good balance of capacitance and ESR, compared with a ceramic capacitor. In this application, the low ESR generates less than 5.0 mV of ripple and the ESL is almost unnoticeable. The ESL of the through−hole OS−CON capacitor give rise to the inductive impedance. It is evident from Figure 17 which shows the step rise of the output ripple on the switch turn−on and large spike on the switch turn−off. The ESL prevents the output capacitor from quickly charging up the parasitic capacitor of the inductor when the switch node is pulled below ground through the catch diode conduction. This results in the spike associated with the falling edge of the switch node. The D package tantalum capacitor used in Figure 18 has the same footprint as the POSCAP, but doubles the height. The ESR of the tantalum capacitor is apparently higher than the POSCAP. The electrolytic and tantalum capacitors provide a low−cost solution with compromised performance. The reliability of the tantalum capacitor is not a serious concern for output filtering because the output capacitor is usually free of surge current and voltage.

### Diode Selection

The diode in the buck converter provides the inductor current path when the power switch turns off. The peak reverse voltage is equal to the maximum input voltage. The peak conducting current is clamped by the current limit of the IC. The average current can be calculated from:

$$I_{D(AVG)} = \frac{I_O(V_{IN} - V_O)}{V_{IN}}$$

The worse case of the diode average current occurs during maximum load current and maximum input voltage. For the diode to survive the short circuit condition, the current rating of the diode should be equal to the Foldback Current Limit. See Table 1 for Schottky diodes from ON Semiconductor which are suggested for use with the NCP1547 regulator.

### Inductor Selection

When choosing inductors, one might have to consider maximum load current, core and copper losses, component height, output ripple, EMI, saturation and cost. Lower inductor values are chosen to reduce the physical size of the inductor. Higher value cuts down the ripple current, core losses and allows more output current. For most applications, the inductor value falls in the range between 2.2 μH and 22 μH. The saturation current ratings of the inductor shall not exceed the $I_{L(PK)}$, calculated according to

$$I_{L(PK)} = I_O + \frac{V_O(V_{IN} - V_O)}{2(f_S)(L)(V_{IN})}$$

The DC current through the inductor is equal to the load current. The worse case occurs during maximum load current. Check the vendor’s spec to adjust the inductor value under current loading. Inductors can lose over 50% of inductance when it nears saturation.

The core materials have a significant effect on inductor performance. The ferrite core has benefits of small physical size, and very low power dissipation. But be careful not to operate these inductors too far beyond their maximum ratings for peak current, as this will saturate the core. Powered Iron cores are low cost and have a more gradual saturation curve. The cores with an open magnetic path, such as rod or barrel, tend to generate high magnetic field radiation. However, they are usually cheap and small. The cores providing a close magnetic loop, such as pot−core and toroid, generate low electro−magnetic interference (EMI).

There are many magnetic component vendors providing standard product lines suitable for the NCP1547. Table 2 lists three vendors, their products and contact information.

**Table 1.**

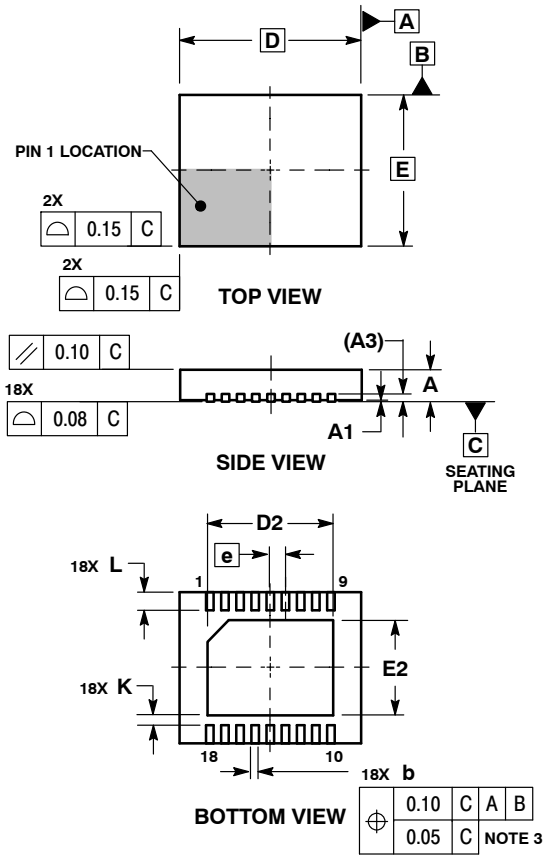
| Part Number | $V_{BREAKDOWN}$ (V) | $I_{AVERAGE}$ (A) | $V_{(F)}$ (V) @ $I_{AVERAGE}$ | Package |
|---|---|---|---|---|
| 1N5817 | 20 | 1.0 | 0.45 | Axial Lead |
| 1N5818 | 30 | 1.0 | 0.55 | Axial Lead |
| 1N5819 | 40 | 1.0 | 0.6 | Axial Lead |
| MBR0520 | 20 | 0.5 | 0.385 | SOD−123 |
| MBR0530 | 30 | 0.5 | 0.43 | SOD−123 |
| MBR0540 | 40 | 0.5 | 0.53 | SOD−123 |
| MBRS120 | 20 | 1.0 | 0.55 | SMB |
| MBRS130 | 30 | 1.0 | 0.395 | SMB |
| MBRS140 | 40 | 1.0 | 0.6 | SMB |

**Table 2.**

| Vendor | Product Family | Web Site | Telephone |
|---|---|---|---|
| Coiltronics | UNI−Pac1/2: SMT, barrel<br>THIN−PAC: SMT, toroid, low profile<br>CTX: Leaded, toroid | www.coiltronics.com | (516) 241−7876 |
| Coilcraft | DO1608: SMT, barrel<br>DS/DT 1608: SMT, barrel, magnetically shielded<br>DO3316: SMT, barrel<br>DS/DT 3316: SMT, barrel, magnetically shielded<br>DO3308: SMT, barrel, low profile | www.coilcraft.com | (800) 322−2645 |
| Pulse | − | www.pulseeng.com | (619) 674−8100 |

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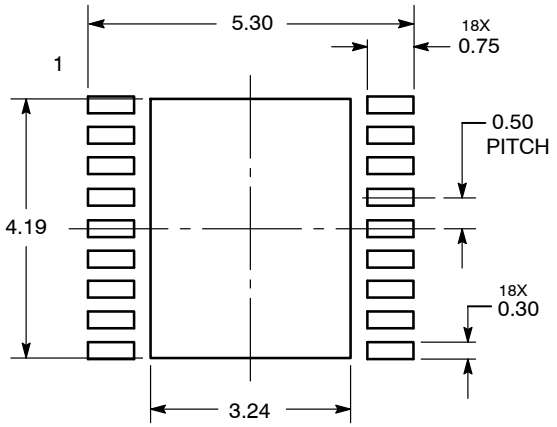
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ISSUE D




NOTES:
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2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 6.00 BSC | |
| D2 | 3.98 | 4.28 |
| E | 5.00 BSC | |
| E2 | 2.98 | 3.28 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.45 | 0.65 |

**SOLDERING FOOTPRINT***

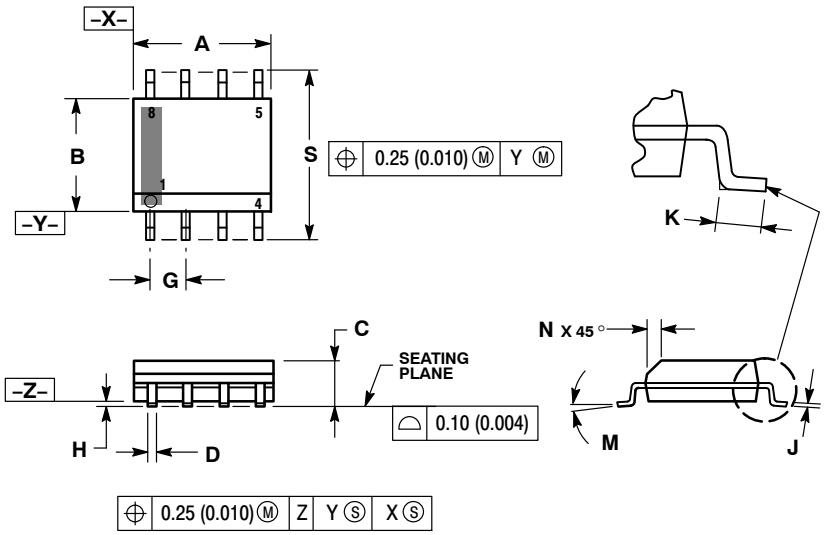



DIMENSIONS: MILLIMETERS

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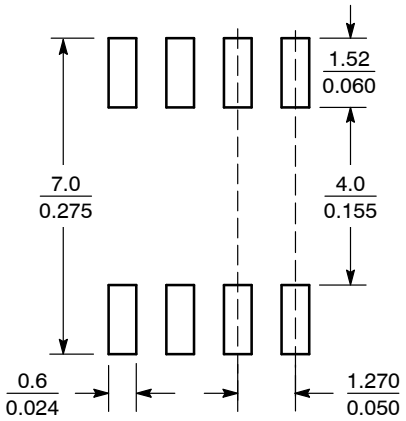
**SOIC−8 NB**
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ISSUE AK




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

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SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

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