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FAIRCHILD SEMICONDUCTOR®

June 2009

FDMC7200

Dual N-Channel PowerTrench® MOSFET

30 V, 12 mΩ and **23.5 mΩ**

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 23.5 mΩ at V_{GS} = 10 V, I_D = 6 A
- Max $r_{DS(on)}$ = 38 mΩ at V_{GS} = 4.5 V, I_D = 5 A

Q2: N-Channel

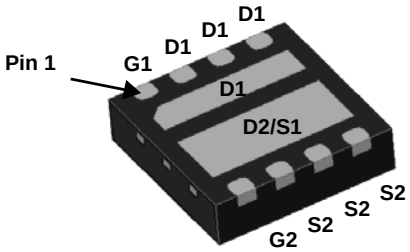
- Max $r_{DS(on)}$ = 12 mΩ at V_{GS} = 10 V, I_D = 8 A
- Max $r_{DS(on)}$ = 18 mΩ at V_{GS} = 4.5 V, I_D = 7 A
- RoHS Compliant

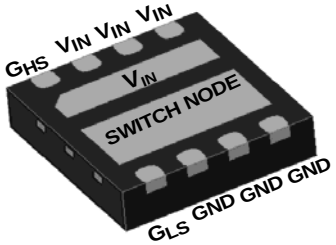
General Description

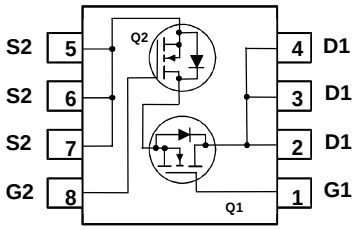
This device includes two specialized N-Channel MOSFETs in a dual Power33 (3mm x 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load







Power 33

MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
I_D	Drain Current - Continuous (Package limited)	T_C = 25 °C	8	8	A
	- Continuous (Silicon limited)	T_C = 25 °C	20	40	
	- Continuous	T_A = 25 °C	6 [1a]	8 [1b]	
	- Pulsed		40	40	
P_D	Power Dissipation	T_A = 25 °C	1.9 [1a]	2.2 [1b]	W
	Power Dissipation	T_A = 25 °C	0.7 [1c]	0.9 [1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 [1a]	55 [1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 [1c]	145 [1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	4	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7200	FDMC7200	Power 33	13 ”	12 mm	3000 units

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Electrical Characteristics T_J = 25 °C unless otherwise noted

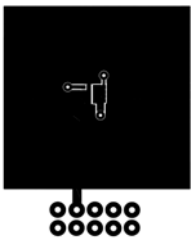
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 250 μA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 250 μA, referenced to 25 °C	Q1 Q2		14 14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 20 V, V_{GS} = 0 V	Q1 Q2			100 100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 250 μA	Q1 Q2	1.0 1.0	2.3 2.3	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 250 μA, referenced to 25 °C	Q1 Q2		-5 -6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6 A V_{GS} = 4.5 V, I_D = 5 A V_{GS} = 10 V, I_D = 6 A, T_J = 125 °C	Q1		19 28 29	23.5 38 35.5	mΩ
		V_{GS} = 10 V, I_D = 8 A V_{GS} = 4.5 V, I_D = 7 A V_{GS} = 10 V, I_D = 8 A, T_J = 125 °C	Q2		10 13 15	12 18 18	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 6 A V_{DD} = 5 V, I_D = 8 A	Q1 Q2		29 56		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		495 1180	660 1570	pF
C_{oss}	Output Capacitance		Q1 Q2		145 330	195 440	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		20 30	30 45	pF
R_g	Gate Resistance		Q1 Q2		1.4 1.4		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	Q1 Q2		11 13	20 23	ns
t_r	Rise Time		Q1 Q2		3.1 4	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	Q1 Q2		35 38	56 60	ns
t_f	Fall Time		Q1 Q2		1.3 6	10 12	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V Q1: V_{DD} = 15 V, I_D = 6 A,	Q1 Q2		7.3 16	10 22	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V	Q1 Q2		3.1 7	4.3 10	nC
Q_{gs}	Gate to Source Charge	Q2: V_{DD} = 15 V, I_D = 8 A,	Q1 Q2		1.8 4.1		nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		1 1.5		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

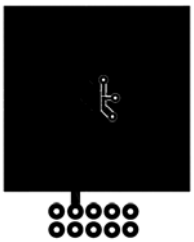
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 6 A (Note 2) V_{GS} = 0 V, I_S = 8 A (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 6 A, di/dt = 100 A/s	Q1 Q2		13 21	24 34	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 8 A, di/dt = 100 A/s	Q1 Q2		2.3 5.6	10 12	nC

Notes:

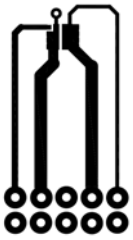
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



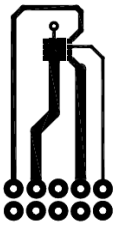
a.65 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b.55 °C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 180 °C/W when mounted on a minimum pad of 2 oz copper



d. 145 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

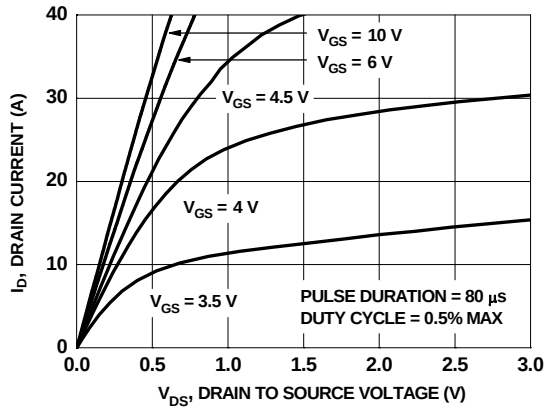


Figure 1. On Region Characteristics

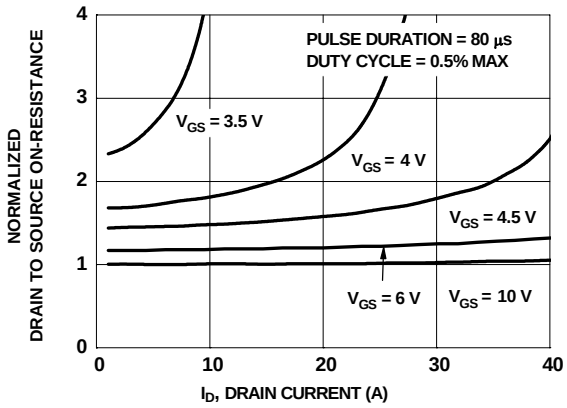


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

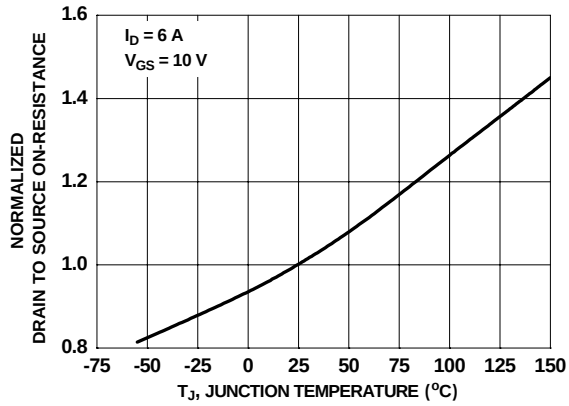


Figure 3. Normalized On Resistance vs Junction Temperature

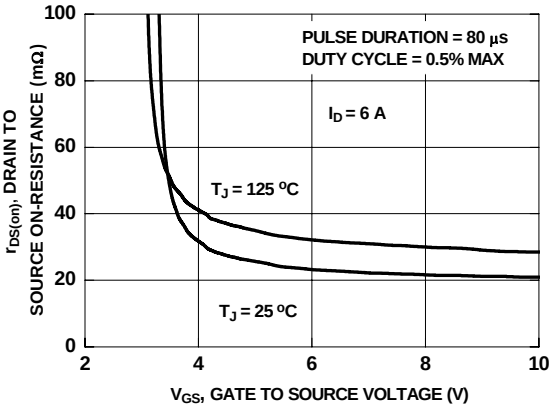


Figure 4. On-Resistance vs Gate to Source Voltage

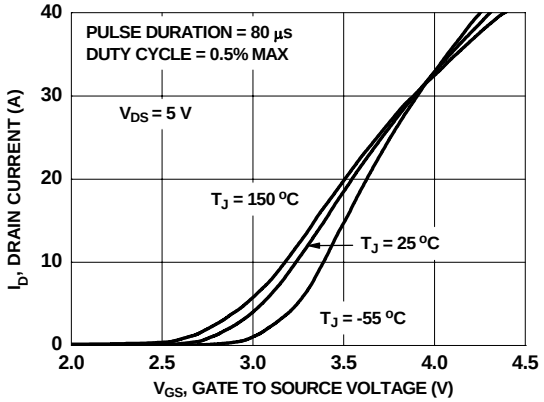


Figure 5. Transfer Characteristics

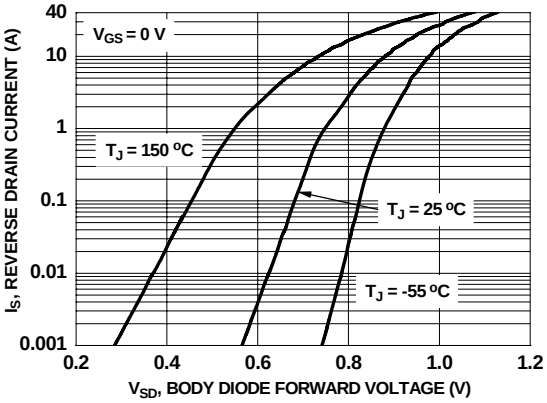


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

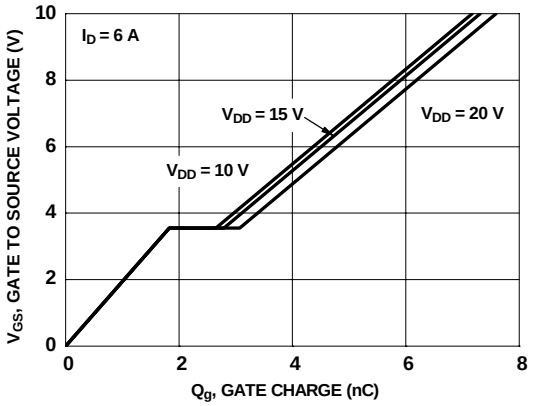


Figure 7. Gate Charge Characteristics

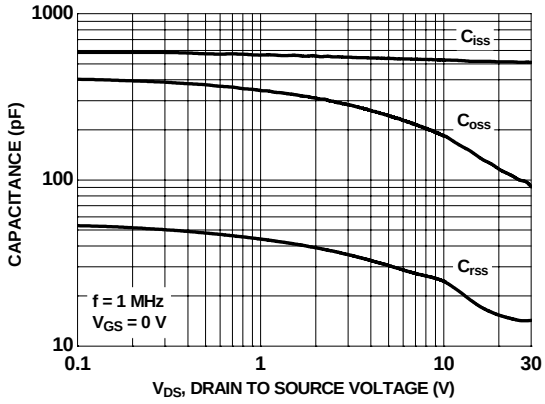


Figure 8. Capacitance vs Drain to Source Voltage

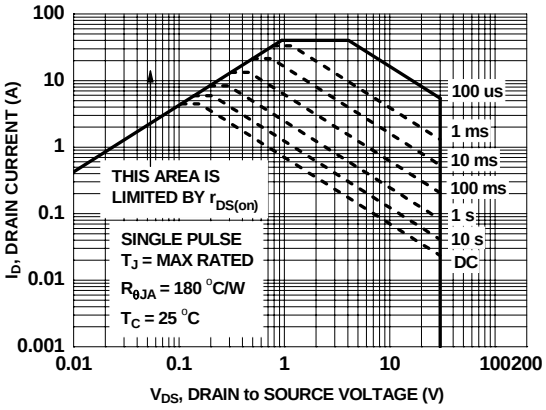


Figure 9. Forward Bias Safe Operating Area

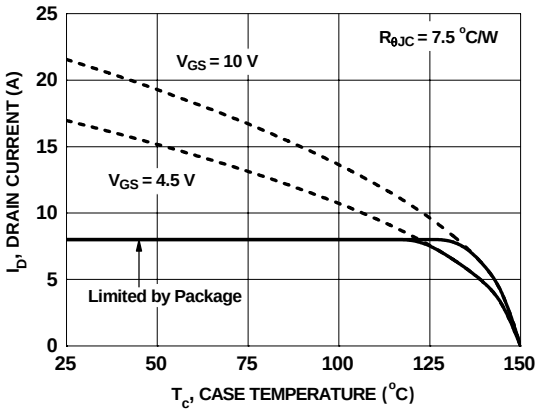


Figure 10. Maximum Continuous Drain Current vs Case Temperature

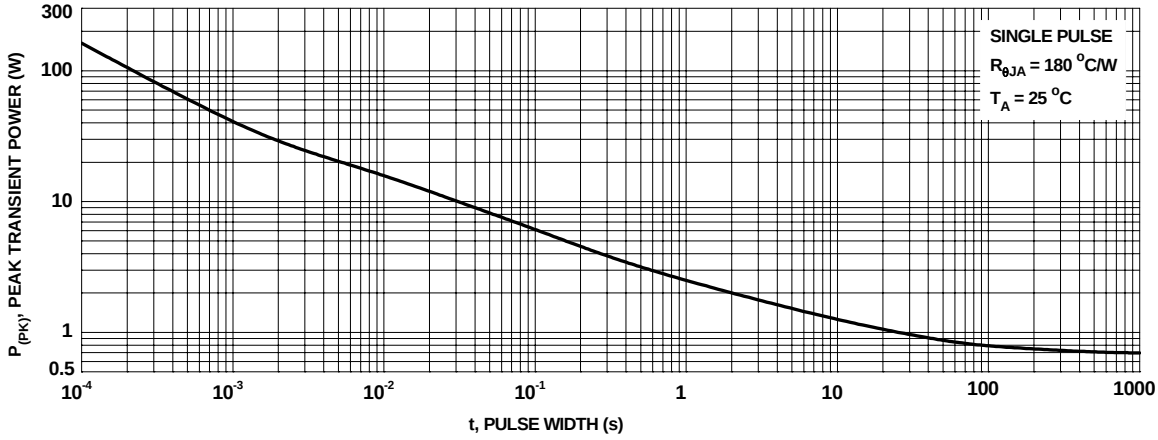


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

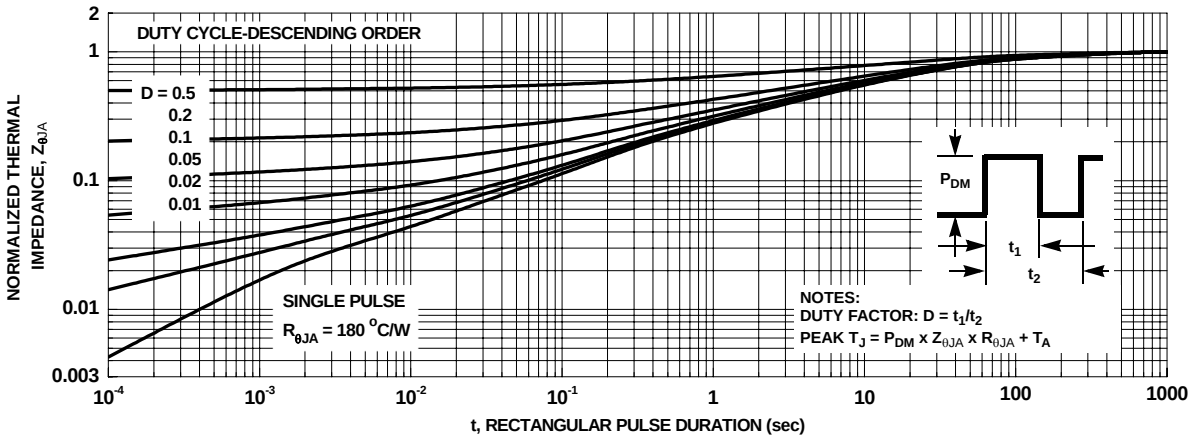


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

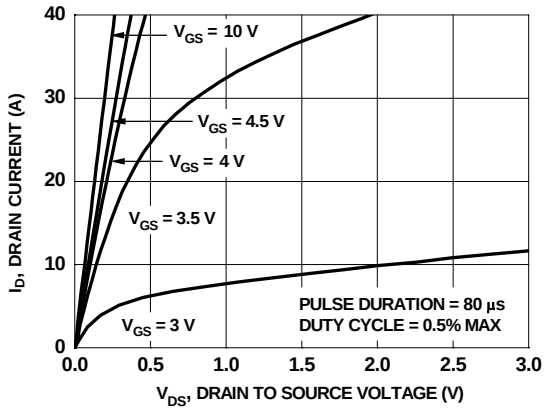


Figure 13. On-Region Characteristics

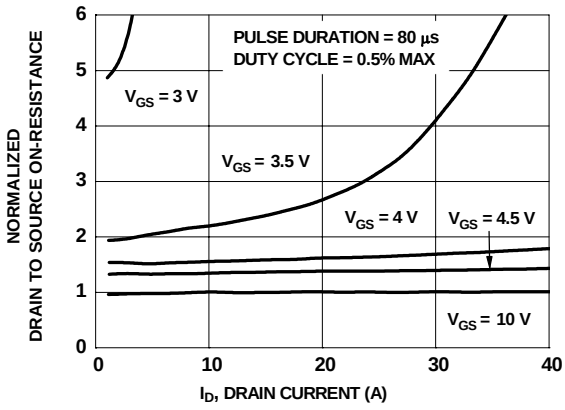


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

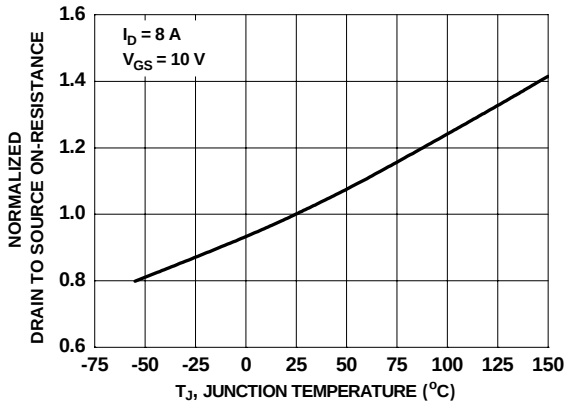


Figure 15. Normalized On-Resistance vs Junction Temperature

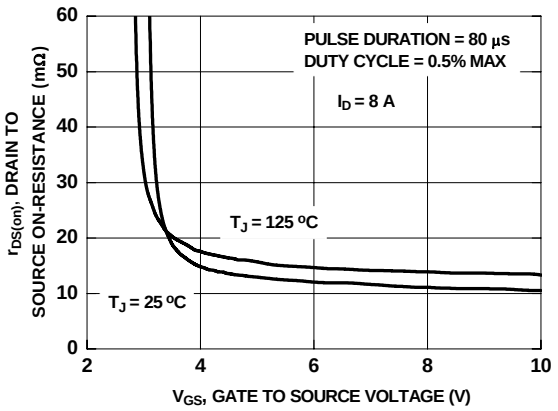


Figure 16. On-Resistance vs Gate to Source Voltage

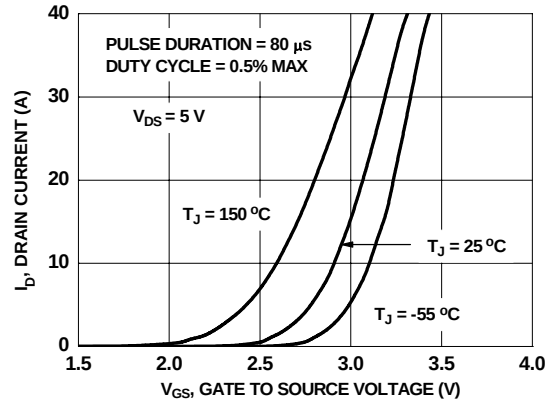


Figure 17. Transfer Characteristics

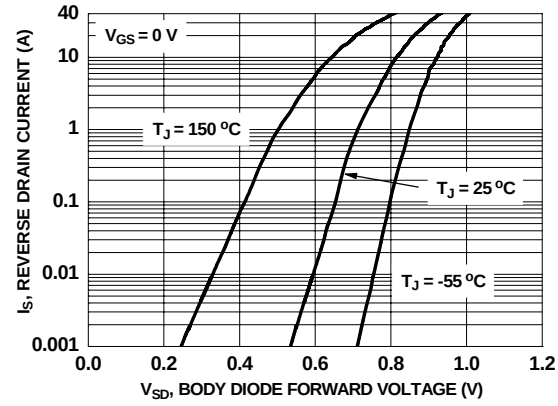


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

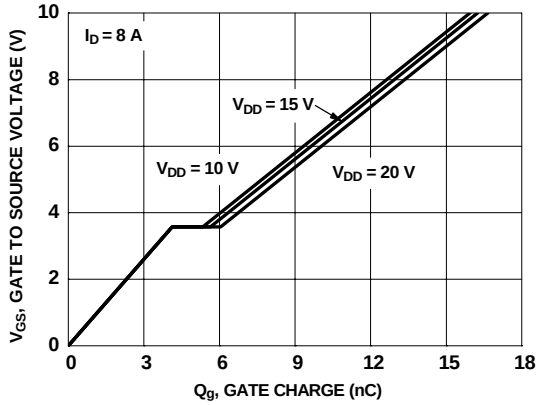


Figure 19. Gate Charge Characteristics

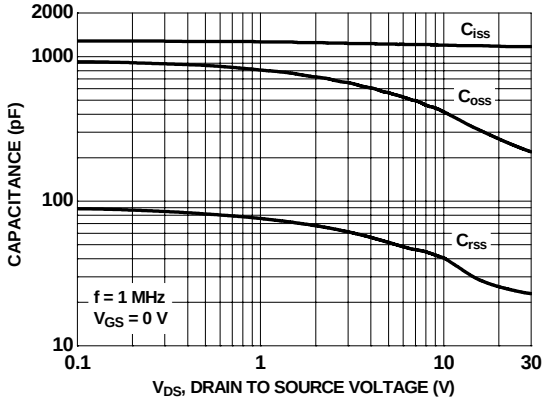


Figure 20. Capacitance vs Drain to Source Voltage

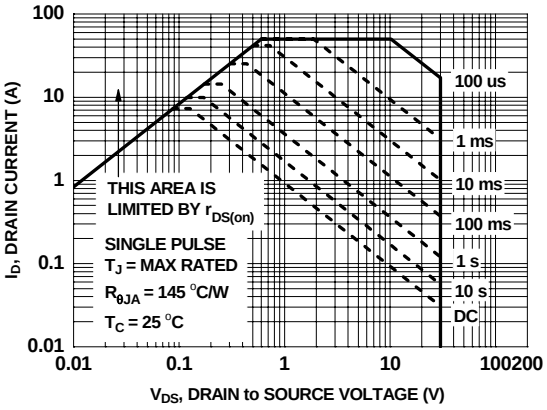


Figure 21. Forward Bias Safe Operating Area

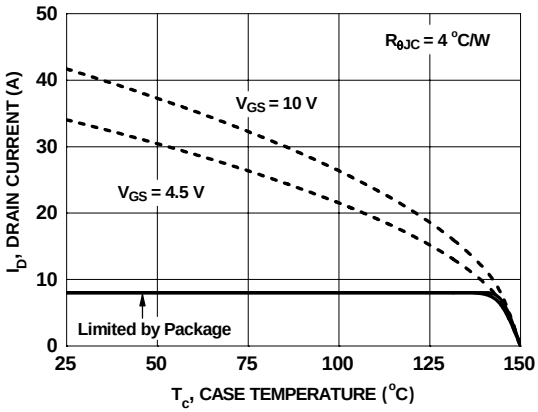


Figure 22. Maximum Continuous Drain Current vs Case Temperature

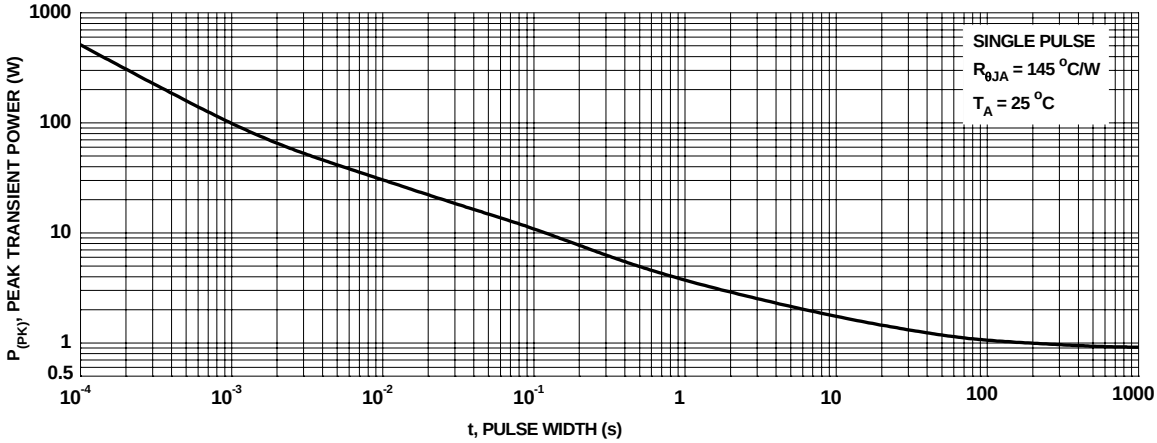


Figure 22. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

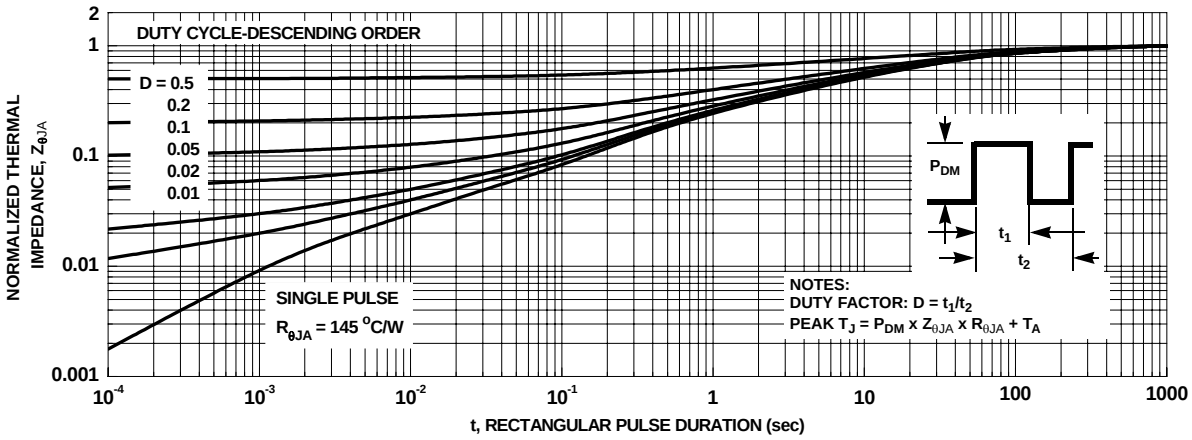
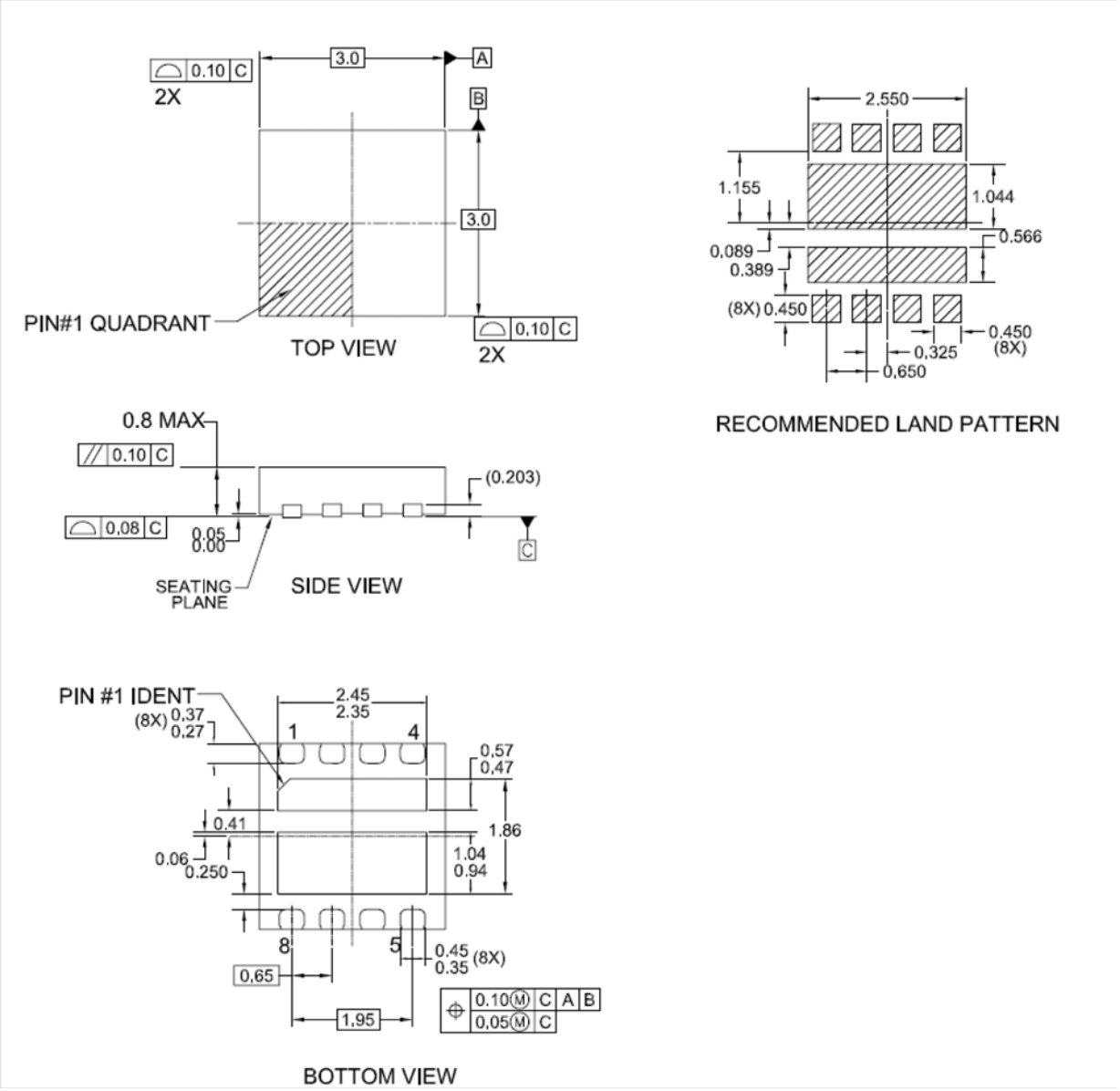


Figure 23. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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MegaBuck™
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