Evaluation Board User Guide
UG-119

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# ADAU1361 Evaluation Board

## PACKAGE CONTENTS

**ADAU1361 evaluation board**
**USBi control interface board**
**USB cable**
**Evaluation board documentation/quick-start guide**

## SUPPORTING DOCUMENTATION

**ADAU1361 data sheet**
**AN-1056 Application Note, *Capless Headphone Virtual Ground Short-Circuit Protection for the ADAU1361 and ADAU1761***
**AN-1006 Application Note, *Using the EVAL-ADUSB2EBZ***
**AN-1007 Application Note, *Using the ADAU1761 in DSP Bypass Mode to Emulate an ADAU1361***
**SigmaStudio Help (included in software installation)**

## GENERAL DESCRIPTION

This user guide explains the design and setup of the ADAU1361 evaluation board.

The EVAL-ADAU1361Z includes both single-ended and differential stereo line-level analog audio inputs as well as a digital audio interface. Single-ended and differential analog outputs are also provided, as well as a stereo capless headphone output.

The USBi provides power and the I²C communications interface to the evaluation board. A switch allows the ADAU1361 to operate at either 3.3 V or 1.8 V. The SigmaStudio™ programming software is used for all register controls and SigmaDSP® core programming.

A header is included for interfacing to stereo digital microphones.

## EVALUATION BOARD BLOCK DIAGRAM

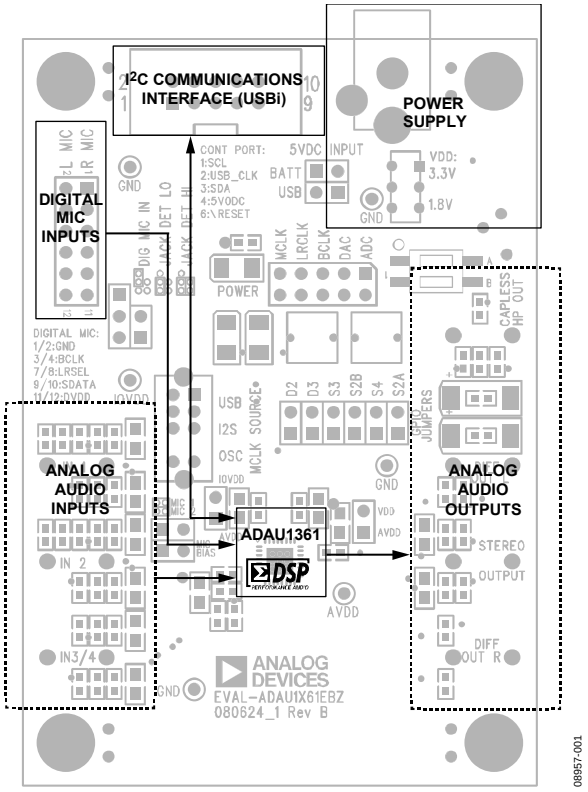


*Figure 1.*

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## REVISION HISTORY

**3/10—Revision 0: Initial Version**

# SETTING UP THE EVALUATION BOARD—QUICK START

## SigmaStudio SOFTWARE INSTALLATION

To install the SigmaStudio software, follow these steps:

1. Open the provided .zip file and extract the files to your PC. Alternately, insert the SigmaStudio CD into the PC optical drive and locate the SigmaStudio folder on the CD.
2. If Microsoft® .NET Framework Version 2.0 is not already installed on the PC, install it by double-clicking **dotnetfx.exe**.
3. Install SigmaStudio by double-clicking **setup.exe** and following the prompts. A computer restart is not required.

## HARDWARE SETUP, USBi

To set up the USBi hardware, follow these steps:

1. Plug the USBi ribbon cable into Header J1.
2. Connect the USB cable to your computer and to the USBi.
3. When prompted for drivers, follow these steps:
   a) Choose **Install from a list or a specific location**.
   b) Choose **Search for the best driver in these locations**.
   c) Check the box for **Include this location in the search**.
   d) The USBi driver is located in **C:\Program Files\Analog Devices Inc\Sigma Studio\USB drivers**.
   e) Click **Next**.
   f) If prompted to choose a driver, select **CyUSB.sys**.
   g) If the PC is running Windows® XP and you receive the message that the software has not passed Windows Logo testing, click **Continue Anyway**.

## POWERING THE BOARD

The board can be powered either by the USBi or by an external power supply. For the board to run independently from the computer, disconnect Jumper J5 and connect the power supply at J2. The power indicator LED D1 should now be lit.

## CONNECTING AUDIO CABLES

In this example, the board is set up for stereo analog inputs and stereo analog outputs, using 3.5 mm (1/8") cables.

1. Connect the audio source to Input Jack J24.
2. Connect Output Jack J19 to your headphones.

## SWITCH AND JUMPER SETTINGS

To configure the board for stereo analog input and output, make sure that the switches and jumpers are set as follows (see Figure 2).

- The ADAU1361 uses the on-board oscillator as a master clock source (S5 switched to OSC).
- Regulator output VDD is set for 3.3 V operation (S1 switched to 3.3 V).
- Power is supplied by USB (J5 is connected with a jumper).
- AVDD is connected to VDD (J17 connected).
- IOVDD and AVDD operate at VDD (J16 connected).
- DAC_SDATA and ADC_SDATA are tied together to loop-back data from ADC to DAC (jumper across two bottom right pins of J6).
- $I^2C$ control mode is hardwired on board.

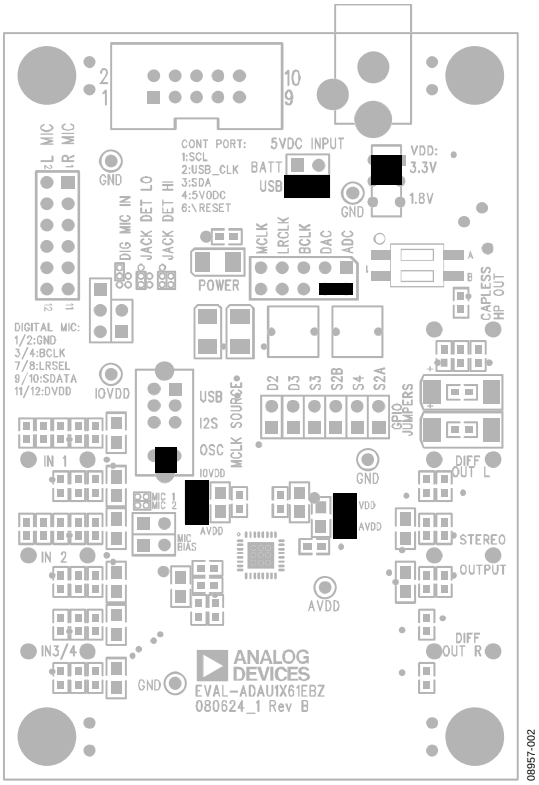


*Figure 2. Evaluation Board Setup and Configuration*

## SETTING UP THE REGISTERS IN SigmaStudio

This section details how to pass an audio signal from the ADC inputs to the DAC outputs using the headphone drivers. The codec is configured with SigmaStudio.

1. Create a new project. The **Hardware Configuration** tab opens.
2. Drag an **ADAU1361** cell and a **USBi** cell into the blank work area.
3. Connect the **USBi** cell to the **ADAU1361** cell by clicking and dragging from the top blue output pin of the **USBi** cell to the green input pin of the **ADAU1361** cell.

   Your screen should now resemble Figure 3.

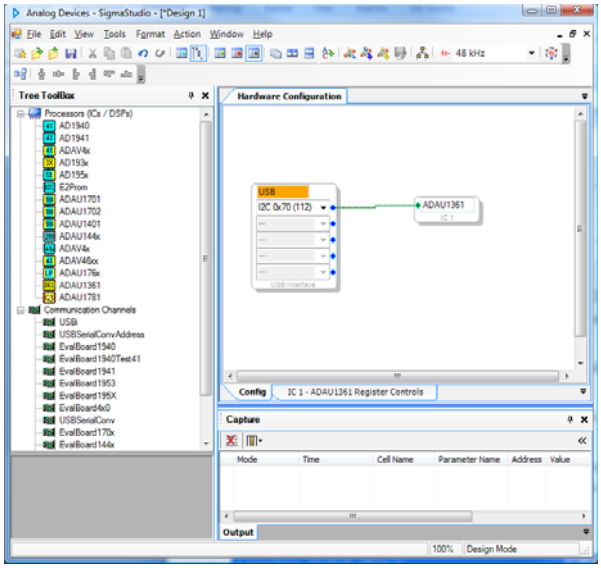


*Figure 3. Hardware Configuration Tab*

1. In the **IC1-ADAU1361 Register Controls** tab, select the **3 and 4 in Capless HP Out** option from the **Automatic Startup** list and click **Load Preset** (see Figure 4).

   This locks the PLL and sets up the registers for proper routing of the record and playback paths. If the PLL has successfully locked, then the box under **PLL Lock Bit** should turn from red to green.
2. Start playing the audio source; you should hear audio on the outputs.

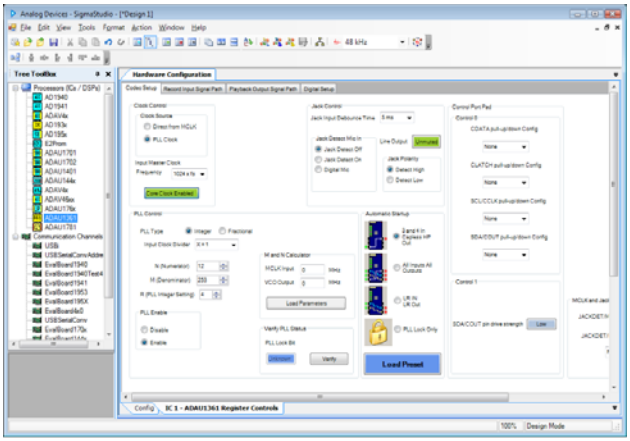


*Figure 4. Hardware Configuration Tab—Register Setup*

# USING THE EVALUATION BOARD

## ADAU1361 LOW-POWER CODEC

The ADAU1361 is a low power, stereo audio codec that supports stereo 48 kHz record and playback at 14 mW from a 1.8 V analog supply. The stereo audio ADCs and DACs support sample rates from 8 kHz to 96 kHz as well as a digital volume control.

The SigmaStudio graphical development tool is used to configure the ADAU1361. SigmaStudio's outputs can be used to easily integrate the ADAU1361 in a system.

The record path includes an integrated microphone bias circuit and six inputs. The inputs can be mixed and muxed before the ADC, or they can be configured to bypass the ADC. The ADAU1361 includes a stereo digital microphone input.

The ADAU1361 includes five high power output drivers (two differential and three single-ended) that support stereo headphones, an earpiece, or other output transducers. AC-coupled or capless configurations are supported. Individual fine level controls are supported on all analog outputs. The output mixer stage allows for flexible routing of audio.

## POWER

The evaluation board uses the ADP3336 low dropout voltage regulator to generate either 3.3 V or 1.8 V for the board. The output voltage VDD of the ADP3336 is set with external resistors that can be switched with S1 to select either 3.3 V or 1.8 V outputs (see Table 1).

**Table 1. VDD Voltage Settings**

| Voltage Regulator Output (V) | S1 Setting |
|---|---|
| 3.3 | Up |
| 1.8 | Down |

The maximum operating current draw from this board is approximately 75 mA. This maximum value is reached with VDD = 3.3 V, headphone outputs enabled, and all LEDs enabled.

Typically, the regulator input comes from the USBi 5 V dc USB supply on Header J1. This supply is enabled with a jumper on J5. To use another 5 V dc supply source, remove the jumper on J5 and connect the other supply either on the J2 power jack (positive tip) or via soldering leads from a supply such as a battery to J3. On J3, Pin 1 (square pad) is ground, and Pin 2 (circle pad) is the power connection.

When the ADP3336 is outputting a regulated voltage, LED D1 is illuminated red.

VDD is connected to the AVDD pin of the ADAU1361 with Jumper J17. To connect the ADAU1361 IOVDD pin to the same supply, connect J16, also. These headers can also be used to separate the supplies of the ADAU1361 from the rest of the board and to connect an external supply to the ADAU1361.

L1 and C24 are connected to the AVDD pin of the ADAU1361 and function as an L-C filter to reject high frequency power supply noise common in GSM mobile applications. This filter is tuned to approximately 1.5 GHz.

## ANALOG AUDIO INPUT

The EVAL-ADAU1361Z has three ac-coupled 1/8" input jacks: two mono differential jacks and one stereo single-ended jack. The tips of the differential input jacks, J20 and J22 (labeled IN 1 and IN 2), are connected to the negative input of the ADAU1361, and the rings are connected to the positive input. The stereo single-ended input on J24 (labeled IN 3) is connected to the LAUX and RAUX inputs of the ADAU1361. IN 1 and IN 2 can also be configured to bias a microphone. This is enabled by connecting the MICBIAS pin of the ADAU1361 to the tip of the input connectors with Jumper J15 and Jumper J18.

At VDD = 3.3 V, the full-scale analog input level of the EVAL-ADAU1361Z is 1.0 V rms (1.0 V rms on the single-ended inputs and 0.5 V rms on each of the two pins of the differential inputs). The full-scale input level scales with VDD.

## ANALOG AUDIO OUTPUT

The EVAL-ADAU1361Z has four 1/8" output jacks: two mono differential, one stereo single-ended, and one stereo capless headphone output. The differential outputs on J21 and J25 (labeled DIFF OUT L and DIFF OUT R, respectively, are biased at AVDD/2 V. The tips of the differential output jacks are connected to the positive output of the ADAU1361, and the rings are connected to the negative outputs. J23 is a stereo, single-ended, ac-coupled output.

At VDD = 3.3 V, the full-scale analog output level of the EVAL-ADAU1361Z is 1.0 V rms (1.0 V rms on the single-ended outputs and 0.5 V rms on each of the two pins of the differential outputs). The differential line outputs of the ADAU1361 can each be boosted by 6 dB to 2.0 V rms. The full-scale output level scales with VDD.

Note that Jack J21 and Jack J25 tie the ring to the sleeve, resulting in a floating ground output. Be aware of this when connecting to these outputs.

**Table 2. Analog and Digital Audio Connectors**

| Jack | Function |
|---|---|
| J4 | Stereo digital microphone input |
| J6 | Serial data port input/output |
| J19 | Capless headphone output |
| J20 | Left differential input |
| J21 | Left differential output |
| J22 | Right differential input |
| J23 | Stereo single-ended line output |
| J24 | Stereo single-ended line input |
| J25 | Right differential output |

## CLOCKING THE EVALUATION BOARD

The EVAL-ADAU1361Z requires a master clock to operate. The source of this clock is set by Switch S5 (see Table 3).

**Table 3. Master Clock Source Settings**

| Clock Source | S5 Setting |
|---|---|
| Do Not Use—Function Disabled on USBi | Up |
| MCLK from Header J6 | Middle |
| On-Board 12.288 MHz Clock Oscillator (U3) | Down |

## EXTERNAL DIGITAL AUDIO HEADER

The LRCLK, BCLK, ADC_SDATA, and DAC_SDATA pins of the ADAU1361 can be connected to external devices with the 5 × 2 header, J6. The pins on the top row of J6 are connected to ground; the pins on the bottom row are the signals indicated on the silkscreen.

## DIGITAL MICROPHONE AND JACK DETECTION INPUT

A pair of digital microphones can be connected to the evaluation board on Header J4. The pin connections for J4 are detailed on the evaluation board silkscreen.

J7 and J8 set up the routing of signals to the JACKDET/MICIN pin of the ADAU1361. These jumper settings are shown in Figure 5, Figure 6, and Figure 7; they are also shown on the PCB silkscreen. Toggling the jack detection signal can be simulated by setting up the jack detect function on the ADAU1361 and then inserting and removing Jumper J8 with J7-B (lower connection) connected.

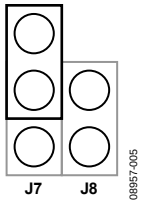


*Figure 5. Jumper Settings (J7 and J8) for Stereo Digital Microphone Input*

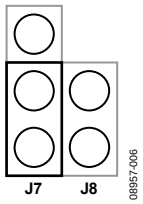


*Figure 6. Jumper Settings (J7 and J8) for Jack Detection (Low Signal Detected)*

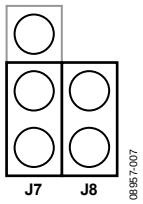


*Figure 7. Jumper Settings (J7 and J8) for Jack Detection (High Signal Detected)*

## I²C COMMUNICATIONS HEADER

The I²C communications header, J1, provides an interface to the ADAU1361 communications port. This header connects to the USBi board (EVAL-ADUSB2), which controls communication between the evaluation board and SigmaStudio on the PC. Additionally, a DSP reset line and USB bus power line are provided. The SigmaStudio hardware configuration for this setup is shown in Figure 8.

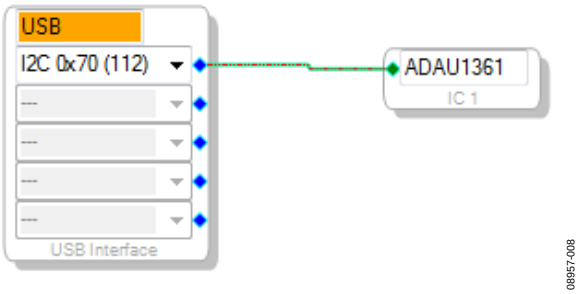


*Figure 8. Using the EVAL-ADAU1361Z and the USBi with SigmaStudio*

# EVALUATION BOARD SCHEMATICS AND ARTWORK

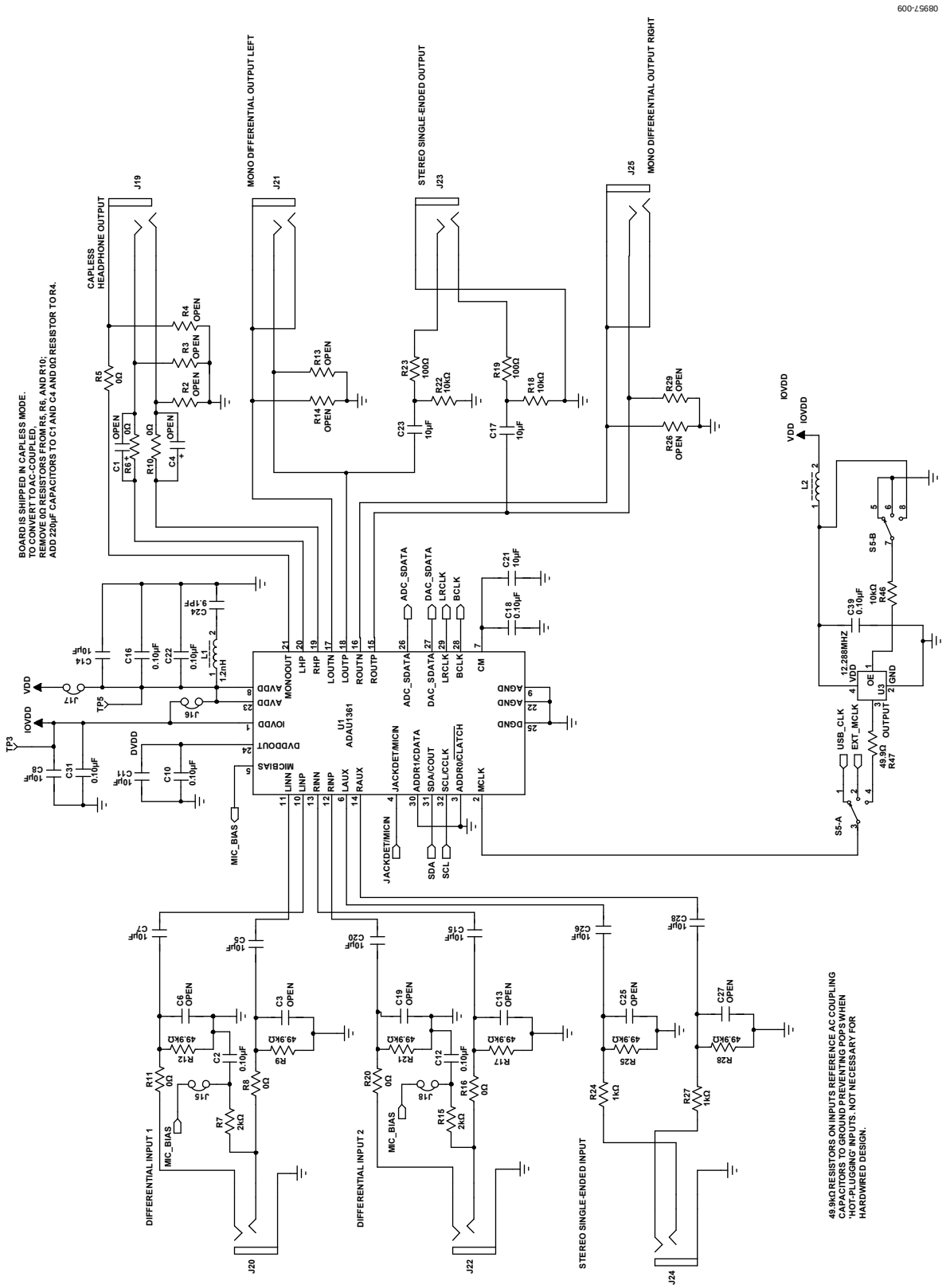


*Figure 9. Board Schematics, Page 1*

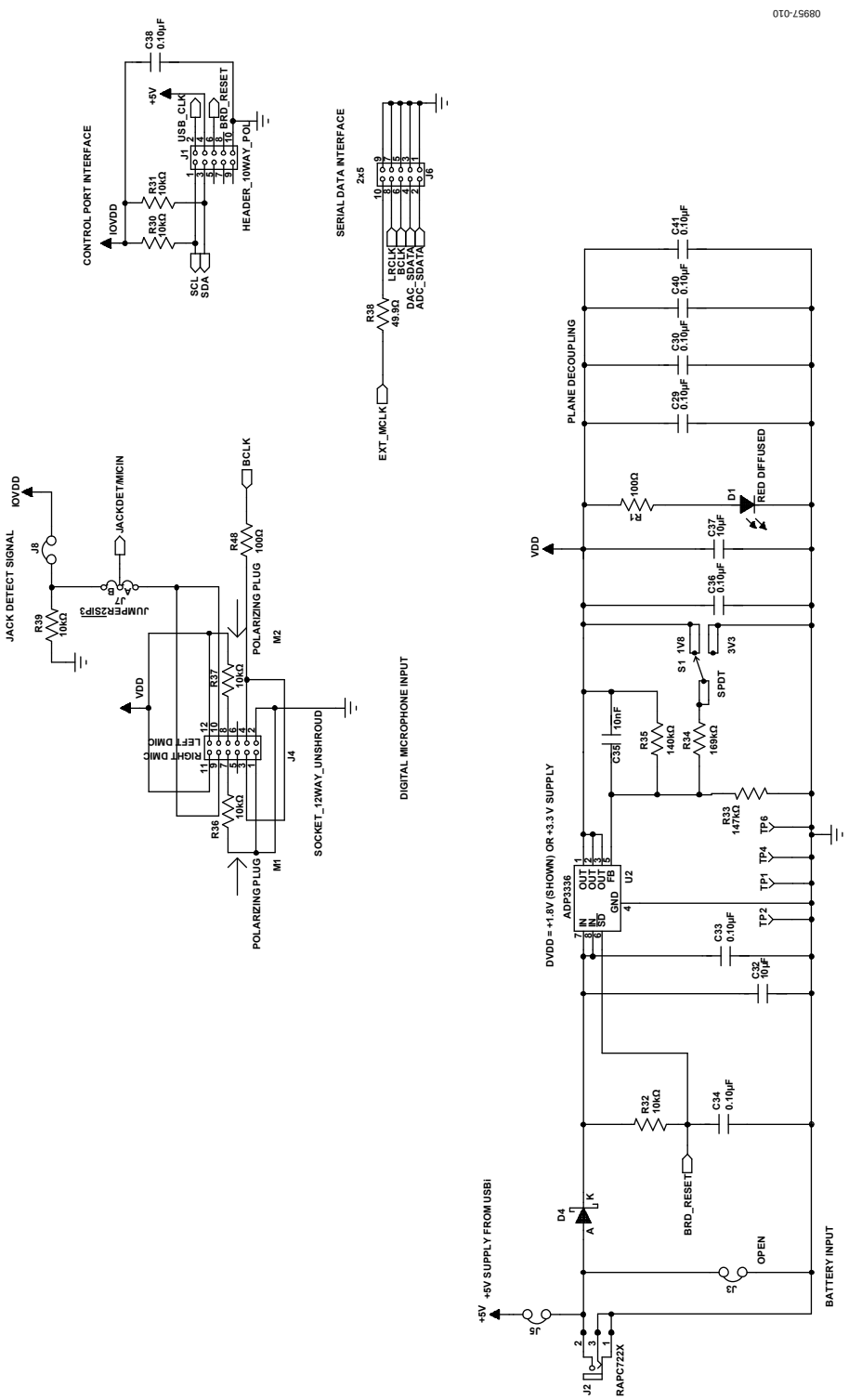


*Figure 10. Board Schematics, Page 2*

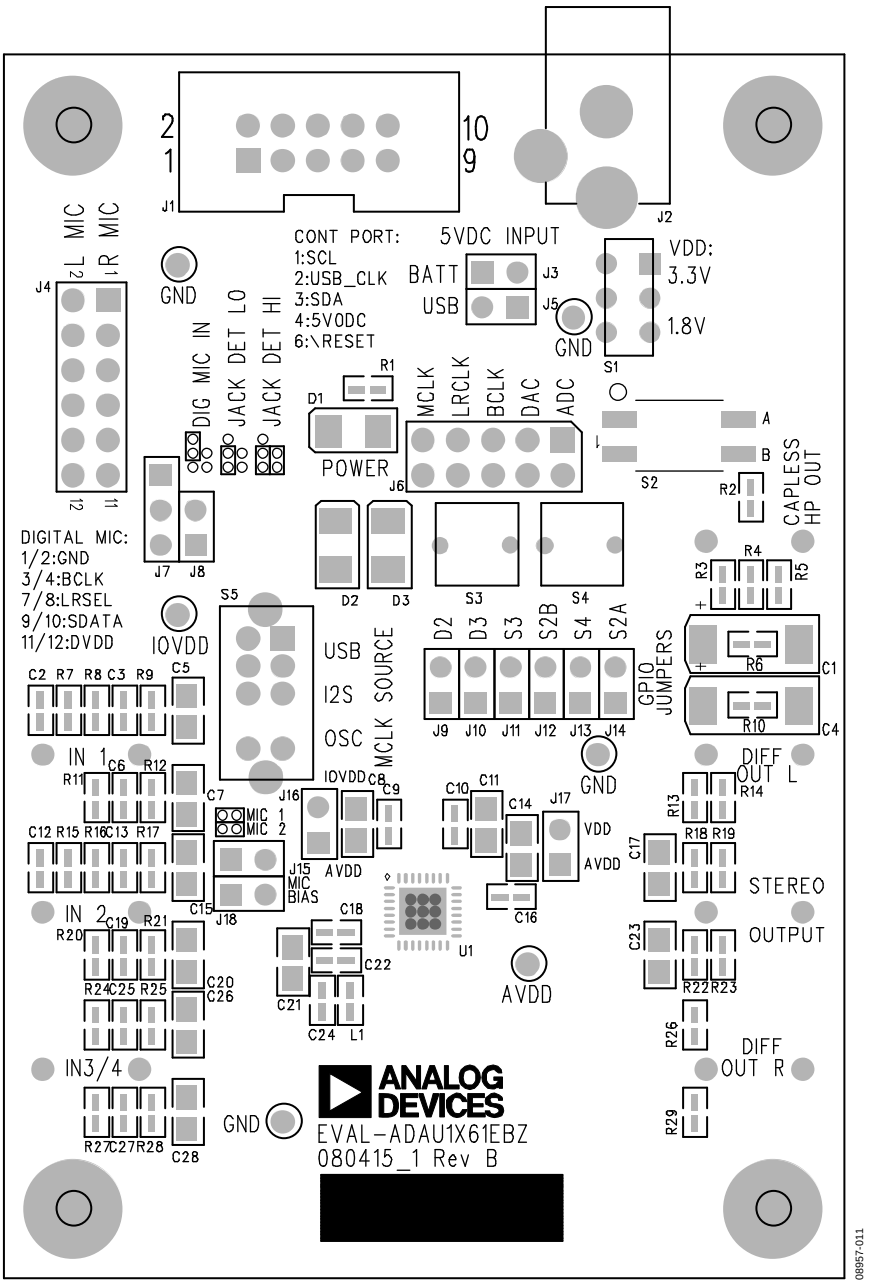


*Figure 11. Board Silkscreen and Parts Placement*

# ORDERING INFORMATION

## BILL OF MATERIALS

**Table 4.**

| Qty | Designator | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| 2 | C1, C4 | Capacitor (open) | | |
| 12 | C2, C10, C12, C16, C18, C22, C31, C33, C34, C36, C38, C39 | Capacitor, multilayer ceramic, 0.10 µF, 50 V, X7R, 0603 | Panasonic | ECJ-1VB1H104K |
| 6 | C3, C6, C13, C19, C25, C27 | Capacitor (open) | | |
| 14 | C5, C7, C8, C11, C14, C15, C17, C20, C21, C23, C26, C28, C32, C37 | Capacitor, multilayer ceramic, 10 µF, 10 V, X7R, 0805 | Murata | GRM21BR71A106KE51L |
| 1 | C24 | Capacitor, multilayer ceramic, 9.1 pF, 50 V, NP0, 0603 | Murata | GQM1885C1H9R1CB01D |
| 4 | C29, C30, C40, C41 | Capacitor, multilayer ceramic, 0.10 µF, 16 V, X7R, 0402 | Panasonic | ECJ-0EX1C104K |
| 1 | C35 | Capacitor, multilayer ceramic, 10 nF, 25 V, NP0, 0603 | TDK | C1608C0G1E103J |
| 1 | D1 | LED, red diffused, 6 millicandela, 635 nm, 1206 | Lumex | SML-LX1206IW-TR |
| 1 | D4 | Schottky diode, 30 V, 0.5 A, SOD-123 | ON Semiconductor | MBR0530T1G |
| 1 | J1 | Header, 10-way (2 × 5), shrouded, polarized | 3M | N2510-6002RB |
| 1 | J2 | Mini power jack, 0.08", R/A T/H | Switchcraft, Inc. | RAPC722X |
| 1 | J3 | Open | | |
| 1 | J4 | Header, 12-way (2 × 6), socket, unshrouded | Sullins Connector Solutions | PPPC062LFBN-RC |
| 6 | J5, J8, J15 to J18 | Header, 2-pin, unshrouded, 2-jumper, 0.10" (use Tyco shunt, 881545-2) | Sullins Connector Solutions | PBC02SAAN |
| 1 | J6 | Header, 10-way (2 × 5), unshrouded | Sullins Connector Solutions | PBC05DAAN |
| 1 | J7 | Header, 3-position, SIP | Sullins Connector Solutions | PBC03SAAN |
| 7 | J19 to J25 | Stereo mini jack, SMT | CUI Inc. | SJ-3523-SMT |
| 1 | L1 | Inductor, 1.2 nH | Jaro Components, Inc. | HFI-160808-1N2S |
| 1 | L2 | Chip ferrite bead, 600 Ω @ 100 MHz | TDK | MPZ1608S601A |
| 4 | R1, R19, R23, R48 | Chip resistor, 100 Ω, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF1000V |
| 7 | R2 to R4, R13, R14, R26, R29 | Resistor, open | | |
| 7 | R5, R6, R8, R10, R11, R16, R20 | Chip resistor, 0 Ω, 5%, 100 mW, thick film, 0603 | Panasonic | ERJ-3GEY0R00V |
| 2 | R7, R15 | Chip resistor, 2 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF2001V |
| 6 | R9, R12, R17, R21, R25, R28 | Chip resistor, 49.9 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF4992V |
| 9 | R18, R22, R30 to R32, R36, R37, R39, R46 | Chip resistor, 10 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF1002V |
| 2 | R24, R27 | Chip resistor, 1 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF1001V |
| 1 | R33 | Chip resistor, 147 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF1473V |
| 1 | R34 | Chip resistor, 169 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF1693V |
| 1 | R35 | Chip resistor, 140 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF1403V |
| 2 | R38, R47 | Chip resistor, 49.9 Ω, 1%, 100 mW, thick film, 0603 | Panasonic | ERJ-3EKF49R9V |
| 1 | S1 | Slide switch, SPDT, PC mount, L = 2 mm | E-Switch | EG1271 |
| 1 | S5 | Slide switch, DP3T, PC mount, L = 4 mm | E-Switch | EG2305 |
| 6 | TP1 to TP6 | Mini test point, white, 0.1" OD | Keystone Electronics | 5002 |
| 1 | U1 | SigmaDSP codec | Analog Devices | ADAU1361BCPZ |
| 1 | U2 | Adjustable low dropout voltage regulator | Analog Devices | ADP3336ARMZ |
| 1 | U3 | SMD oscillator, 12.288 MHz, fixed, 1.8 VDC to 3.3 VDC | Abracon Corporation | AP3S-12.288MHz-F-J-B |

## NOTES

# NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



**UG08957-0-3/10(0)**


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