5-Bit Adjustable High Efficiency Synchronous Step-Down Switching Regulator

FEATURES

- Dual N-Channel MOSFET Synchronous Drive
- **Synchronizable/Programmable Fixed Frequency**
- Wide V_{IN} Range: 3.5V to 36V Operation
- 5-Bit Digital-to-Analog V_{OUT} Selection: 0.925V to 2.00V Range with 50mV/25mV Steps
- **OPTI-LOOP™ Compensation Minimizes C_{OUT}**
- **±1% Output Voltage Accuracy**
- Power Good Output Voltage Monitor
- Active Voltage Positioning Compatible
- Output Overvoltage Crowbar Protection
- Internal Current Foldback
- Latched Short-Circuit Shutdown Timer with Defeat Option
- Forced Continuous Control Pin
- Optional Programmable Soft-Start
- Remote Output Voltage Sense
- Available in 24-Lead SSOP Package

APPLICATIONS

- Notebook and Palmtop Computers, PDAs
- Power Supply for Mobile Pentium® II and Pentium III Processors
- Low Voltage Power Supplies

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DESCRIPTION

The LTC®1736 is a synchronous step-down switching regulator controller optimized for CPU power. The output voltage is programmed by a 5-bit digital-to-analog converter (DAC) that adjusts the output voltage from 0.925V to 2.00V according to Intel mobile VID specifications. The 0.8V reference is compatible with future microprocessor generations.

The operating frequency (synchronizable up to 500kHz) is set by an external capacitor allowing maximum flexibility in optimizing efficiency. The output voltage is monitored by a power good window comparator that indicates when the output is within 7.5% of its programmed value.

Protection features include: internal foldback current limiting, output overvoltage crowbar and optional short-circuit shutdown. Soft-start is provided by an external capacitor that can be used to properly sequence supplies. The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V to 30V (36V maximum).

Pin defeatable Burst Mode™ operation provides high efficiency at low load currents. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

TYPICAL APPLICATION

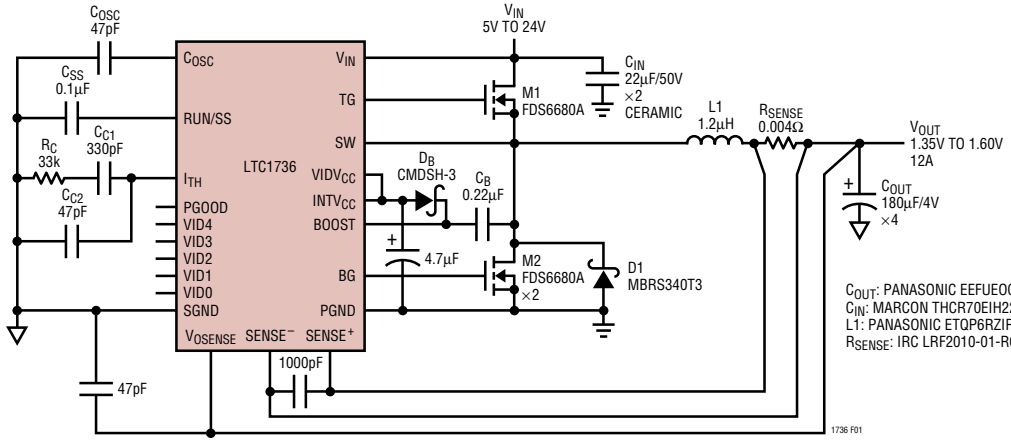


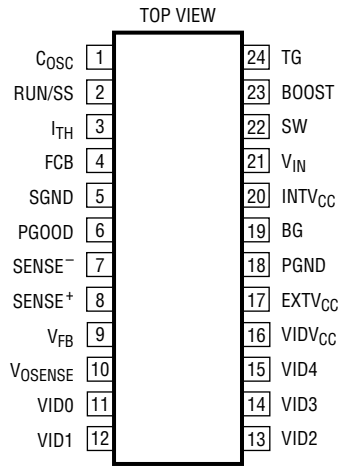
Figure 1. High Efficiency Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Supply Voltage (BOOST) .... 42V to –0.3V
Switch Voltage (SW) ..... 36V to –5V
$EXTV_{CC}$, $VIDV_{CC}$, (BOOST – SW) Voltages .. 7V to –0.3V
$SENSE^+$, $SENSE^-$ ..... 1.1($INTV_{CC}$) to –0.3V
FCB Voltage ..... ($INTV_{CC}$ + 0.3V) to –0.3V
I_{TH}, V_{OSENSE}, V_{FB} Voltage ..... 2.7V to –0.3V
RUN/SS, VID0 to VID4, PGOOD Voltages .... 7V to –0.3V
Peak Driver Output Current <10µs (TG, BG) 3A
$INTV_{CC}$ Output Current 50mA
Operating Ambient Temperature Range
LTC1736C ..... 0°C to 85°C
LTC1736I ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1736CG
LTC1736IG

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{OSENSE}	Output Voltage Set Accuracy	(Note 3) See Table 1	●			1	%
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 30V (Note 3)			0.001	0.02	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop; V_{ITH} = 0.7V Measured in Servo Loop; V_{ITH} = 2V	 ● ●		 0.1 –0.1	 0.3 –0.3	 % %
g_m	Transconductance Amplifier g_m				1.3		mmho
V_{FCB}	Forced Continuous Threshold		●	0.76	0.8	0.84	V
I_{FCB}	Forced Continuous Current	V_{FCB} = 0.85V			–0.17	–0.3	µA
V_{OVL}	Feedback Overvoltage Lockout		●	0.84	0.86	0.88	V
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 4) $V_{RUN/SS}$ = 0V			 450 15	 25	 µA µA
$V_{RUN/SS}$	Run Pin Start Threshold	$V_{RUN/SS}$, Ramping Positive		1.0	1.5	1.9	V
$V_{RUN/SS}$	Run Pin Begin Latchoff Threshold	$V_{RUN/SS}$, Ramping Positive			4.1	4.5	V
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 0V		–0.7	–1.2		µA
I_{SCL}	RUN/SS Discharge Current	Soft Short Condition, V_{FB} = 0.5V, $V_{RUN/SS}$ = 4.5V		0.5	2	4	µA
UVLO	Undervoltage Lockout	Measured at V_{IN} Pin (V_{IN} Ramping Down)	●		3.5	3.9	V
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 0.7V	●	60	75	85	mV
I_{SENSE}	SENSE Pins Total Source Current	V_{SENSE^-} = V_{SENSE^+} = 0.8V			60	80	µA
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 8)			160	200	ns
 TG t_r TG t_f	TG Transition Time: Rise Time Fall Time	(Note 9) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 50 50	 90 90	 ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	BG Transition Time:	(Note 9)					
BG t_r	Rise Time	C_{LOAD} = 3300pF			50	90	ns
BG t_f	Fall Time	C_{LOAD} = 3300pF			40	80	ns
TG/BG T1D	Top Gate Off to Synchronous Gate-On Delay Time	C_{LOAD} = 3300pF Each Driver			100		ns
TG/BG T2D	Synchronous Gate Off to Top Gate-On Delay Time	C_{LOAD} = 3300pF Each Driver			70		ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V		5.0	5.2	5.4	V
$V_{LDO(INT)}$	Internal V_{CC} Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 4V			0.2	1	%
$V_{LDO(EXT)}$	$EXTV_{CC}$ Drop Voltage	I_{CC} = 20mA, V_{EXTVCC} = 5V			130	200	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
$V_{EXTVCC(HYS)}$	$EXTV_{CC}$ Hysteresis				0.2		V
Oscillator							
f_{OSC}	Oscillator Frequency	(Note 5), C_{OSC} = 43pF		265	300	335	kHz
f_H/f_{OSC}	Maximum Sync Frequency Ratio				1.3		
$f_{FCB(SYNC)}$	FCB Pin Threshold For Sync	Ramping Negative		0.9	1.2		V
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			110	200	mV
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{OSENSE} with Respect to Set Output Voltage					
		V_{OSENSE} Ramping Negative		–6.0	–7.5	–9.5	%
		V_{OSENSE} Ramping Positive		6.0	7.5	9.5	%
VID Control							
$VIDV_{CC}$	VID Operating Supply Voltage			2.7		5.5	V
I_{VIDVCC}	VID Supply Current	(Note 6) $VIDV_{CC}$ = 3.3V			0.01	5	µA
$R_{VFB/VOSENSE}$	Resistance Between V_{OSENSE} and V_{FB}				10		kΩ
R_{RATIO}	Resistor Ratio Accuracy	Programmed from 0.925V to 2.00V			±0.05		%
$R_{PULL-UP}$	VID0 to VID4 Pull-Up Resistance	(Note 7) V_{DIODE} = 0.6V			40		kΩ
V_{IDT}	VID Input Voltage Threshold			0.4	1.0	1.6	V
$I_{VIDLEAK}$	VID Input Leakage Current	(Note 7) $VIDV_{CC}$ < VID < 7V			0.01	±1	µA
$V_{PULL-UP}$	VID Pull-Up Voltage	$VIDV_{CC}$ = 3.3V			2.8		V
		$VIDV_{CC}$ = 5V			4.5		V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1736CG, LTC1736IG: $T_J = T_A + (P_D \bullet 110°C/W)$

Note 3: The LTC1736 is tested in a feedback loop that servos V_{FB} to the balance point for the error amplifier (V_{ITH} = 1.2V).

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: Oscillator frequency is tested by measuring the C_{OSC} charge current (I_{OSC}) and applying the formula:

$$f_{OSC} = \left(\frac{8.477(10^{11})}{C_{OSC}(pF)+11}\right)\left(\frac{1}{I_{CHG}}+\frac{1}{I_{DIS}}\right)^{-1}$$

Note 6: With all five VID inputs floating (or tied to $VIDV_{CC}$) the $VIDV_{CC}$ current is typically <1µA. However, the $VIDV_{CC}$ current will rise and be approximately equal to the number of grounded VID input pins times ($VIDV_{CC}$ – 0.6V)/40k. (See the Applications Information section for more detail.)

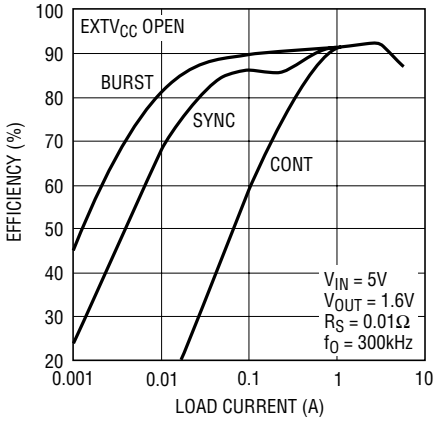
Note 7: Each built-in pull-up resistor attached to the VID inputs also has a series diode to allow input voltages higher than the $VIDV_{CC}$ supply without damage or clamping. (See the Applications Information section for more detail.)

Note 8: The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information section).

Note 9: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

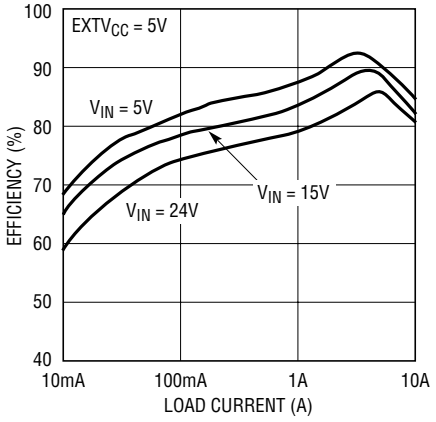
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Load Current (3 Operating Modes)



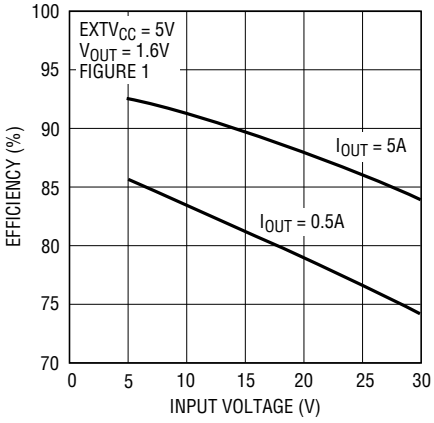
1736 G01

Efficiency vs Load Current



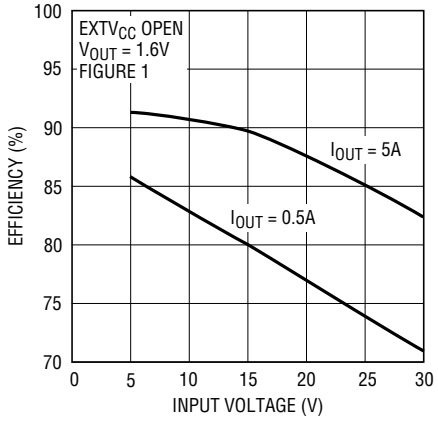
1736 G02

Efficiency vs Input Voltage



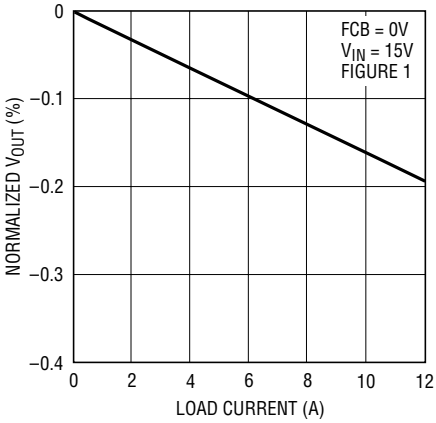
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Efficiency vs Input Voltage



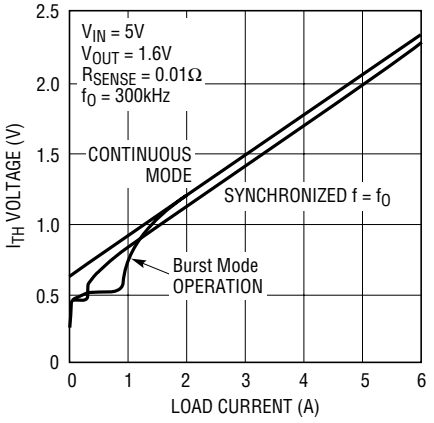
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Load Regulation



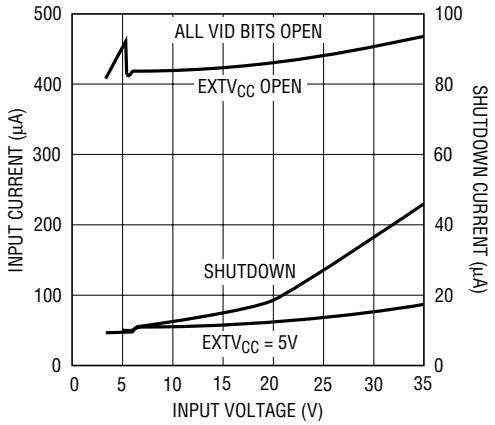
1736 G05

I_{TH} Voltage vs Load Current



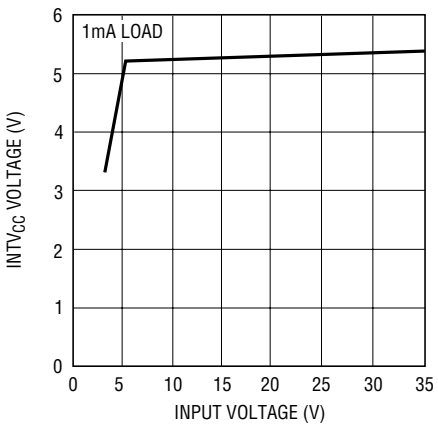
1736 G06

Input and Shutdown Currents vs Input Voltage



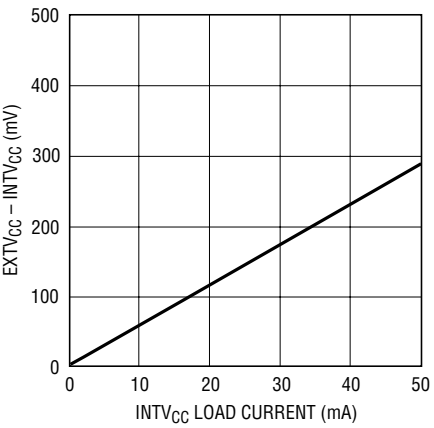
1736 G07

$INTV_{CC}$ Line Regulation



1736 G08

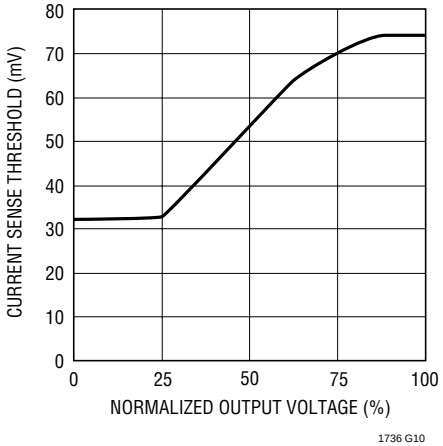
$EXTV_{CC}$ Switch Drop vs $INTV_{CC}$ Load Current



1736 G09

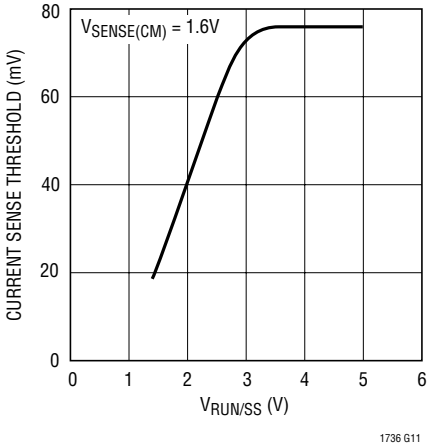
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Threshold vs Normalized Output Voltage (Foldback)



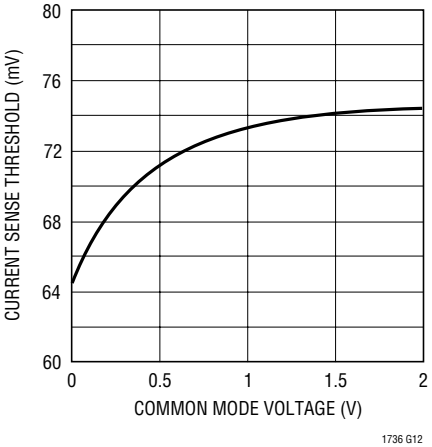
1736 G10

Maximum Current Sense Threshold vs $V_{RUN/SS}$



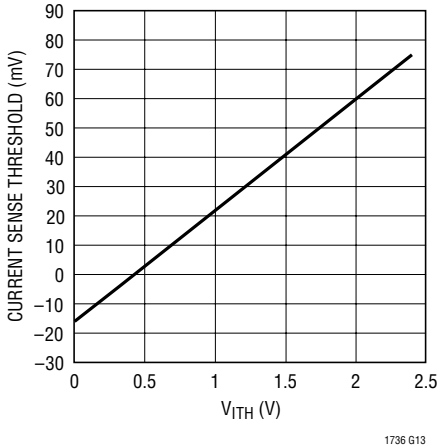
1736 G11

Maximum Current Sense Threshold vs Sense Common Mode Voltage



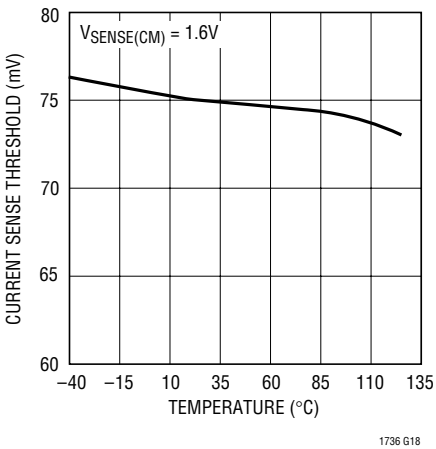
1736 G12

Maximum Current Sense Threshold vs I_{TH} Voltage



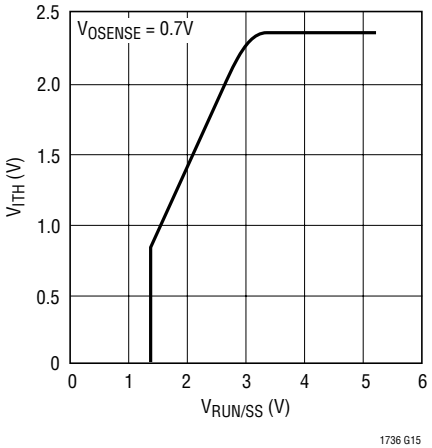
1736 G13

Maximum Current Sense Threshold vs Temperature



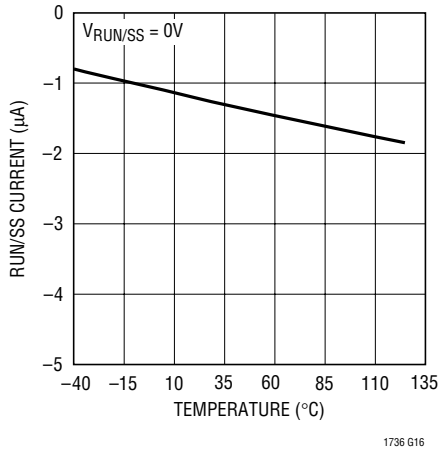
1736 G18

V_{ITH} vs $V_{RUN/SS}$



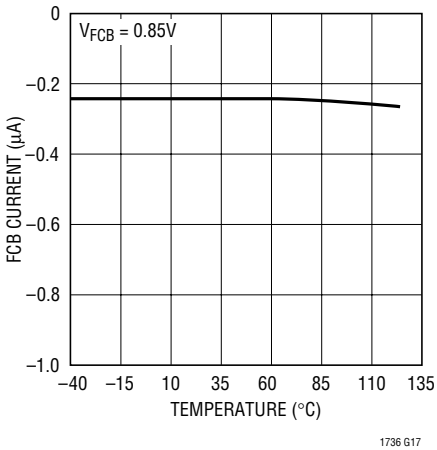
1736 G15

RUN/SS Pin Current vs Temperature



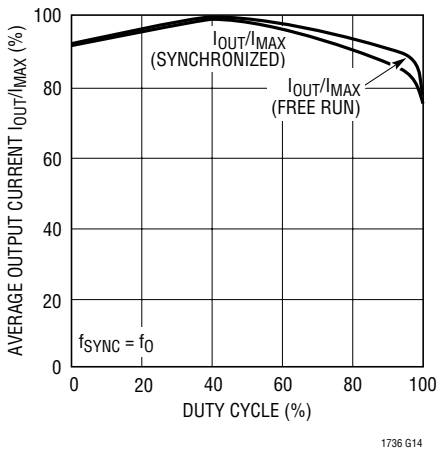
1736 G16

FCB Pin Current vs Temperature



1736 G17

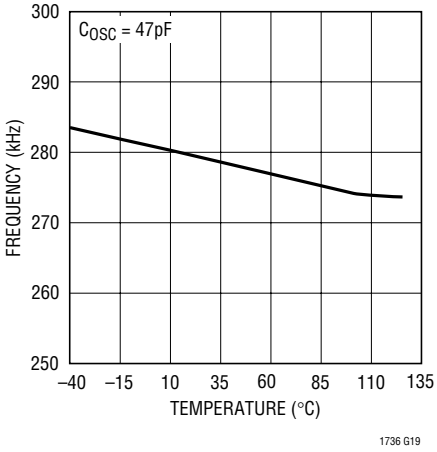
Output Current vs Duty Cycle



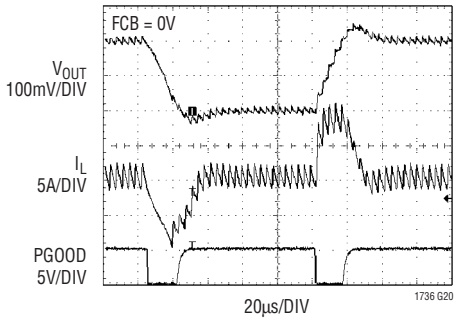
1736 G14

TYPICAL PERFORMANCE CHARACTERISTICS

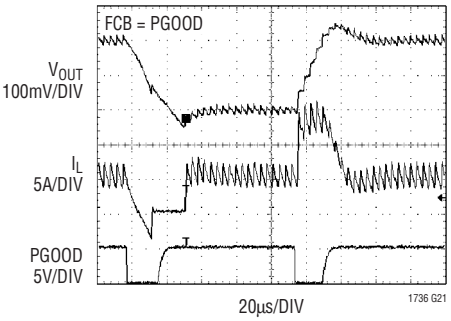
Oscillator Frequency vs Temperature



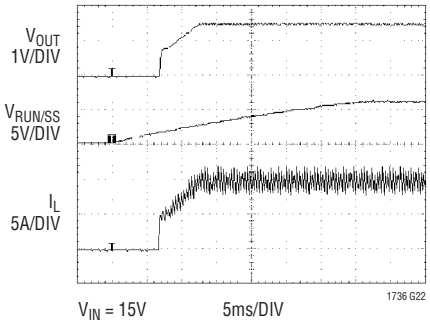
Dynamic VID Change, Burst Mode Operation Defeated



Dynamic VID Change, Burst Mode Operation Enabled

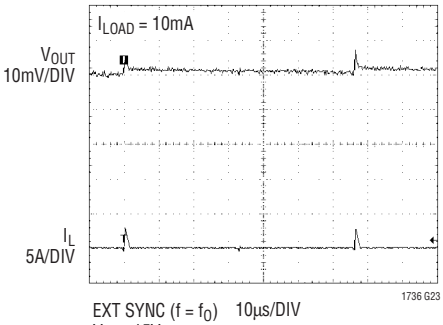


Start-Up



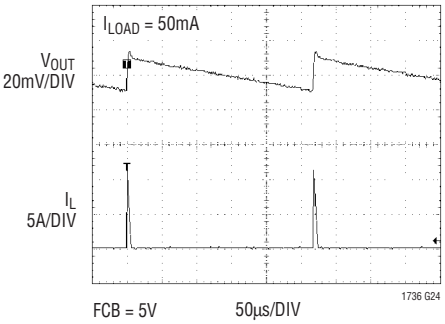
V_{IN} = 15V 5ms/DIV
V_{OUT} = 1.6V
R_{LOAD} = 0.16Ω

$V_{OUT(RIPPLE)}$ (Synchronized)



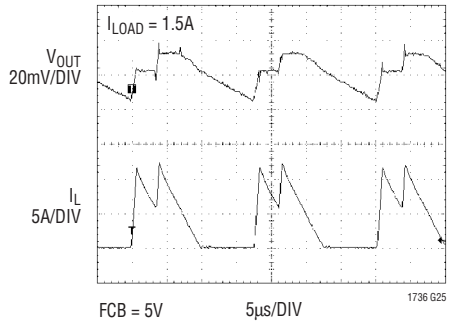
EXT SYNC (f = f_O) 10µs/DIV
V_{IN} = 15V
V_{OUT} = 1.6V

$V_{OUT(RIPPLE)}$ (Burst Mode Operation)



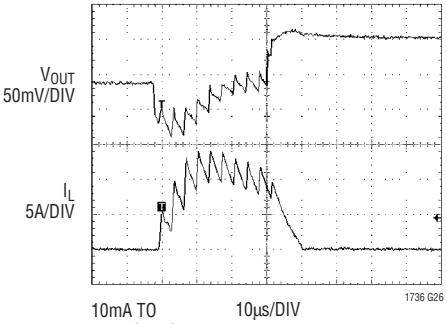
FCB = 5V 50µs/DIV
V_{IN} = 15V
V_{OUT} = 1.6V

$V_{OUT(RIPPLE)}$ (Burst Mode Operation)



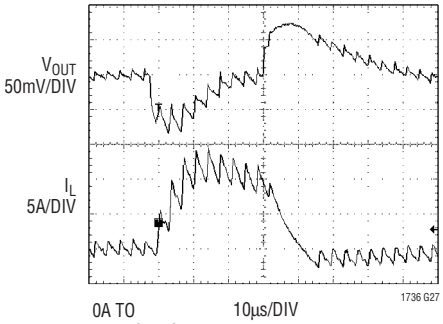
FCB = 5V 5µs/DIV
V_{IN} = 15V
V_{OUT} = 1.6V

Load Step (Burst Mode Operation)



10mA TO 11A LOAD STEP 10µs/DIV
FCB = 5V
V_{IN} = 15V
V_{OUT} = 1.6V

Load Step (Continuous Mode)



0A TO 11A LOAD STEP 10µs/DIV
FCB = 0V
V_{IN} = 15V
V_{OUT} = 1.6V

PIN FUNCTIONS

C_{OSC} (Pin 1): External capacitor C_{OSC} from this pin to ground sets the operating frequency.

RUN/SS (Pin 2): Combination of Soft-Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full output current. The time is approximately 1.25s/μF. Forcing this pin below 1.5V causes the device to be shut down. In shutdown all functions are disabled. Latchoff overcurrent protection is also invoked via this pin as described in the Applications Information section.

I_{TH} (Pin 3): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 2.4V.

FCB (Pin 4): Forced Continuous/Synchronization Input. Tie this pin to ground for continuous synchronous operation, to a resistive divider from the secondary output when using a secondary winding, or to $INTV_{CC}$ to enable Burst Mode operation at low load currents. Clocking this pin with a signal above $1.5V_{P-P}$ disables Burst Mode operation but allows cycle skipping at low load currents and synchronizes the internal oscillator with the external clock.

SGND (Pin 5): Small-Signal Ground. All small-signal components such as C_{OSC}, C_{SS} plus the loop compensation resistors and capacitor(s) should single-point tie to this pin. This pin should, in turn, connect to PGND.

PGOOD (Pin 6): Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the V_{OSENSE} pin is not within ±7.5% of its set point.

$SENSE^-$ (Pin 7): The (–) Input to the Current Comparator.

$SENSE^+$ (Pin 8): The (+) Input to the Current Comparator. Built-in offsets between $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

V_{FB} (Pin 9): Divided Down V_{OSENSE} Voltage Feeding the Error Amplifier of the Regulator. The VID inputs program a resistive divider between V_{OSENSE} and SGND; the tap point on the divider is V_{FB}. The voltage on V_{FB} is 0.8V when the output is in regulation. This pin can be bypassed to SGND with 50pF to 100pF.

V_{OSENSE} (Pin 10): Receives the remotely sensed feedback voltage from the output.

VID0 to VID4 (Pins 11 to 15): Digital Inputs for controlling the output voltage from 0.925V to 2.0V. Table 1 specifies the V_{OSENSE} voltages for the 32 combinations of digital inputs. The LSB (VID0) represents 50mV increments in the upper voltage range (2.00V to 1.30V) and 25mV increments in the lower voltage range (1.275V to 0.925V). Logic Low = GND, Logic High = $VIDV_{CC}$ or Float.

$VIDV_{CC}$ (Pin 16): VID Input Supply Voltage. Can range from 2.7V to 7V. Typically this pin is tied to $INTV_{CC}$.

$EXTV_{CC}$ (Pin 17): Input to the Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies V_{CC} power whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ connection in the Applications Information section. Do not exceed 7V to this pin and ensure $EXTV_{CC} \leq V_{IN}$.

PGND (Pin 18): Driver Power Ground. This pin connects to the source of the bottom N-channel MOSFET, the anode of the Schottky diode and the (–) terminal of C_{IN}.

BG (Pin 19): High Current Gate Drive for Bottom N-Channel MOSFET. Voltage swing at this pin is from ground to $INTV_{CC}$.

$INTV_{CC}$ (Pin 20): Output of the Internal 5.2V Regulator and $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage. Decouple to power ground with a 1μF ceramic capacitor placed directly adjacent to the IC together with a minimum of 4.7μF tantalum or other low ESR capacitor.

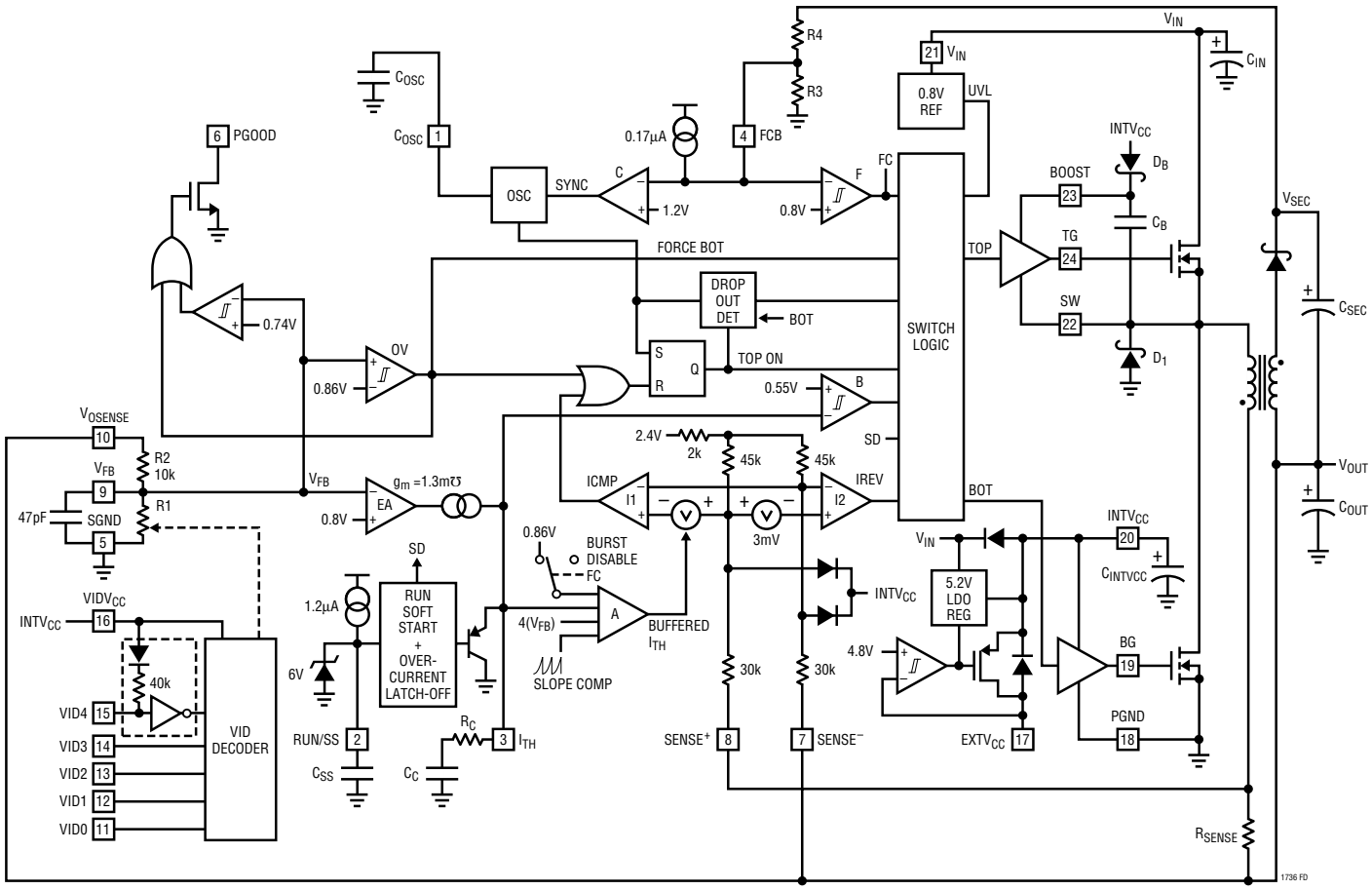
V_{IN} (Pin 21): Main Supply Pin. This pin must be closely decoupled to power ground.

SW (Pin 22): Switch Node Connection to Inductor and Bootstrap Capacitor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST (Pin 23): Supply to Topside Floating Driver. The bootstrap capacitor is returned to this pin. Voltage swing at this pin is from a diode drop below $INTV_{CC}$ to V_{IN} + $INTV_{CC}$.

TG (Pin 24): High Current Gate Drive for Top N-Channel MOSFET. This is the output of a floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1736 uses a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator I1 resets the RS latch. The peak inductor current at which I1 resets the RS latch is controlled by the voltage on Pin I_{TH}, which is the output of the error amplifier EA. Pin V_{OSENSE}, described in the Pin Functions, allows EA to receive an output feedback voltage V_{FB} from the internal resistive divider. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I2, or the beginning of the next cycle.

The top MOSFET driver is powered from a floating bootstrap capacitor C_B. This capacitor is normally recharged from $INTV_{CC}$ through an external Schottky diode when the top MOSFET is turned off. As V_{IN} decreases towards V_{OUT}, the converter will attempt to turn on the top MOSFET continuously (''dropout''). A dropout counter detects this condition and forces the top MOSFET to turn off for about 500ns every tenth cycle to recharge the bootstrap capacitor.

OPERATION (Refer to Functional Diagram)

The main control loop is shut down by pulling Pin 2 (RUN/SS) low. Releasing RUN/SS allows an internal 1.2µA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1.5V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume. If V_{OUT} has not reached 70% of its final value when C_{SS} has charged to 4.1V, latchoff can be invoked as described in the Applications Information section.

The internal oscillator can be synchronized to an external clock applied to the FCB pin and can lock to a frequency between 90% and 130% of its nominal rate set by capacitor C_{OSC}.

An overvoltage comparator OV guards against transient overshoots (>7.5%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Foldback current limiting for an output shorted to ground is provided by amplifier A. As V_{FB} drops below 0.6V, the buffered I_{TH} input to the current comparator is gradually pulled down to a 0.86V clamp. This reduces peak inductor current to about 1/4 of its maximum value.

Low Current Operation

The LTC1736 has three low current modes controlled by the FCB pin. Burst Mode operation is selected when the FCB pin is above 0.8V (typically tied to $INTV_{CC}$). During Burst Mode operation, if the error amplifier drives the I_{TH} voltage below 0.86V, the buffered I_{TH} input to the current comparator will be clamped at 0.86V. The inductor current peak is then held at approximately $20mV/R_{SENSE}$ (about 1/4 of maximum output current). If I_{TH} then drops below 0.5V, the Burst Mode comparator B will turn off both MOSFETs to maximize efficiency. The load current will be supplied solely by the output capacitor until I_{TH} rises above the 60mV hysteresis of the comparator and switching is resumed. Burst Mode operation is disabled by comparator F when the FCB pin is brought below 0.8V. This forces continuous operation and can assist secondary winding regulation.

When the FCB pin is driven by an external oscillator, a low noise cycle-skipping mode is invoked and the internal oscillator is synchronized to the external clock by comparator C. In this mode the 25% minimum inductor current clamp is removed, providing constant frequency discontinuous operation over the widest possible output current range. This constant frequency operation is not quite as efficient as Burst Mode operation, but provides a lower noise, constant frequency spectrum.

The FCB pin is tied to ground when forced continuous operation is desired. This operation is the least efficient mode, but is desirable in certain applications. The output can source or sink current in this mode. When sinking current while in forced continuous operation, current will be forced back into the main power supply potentially boosting the input supply to dangerous voltage levels—BEWARE.

Foldback Current, Short-Circuit Detection and Short-Circuit Latchoff

The RUN/SS capacitor, C_{SS}, is used initially to limit the inrush current of the switching regulator. After the controller has been started and been given adequate time to charge up the output capacitors and provide full load current, C_{SS} is used as a short-circuit time-out circuit. If the output voltage falls to less than 70% of its nominal output voltage, C_{SS} begins discharging on the assumption that the output is in an overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overridden by providing a current >5µA at a compliance of 5V to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of C_{SS} during an overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled.

OPERATION (Refer to Functional Diagram)

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the internal circuitry of the LTC1736 is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open, an internal 5.2V low dropout regulator supplies the $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is raised above 4.7V, the internal regulator is turned off and an internal switch connects $EXTV_{CC}$ to $INTV_{CC}$. This allows a high efficiency source, such as the notebook main 5V system supply or a secondary output of the converter itself, to provide the $INTV_{CC}$ power. Voltages up to 7V can be applied to $EXTV_{CC}$ for additional gate drive capability.

To provide clean start-up and to protect the MOSFETs, undervoltage lockout is used to keep both MOSFETs off until the input voltage is above 3.5V.

VID Control

Bits VID0 to VID4 are logic inputs setting the output voltage using an internal 5-bit DAC as a feedback resistive voltage divider. The output voltage can be set in 50mV or 25mV increments from 0.925V to 2.0V according to Table 1. Pins VID0 to VID4 are internally pulled up to $VIDV_{CC}$.

PGOOD

A window comparator monitors the output voltage and its open-drain output is pulled low when the divided down output voltage is not within ±7.5% of the reference voltage of 0.8V.

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The basic LTC1736 application circuit is shown in Figure 1 on the first page of this data sheet. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_{OSC} and L can be chosen. Next, the power MOSFETs and D1 are selected. The operating frequency and the inductor are chosen based largely on the desired amount of ripple current. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specifications. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection For Output Current

R_{SENSE} is chosen based on the required output current. The LTC1736 current comparator has a maximum threshold of 75mV/R_{SENSE} and an input common mode range of SGND to 1.1($INTV_{CC}$). The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the LTC1736 and external component values yields:

$$R_{SENSE} = \frac{50mV}{I_{MAX}}$$

C_{OSC} Selection for Operating Frequency and Synchronization

The choice of operating frequency and inductor value is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The LTC1736 uses a constant-frequency architecture with the frequency determined by an external oscillator capacitor C_{OSC}. Each time the topside MOSFET turns on, the voltage on C_{OSC} is reset to ground. During the on-time C_{OSC} is charged by a fixed current. When the voltage on the capacitor reaches 1.19V, C_{OSC} is reset to ground. The process then repeats.

The value of C_{OSC} is calculated from the desired operating frequency assuming no external clock input on the FCB pin:

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$$C_{OSC}(pF) = \left[\frac{1.61(10^7)}{Frequency}\right] - 11$$

A graph for selecting C_{OSC} versus frequency is given in Figure 2. The maximum recommended switching frequency is 550kHz .

The internal oscillator runs at its nominal frequency (f_O) when the FCB pin is pulled high to $INTV_{CC}$ or connected to ground. Clocking the FCB pin above and below 0.8V will cause the internal oscillator to lock to an external clock signal with a frequency between $0.9f_O$ and $1.3f_O$. The clock high level must exceed 1.3V for at least 0.3µs, and the clock low level must be less than 0.3V for at least 0.3µs. The top MOSFET turn-on will synchronize with the rising edge of the external clock.

Attempting to synchronize to too high an external frequency (above $1.3f_O$) can result in inadequate slope compensation and possible loop instability at high duty cycles. If this condition exists simply lower the value of C_{OSC} so $f_{EXT} = f_O$ according to Figure 2.

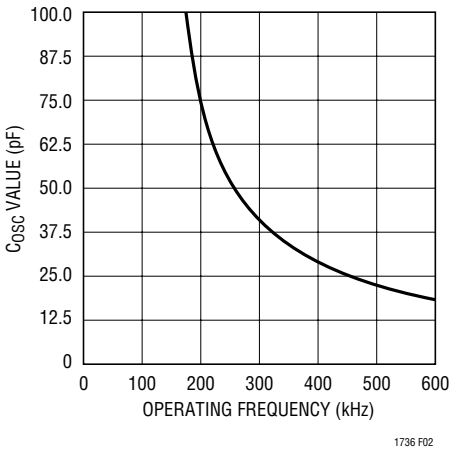


Figure 2. Timing Capacitor Value

When synchronized to an external clock, Burst Mode operation is disabled but the inductor current is not allowed to reverse. The 25% minimum inductor current clamp present in Burst Mode operation is removed, providing constant frequency discontinuous operation over the widest possible output current range. In this mode the synchronous MOSFET is forced on once every 10 clock cycles to recharge the bootstrap capacitor. This minimizes audible noise while maintaining reasonably high efficiency.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate-charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3$ to $0.4(I_{MAX})$. Remember, the maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite,

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molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available that do not increase the height significantly.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1736: An N-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.2V during start-up. (See $EXTV_{CC}$ Pin Connection.) Consequently, logic-level threshold MOSFETs must be used in most LTC1736 applications. The only exception is when low input voltage is expected (V_{IN} < 5V); then, sublogic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the LTC1736 is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2\left(1+\delta\right)R_{DS(ON)} + k\left(V_{IN}\right)^2\left(I_{MAX}\right)\left(C_{RSS}\right)\left(f\right)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2\left(1+\delta\right)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the topside N-Channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 1.7 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diode D1 shown in Figure 1 conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 3A Schottky is generally a good size for 10A to 12A regulators due to the relatively small average current.

Kool Mμ is a registered trademark of Magnetics, Inc.

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Larger diodes can result in additional transition losses due to their larger junction capacitance. The diode may be omitted if the efficiency loss can be tolerated.

C_{IN} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

C_{OUT} Selection

The selection of C_{OUT} is primarily determined by the effective series resistance (ESR) to minimize voltage ripple. The output ripple (ΔV_{OUT}) in continuous mode is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Where f = operating frequency, C_{OUT} = output capacitance, and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. With $\Delta I_L = 0.3 I_{OUT(MAX)}$ the output ripple will be less than 50mV at max V_{IN} assuming:

C_{OUT} required ESR < 2.2 R_{SENSE}

$C_{OUT} > 1/(8fR_{SENSE})$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

The selection of output capacitors for CPU or other applications with large load current transients is primarily determined by the voltage tolerance specifications of the load. The resistive component of the capacitor, ESR, multiplied by the load current change plus any output voltage ripple must be within the voltage tolerance of the load (CPU).

The required ESR due to a load current step is:

$R_{ESR} < \Delta V/\Delta I$

where ΔI is the change in current from full load to zero load (or minimum load) and ΔV is the allowed voltage deviation (not including any droop due to finite capacitance).

The amount of capacitance needed is determined by the maximum energy stored in the inductor. The capacitance must be sufficient to absorb the change in inductor current when a high current to low current transition occurs. The opposite load current transition is generally determined by the control loop OPTI-LOOP components, so make sure not to over compensate and slow down the response. The minimum capacitance to assure the inductors' energy is adequately absorbed is:

$$C_{OUT} > \frac{L(\Delta I)^2}{2(\Delta V)V_{OUT}}$$

where ΔI is the change in load current.

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Manufacturers such as Nichicon, United Chemicon and Sanyo can be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the inductance effects.

In surface mount applications multiple capacitors may need to be used in parallel to meet the ESR, RMS current handling, and load step requirements of the application. Aluminum electrolytic, dry tantalum and special polymer capacitors are available in surface mount packages. Special polymer surface mount capacitors offer very low ESR but have much lower capacitive density per unit volume than other capacitor types. These capacitors offer a very cost-effective output capacitor solution and are an ideal choice when combined with a controller having high loop bandwidth. Tantalum capacitors offer the highest capacitance density and are often used as output capacitors for switching regulators having controlled soft-start. Several excellent surge-tested choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors can be used in cost-driven applications providing that consideration is given to ripple current ratings, temperature and long-term reliability. A typical application will require several to many aluminum electrolytic capacitors in parallel. A combination of the above mentioned capacitors will often result in maximizing performance and minimizing overall cost. Other capacitor types include Nichicon PL series, NEC Neocap, Panasonic SP and Sprague 595D series. Consult manufacturers for other specific recommendations.

Like all components, capacitors are not ideal. Each capacitor has its own benefits and limitations. Combinations of different capacitor types have proven to be a very cost effective solution. Remember also to include high frequency decoupling capacitors. They should be placed as close as possible to the power pins of the load. Any inductance present in the circuit board traces negates their usefulness.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5.2V supply that powers the drivers and internal circuitry within the LTC1736. The $INTV_{CC}$ pin can supply a maximum RMS current of 50mA and must be bypassed to ground with a minimum of 4.7µF tantalum, 10µF special polymer or low ESR type electrolytic capacitor. Good bypassing is required to supply the high transient currents required by the MOSFET gate drivers.

Higher input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC1736 to be exceeded. The system supply current is normally dominated by the gate charge current. Additional loading of $INTV_{CC}$ also needs to be taken into account for the power dissipation calculations. The total $INTV_{CC}$ current can be supplied by either the 5.2V internal linear regulator or by the $EXTV_{CC}$ input pin. When the voltage applied to the $EXTV_{CC}$ pin is less than 4.7V, all of the $INTV_{CC}$ current is supplied by the internal 5.2V linear regulator. Power dissipation for the IC in this case is highest: $(V_{IN})(I_{INTVCC})$, and overall efficiency is lowered. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC1736G is limited to less than 17mA from a 30V supply when not using the $EXTV_{CC}$ pin as follows:

$T_J = 70°C + (17mA)(30V)(110°C/W) = 126°C$

Use of the $EXTV_{CC}$ input pin reduces the junction temperature to:

$T_J = 70°C + (17mA)(5V)(110°C/W) = 79°C$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V_{IN}.

$EXTV_{CC}$ Connection

The LTC1736 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Whenever the $EXTV_{CC}$ pin is above 4.7V the internal 5.2V

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regulator shuts off, the switch closes and $INTV_{CC}$ power is supplied via $EXTV_{CC}$ until $EXTV_{CC}$ drops below 4.5V. This allows the MOSFET gate drive and control power to be derived from the output or other external source during normal operation. When the output is out of regulation (start-up, short circuit) power is supplied from the internal regulator. Do not apply greater than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V regulators this simply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for VID programmed regulators and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Left Open (or Grounded). This will cause $INTV_{CC}$ to be powered from the internal 5.2V regulator resulting in a low current efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ Connected to an External Supply (this option is the most likely used). If an external supply is available in the 5V to 7V range, such as notebook main 5V system power, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. This is the typical case as the 5V power is almost always present and is derived by another high efficiency regulator.
3. $EXTV_{CC}$ Connected to an Output-Derived Boost Network. For this low output voltage regulator, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V. This can be done with either the inductive boost winding or the capacitive charge pump circuits. Refer to the LTC1735 data sheet for details. The charge pump has the advantage of simple magnetics.

Output Voltage Programming

The output voltage is digitally set to levels between 0.925V and 2.00V using the voltage identification (VID) inputs VID0 to VID4. The internal 5-bit DAC configured as a precision resistive voltage divider sets the output voltage in 50mV or 25mV increments according to Table 1.

The VID codes (00000-11110) are engineered to be compatible with Intel Mobile Pentium II and Pentium III processor specifications for output voltages from 0.925V to 2.00V.

The LSB (VID0) represents 50mV increments in the upper voltage range (1.30V to 2.00V) and 25mV increments in the lower voltage range (0.925V to 1.275V). The MSB is VID4. When all bits are low, or grounded, the output voltage is 2.00V.

Between the V_{FB} pin and ground is a variable resistor, R1, whose value is controlled by the five input pins (VID0 to VID4). Another resistor, R2, between the V_{OSENSE} and the V_{FB} pins completes the resistive divider. The output voltage is thus set by the ratio of (R1 + R2) to R1.

The LTC1736 has remote sense capability. The top of the internal resistive divider is connected to V_{OSENSE}, and it is referenced to the SGND pin. This allows a kelvin connection for remotely sensing the output voltage directly across the load, eliminating any PC board trace resistance errors.

Each VID digital input is pulled up by a 40k resistor in series with a diode from $VIDV_{CC}$. Therefore, it must be grounded to get a digital low input, and can be either floated or connected to $VIDV_{CC}$ to get a digital high input. The series diode is used to prevent the digital inputs from being damaged or clamped if they are driven higher than $VIDV_{CC}$. The digital inputs accept CMOS voltage levels.

$VIDV_{CC}$ is the supply voltage for the VID section. It is normally connected to $INTV_{CC}$ but can be driven from other sources such as a 3.3V supply. If it is driven from another source, that source MUST be in the range of 2.7V to 5.5V and MUST be alive prior to enabling the LTC1736.

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Table 1. VID Output Voltage Programming

VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	0	0	0	0	2.000V
0	0	0	0	1	1.950V
0	0	0	1	0	1.900V
0	0	0	1	1	1.850V
0	0	1	0	0	1.800V
0	0	1	0	1	1.750V
0	0	1	1	0	1.700V
0	0	1	1	1	1.650V
0	1	0	0	0	1.600V
0	1	0	0	1	1.550V
0	1	0	1	0	1.500V
0	1	0	1	1	1.450V
0	1	1	0	0	1.400V
0	1	1	0	1	1.350V
0	1	1	1	0	1.300V
0	1	1	1	1	*
1	0	0	0	0	1.275V
1	0	0	0	1	1.250V
1	0	0	1	0	1.225V
1	0	0	1	1	1.200V
1	0	1	0	0	1.175V
1	0	1	0	1	1.150V
1	0	1	1	0	1.125V
1	0	1	1	1	1.100V
1	1	0	0	0	1.075V
1	1	0	0	1	1.050V
1	1	0	1	0	1.025V
1	1	0	1	1	1.000V
1	1	1	0	0	0.975V
1	1	1	0	1	0.950V
1	1	1	1	0	0.925V
1	1	1	1	1	**

Note: *, ** represents codes without a defined output voltage as specified in Intel specifications. The LTC1736 interprets these codes as valid inputs and produces output voltages as follows: [01111] = 1.250V, [11111] = 0.900V.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. Note that the voltage across C_B is about a diode drop below $INTV_{CC}$. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage SW rises to V_{IN} and the BOOST pin rises to V_{IN} + $INTV_{CC}$. The value of the boost capacitor C_B needs to be 100 times greater than the total input capacitance of the topside MOSFET. In most applications 0.1µF to 0.33µF is adequate. The reverse breakdown on D_B must be greater than $V_{IN(MAX)}$.

When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If you make a change and the input current decreases, then you improve the efficiency. If there is no change in input current, then there is no change in efficiency.

SENSE$^+$/SENSE$^-$ Pins

The common mode input range of the current comparator is from 0V to 1.1($INTV_{CC}$). Continuous linear operation is guaranteed throughout this range allowing output voltages anywhere from 0.8V to 7V (although the VID control pins only program a 0.925V to 2.00V output range). A differential NPN input stage is used and is biased with internal resistors from an internal 2.4V source as shown in the Functional Diagram. This causes current to flow out of both sense pins to the main output. This forces a minimum load current which is sunk by the internal resistive divider resistors R1 and R2. The maximum current flowing out of the sense pins is:

$$I_{SENSE^+} + I_{SENSE^-} = (2.4V - V_{OUT})/24k$$

Remember to take this current into account if resistance is placed in series with the sense pins for filtering.

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Soft-Start/Run Function

The RUN/SS pin is a multipurpose pin that provides a soft-start function and a means to shut down the LTC1736. Soft-start reduces surge currents from V_{IN} by gradually increasing the controller's current limit $I_{TH(MAX)}$. This pin can also be used for power supply sequencing.

Pulling the RUN/SS pin below 1.5V puts the LTC1736 into a low quiescent current shutdown ($I_Q < 25\mu A$). This pin can be driven directly from logic as shown in Figure 3. Releasing the RUN/SS pin allows an internal 1.2μA current source to charge up the external soft-start capacitor C_{SS}. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = \left(1.25s/\mu F\right) C_{SS}$$

When the voltage on RUN/SS reaches 1.5V the LTC1736 begins operating with a current limit at approximately $25mV/R_{SENSE}$. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from $25mV/R_{SENSE}$ to $75mV/R_{SENSE}$. The output current limit ramps up slowly, taking an additional 1.25s/μF to reach full current. The output current thus ramps up slowly reducing the starting surge current required from the input power supply.

Diode D1 in Figure 3 reduces the start delay while allowing C_{SS} to charge up slowly for the soft-start function. This diode and C_{SS} can be deleted if soft-start is not needed. The RUN/SS pin has an internal 6V zener clamp (See Functional Diagram).

Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to shut off the controller and latchoff when an overcurrent condition is detected. The RUN/SS capacitor C_{SS} is used initially to turn on and limit the inrush current of the controller. After the controller has been started and given adequate time to charge up the output capacitor and provide full load current, C_{SS} is used as a short-circuit timer. If the output voltage falls to less than 70% of its nominal output voltage *after C_{SS} reaches 4.1V*, the assumption is made that the output is in a severe overcurrent and/or short-circuit condition and C_{SS} begins discharging. If the condition lasts for a long enough period as determined by the size of C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled.

This built-in latchoff can be overridden by providing a current > 5μA at a compliance of 5V to the RUN/SS pin as shown in Figure 4. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. When deriving the 5μA current from V_{IN} as in Figure 4a, current latchoff is always defeated. A diode connecting this pull-up resistor to $INTV_{CC}$, as in Figure 4b, eliminates any extra supply current during controller shutdown while eliminating the $INTV_{CC}$ loading from preventing controller start-up. If the voltage on C_{SS} does not exceed 4.1V, the overcurrent latch is not armed and the function is disabled.

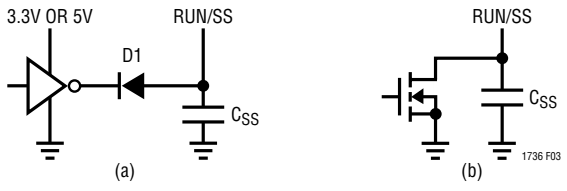


Figure 3. RUN/SS Pin Interfacing

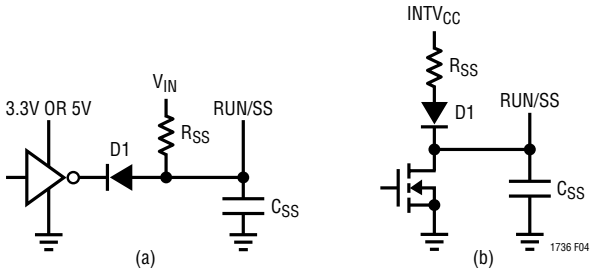


Figure 4. RUN/SS Pin Interfacing with Latchoff Defeated

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Why should you defeat overcurrent latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off. Defeating this feature will easily allow trouble-shooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. After the design is complete, a decision can be made whether to enable the latchoff feature.

The value of the soft-start capacitor C_{SS} will need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

The minimum recommended soft-start capacitor of C_{SS} = 0.1µF will be sufficient for most applications.

Fault Conditions: Current Limit and Current Foldback

The LTC1736 current comparator has a maximum sense voltage of 75mV resulting in a maximum MOSFET current of $75mV/R_{SENSE}$.

The LTC1736 includes current foldback to help further limit load current when the output is shorted to ground. The foldback circuit is active even when the overload shutdown latch described above is defeated. If the output falls by more than half, then the maximum sense voltage is progressively lowered from 75mV to 30mV. Under short-circuit conditions with very low duty cycle, the LTC1736 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be conducting the peak current. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC1736 (less than 200ns), the input voltage, and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)}\ V_{IN}/L.$$

The resulting short circuit current is:

$$I_{SC} = \frac{30mV}{R_{SENSE}} + \frac{1}{2}\Delta I_{L(SC)}$$

The current foldback function is always active and is not effected by the current latchoff function.

Fault Conditions: Output Overvoltage Protection (Crowbar)

The output overvoltage crowbar is designed to blow a system fuse in the input lead when the output of the regulator rises much higher than nominal levels. This condition causes huge currents to flow, much greater than in normal operation. This feature is designed to protect against a shorted top MOSFET; it does not protect against a failure of the controller itself.

The comparator (OV in the Functional Diagram) detects overvoltage faults greater than 7.5% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is forced on. The bottom MOSFET remains on continuously for as long as the OV condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes. Note that VID controlled output voltage decreases may cause the overvoltage protection to be momentarily activated. This will not cause permanent latchoff nor will it disrupt the desired voltage change.

With soft-latch overvoltage protection, dynamic VID code changes are allowed and the overvoltage protection tracks the new VID code, always protecting the load (CPU). If dynamic VID code changes are anticipated and the minimum load current is light, it may be necessary to either force continuous operation by pulling FCB low during the transition to maximize current sinking capability or connect PGOOD to FCB to automatically force continuous operation during VID transitions.

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Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest amount of time that the LTC1736 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC1736 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and voltage will increase.

The minimum on-time for the LTC1736 in a properly configured application is generally less than 200ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases as shown in Figure 5. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that is low enough in value to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule keep the inductor ripple current equal or greater than 30% of $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.*

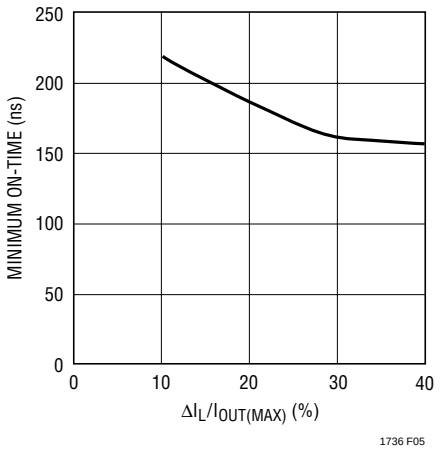


Figure 5. Minimum On-Time vs ΔI_L

FCB Pin Operation

When the DC voltage on the FCB pin drops below its 0.8V threshold, continuous mode operation is forced. In this case, the top and bottom MOSFETs continue to be driven synchronously regardless of the load on the main output. Burst Mode operation is disabled and current reversal is allowed in the inductor.

In addition to providing a logic input to force continuous synchronous operation and external synchronization, the FCB pin provides a means to regulate a flyback winding output. During continuous mode, current flows continuously in the transformer primary. The secondary winding(s) draw current only when the bottom synchronous switch is on. When primary load currents are low and/or the V_{IN}/V_{OUT} ratio is low, the synchronous switch may not be on for a sufficient amount of time to transfer power from the output capacitor to the secondary load. Forced continuous operation will support secondary windings provided there is sufficient synchronous switch duty factor. Thus, the FCB input pin removes the requirement that power must be drawn from the inductor primary in order to extract power from the auxiliary windings. With the loop in continuous mode, the auxiliary output may nominally be loaded without regard to the primary output load.

The secondary output voltage V_{SEC} is normally set as shown in the Functional Diagram by the turns ratio N of the transformer:

$$V_{SEC} \cong (N + 1)\ V_{OUT}$$

However, if the controller goes into Burst Mode operation and halts switching due to a light primary load current, then V_{SEC} will droop. An external resistive divider from V_{SEC} to the FCB pin sets a minimum voltage $V_{SEC(MIN)}$:

$$V_{SEC(MIN)} \approx 0.8V\left(1+\frac{R4}{R3}\right)$$

If V_{SEC} drops below this level, the FCB voltage forces continuous switching operation until V_{SEC} is again above its minimum.

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In order to prevent erratic operation if no external connections are made to the FCB pin, the FCB pin has a 0.17μA internal current source pulling the pin high. Remember to include this current when choosing resistor values R3 and R4.

The internal LTC1736 oscillator can be synchronized to an external oscillator by clocking the FCB pin with a signal above $1.5V_{P-P}$. When synchronized to an external frequency, Burst Mode operation is disabled, but cycle skipping is allowed at low load currents since current reversal is inhibited. The bottom gate will come on every 10 clock cycles to assure the boostrap cap, C_B, is kept refreshed. The rising edge of an external clock applied to the FCB pin starts a new cycle.

The range of synchronization is from $0.9f_O$ to $1.3f_O$, with f_O set by C_{OSC}. Attempting to synchronize to a higher frequency than $1.3f_O$ can result in inadequate slope comensation and cause loop instability with high duty cycles. If loop instability is observed while synchronized, additional slope compensation can be obtained by simply decreasing C_{OSC}.

The following table summarizes the possible states available on the FCB pin:

Table 2

FCB Pin	Condition
DC Voltage: 0V to 0.7V	Burst Disabled/Forced Continuous Current Reversal Enabled
DC Voltage: ≥0.9V	Burst Mode Operation, No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
Ext Clock: (0V to $V_{FCBSYNC}$) ($V_{FCBSYNC} \geq 1.5V$)	Burst Mode Operation Disabled No Current Reversal

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% - (L1 + L2 + L3 + ...)

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1736 circuits: 1) LTC1736 V_{IN} current, 2) $INTV_{CC}$ current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom-side MOSFETs.

   Supplying $INTV_{CC}$ power through the $EXTV_{CC}$ switch input from an output-derived or other high efficiency source will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 15V to 1.8V application, 10mA of $INTV_{CC}$ current results in approximately 1.2mA of V_{IN} current. This reduces the low current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R Losses are predicted from the DC resistances of the MOSFETs, inductor and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside main MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.02\Omega$, $R_L = 0.03\Omega$, and $R_{SENSE} = 0.01\Omega$, then the total resistance is

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0.06Ω. This results in losses ranging from 3% to 17% as the output current increases from 1A to 5A for a 1.8V output, or 4% to 20% for a 1.5V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and power level. I^2R losses cause the efficiency to drop at high output currents.

4. Transition losses apply only to the topside MOSFET(s), and only become significant when operating at high input voltages (typically 12V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)(V_{IN}^2)(I_{O(MAX)})(C_{RSS})(f)$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 0.01Ω to 0.02Ω of ESR. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second-order overshoot/DC ratio cannot be used determine phase margin. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

Improve Transient Response and Reduce Output Capacitance with Active Voltage Positioning

Fast load transient response, limited board space and low cost are requirements of microprocessor power supplies. Active voltage positioning improves transient response and reduces the output capacitance required to power a microprocessor where a typical load step can be from 0.2A

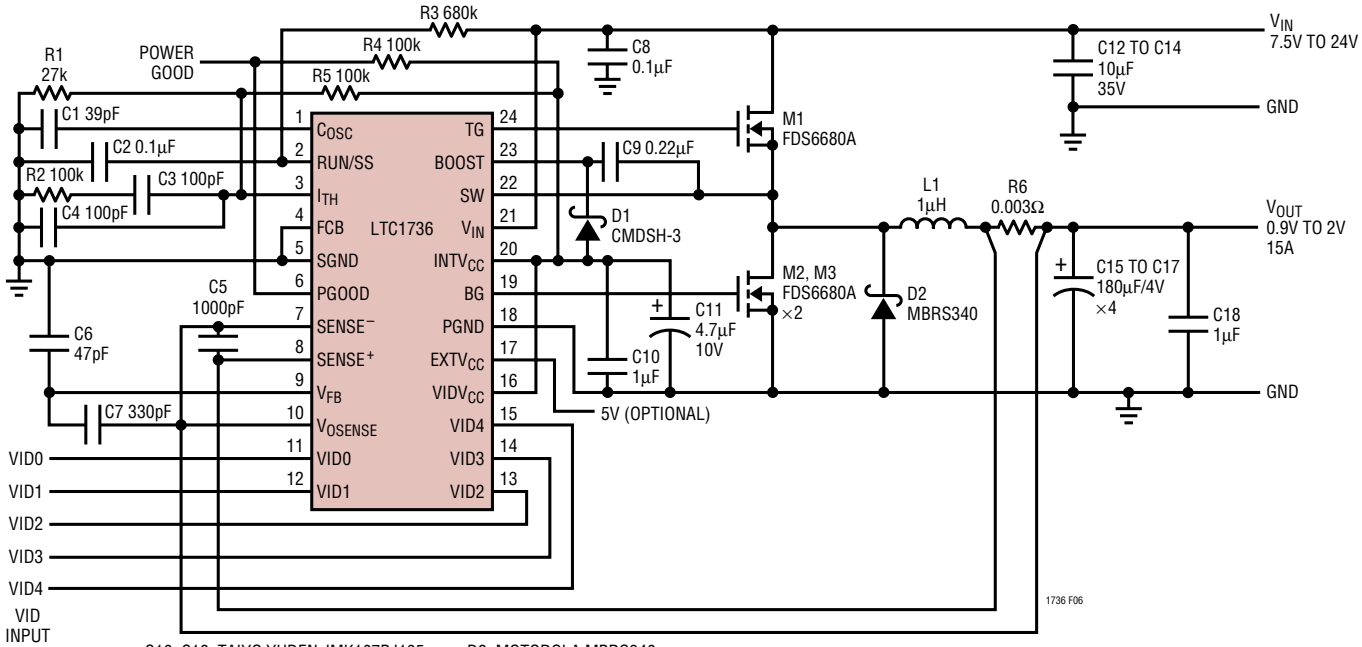
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to 15A in 100ns or 15A to 0.2A in 100ns. The voltage at the microprocessor must be held to about ±0.1V of nominal in spite of these load current steps. Since the control loop cannot respond this fast, the output capacitors must supply the load current until the control loop can respond. Capacitor ESR and ESL primarily determine the amount of droop or overshoot in the output voltage. Normally, several capacitors in parallel are required to meet microprocessor transient requirements.

Active voltage positioning is a form of deregulation. It sets the output voltage high for light loads and low for heavy loads. When load current suddenly increases, the output voltage starts from a level higher than nominal so the output voltage can droop more and stay within the specified voltage range. When load current suddenly decreases the output voltage starts at a level lower than nominal so the output voltage can have more overshoot and stay within the specified voltage range. Less output capacitance is required when voltage positioning is used because more voltage variation is allowed on the output capacitors.

Active voltage positioning can be implemented using the OPTI-LOOP architecture of the LTC1736 with two external resistors. An input voltage offset is introduced when the error amplifier has to drive a resistive load. This offset is limited to ±30mV at the input of the error amplifier. The resulting change in output voltage is the product of input offset and the feedback voltage divider ratio.

Figure 6 shows a CPU-core-voltage regulator with active voltage positioning. Resistors R1 and R5 force the input voltage offset that sets the output voltage according to the load current level. To select values for R1 and R5, first determine the amount of output deregulation allowed. The actual specification for a typical microprocessor allows the output to vary ±0.112V. The LTC1736 output voltage



C10, C18: TAIYO YUDEN JMK107BJ105
C11: KEMET T494A475M010AS
C12 TO C14: TAIYO YUDEN GMK325F106
C15 TO C17: PANASONIC EEFUE0G181R
D1: CENTRAL SEMI CMDSH-3
D2: MOTOROLA MBRS340
L1: PANASONIC ETQP6F1R0SA
M1 TO M3: FAIRCHILD FDS6680A
R6: IRC LRF2512-01-R003-J
U1: LINEAR TECHNOLOGY LTC1736CG

Figure 6. CPU-Core-Voltage Regulator with Active Voltage Positioning

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accuracy is ±1%, so the output transient voltage cannot exceed ±0.097V. At V_{OUT} = 1.5V, the maximum output voltage change controlled by the I_{TH} pin would be:

$$\Delta V_{OSENSE} = \frac{\text{Input Offset} \bullet V_{OUT}}{V_{REF}} = \frac{\pm 0.03V \bullet 1.5}{0.8V} = \pm 56mV$$

With optimum resistor values at the I_{TH} pin, the output voltage will swing from 1.55V at minimum load to 1.44V at full load. At this output voltage, active voltage positioning provides an additional 56mV to the allowable transient voltage on the output capacitors, a 58% improvement over the 97mV allowed without active voltage positioning.

The next step is to calculate the I_{TH} pin voltage, V_{ITH}, scale factor. The V_{ITH} scale factor reflects the I_{TH} pin voltage required for a given load current. V_{ITH} controls the peak sense resistor voltage, which represents the DC output current plus one half of the peak-to-peak inductor current. The no load to full load V_{ITH} range is from 0.3V to 2.4V, which controls the sense resistor voltage from 0V to the $\Delta V_{SENSE(MAX)}$ voltage of 75mV. The calculated V_{ITH} scale factor with a 0.003Ω sense resistor is:

$$V_{ITH}\ \text{Scale Factor} = \frac{V_{ITH}\ \text{Range} \bullet \text{Sense Resistor Value}}{\Delta V_{SENSE(MAX)}} = \frac{(2.4V - 0.3V) \bullet 0.003}{0.075V} = 0.084V/A$$

V_{ITH} at any load current is:

$$V_{ITH} = \left[\left(I_{OUT(DC)} + \frac{\Delta I_L}{2}\right) \bullet V_{ITH}\ \text{Scale Factor}\right] + V_{ITH}\ \text{Offset}$$

At full load current:

$$V_{ITH(MAX)} = \left[\left(15A + \frac{5A_{P-P}}{2}\right) \bullet 0.084V/A\right] + 0.3V = 1.77V$$

At minimum load current:

$$V_{ITH(MIN)} = \left[\left(0.2A + \frac{2A_{P-P}}{2}\right) \bullet 0.084V/A\right] + 0.3V = 0.40V$$

In this circuit, V_{ITH} changes from 0.40V at light load to 1.77V at full load, a 1.37V change. Notice that ΔI_L, the peak-to-peak inductor current, changes from light load to full load. Increasing the DC inductor current decreases the permeability of the inductor core material, which decreases the inductance and increases ΔI_L. The amount of inductance change is a function of the inductor design.

To create the 30mV input offset, the gain of the error amplifier must be limited. The desired gain is:

$$A_V = \frac{\Delta V_{ITH}}{\text{Input Offset}} = \frac{1.37V}{2(0.03V)} = 22.8$$

Connecting a resistor to the output of the transconductance error amplifier will limit the voltage gain. The value of this resistor is:

$$R_{ITH} = \frac{A_V}{\text{Error Amplifier } g_m} = \frac{22.8}{1.3ms} = 17.54k$$

To center the output voltage variation, V_{ITH} must be centered so that no I_{TH} pin current flows when the output voltage is nominal. $V_{ITH(NOM)}$ is the average voltage between V_{ITH} at maximum output current and minimum output current:

$$V_{ITH(NOM)} = \frac{V_{ITH(MAX)} - V_{ITH(MIN)}}{2} + V_{ITH(MIN)} = \frac{1.77V - 0.40V}{2} + 0.40V = 1.085V$$

The Thevenin equivalent of the gain limiting resistance value of 17.54k is made up of a resistor R5 that sources current into the I_{TH} pin and resistor R1 that sinks current to SGND.

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To calculate the resistor values, first determine the ratio between them:

$$k = \frac{V_{INTVCC} - V_{ITH(NOM)}}{V_{ITH(NOM)}} = \frac{5.2V - 1.085V}{1.085V} = 3.79$$

V_{INTVCC} is equal to V_{EXTVCC} or 5.2V if EXTVCC is not used.

Resistor R5 is:

$$R4 = (k+1) \bullet R_{ITH} = (3.79+1) \bullet 17.54k = 84.0k$$

Resistor R1 is:

$$R1 = \frac{(k+1) \bullet R_{ITH}}{k} = \frac{(3.79+1) \bullet 17.54k}{3.79} = 22.17k$$

Unfortunately, PCB noise can add to the voltage developed across the sense resistor, R6, causing the ITH pin voltage to be slightly higher than calculated for a given output current. The amount of noise is proportional to the output current level. This PCB noise does not present a serious problem but it does change the effective value of R6 so the calculated values of R1 and R5 may need to be adjusted to achieve the required results. Since PCB noise is a function of the layout, it will be the same on all boards with the same layout.

Figures 7 and 8 show the transient response before and after active voltage positioning is implemented. Notice that the output voltage droop and overshoot levels don't change but the peak-to-peak output voltage reduces considerably with active voltage positioning.

Refer to Design Solutions 10 for more information about active voltage positioning.

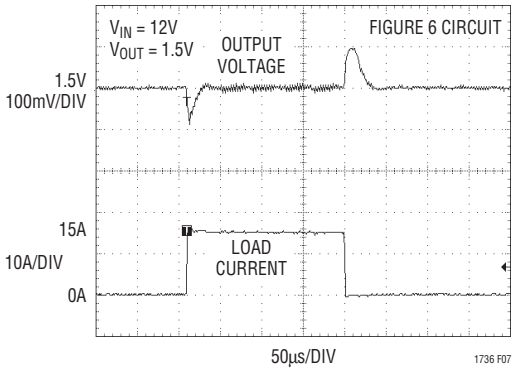


Figure 7. Normal Transient Response (Without R1, R5)

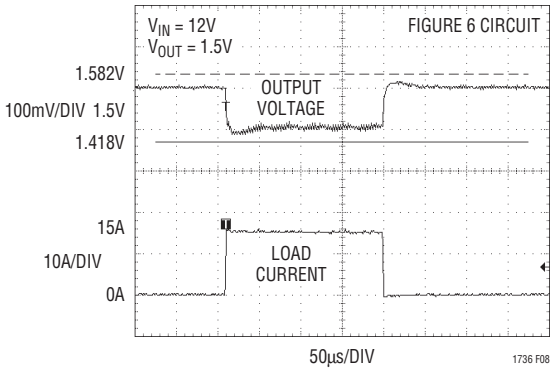


Figure 8. Transient Response with Active Voltage Positioning

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main power line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery, and double battery.

Load dump is the result of a loose power cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 9 is the most straight forward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LTC1736 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV_{DSS}.

APPLICATIONS INFORMATION

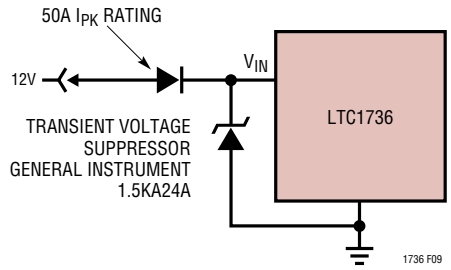


Figure 9. Plugging into the Cigarette Lighter

Design Example

As a design example, assume V_{IN} = 12V(nominal), V_{IN} = 22V(max), V_{OUT} = 1.6V(nominal), 1.8V to 1.3V range, I_{MAX} = 12A and f = 275kHz. R_{SENSE} and C_{OSC} can immediately be calculated:

R_{SENSE} = 50mV/12A = 0.0042Ω

C_{OSC} = 1.61(10^7)/(275kHz) – 11pF = 47pF

Assume a 1.2µH inductor and check the actual value of the ripple current. The following equation is used :

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The highest value of the ripple current occurs at the maximum input and output voltages:

$$\Delta I_L = \frac{1.8V}{275kHz(1.2\mu H)}\left(1-\frac{1.8V}{22V}\right) = 5A$$

The maximum ripple current is 42% of maximum output current, which is about right.

Next, verify the minimum on-time of 200ns is not violated. The minimum on-time occurs at maximum V_{IN} and minimum V_{OUT}.

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{1.3V}{22V(275kHz)} = 215ns$$

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6612A results in: $R_{DS(ON)}$ = 0.03Ω, C_{RSS} = 80pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{1.6V}{22V}(12)^2\left[1+(0.005)(50°C-25°C)\right](0.03\Omega) + 1.7(22V)^2(12A)(80pF)(275kHz) = 571mW$$

Because the duty cycle of the bottom MOSFET is much greater than the top, two larger MOSFETs must be paralleled. Choosing Fairchild FDS6680A MOSFETs yields a parallel $R_{DS(ON)}$ of 0.0065Ω. The total power dissipaton for both bottom MOSFETs, again assuming T = 50°C, is:

$$P_{SYNC} = \frac{22V-1.6V}{22V}(12A)^2(1.1)(0.0065\Omega) = 955mW$$

Thanks to current foldback, the bottom MOSFET dissipaton in short circuit will be less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 6A at temperature. C_{OUT} is chosen with an ESR of 0.01Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE}$ = $R_{ESR}(\Delta I_L)$ = 0.01Ω(5A) = 50mV_{P-P}

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1736. These items are also illustrated graphically in the layout diagram of Figure 10. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1736 PGND pin should tie to the GND plane close to the input capacitor. The SGND pin should then connect to PGND and all components that connect to SGND should make a single point tie to the SGND pin. The low side FET source pins should connect directly to the input capacitor ground.

APPLICATIONS INFORMATION

2. Does the V_{OSENSE} pin connect as close as possible to the load? The optional 50pF to 100pF capacitor from V_{FB} to SGND should be as close as possible to the LTC1736.

3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE$^+$ and SENSE$^-$ should be as close as possible to the LTC1736. Ensure accurate current sensing with kelvin connections as shown in Figure 11. Series resistance can be added to the SENSE lines to increase noise rejection.

4. Does the (+) terminal of C_{IN} connect to the drain of the topside MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).

5. Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance.

6. Keep the switching node (SW), Top Gate node (TG) and Boost node (BOOST) away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" (Pins 13 to 24) of the LTC1736 and occupy minimum PC trace area.

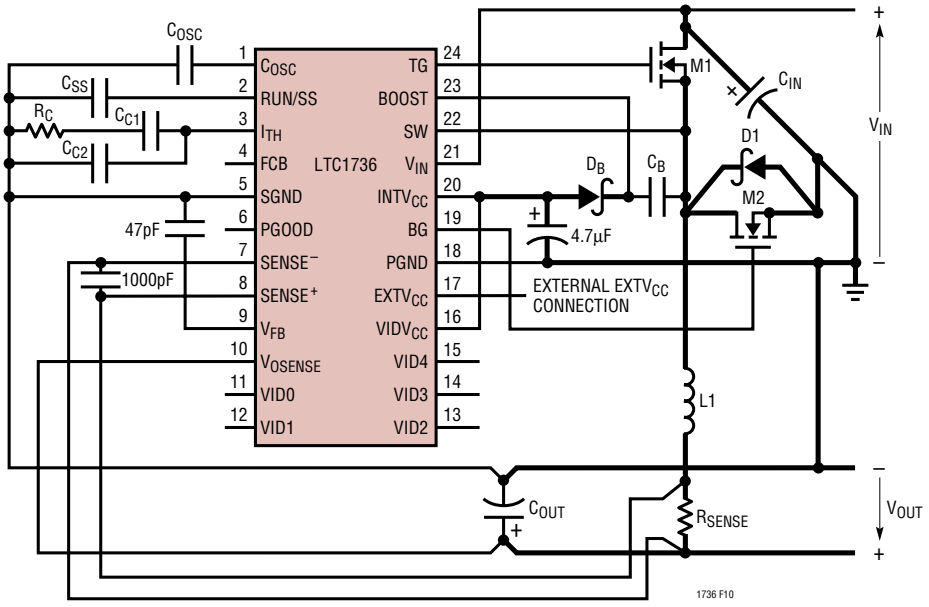


Figure 10. LTC1736 Layout Diagram

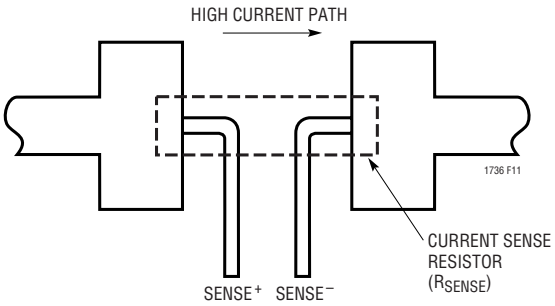
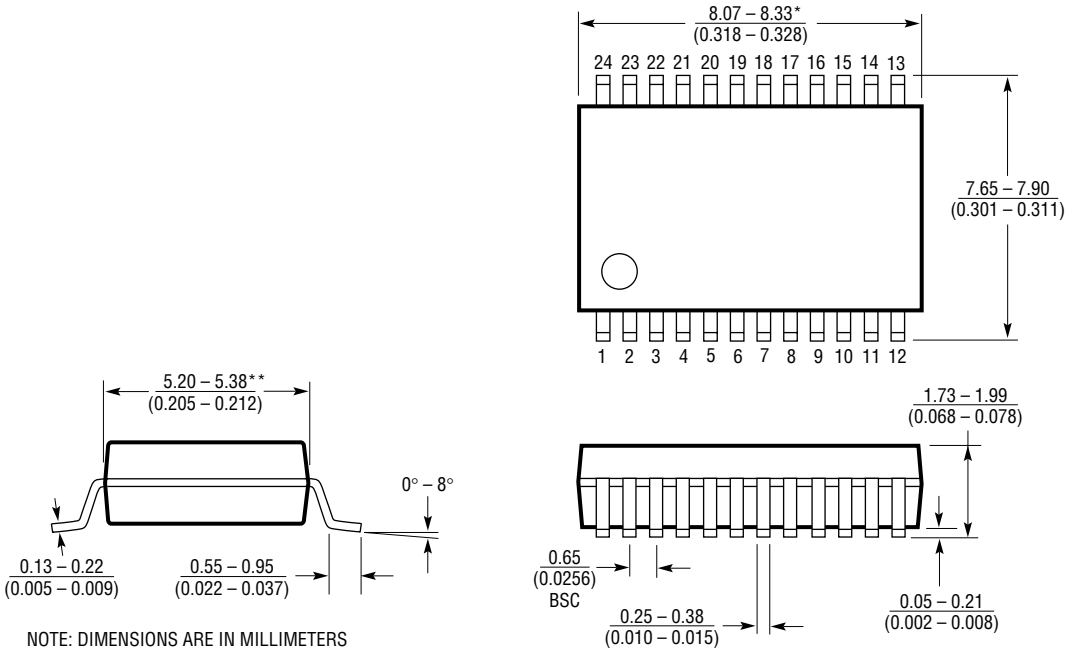


Figure 11. Kelvin Sensing R_{SENSE}

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

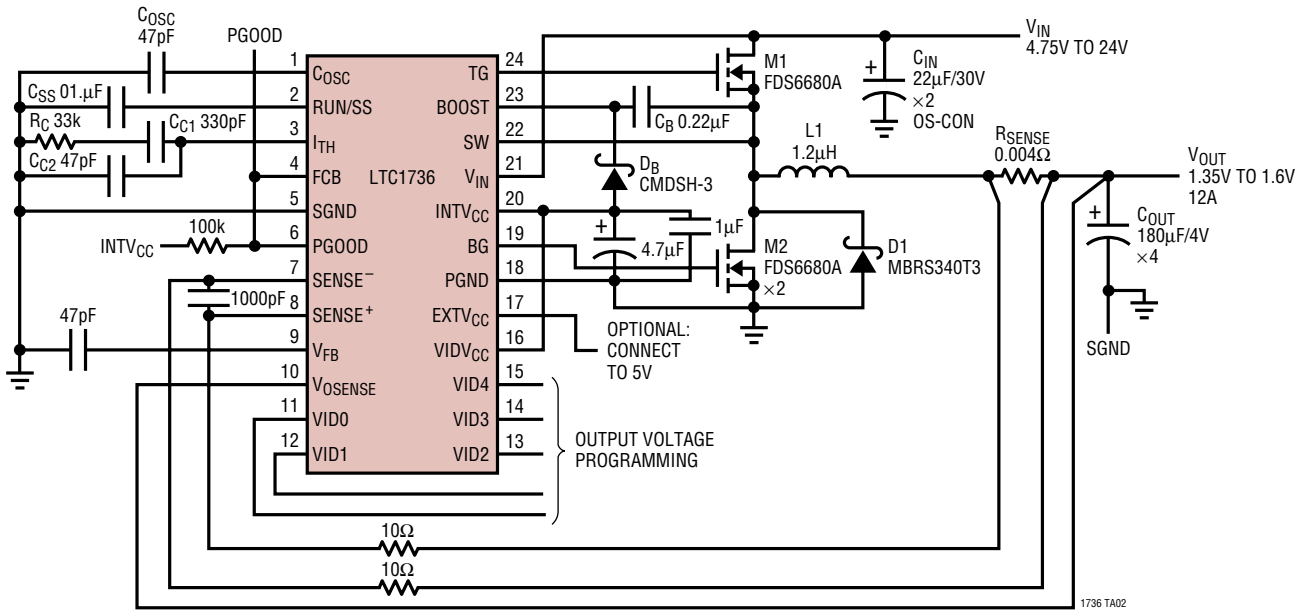
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G24 SSOP 1098

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TYPICAL APPLICATION

12A Converter with FCB Tied to PGOOD for CPU Power; Optimized for Output Voltages of 1.3V to 1.6V



C_{OUT}: 4-180µF/4V PANASONIC EEFUE0G181R (AS SHOWN)
3-470µF/6.3V KEMIT T51CX447M006AS (ALTERNATE)
1-820µF/4V SANYO 4SP820M + 1-180µF/4V PANASONIC EEFUE0G181R (ALTERNATE)
C_{IN}: SANYO OS-CON 305C22M
L1: PANASONIC ETQP6RZ1RZ0HFA

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1147	High Efficiency Step-Down Controller	100% DC, Burst Mode Operation, SO-8
LTC1148HV/LTC1148	High Efficiency Synchronous Step-Down Controllers	100% DC, Burst Mode Operation, V_{IN} < 20V
LTC1149	High Efficiency Synchronous Step-Down Controller	100% DC, Std Threshold MOSFETs, V_{IN} < 48V
LTC1159	High Efficiency Synchronous Step-Down Controller	100% DC, Logic Level MOSFETs, V_{IN} < 40V
LTC1265	1.2A Monolithic High Efficiency Step-Down Switching Regulator	100% DC, Burst Mode Operation, 14-Pin SO
LT1375/LT1376	1.5A 500kHz Step-Down Switching Regulators	High Efficiency, Constant Frequency, SO-8
LTC1435A	High Efficiency Synchronous Step-Down Controller, N-Ch Drive	Burst Mode Operation, 16-Pin Narrow SO
LTC1436A/LTC1436A-PLL	High Efficiency Low Noise Synchronous Step-Down Converters, N-Ch Drive	Adaptive Power™ Mode, 20-Pin/24-Pin SSOP
LTC1474/LTC1475	Ultralow Quiescent Current Step-Down Monolithic Switching Regulators	I_Q = 10µA, 100% DC, 8-Pin MSOP
LTC1625/LTC1775	No R_{SENSE}™ Current Mode Synchronous Step-Down Controllers	Up to 97% Efficiency, Burst Mode Operation, 16-Pin SSOP
LTC1628	Dual High Efficiency 2-Phase Step-Down Controller	Antiphase Drive, 28-Pin SSOP Package
LTC1703	550kHz Dual Output Synchronous Step-Down DC/DC Controller	5-Bit, Mobile VID On Output 1, No R_{SENSE}
LTC1735	High Efficiency Synchronous Step-Down Controller, N-Ch Drive	Burst Mode Operation, 16-Pin Narrow SSOP
LTC1735-1	High Efficiency Step-Down Controller with Power Good	Output Fault Protection, 16-Pin SSOP and SO-8

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