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FAIRCHILD SEMICONDUCTOR®

May 2008

74VHCT74A
Dual D-Type Flip-Flop with Preset and Clear

Features

- High speed: f_{MAX} = 160MHz (Typ.) at T_A = 25°C
- High noise immunity: V_{IH} = 2.0V, V_{IL} = 0.8V
- Power down protection is provided on all inputs and outputs
- Low power dissipation: I_{CC} = 2μA (Max.) at T_A = 25°C
- Pin and function compatible with 74HCT74

General Description

The VHCT74A is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to the Q OUTPUT during the positive going transition of the CK pulse. CLR and PR are independent of the CK and are accomplished by setting the appropriate input LOW.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with V_{CC} = 0V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

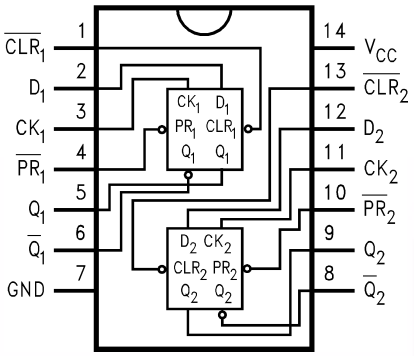
Ordering Information

Order Number	Package Number	Package Description
74VHCT74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHCT74ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

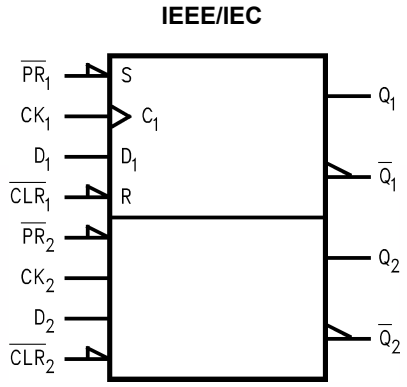
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1$, $\overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1$, $\overline{PR}_2$	Direct Preset Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Truth Table

Inputs				Outputs		
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	Function
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q_n	Q_n	No Change

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	
	Note 1	–0.5V to V_{CC} + 0.5V
	Note 2	–0.5V to 7.0V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current(3)	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(4)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	
	Note 1	0V to V_{CC}
	Note 2	0V to 5.5V
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time	
	V_{CC} = 5.0V ±0.5V	0ns/V ~ 20ns/V

Notes:

1. HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.
2. V_{CC} = 0V.
3. V_{OUT} < GND, V_{OUT} > V_{CC} (Outputs Active).
4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	4.5			2.0			2.0		V
		5.5			2.0			2.0		
V_{IL}	LOW Level Input Voltage	4.5					0.8		0.8	V
		5.5					0.8		0.8	
V_{OH}	HIGH Level Output Voltage	4.5	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50μA	4.40	4.50		4.40		V
		4.5		I_{OH} = –8mA	3.94			3.80		
V_{OL}	LOW Level Output Voltage	4.5	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA		0.0	0.1		0.1	V
		4.5		I_{OL} = 8mA			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND				2.0		20.0	μA
I_{CCT}	Maximum I_{CC} / Input	5.5	V_{IN} = 3.4V, Other Inputs = V_{CC} or GND				1.35		1.50	mA
I_{OFF}	Output Leakage Current (Power Down State)	0.0	V_{OUT} = 5.5V				+0.5		+5.0	μA

AC Electrical Characteristics

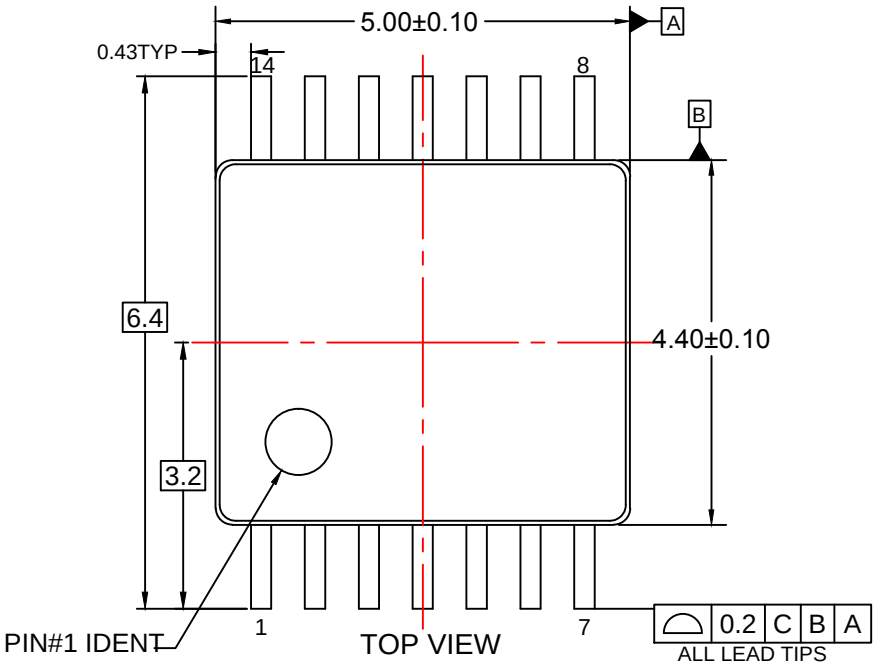
Symbol	Parameter	V_{CC} (V)[5]	Conditions	T_A = 25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	5.0	C_L = 15pF	100	160		80		MHz
		5.0	C_L = 50pF	80	140		65		
t_{PLH}, t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	5.0	C_L = 15pF		5.8	7.8	1.0	9.0	ns
		5.0	C_L = 50pF		6.3	8.8	1.0	10.0	
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	5.0	C_L = 15pF		7.6	10.4	1.0	12.0	ns
		5.0	C_L = 50pF		8.1	11.4	1.0	13.0	
C_{IN}	Input Capacitance		V_{CC} = Open		4	10		10	pF
C_{PD}	Power Dissipation Capacitance		[6]		24				pF

Notes:

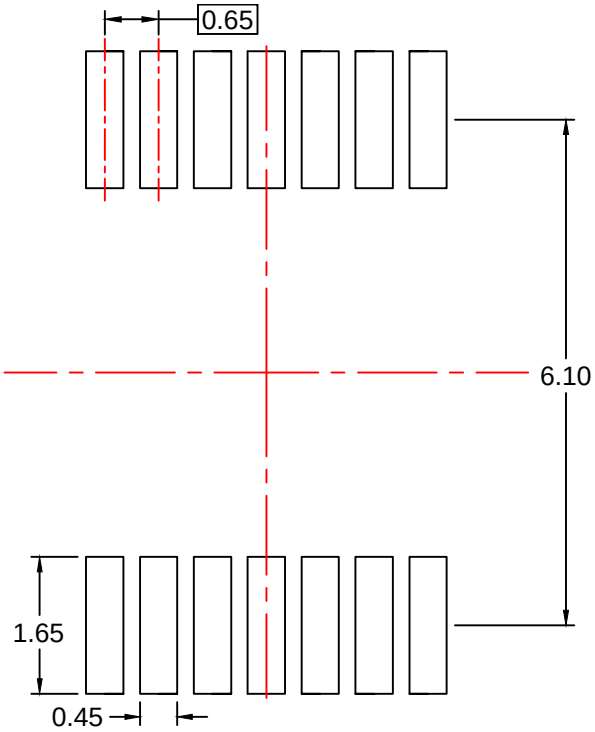
5. V_{CC} is 5.0 ± 0.5V
6. C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC} / 2 (per flip-flop).

AC Operating Requirements

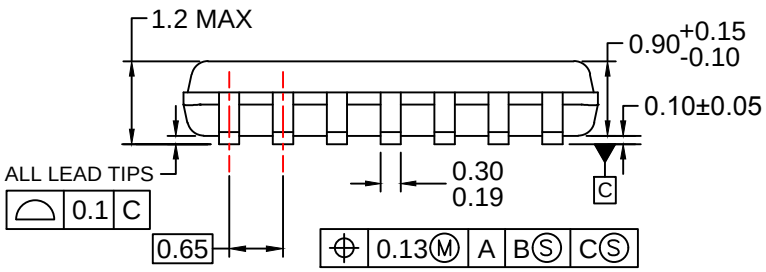
Symbol	Parameter	V_{CC} (V)	T_A = 25°C		T_A = –40°C to +85°C	Units
			Typ.	Guaranteed Minimum		
$t_W(L)$, $t_W(H)$	Minimum Pulse Width (CK)	5.0 ± 0.5		5.0	5.0	ns
$t_W(L)$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		5.0	5.0	ns
t_S	Minimum Setup Time	5.0 ± 0.5		5.0	5.0	ns
t_H	Minimum Hold Time	5.0 ± 0.5		0	0	ns
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		3.5	3.5	ns



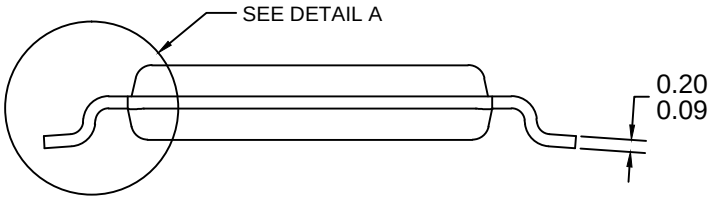
TOP VIEW

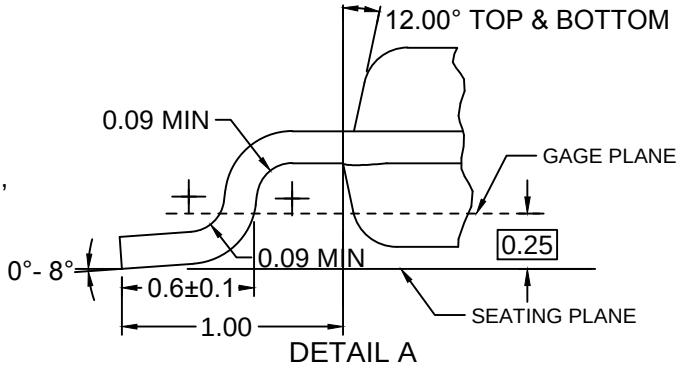


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

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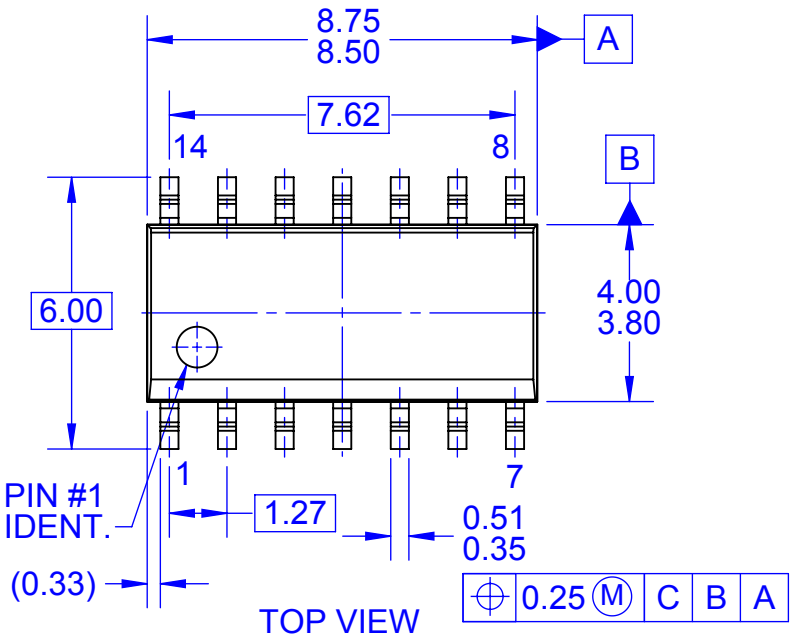
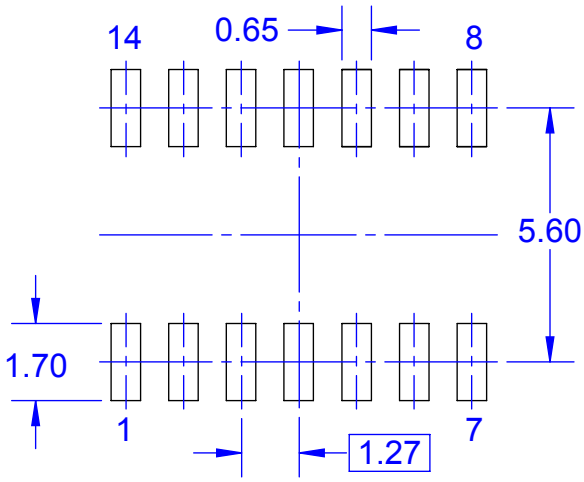
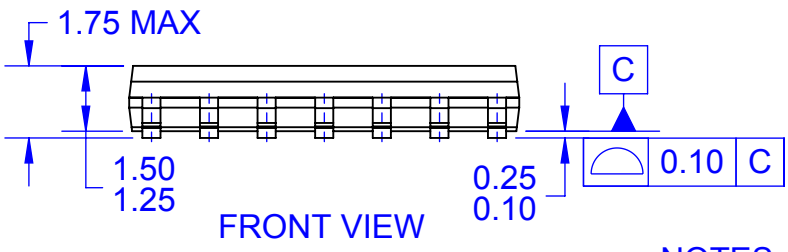


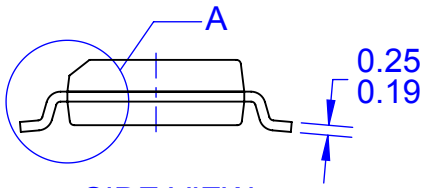
TOP VIEW



LAND PATTERN RECOMMENDATION



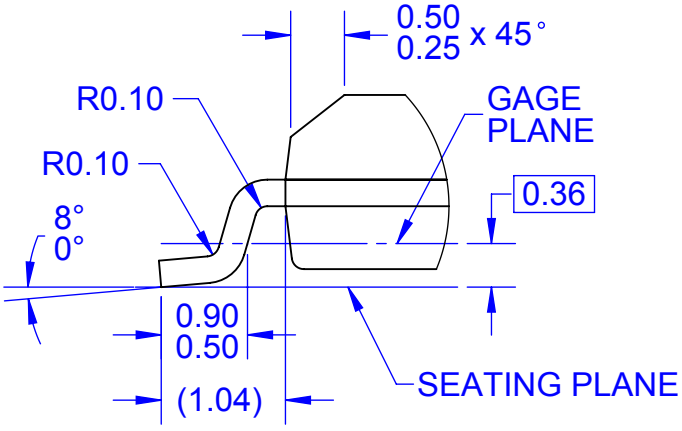
FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14



DETAIL A
SCALE 16 : 1

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