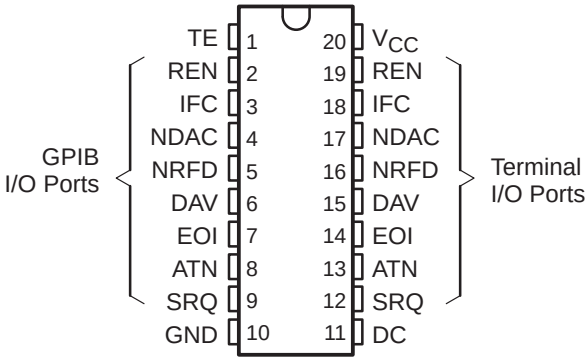
SLLS019F − JUNE 1986 − REVISED JULY 2004

- **Suitable for IEEE Standard 488-1978 (GPIB)**
- **8-Channel Bidirectional Transceivers**
- **Designed to Implement Control Bus Interface**
- **Designed for Single Controller**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 46 mW Max Per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance pnp Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch Free)**

DW OR N PACKAGE
(TOP VIEW)



CHANNEL-IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

description/ordering information

The SN75ALS161 eight-channel general-purpose interface bus transceivers are high-speed, advanced low-power Schottky-process devices designed to provide the bus-management and data-transfer signals between operating units of a single-controller instrumentation system. When combined with the SN75ALS160 octal bus transceivers, this device provides a complete 16-wire interface for the IEEE 488 bus.

The SN75ALS161 device features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the direction-control (DC) and talk-enable (TE) signals.

The driver outputs general-purpose interface bus (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle sink-current loads up to 48 mA. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV on the commercial part, and 250 mV on the military part, minimum, for increased noise immunity. All receivers have 3-state outputs, to present a high impedance to the terminal when disabled.

The SN75ALS161 is characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 20	SN75ALS161N	SN75ALS161N
	SOIC (DW)	Tube of 25	SN75ALS161DW	75ALS161
		Reel of 2000	SN75ALS161DWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(CONTROLLED BY DC)					(CONTROLLED BY TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

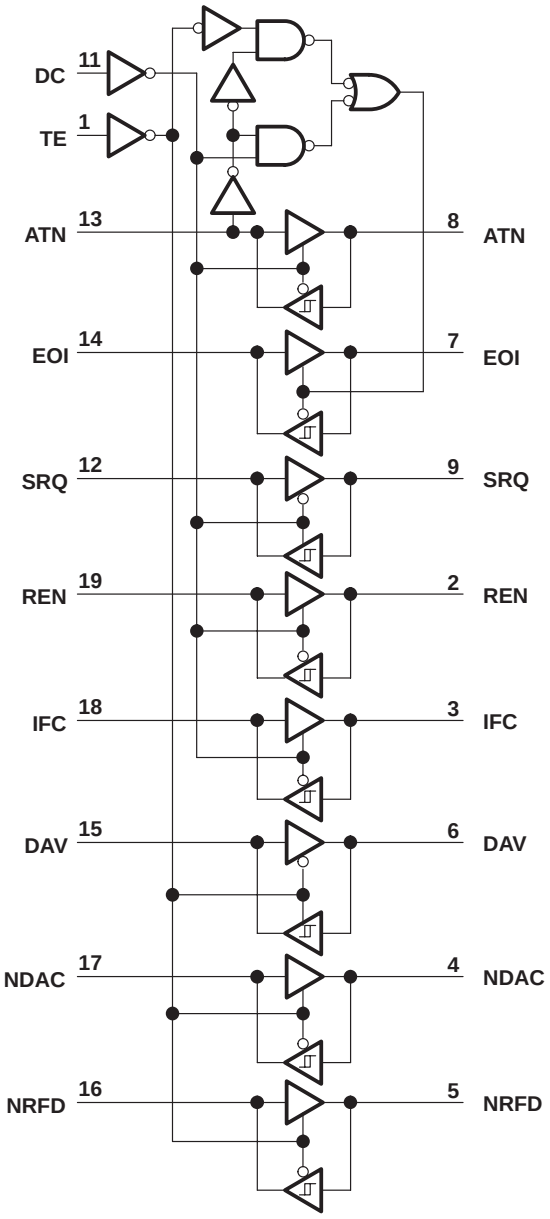
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.

Data transfer is noninverting in both directions.

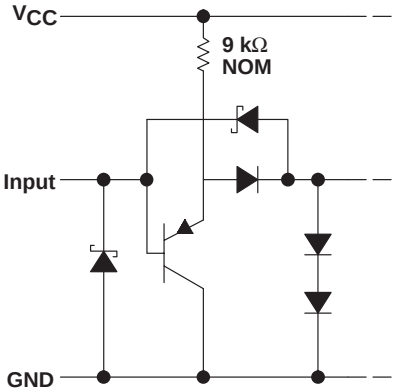
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

logic diagram (positive logic)

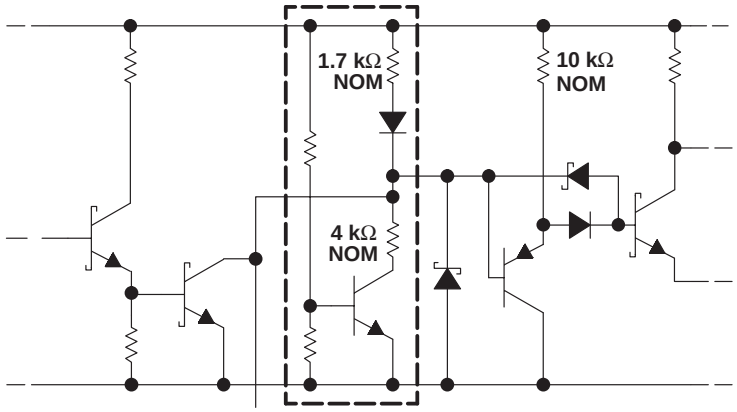


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

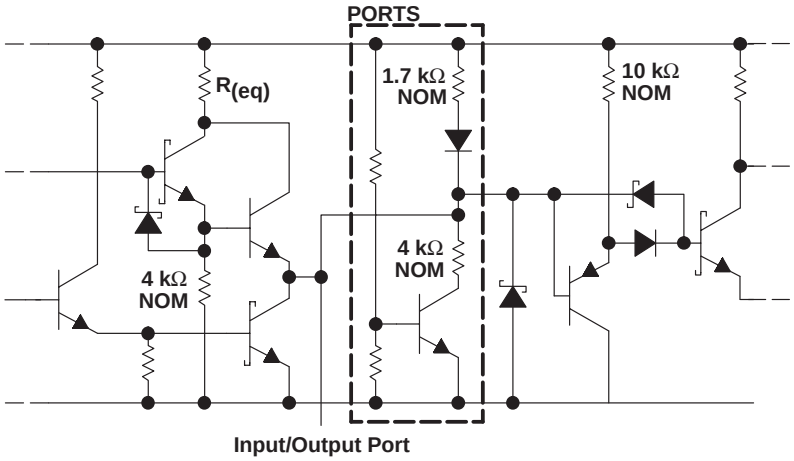


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS, EXCEPT SRQ, NDAC, AND NRFD GPIB I/O PORTS



Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
$R_{(eq)}$ = equivalent resistor
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Low-level driver output current, I_{OL} . . . . . 100 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Bus ports with pullups active			− 5.2	mA
		Terminal ports			− 800	µA
I_{OL}	Low-level output current	Bus ports			48	mA
		Terminal ports			16	
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA				−0.8	−1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus				0.4	0.65		V
V_{OH}§	High-level output voltage	Terminal	I_{OH} = − 800 μA,	V_{CC} = MIN	T_A = 25°C and MAX	2.7	3.5		V
					T_A = MIN	2.7	3.5		
		Bus	I_{OH} = − 5.2 mA,	V_{CC} = MIN	T_A = 25°C and MAX	2.2			
					T_A = MIN	2.2			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	V_{CC} = MIN			0.3	0.5	V
		Bus	I_{OL} = 48 mA,	V_{CC} = MIN			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V,	V_{CC} = MAX			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V,	V_{CC} = MAX			0.1	20	μA
$V_{I/O}$	Voltage at GPIB I/O port		$I_{I(bus)}$ = 0			2.5	3	3.7	V
			$I_{I(bus)}$ = 0			2.5	3	3.7	
			$I_{I(bus)}$ = −12 mA					−1.5	
I_{IL}	Low-level input current	Terminal and control inputs	V_I = 0.5 V,	V_{CC} = MAX			−10	−100	μA
$I_{I/O}$	Current into GPIB I/O port	Power on	$V_{I(bus)}$ = −1.5 V to 0.4 V			−1.3			mA
			$V_{I(bus)}$ = 0.4 V to 2.5 V			0		−3.2	
			$V_{I(bus)}$ = 2.5 V to 3.7 V					2.5 −3.2	
			$V_{I(bus)}$ = 3.7 V to 5 V			0		2.5	
			$V_{I(bus)}$ = 5 V to 5.5 V			0.7		2.5	
		Power off	V_{CC} = 0	$V_{I(bus)}$ = 0 to 2.5 V				40	μA
I_{OS}§	Short-circuit output current	Terminal	V_{CC} = MAX			−15	−35	−75	mA
		Bus				−25	−50	−125	
I_{CC}	Supply current		No load,	TE and DC low, V_{CC} = MAX			55	75	mA
$C_{I/O}$	GPIB I/O port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V,	f = 1 MHz		30		pF

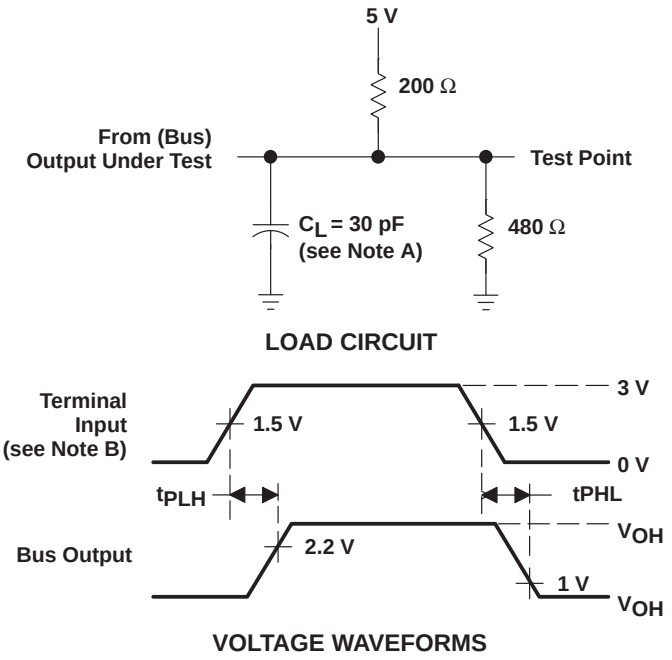
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ V_{OH} and I_{OS} apply to 3-state outputs only.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					12	20	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high- to low-level output					7	14	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

† All typical values are at T_A = 25°C.

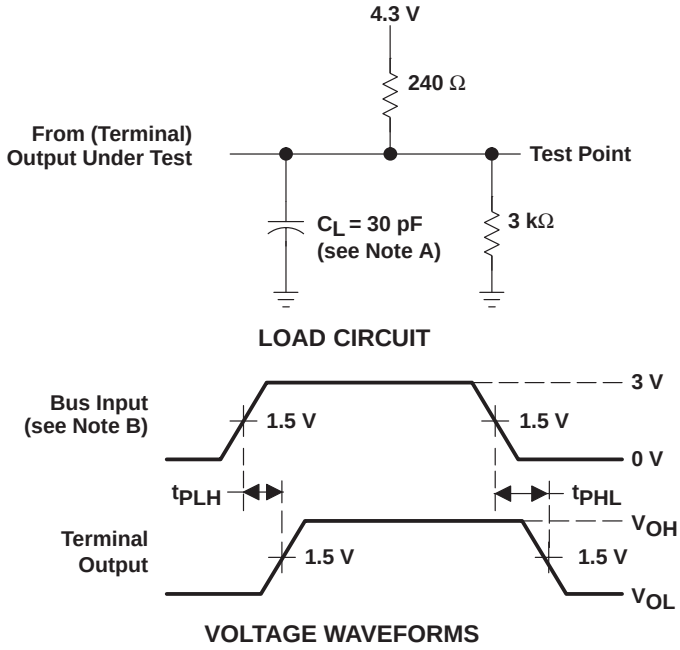
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

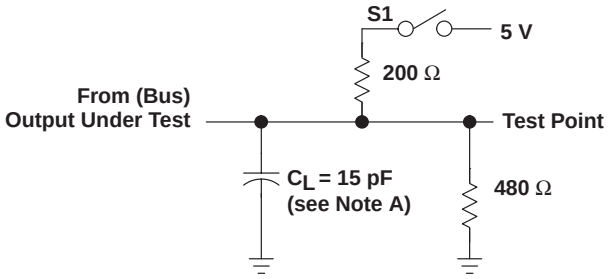
PARAMETER MEASUREMENT INFORMATION



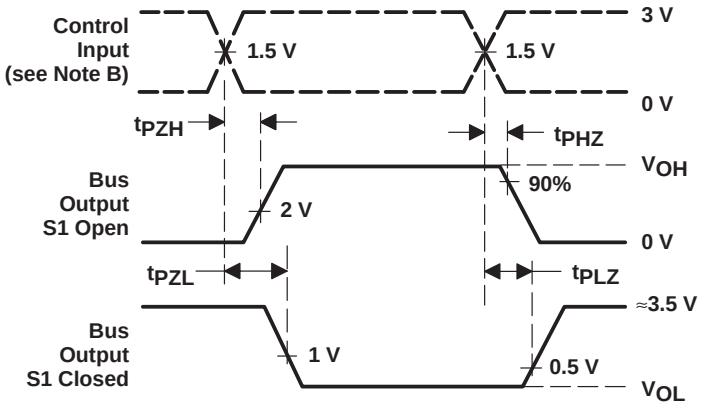
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

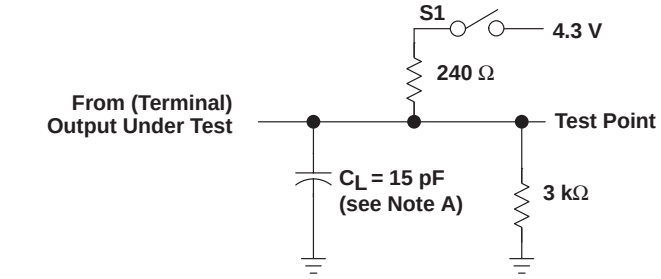


VOLTAGE WAVEFORMS

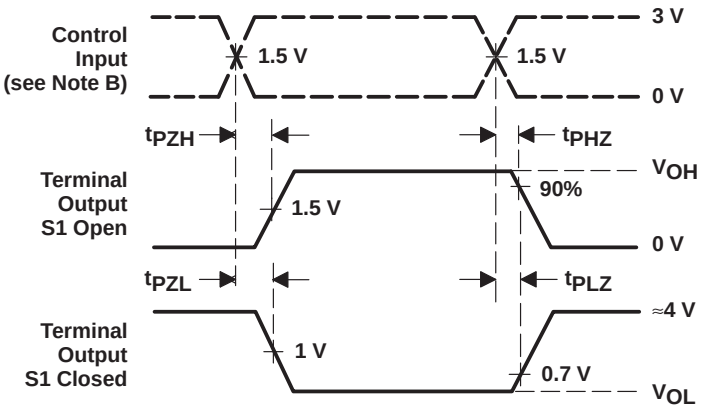
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Bus Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Terminal Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

**TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

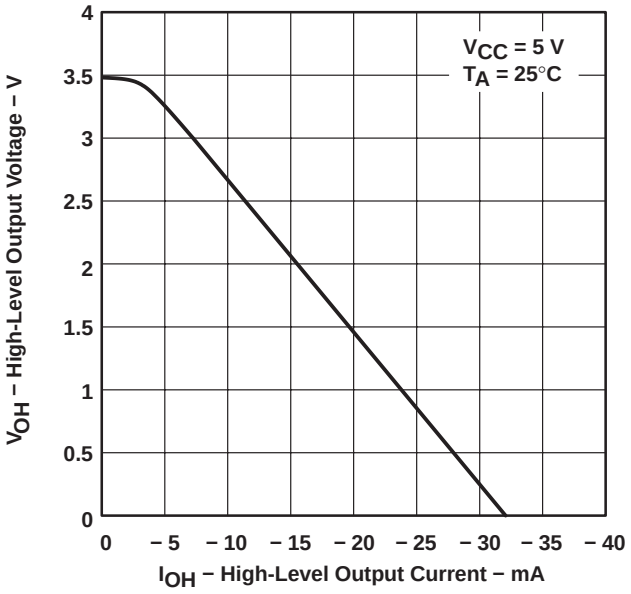


Figure 5

**TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

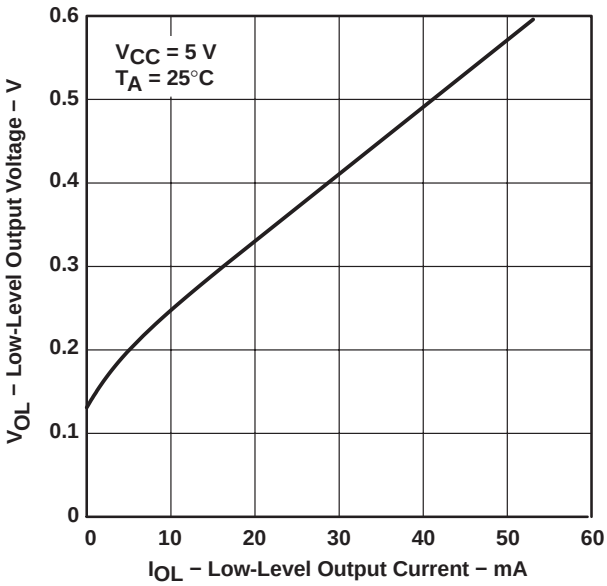


Figure 6

**TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE**

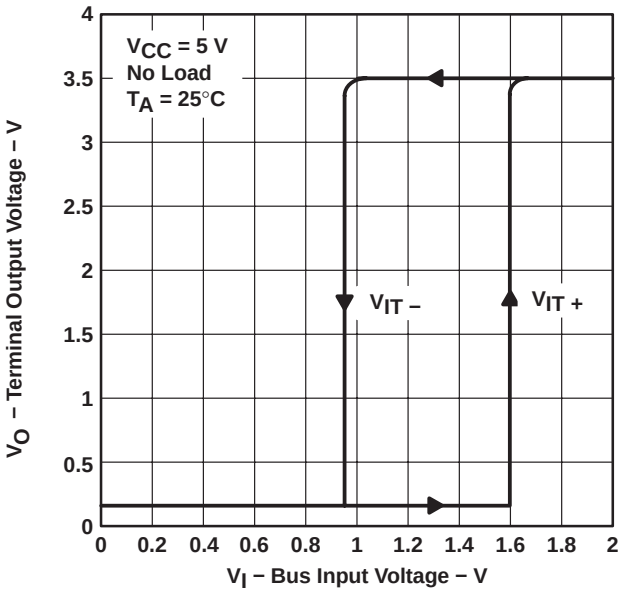


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

**GPIB I/O BUS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

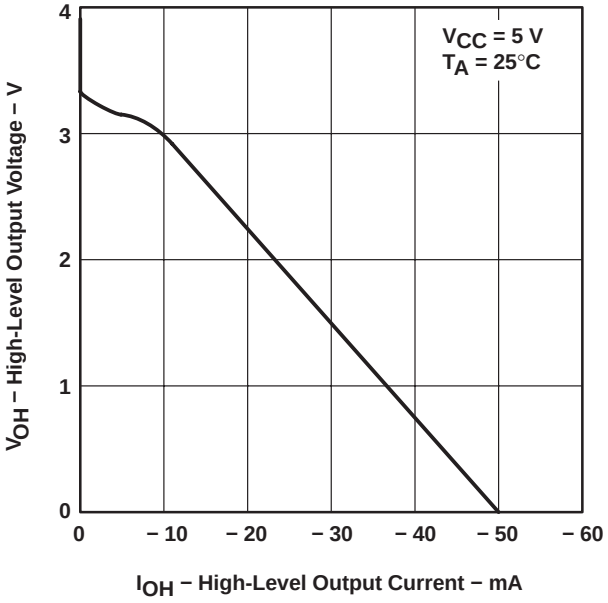


Figure 8

**GPIB I/O BUS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

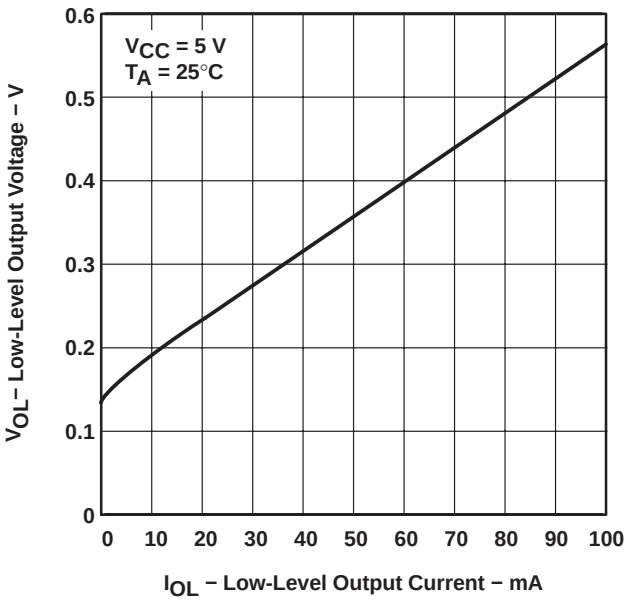


Figure 9

**BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE**

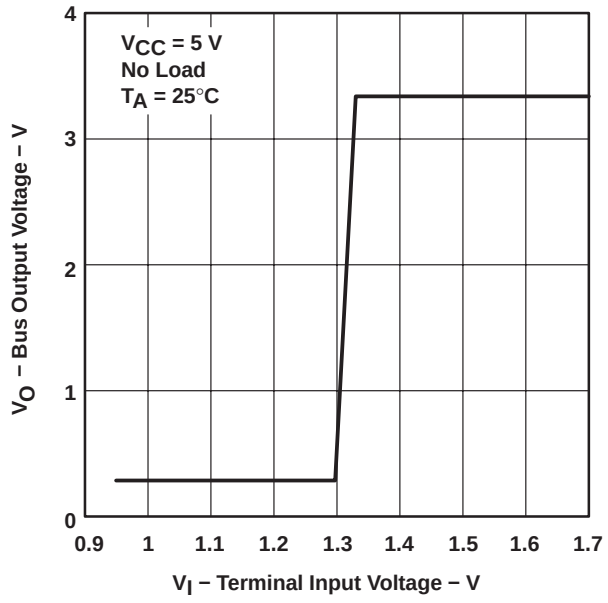


Figure 10

**GPIB I/O BUS
CURRENT
vs
VOLTAGE**

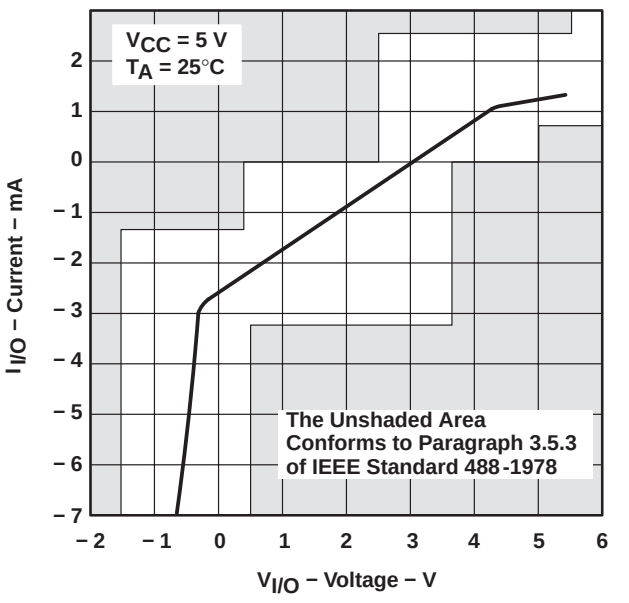


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS161DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS161	Samples
SN75ALS161DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS161	Samples
SN75ALS161DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS161	Samples
SN75ALS161DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS161	Samples
SN75ALS161N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS161N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

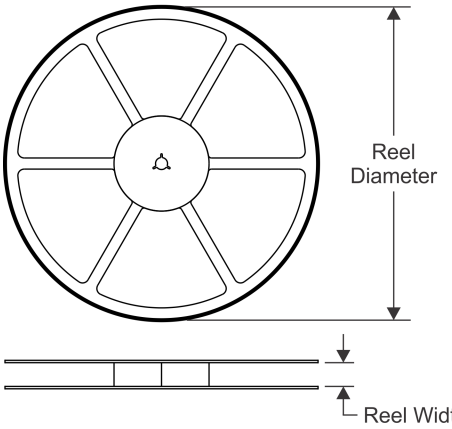
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

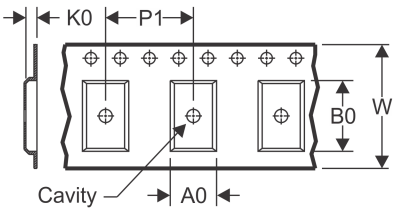
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

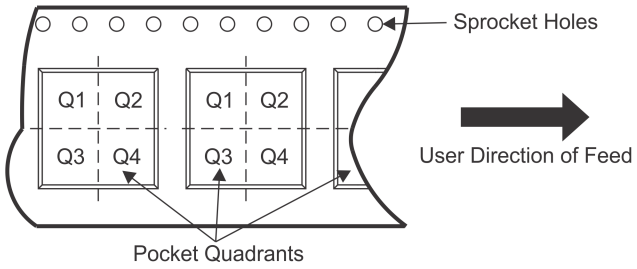


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

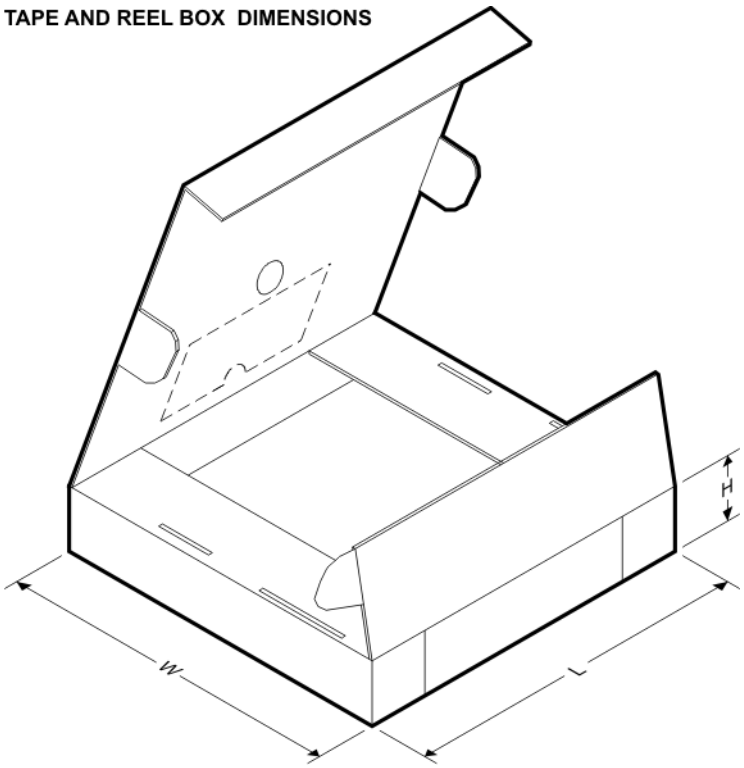
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS161DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



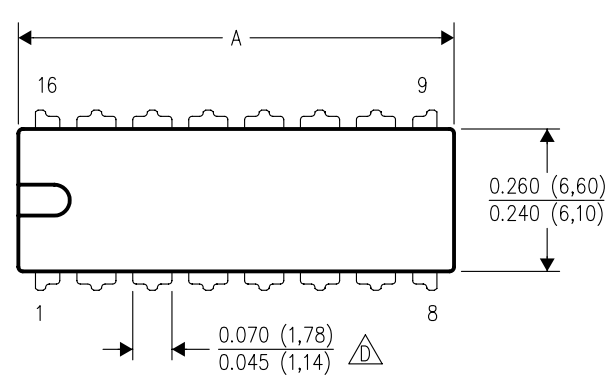
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS161DWR	SOIC	DW	20	2000	350.0	350.0	43.0

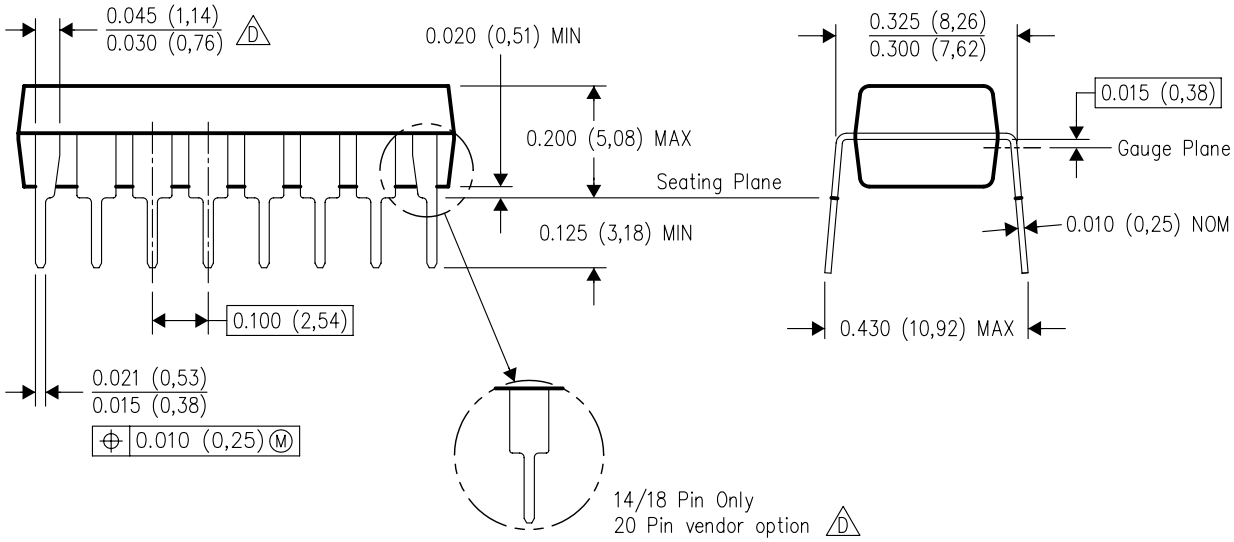
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

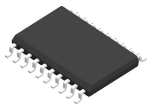


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

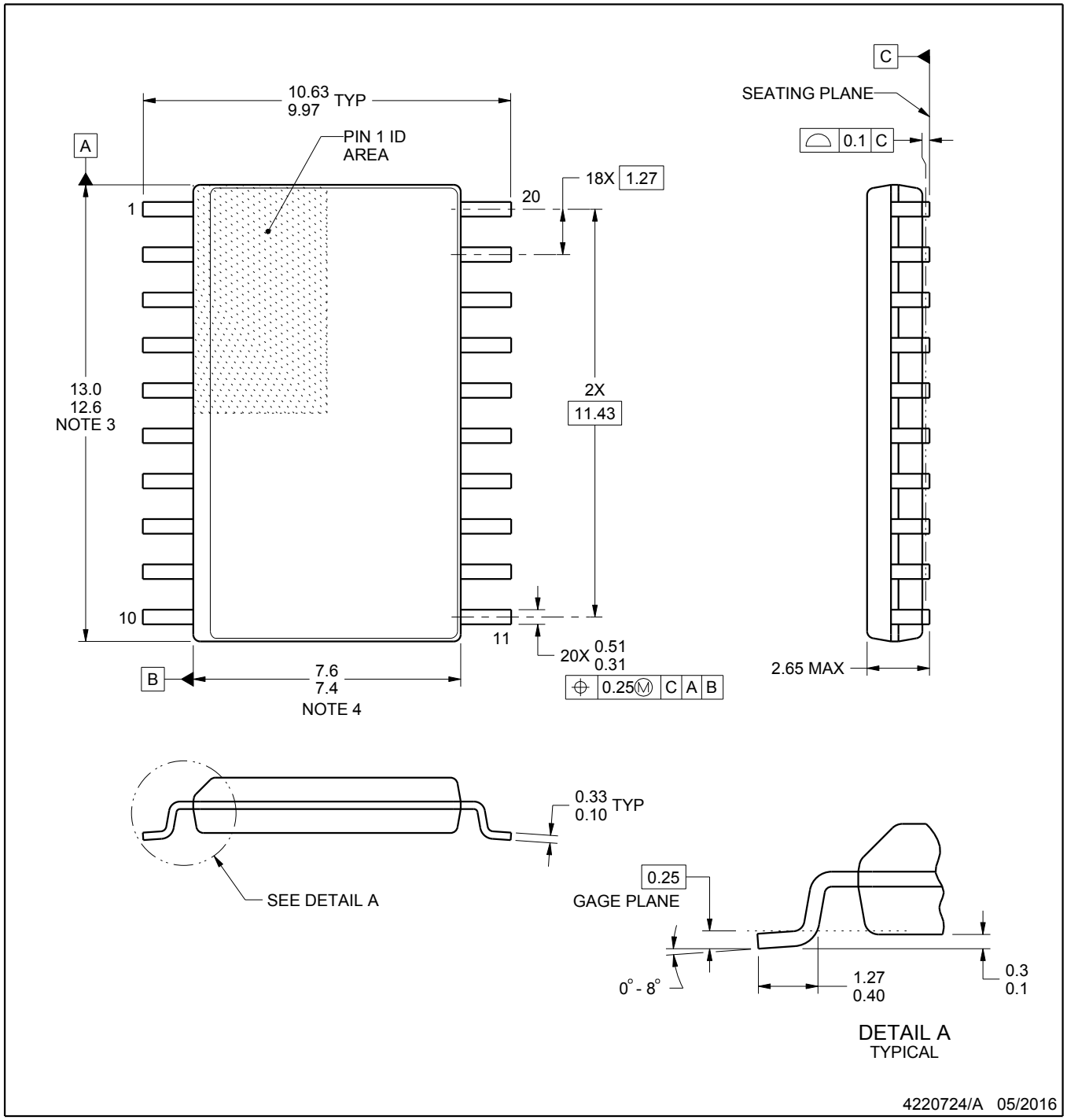


PACKAGE OUTLINE

DW0020A

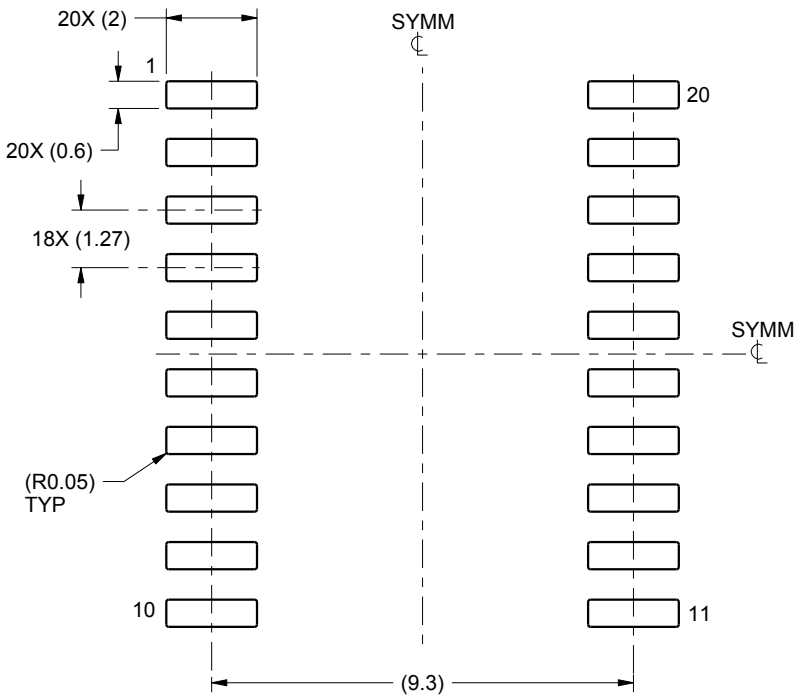
SOIC - 2.65 mm max height

SOIC

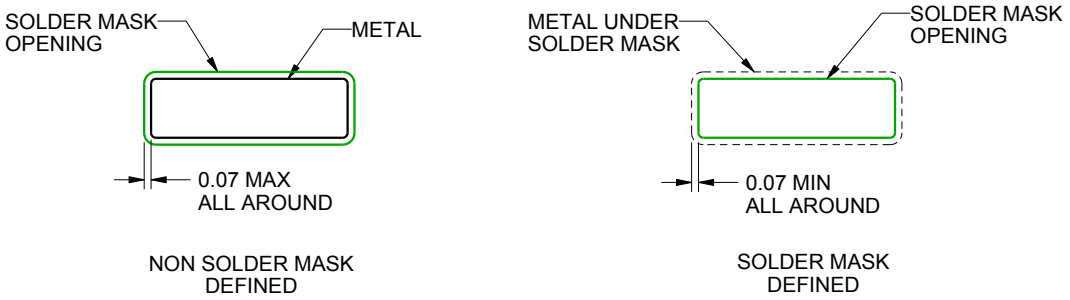


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

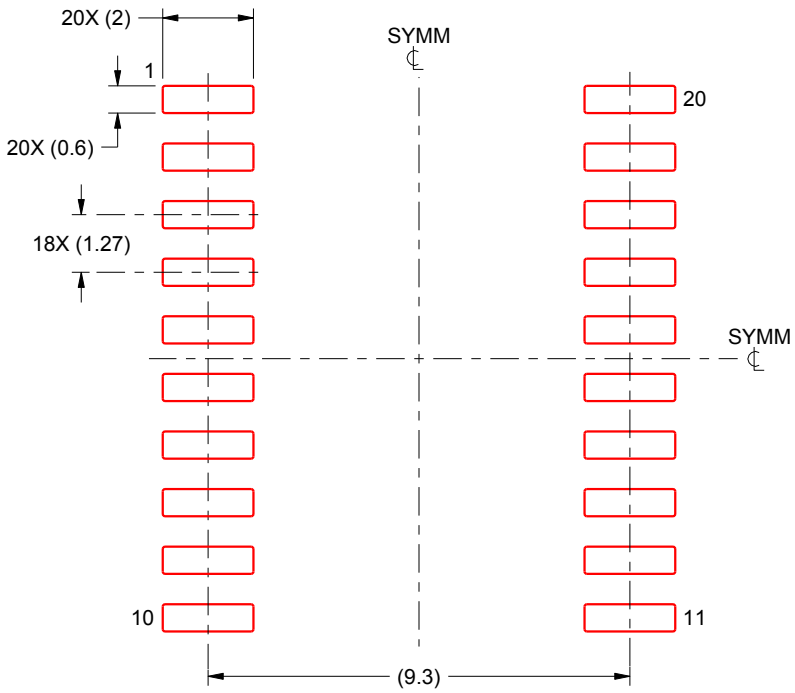


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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