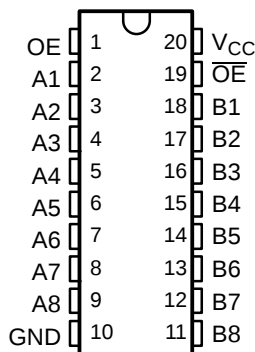


## FEATURES

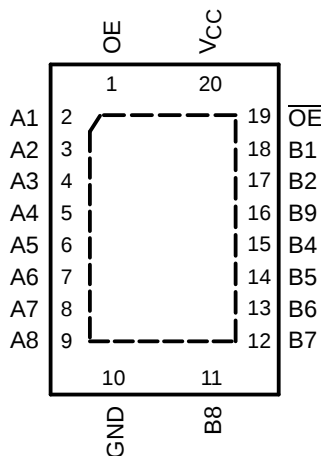
- High-Bandwidth Data Path (up to 500 MHz <sup>(1)</sup>)
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance ( $r_{on}$ ) Characteristics Over Operating Range ( $r_{on} = 4\ \Omega$  Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0- to 5-V Switching With 3.3-V  $V_{CC}$
  - 0- to 3.3-V Switching With 2.5-V  $V_{CC}$
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 4\text{ pF}$  Typ)
- Fast Switching Frequency ( $f_{OE} = 20\text{ MHz Max}$ )
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 0.7\text{ mA Typ}$ )
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

(1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DBQ, DGV, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74CB3Q3345

## 8-BIT FET BUS SWITCH

### 2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS144B–OCTOBER 2003–REVISED MARCH 2005

## DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q3345 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3345 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3384A is organized as an 8-bit bus switch with two output-enable (OE,  $\overline{OE}$ ) inputs. When OE is high or  $\overline{OE}$  is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low and  $\overline{OE}$  is high, the bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

## ORDERING INFORMATION

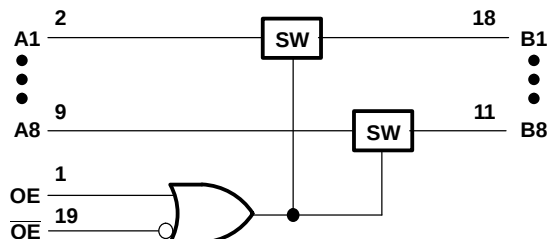
| $T_A$         | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY              | Tape and reel | SN74CB3Q3345RGYR      | BU345            |
|               | SSOP (QSOP) – DBQ      | Tape and reel | SN74CB3Q3345DBQR      | CB3Q3345         |
|               | TSSOP – PW             | Tube          | SN74CB3Q3345PW        | BU345            |
|               |                        | Tape and reel | SN74CB3Q3345PWR       |                  |
|               | TVSOP – DGV            | Tape and reel | SN74CB3Q3345DGV       | BU345            |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

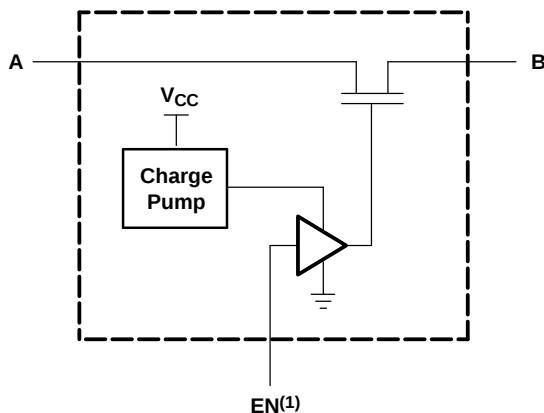
## FUNCTION TABLE

| INPUTS |                 | INPUT/OUTPUT<br>A | FUNCTION        |
|--------|-----------------|-------------------|-----------------|
| OE     | $\overline{OE}$ |                   |                 |
| H      | X               | B                 | A port = B port |
| X      | L               | B                 | A port = B port |
| L      | H               | Z                 | Disconnect      |

## LOGIC DIAGRAM (POSITIVE LOGIC)



### SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                               | MIN                        | MAX  | UNIT |
|---------------|-----------------------------------------------|----------------------------|------|------|
| $V_{CC}$      | Supply voltage range                          | -0.5                       | 4.6  | V    |
| $V_{IN}$      | Control input voltage range <sup>(2)(3)</sup> | -0.5                       | 7    | V    |
| $V_{I/O}$     | Switch I/O voltage range <sup>(2)(3)(4)</sup> | -0.5                       | 7    | V    |
| $I_{I/K}$     | Control input clamp current                   |                            | -50  | mA   |
| $I_{I/OK}$    | I/O port clamp current                        |                            | -50  | mA   |
| $I_{IO}$      | ON-state switch current <sup>(5)</sup>        |                            | ±64  | mA   |
|               | Continuous current through $V_{CC}$ or GND    |                            | ±100 | mA   |
| $\theta_{JA}$ | Package thermal impedance                     | DBQ package <sup>(6)</sup> |      | 68   |
|               |                                               | DGV package <sup>(6)</sup> |      | 92   |
|               |                                               | PW package <sup>(6)</sup>  |      | 83   |
|               |                                               | RGY package <sup>(7)</sup> |      | 37   |
| $T_{stg}$     | Storage temperature range                     | -65                        | 150  | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.
- (7) The package thermal impedance is calculated in accordance with JESD 51-5.

**SN74CB3Q3345**  
**8-BIT FET BUS SWITCH**  
**2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH**

SCDS144B–OCTOBER 2003–REVISED MARCH 2005

**Recommended Operating Conditions<sup>(1)</sup>**

|                  |                                  |                                  | MIN | MAX | UNIT |
|------------------|----------------------------------|----------------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage                   |                                  | 2.3 | 3.6 | V    |
| V <sub>IH</sub>  | High-level control input voltage | V <sub>CC</sub> = 2.3 V to 2.7 V | 1.7 | 5.5 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7 V to 3.6 V | 2   | 5.5 |      |
| V <sub>IL</sub>  | Low-level control input voltage  | V <sub>CC</sub> = 2.3 V to 2.7 V | 0   | 0.7 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7 V to 3.6 V | 0   | 0.8 |      |
| V <sub>I/O</sub> | Data input/output voltage        |                                  | 0   | 5.5 | V    |
| T <sub>A</sub>   | Operating free-air temperature   |                                  | –40 | 85  | °C   |

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics<sup>(1)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |                   | TEST CONDITIONS                                                       |                                                                                                             | MIN | TYP <sup>(2)</sup> | MAX  | UNIT       |
|---------------------------------|-------------------|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-----|--------------------|------|------------|
| V <sub>IK</sub>                 |                   | V <sub>CC</sub> = 3.6 V,                                              | I <sub>I</sub> = –18 mA                                                                                     |     |                    | –1.8 | V          |
| I <sub>IN</sub>                 | Control inputs    | V <sub>CC</sub> = 3.6 V,                                              | V <sub>IN</sub> = 0 to 5.5 V                                                                                |     |                    | ±1   | μA         |
| I <sub>OZ</sub> <sup>(3)</sup>  |                   | V <sub>CC</sub> = 3.6 V,                                              | V <sub>O</sub> = 0 to 5.5 V,<br>V <sub>I</sub> = 0, Switch OFF,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND |     |                    | ±1   | μA         |
| I <sub>off</sub>                |                   | V <sub>CC</sub> = 0,                                                  | V <sub>O</sub> = 0 to 5.5 V,<br>V <sub>I</sub> = 0                                                          |     |                    | 1    | μA         |
| I <sub>CC</sub>                 |                   | V <sub>CC</sub> = 3.6 V,                                              | I <sub>I/O</sub> = 0,<br>Switch ON or OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND                         |     | 0.7                | 2    | mA         |
| ΔI <sub>CC</sub> <sup>(4)</sup> | Control inputs    | V <sub>CC</sub> = 3.6 V,                                              | One input at 3 V, Other inputs at V <sub>CC</sub> or GND                                                    |     |                    | 30   | μA         |
| I <sub>CCD</sub> <sup>(5)</sup> | Per control input | V <sub>CC</sub> = 3.6 V,<br>Control input switching at 50% duty cycle | A and B ports open,                                                                                         |     | 0.13               | 0.14 | mA/<br>MHz |
| C <sub>in</sub>                 | Control inputs    | V <sub>CC</sub> = 3.3 V,                                              | V <sub>IN</sub> = 5.5 V, 3.3 V, or 0                                                                        |     | 2.5                | 3.5  | pF         |
| C <sub>io(OFF)</sub>            |                   | V <sub>CC</sub> = 3.3 V,                                              | Switch OFF,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0              |     | 3.5                | 5    | pF         |
| C <sub>io(ON)</sub>             |                   | V <sub>CC</sub> = 3.3 V,                                              | Switch ON,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0               |     | 9                  | 11.5 | pF         |
| r <sub>on</sub> <sup>(6)</sup>  |                   | V <sub>CC</sub> = 2.3 V,<br>TYP at V <sub>CC</sub> = 2.5 V            | V <sub>I</sub> = 0, I <sub>O</sub> = 30 mA                                                                  |     | 4                  | 8    | Ω          |
|                                 |                   |                                                                       | V <sub>I</sub> = 1.7 V, I <sub>O</sub> = –15 mA                                                             |     | 4.5                | 9    |            |
|                                 |                   | V <sub>CC</sub> = 3 V                                                 | V <sub>I</sub> = 0, I <sub>O</sub> = 30 mA                                                                  |     | 4                  | 6    |            |
|                                 |                   |                                                                       | V <sub>I</sub> = 2.4 V, I <sub>O</sub> = –15 mA                                                             |     | 4.5                | 8    |            |

- (1) V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.  
(2) All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.  
(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.  
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.  
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).  
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER                                      | FROM<br>(INPUT)       | TO<br>(OUTPUT) | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ |      | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ |     | UNIT |
|------------------------------------------------|-----------------------|----------------|--------------------------------------------|------|--------------------------------------------|-----|------|
|                                                |                       |                | MIN                                        | MAX  | MIN                                        | MAX |      |
| $f_{OE}$ or $f_{\overline{OE}}$ <sup>(1)</sup> | OE or $\overline{OE}$ | A or B         |                                            | 10   |                                            | 20  | MHz  |
| $t_{pd}$ <sup>(2)</sup>                        | A or B                | B or A         |                                            | 0.12 |                                            | 0.2 | ns   |
| $t_{en}$                                       | OE or $\overline{OE}$ | A or B         | 1.5                                        | 7.7  | 1.5                                        | 6.5 | ns   |
| $t_{dis}$                                      | OE or $\overline{OE}$ | A or B         | 1                                          | 6.9  | 1                                          | 6.8 | ns   |

- (1) Maximum switching frequency for control input ( $V_O > V_{CC}$ ,  $V_I = 5 \text{ V}$ ,  $R_L \geq 1 \text{ M}\Omega$ ,  $C_L = 0$ )  
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

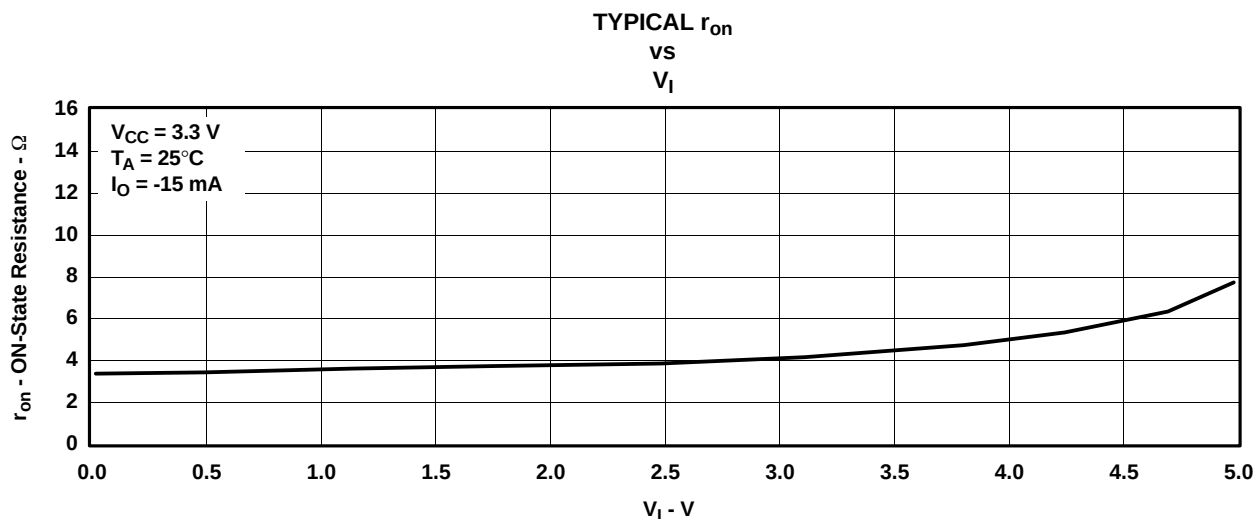


Figure 1. Typical  $r_{on}$  vs  $V_I$

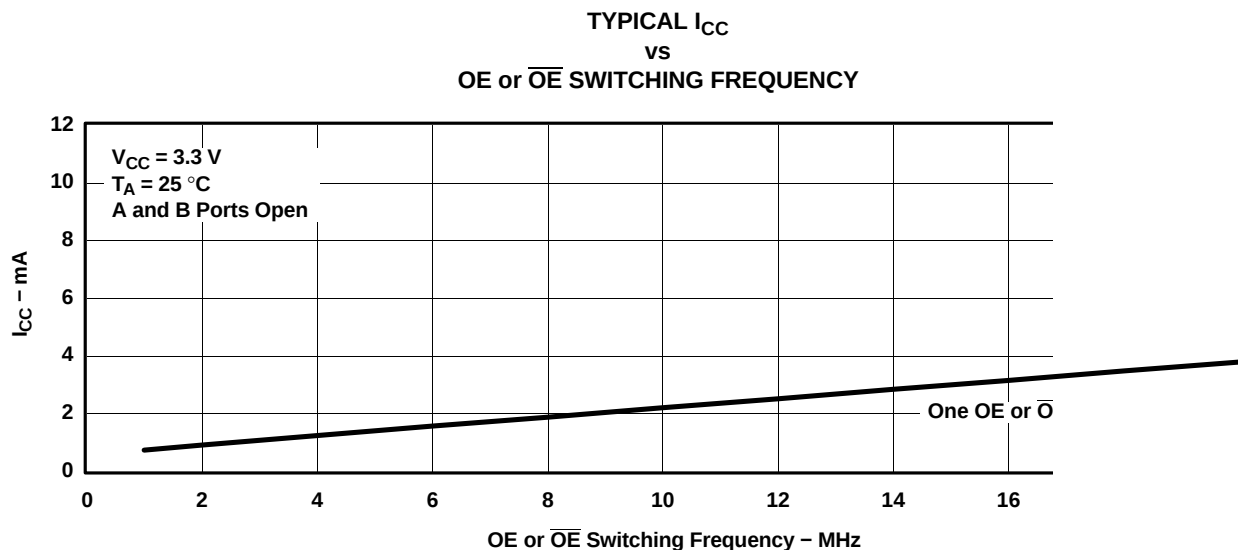
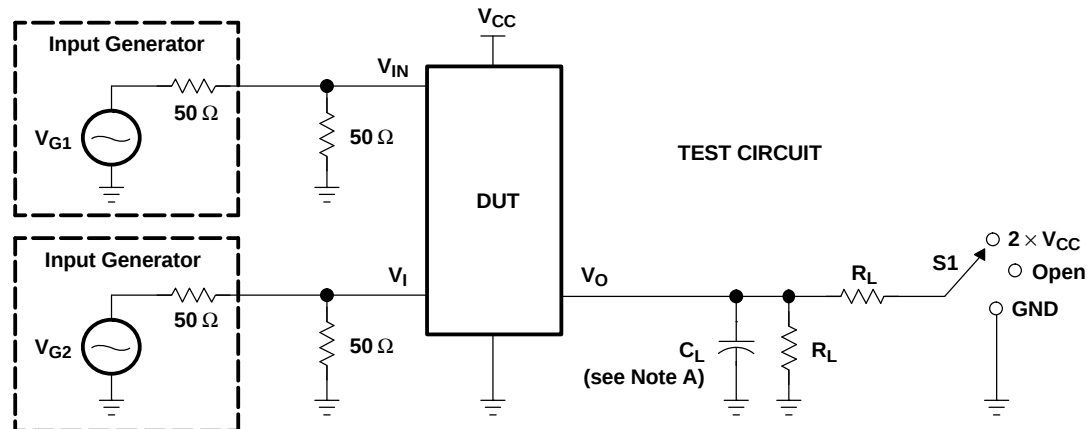
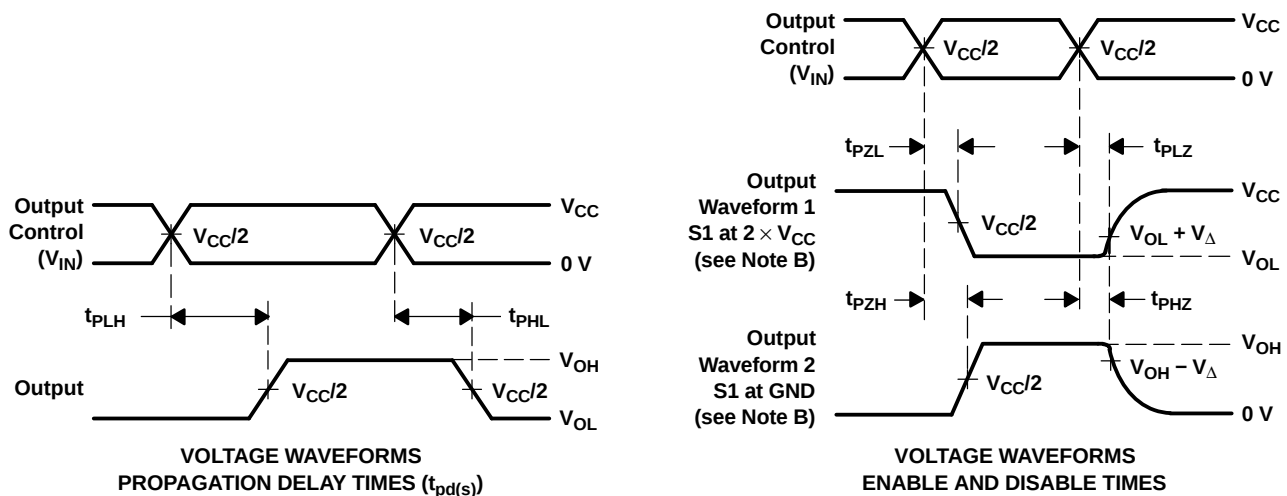


Figure 2. Typical  $I_{CC}$  vs OE or  $\overline{OE}$  Switching Frequency

## PARAMETER MEASUREMENT INFORMATION



| TEST                               | V <sub>CC</sub>                | S1                                         | R <sub>L</sub> | V <sub>I</sub>                                   | C <sub>L</sub> | V <sub>Δ</sub>  |
|------------------------------------|--------------------------------|--------------------------------------------|----------------|--------------------------------------------------|----------------|-----------------|
| t <sub>pd(s)</sub>                 | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | Open<br>Open                               | 500 Ω<br>500 Ω | V <sub>CC</sub> or GND<br>V <sub>CC</sub> or GND | 30 pF<br>50 pF |                 |
| t <sub>PLZ</sub> /t <sub>PZL</sub> | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | 2 × V <sub>CC</sub><br>2 × V <sub>CC</sub> | 500 Ω<br>500 Ω | GND<br>GND                                       | 30 pF<br>50 pF | 0.15 V<br>0.3 V |
| t <sub>PHZ</sub> /t <sub>PZH</sub> | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | GND<br>GND                                 | 500 Ω<br>500 Ω | V <sub>CC</sub><br>V <sub>CC</sub>               | 30 pF<br>50 pF | 0.15 V<br>0.3 V |



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74CB3Q3345DBQR | ACTIVE        | SSOP         | DBQ                | 20   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 85    | CB3Q3345                | <a href="#">Samples</a> |
| SN74CB3Q3345DGVR | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | BU345                   | <a href="#">Samples</a> |
| SN74CB3Q3345PW   | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | BU345                   | <a href="#">Samples</a> |
| SN74CB3Q3345PWR  | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | BU345                   | <a href="#">Samples</a> |
| SN74CB3Q3345RGYR | ACTIVE        | VQFN         | RGY                | 20   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 85    | BU345                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CB3Q3345DBQR | SSOP         | DBQ             | 20   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CB3Q3345DGVR | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3345PWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74CB3Q3345RGYR | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CB3Q3345DBQR | SSOP         | DBQ             | 20   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74CB3Q3345DGVR | TVSOP        | DGV             | 20   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CB3Q3345PWR  | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74CB3Q3345RGYR | VQFN         | RGY             | 20   | 3000 | 367.0       | 367.0      | 35.0        |

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G20)

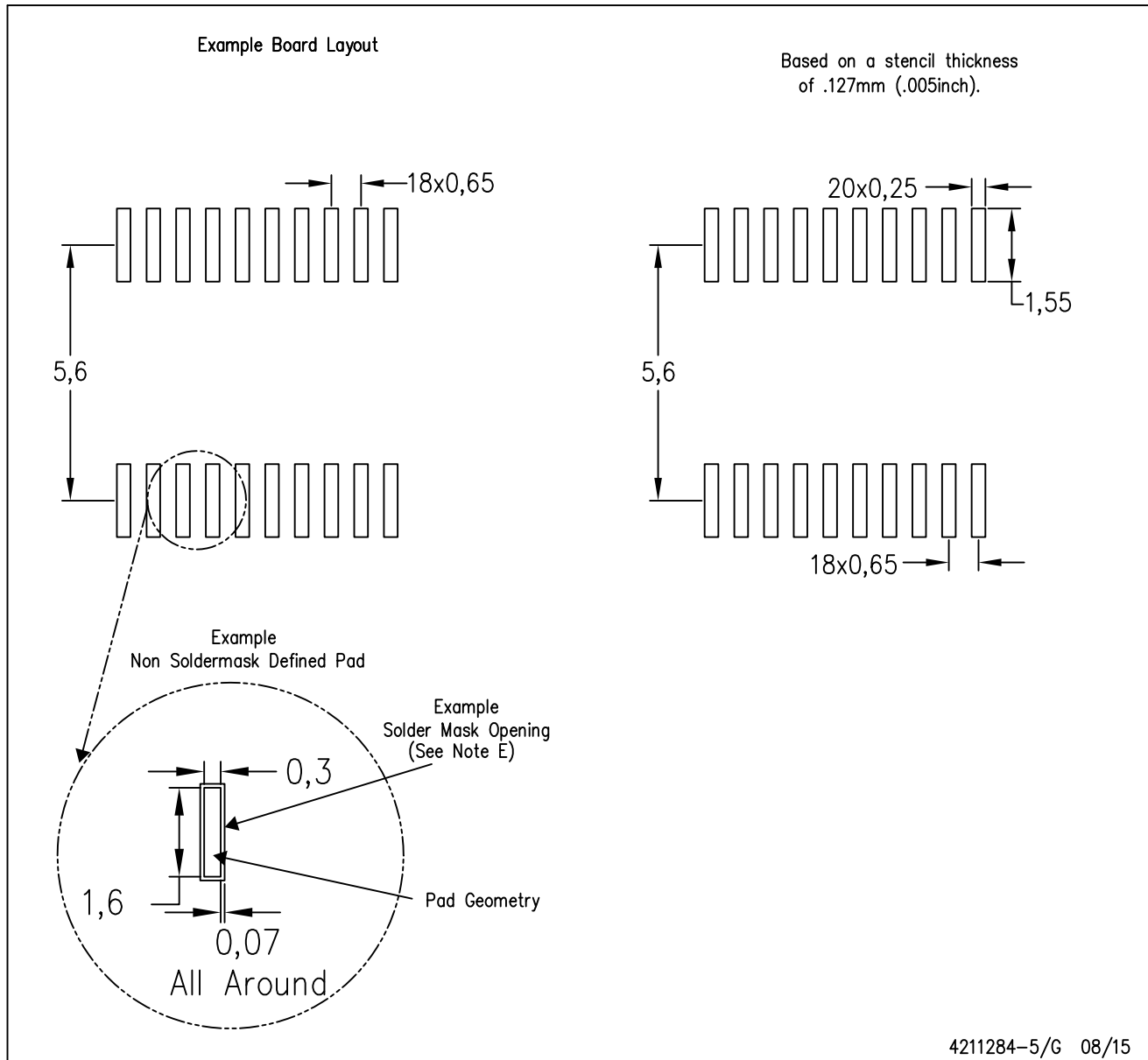
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## GENERIC PACKAGE VIEW

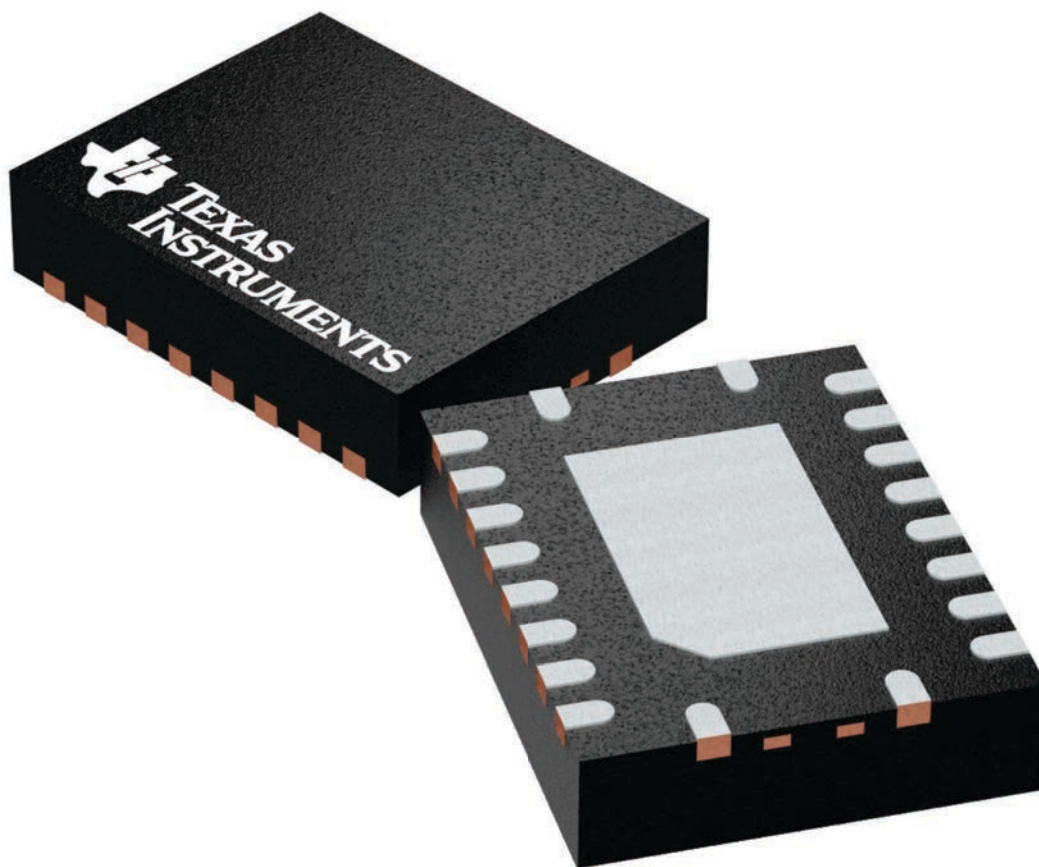
**RGY 20**

**VQFN - 1 mm max height**

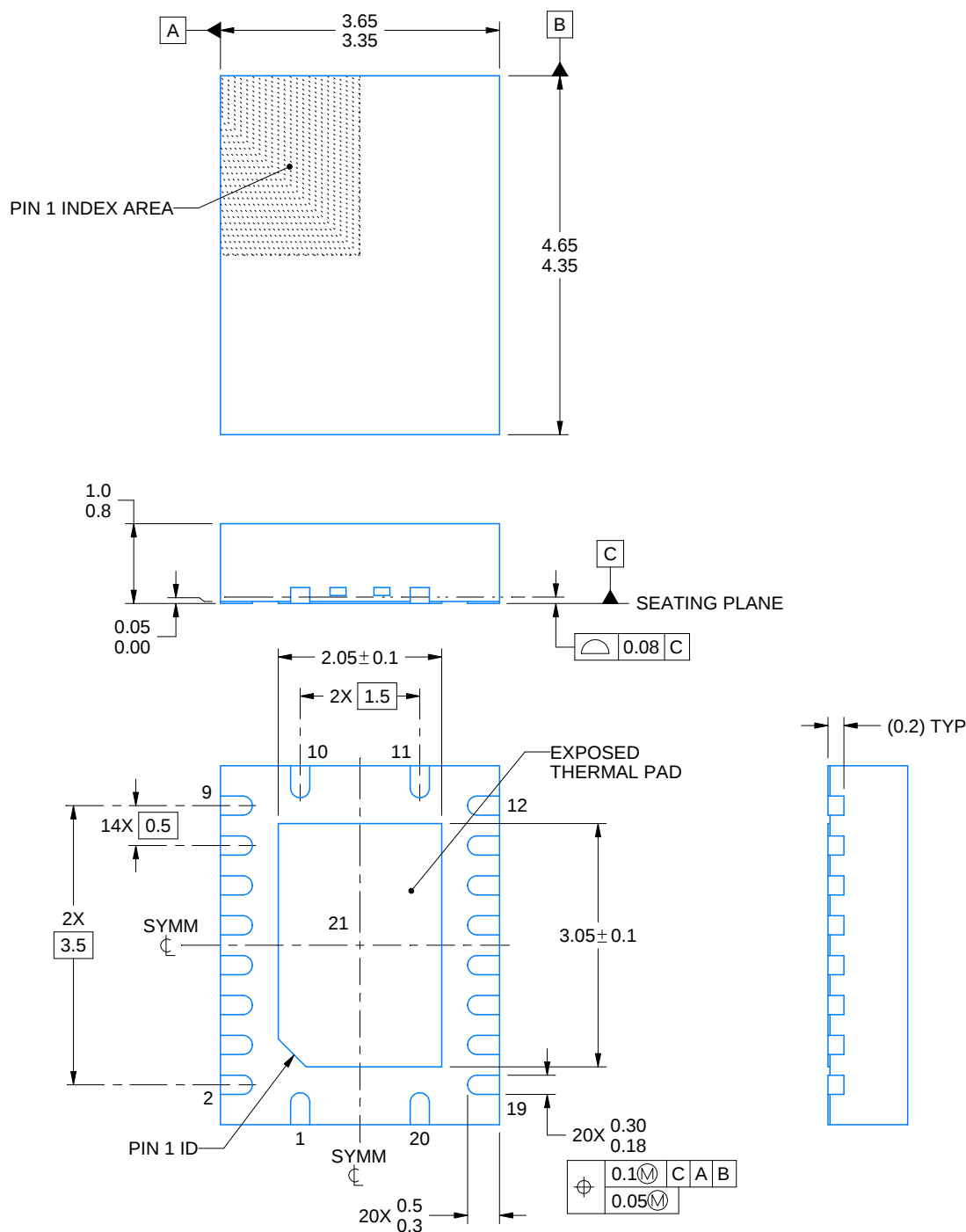
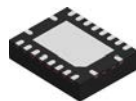
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



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NOTES:

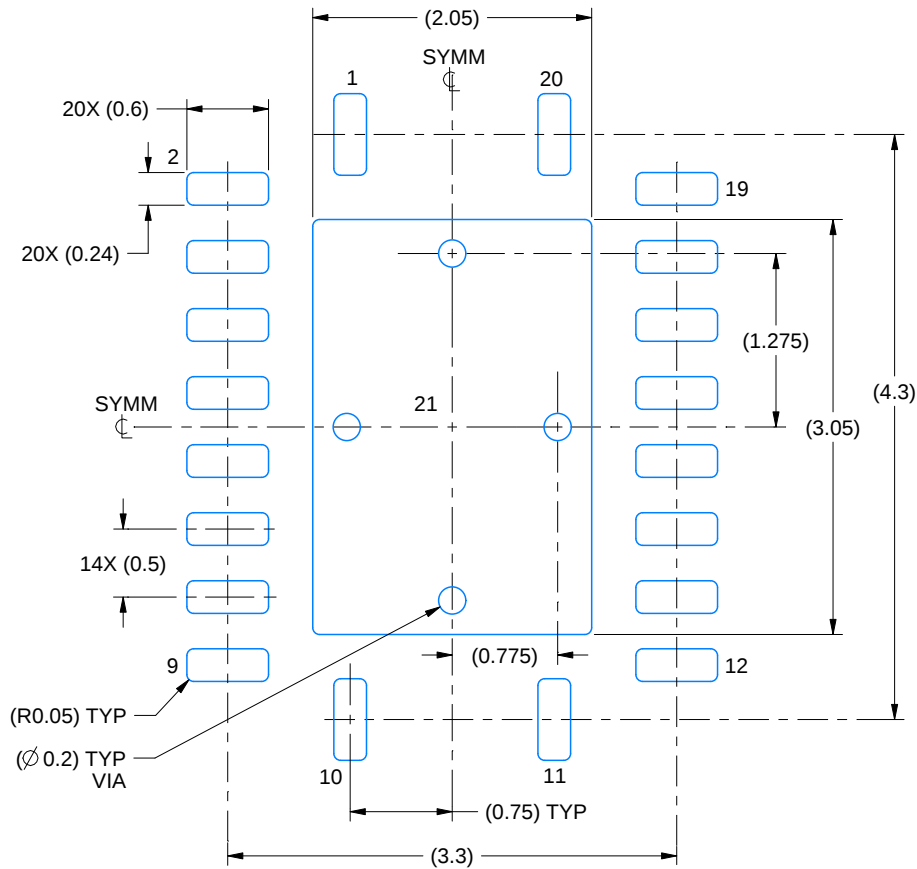
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

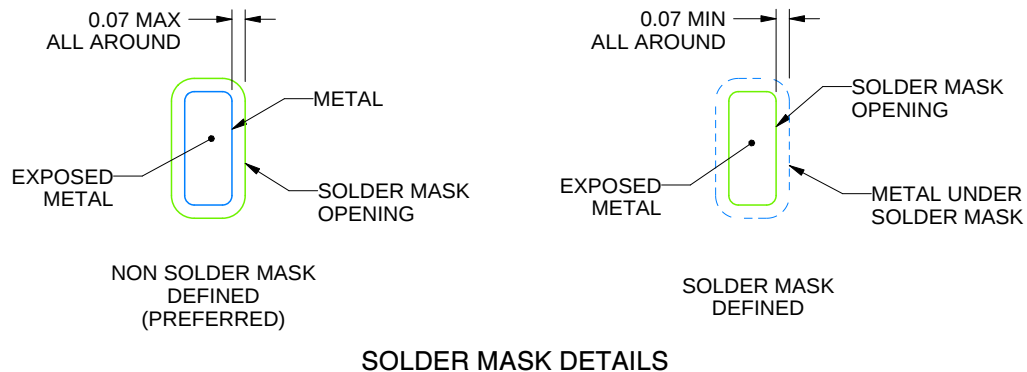
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



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NOTES: (continued)

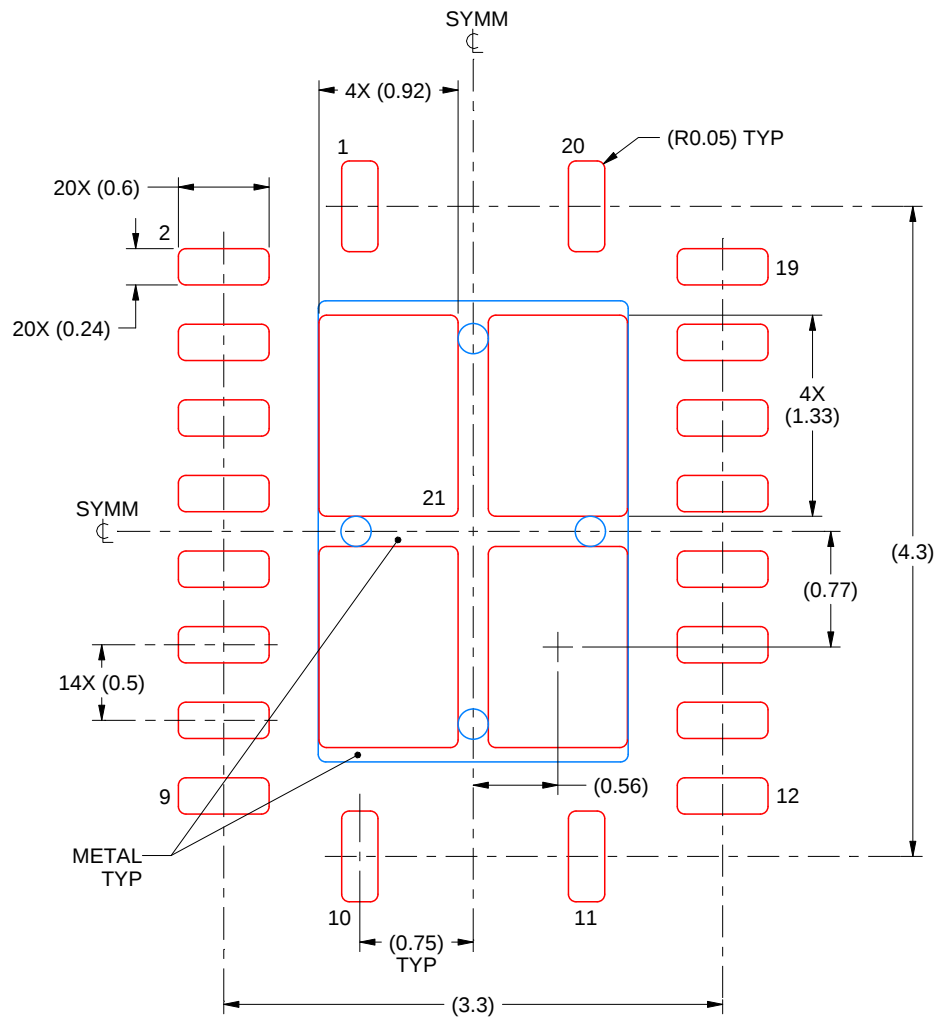
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

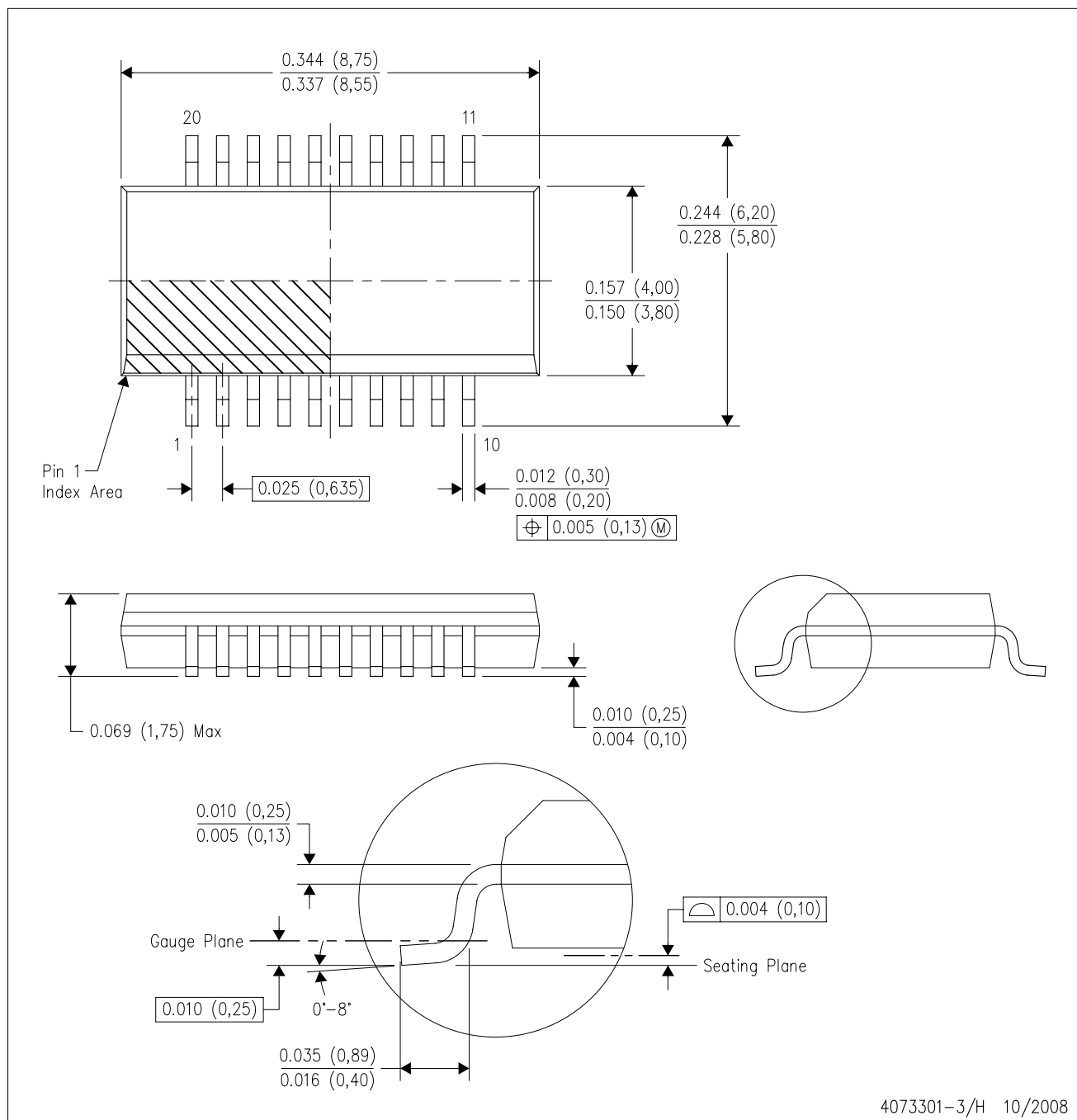
4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBQ (R-PDSO-G20)

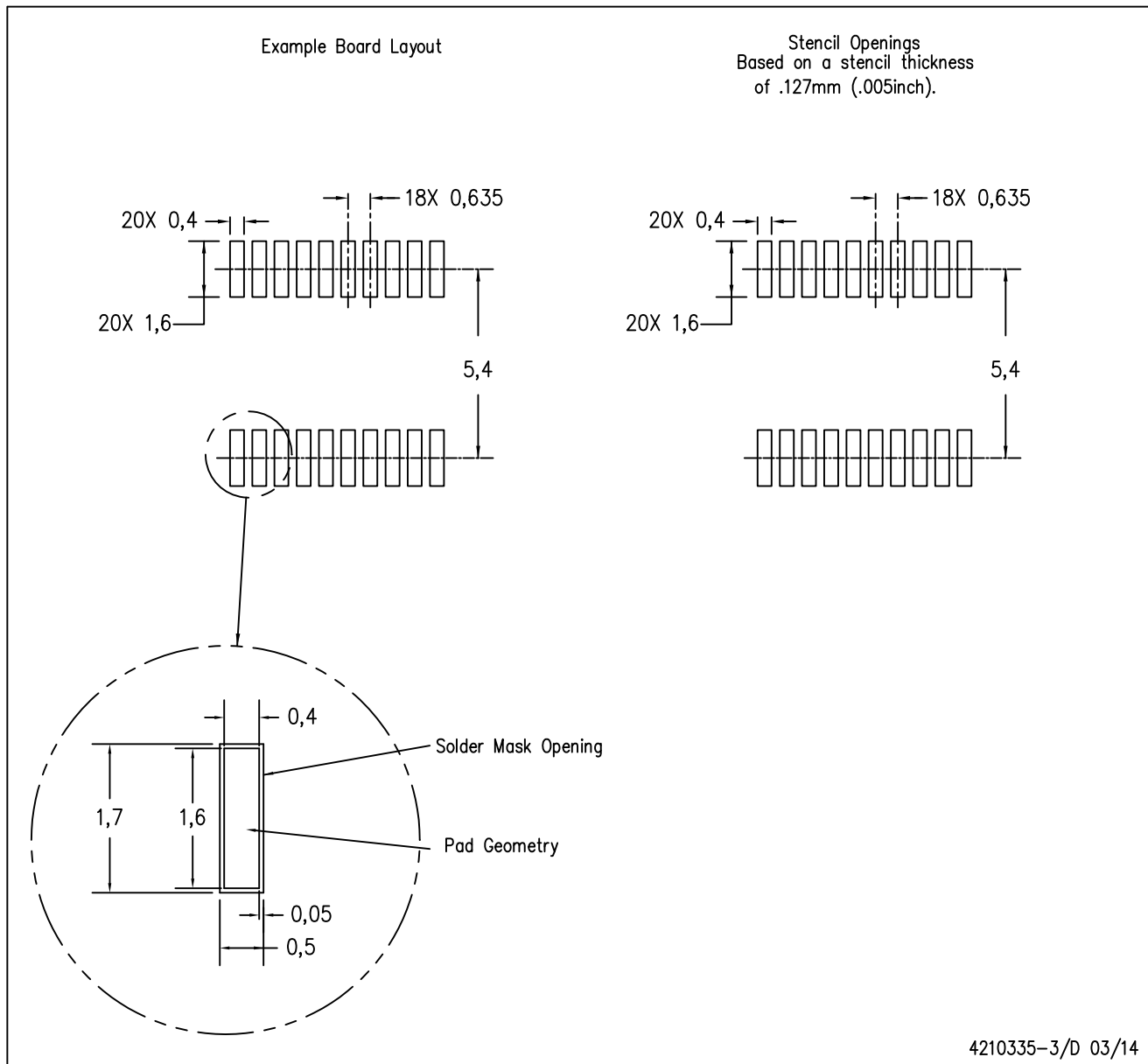
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AD.

DBQ (R-PDSO-G20)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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