SP701 Evaluation Board

User Guide

UG1319 (v1.0) July 12, 2019

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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
07/12/2019 Version 1.0	
Initial release.	N/A

Table of Contents

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Chapter 1

Introduction

Overview

The SP701 evaluation board is based on the XC7S100FGGA676 device, a member of the Xilinx® 7 series FPGA family. It is optimized for low cost, low power, and high I/O performance. It comes with advanced high-performance FPGA logic based on real6-input look up table (LUT), 36 Kb dual-port block RAM, support for DDR3L interface up to 1866 Mb/s, XADC with 12-bit 1 MSPA ADC with on-chip thermal and supply sensors, and powerful clock management tiles (CMTs). The board is designed for high-performance and lower power with a 28 nm, 1V core voltage process. For lower power, it has a 0.9V core voltage option.

Table 1: **XC7S100 Resources**

Spartan®-7 FPGA Resources	Component			Features
Logic Resources	Part Number			XCS7100
	Logic Cells			102,400
	Slices			16,000
	CLB Flip-flops			128,000
Memory Resources	Max. Distributed RAM (Kb)			1,100
	Block RAM/FIFO w/EEC (36 Kb each)			120
	Total Block RAM (Kb)			4,320
Clock Resources	Clock Mgmt. Tiles (1 MMCM + 1 PLL)			8
I/O Resources	Max. Single-Ended I/O Pins			400
	Max. Differential I/O Pins			192
Embedded Hard IP Resources	DSP Slices			160
	Analog Mixed Signal (AMS)/XADC			1
	Configuration AES/HMAC Blocks			1
Speed Grades	Commercial Temp (C)			-1, -2
	Industrial Temp (I)			-1, -2, -1L
	Expanded Temp (Q)			-1
	Package	Body Area (mm)	Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ technology HR I/O
	FGGA676	27 x 27	1.0	400

The following table lists the models for this board. See the SP701 evaluation board product page for details.

Table 2: **Models of SP701 Boards**

Kit	Description
EK-S7-SP701-G	Xilinx Spartan-7 FPGA SP701 Evaluation Kit
EK-S7-SP701-G-J	Xilinx Spartan-7 FPGA SP701 Evaluation Kit, Japan Specific

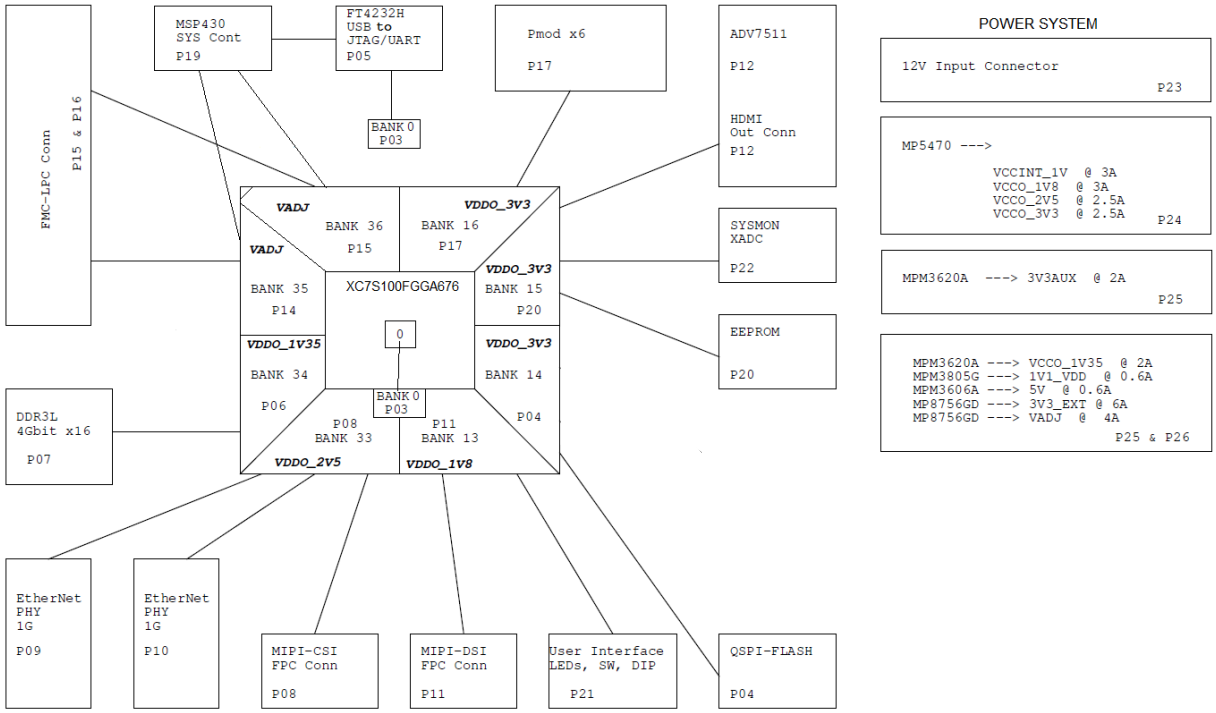
Additional Resources

See Appendix D: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the SP701 evaluation board.

Block Diagram

The following figure shows the various components of the SP701 Evaluation Board.

Figure 1: **SP701 Evaluation Board Block Diagram**



Board Features

The SP701 evaluation board features are listed here. Detailed information for each feature is provided in Chapter 3: Board Component Descriptions.

- XC7S100-2FGGA676 package
- Form factor: 6.00 in (152.4 mm) square, 0.08844 in (88.44 mils) thick
- Configuration:
  - Quad SPI (QSPI) 1 Gb
  - Direct QSPI flash program header
  - USB-to-JTAG bridge
- DDR3L SDRAM memory:
  - 256Mx16 4 Gb DDR3-1866
- 32 Kb I2C EEPROM for hardware ID storage accessible by FPGA and System Controller
- Clocks:
  - I2C programmable SYSCLK oscillator 33.33 MHz
- VITA 57.1 FMC-LPC connector:
  - 34 differential pairs or 68 single-ended LA[00-33] bus
- 2x 10/100/1000 Tri-Speed Ethernet PHY
- Mobile industry processor interface (MIPI) features:
  - MIPI-CSI Camera Serial Interface (for PCAM 5C from Digilent)
  - MIPI-DSI Display Serial Interface
- HDMI output (1.4 specification support)
- USB-UART interface:
  - FT4232H JTAG/3xUART
- System Controller (MSP430)
- I2C Bus
- 6x Pmod rt-angle receptacle (Digilent Pmod IF 1.2.0 specification support)
- General purpose I/O (GPIO):
  - 8x LED (GPIO_LED[0:7]) (active-High)
  - 5x pushbutton switch, geographical, GPIO_SW_[N,E,S,W,C] (active-High)

- 1x pushbutton switch, CPU_RESET (active-High)
- 2x 8-pole DIP switch, GPIO_DIP_SW_B[0:15] (active-High)

- Operational Switches:
  - Power On-Off slide switch
  - PROG_B pushbutton switch (active-Low)
  - 4-pole configuration mode DIP switch M[0:2]_0_SW, INIT_B_0 (active-Low)
- Operational Status LEDs:
  - Done
  - Power On
  - PG (Power Good)
- Power System:
  - V_{ccint} 0.90V or 1.00V (I2C selectable)
  - I2C telemetry on 12V input and V_{ccint}

Board Specifications

Dimensions

- Height: 6.00 in (152.4 mm)
- Width: 6.00 in (152.4 mm)
- Thickness: 0.08844 in (88.44 mils)

***Note*:** A 3D model of this board is not available.

See the SP701 board website documentation tab (Board Files check box) for the XDC listing and board schematics (0381874).

Environmental

- Temperature
  - Operating: 0°C to +45°C
  - Storage: –25°C to +60°C
- Humidity
  - 10% to 90% non-condensing

Operating Voltage

- $+12V_{DC}$

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Chapter 2

Board Setup and Configuration

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

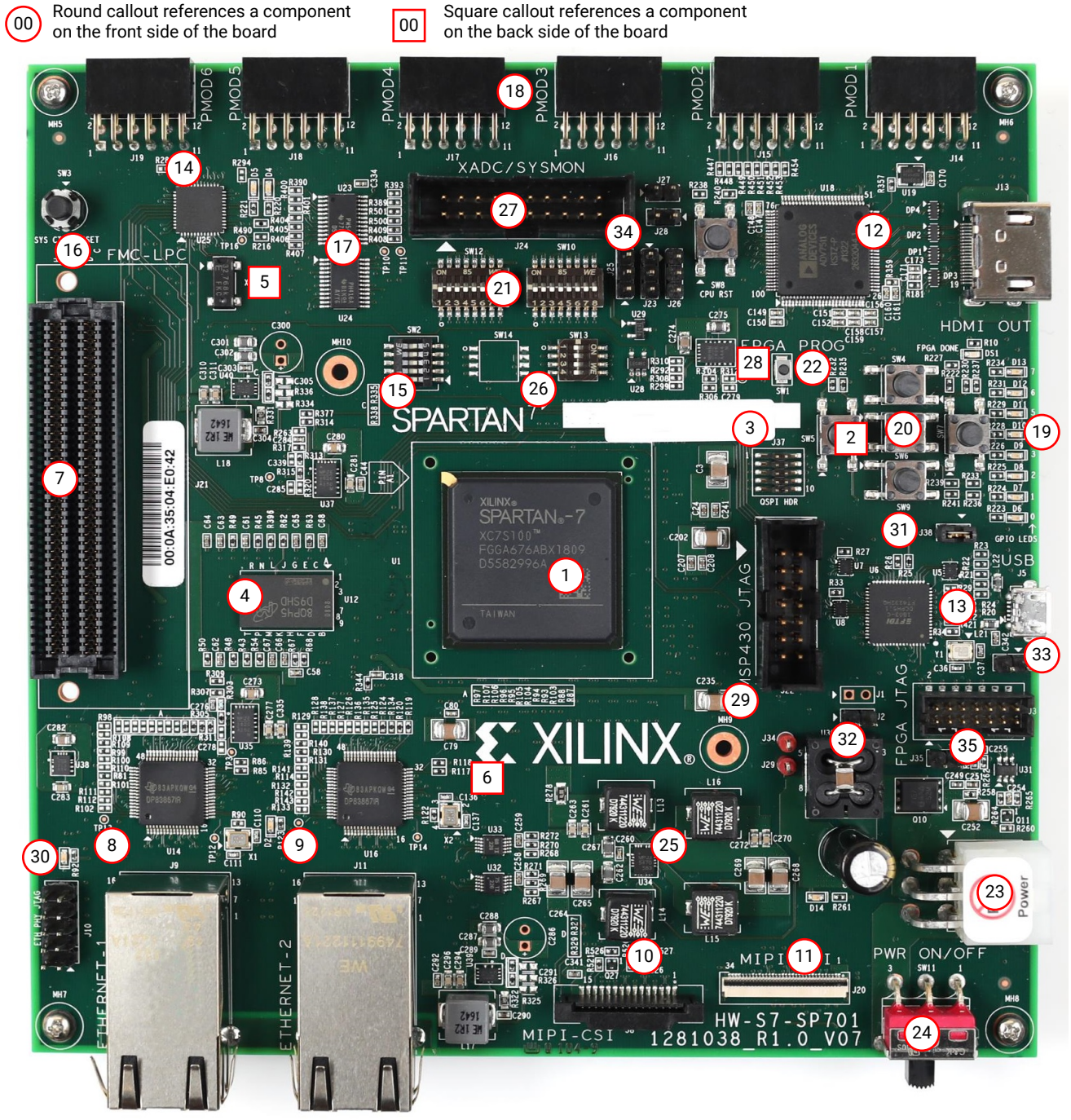
- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx® Product Support, place it back in its antistatic bag immediately.

Board Components

The following figure shows the SP701 board component locations. Each numbered component is keyed to the table in Board Component Location.

IMPORTANT! *The following figure is for visual reference only and might not reflect the current revision of the board. There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific SP701 version of interest for such details.*

Figure 2: **SP701 Evaluation Board Components**



Board Component Location

The following table identifies the components, references the respective schematic (0381874) page numbers, and links to a detailed functional description of the components and board features in Chapter 3: Board Component Descriptions.

Table 3: **Board Component Locations**

Callout	Feature [#] = Bottom	Notes	Schematic Page Number
1	Spartan-7 XC7S100 FPGA (U1)	XC7S100-2FGGA676C	
2	1Gb QSPI Flash 4-bit [U3]	Micron MT25QL01GBBB8ESF-0SIT	4
3	Direct QSPI Flash Program Header (J37) 2X5 1.27 mm pitch male header	Samtec FTSH-105-01-F-DV	3
4	DDR3L Component Memory (U12)	Micron MT41K256M16TW	7
5	IIC EEPROM [U27]	ST Microelectronics M24C32-WDW6	8
6	I2C Programmable Clock, LVDS [U45]	Silicon Labs SI570BAB000875DG (default 33.3333 MHz)	8
7	FMC LPC Connector J21	Samtec ASP-134603-01	15-16
8	10/100/1000 Mb/s Tri-speed Ethernet PHY (RGMII) with RJ45, SGMII mode only (U14), (J9)	TI DP83867IRPAP with Wurth 7499111221A RJ45 (with magnetics)	9
9	10/100/1000 Mb/s Tri-speed Ethernet PHY (RGMII) with RJ45, SGMII mode only (U16), (J11)	TI DP83867IRPAP with Wurth 7499111221A RJ45 (with magnetics)	10
10	MIPI-CSI Camera Serial Interface (J8)	TE Connectivity 1-1734248-5	8
11	MIPI-DSI Display Serial Interface (J20)	Hirose FH34SJ-34S-0.5SH	11
12	HDMI Video Output (U18), (J13)	Analog Devices ADV7511KSTZ, Molex 47151-1001	12,13
13	USB UART Interface, USB bridge (U6) with micro-AB USB connector (J5), and 2x7 2 mm keyed program cable connector (J3)	FTDI FT4232HQ_QFN64, Hirose ZX62D-AB-5P8(30), Molex 87832-1420	3, 5
14	System Controller MSP430 (U25)	TI MSP430F5342IRGZ	19
15	System Controller MSP430 4-pole GPIO DIP switch (SW2)	Wurth 416131160804	19
16	System Controller MSP430 reset pushbutton (SW3, active-Low)	Panasonic EVQ-11L07K	19
17	I2C Bus Switch (U23) I2C_MSP430 Bus Port Expander (U24)	TI TCA9548A TI TCA6416A	19
18	PMOD Interface 6x 2x6 Rt-Angle receptacles (J14-J19)	Sullins PPPC062LJBN-RC	17
19	User 8x LEDs, Green, active-High (D6-D13)	Lumex SML-LX0603GW-TR	21
20	User 6x pushbutton, active-High (SW4-SW9)	E-Switch TL3301EF100QG	21
21	User 2x 8-pole DIP switch, 1.27 mm pitch, active-High (SW10, SW12)	Wurth 416131160808	21
22	FPGA Program pushbutton, (SW1), active-Low	Omron B3U-1000P	3
23	Power Input Connector, 2x6 (J30)	Molex-39-30-1060	23
24	Power On/Off Slide Switch (SW11)	C&K 1101M2S3AQE2	23
25	SP701 Board Power System, MPS (top and bottom)	Monolithic Power Systems (MPS)	24-26

Table 3: **Board Component Locations** *(cont'd)*

Callout	Feature [#] = Bottom	Notes	Schematic Page Number
26	Configuration options, FPGA U1 configuration mode 4-pole DIP switch, (SW13)	Wurth 416131160804	3
27	XADC/SYSMON 2x10 shrouded/keyed Header (J24)	Samtec TST-110-01-G-D	22
28	Encryption Key Battery Backup Circuit Battery retainer [B1]	Keystone 2998	3
29	System Controller MSP430 2x7 0.1" JTAG Header (J22)	Tyco 5103308-2	19
30	Ethernet 1x4 0.1" JTAG header (J10)	Sullins PBC36DAAN	9

Default Switch and Jumper Settings

Jumpers

Default jumper settings are listed in the following table. The table also references the respective schematic (0381874) page numbers.

Table 4: **Default Jumper Settings**

Callout	Jumper	Type	Function	Default	Schematic Page Number
31	J38	2-pin male header	USB JTAG enable	Jumper ON	5
32	J2	2-pin male header	FPGA U1 CFGBVS_0	Jumper OFF	3
33	J6	2-pin male header	FT4232 U6 SUSPEND	Jumper OFF	5
34	J23	3-pin male header	FPGA U1 XADC_VCC Select	2-3	22
34	J25	3-pin male header	REF3012 U29 V_{in} Select	1-2	22
34	J26	3-pin male header	FPGA U1 XADC_VREFP Select	1-2	22
34	J27	2-pin male header	GND-to-J28/L12	Jumper ON	22
34	J28	2-pin male header	J28/L12-to-XADC_GND	Jumper OFF	22
35	J35	2-pin male header	Power System Inhibit	Jumper OFF	23

Switches

Default switch settings are listed in the following table. The table also references the respective schematic (0381874) page numbers.

Table 5: **Default Switch Settings**

Callout	Switch	Type	Function	Default	Schematic Page Number
15	SW2	5-pole DIP	MSP430 U25 GPIO	OFF, OFF, OFF, OFF, OFF	19
21	SW10	8-pole	FPGA U1 GPIO	All OFF	21
21	SW12	8-pole	FPGA U1 GPIO	All OFF	21
26	SW13	4-pole DIP	FPGA U1 Configuration:	OFF, ON, OFF=101 OFF	3
			Switch OFF = 1 = High; ON = 0 = Low		
			Mode = SW13[4:2] = Mode[2:0]		
			JTAG: SW13[4:2] = OFF, ON, OFF = Mode[101]		
			MASTER SPI: SW13[4:2] = ON, ON, OFF = Mode[001]		
			SW13[1] = INIT_B, OFF = OPEN, ON = 0 = Low		

Spartan-7 Device Configuration

The SP701 board supports two of the 7 series FPGA configuration modes:

- Master SPI flash memory using the onboard QSPI flash memory
- JTAG
  - J5 micro-AB USB-JTAG interface connector
    - USB A-to-micro-B PC to SP701 cable connection
  - J3 2x7 2 mm keyed JTAG pod flat cable header
    - Platform cable USB II/Parallel cable IV type connection

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in the following table.

The mode switches M2, M1, and M0 are on SW13 positions 4, 3, and 2, respectively.

Table 6: **SP701 Board FPGA Configuration Modes**

Configuration Mode	SW13 Switch Settings M[2:0]
Master SPI	001
JTAG (default)	101

See Table 5, callout 26 SW13 for more information on the switch position.

JTAG

Vivado® design tools, Xilinx® SDK, or third-party tools can establish a JTAG connection to the Spartan-7 device through the FTDI FT4232 USB-to-JTAG/USB UART device (U6) connected to the micro-USB connector (J5).

To use the JTAG pod cable with the FTDI used for the UART only on J5, remove the jumper from J38 when using the PC4/USB cable for JTAG.

To use the FPGA programming tools to detect the JTAG chain and program the FPGA, connect the PC4/USB JTAG pod flat cable to the 2x7 2 mm keyed shrouded connector J3.

Quad SPI

To boot from the QSPI nonvolatile configuration memory, use the following procedure:

1. Store a valid Spartan-7 boot image in the SPI flash device. See the *7 Series FPGAs Configuration User Guide* (UG470) for information on programming the SPI.
2. Set the boot mode pins SW13 [4:2] MODE[2:0] as indicated in the table in Spartan-7 Device Configuration for Master SPI.
3. Power-cycle the SP701 board. SW13 is callout 30 in Board Components.

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Chapter 3

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the components and features of the SP701 board. Board Component Location identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Board Components.

Component Descriptions

Spartan-7 XC7S100 FPGA

[Figure 2, callout 1]

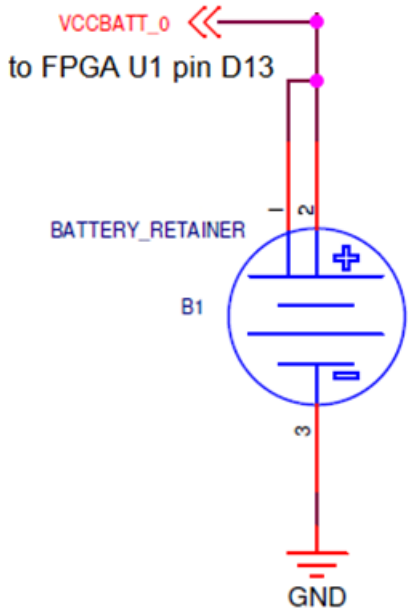
A Spartan-7 XC7S100-2FGGA676C FPGA is installed on the SP701 evaluation board. The Spartan-7 family is optimized for low cost, lowest power, and high I/O performance.

For further information on Spartan-7 FPGAs, see *7 Series FPGAs Data Sheet: Overview* (DS180).

Encryption Key Battery Backup Circuit

The XC7S100 FPGA U1 implements bitstream encryption key technology. The SP701 board provides the encryption key backup battery circuit shown in the following figure.

Figure 3: **Encryption Key Backup Circuit**



The Keystone 2998 battery retainer B1 is soldered to the board with the positive output connected to the FPGA U1 VCC_PSBATT pin D13. The B1 retainer accepts a 6.8 mm 1.5V single-cell, coin type battery similar to Seiko part number SR621SW, silver oxide, 1.55V non-rechargeable battery.

Bank Voltage Rails

The XC7S100 FPGA U1 bank voltages are listed in the following table.

Table 7: **FPGA U1 Bank Voltage Rails**

XC7S100 U1 Bank	Power Net Name	Voltage	Connected To
0	VCCO_3V3	3.3V	FPGA Configuration I/F
13	VCCO_1V8	1.8V	MIPI_DSI, GPIO Switches, FT4232_C_UART, I2C3_DSI Bus
14	VCCO_3V3	3.3V	FLASH_SPI, FT4232_B_UART
15	VCCO_3V3	3.3V	HDMI Out, I2C4_HDMI Bus, GPIO LEDs, XADC I/F
16	VCCO_3V3	3.3V	PMOD[1:6] I/F
33	VCCO_2V5	2.5V	Ethernet PHY 1/2 I/F, MIPI_CSI, I2C2_CAM
34	VCCO_1V35	1.35V	DDR3L I/F
35	VADJ	1.8V (nom), 3.3V, 2.5V	LPC FMC I/F, MPS430_GPIO
36	VADJ	1.8V (nom), 3.3V, 2.5V	LPC FMC I/F, MPS430_GPIO

DDR3L Component Memory

[Figure 2, callout 4]

The 4 Gb, 16-bit wide DDR3L memory system is comprised of one 4 Gb x 16 SDRAM U12.

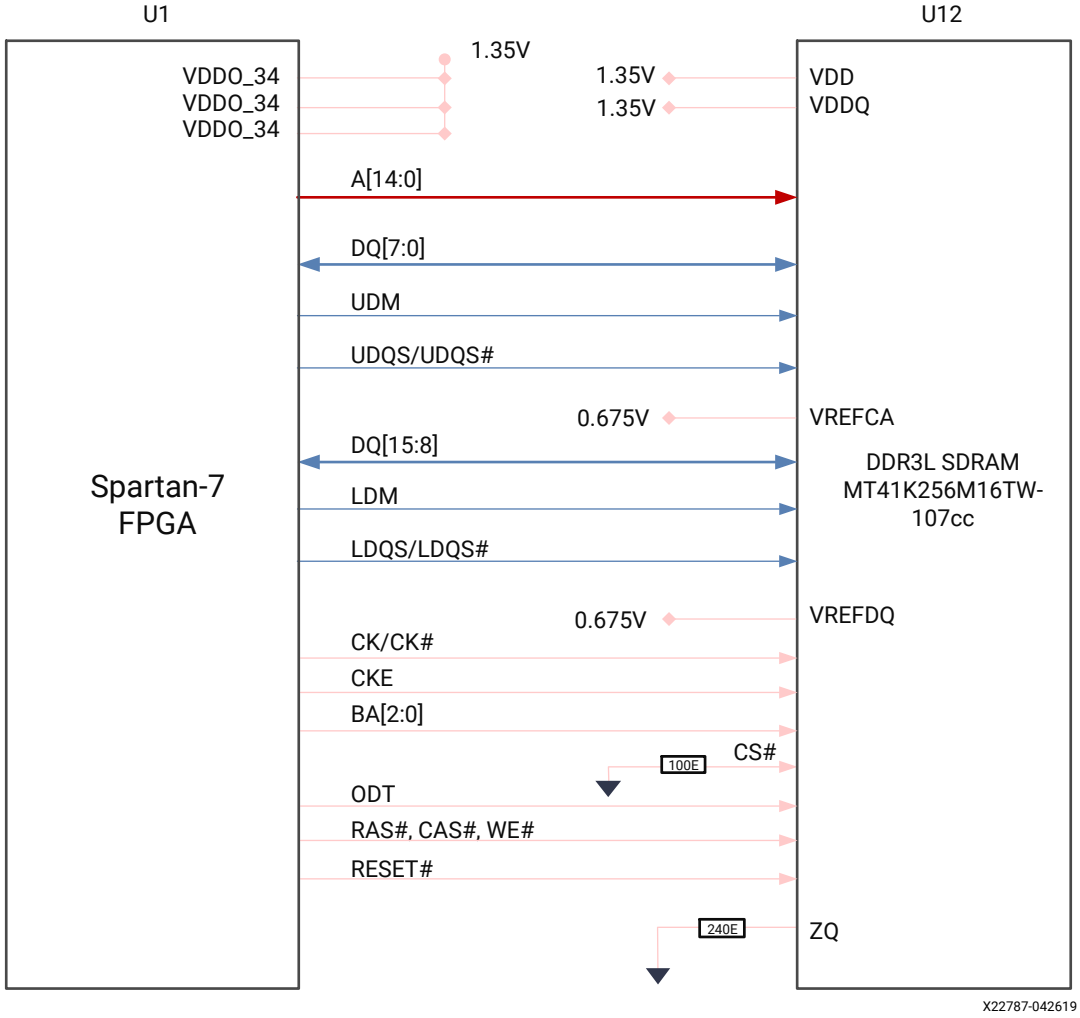
- Manufacturer: Micron
- Part Number: MT41K256M16TW-107:P
- Description:
  - 4 Gb (256 Mb x 16)
  - 1.35V 96-ball TFBGA

The Spartan-7 DDR interface performance is documented in the *Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS189).

This memory system is connected to FPGA U1 bank 34. The DDR3L 0.675V VTT termination voltage is supplied from MP20073DH regulator U13.

The following figure shows the DDR3L memory interface.

Figure 4: **DDR3L Memory Interface**



For more details, see the Micron MT41K256M16TW-107 data sheet at the Micron Technology website.

The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints. For more information, see the *Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions* (UG586).

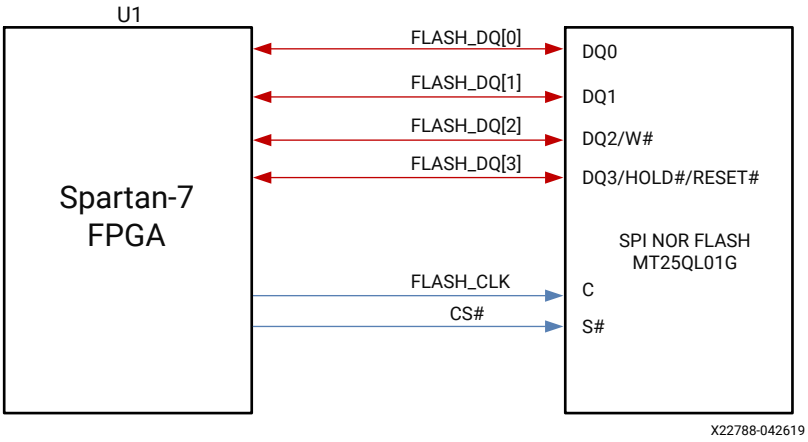
Quad SPI Flash Memory

[Figure 2, callout 2]

A single Micron MT25QL01GBBBESF-0SIT 1 Gb serial NOR Flash memory (U3) holds the boot images for the XC7S100 device. The Spartan-7 configuration clock is 66 MHz resulting in a typical configuration time of 112 ms. This memory can also be used for user data.

The following figure shows the configuration flash memory interface.

Figure 5: **Configuration Flash Memory Interface**



The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

SP701 JTAG Chain

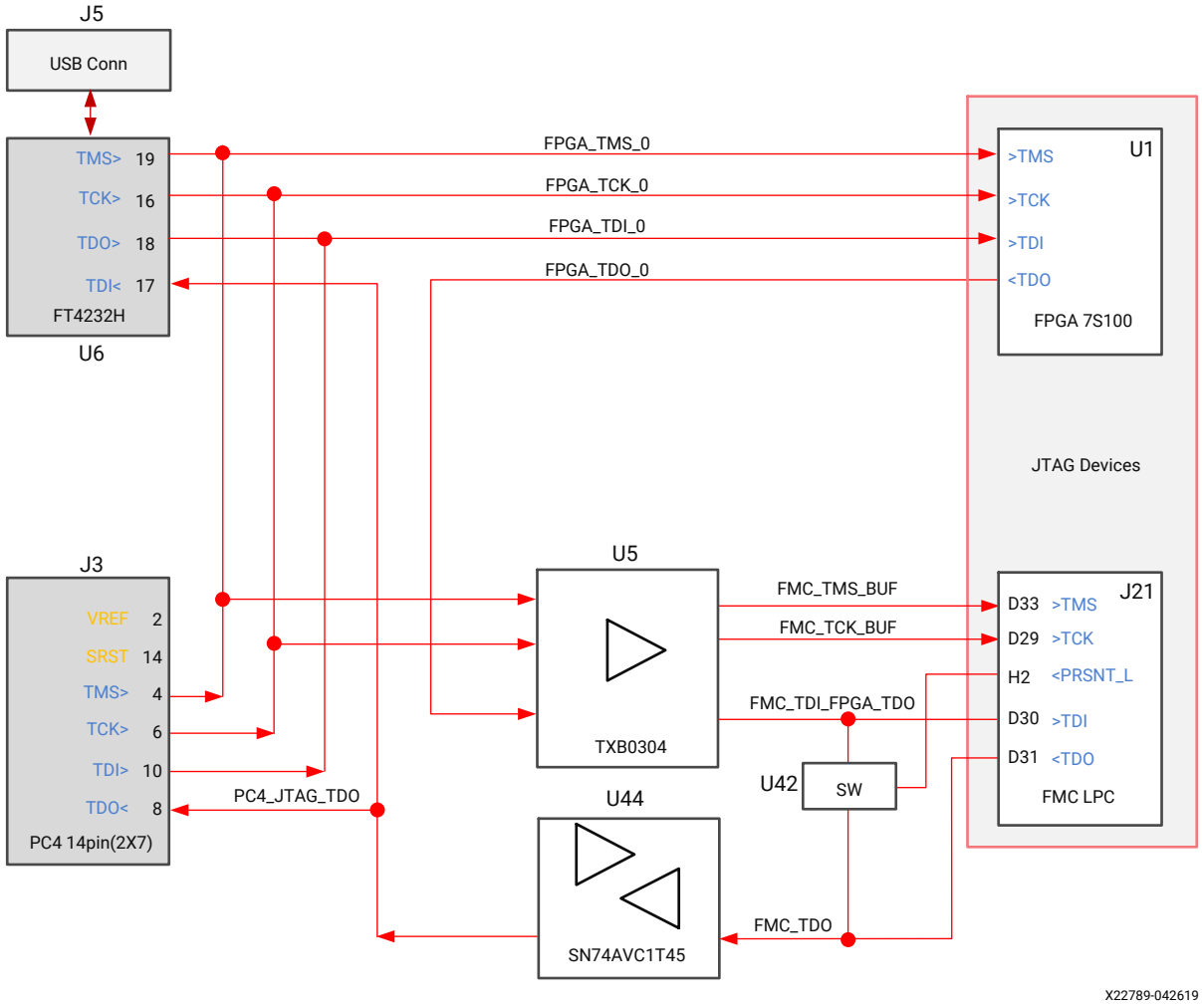
[Figure 2, callout 13]

The SP701 JTAG chain has the following components:

- J5 USB micro-AB connector connected to U6 FT4232HQ USB-JTAG bridge
- U1 XCS700 FPGA
- J21 FMC LPC connector
- J3 2x7 2 mm shrouded, keyed JTAG pod flat cable connector

The SP701 board JTAG chain is shown in the following figure.

Figure 6: **SP701 JTAG Chain**



FMC LPC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to J21, it is automatically added to the JTAG chain through an electronically controlled single-pole single-throw (SPST) switch, U42. The SPST switch is normally closed and transitions to an open state when an FMC is attached. Switch U42 adds an attached FMC to the JTAG chain as determined by the FMC_PRSNT_M2C_L signal. The attached FMC card must implement a TDI-to-TDO connection using a device or bypass jumper to ensure that the JTAG chain connects to the U1 XC7S100 FPGA.

The U5 TXBN0304 translator between the U6 FTDI JTAG/UART interface and the J3 JTAG pod flat cable connector J3 is normally not enabled (2-pin U5 enable header J38 jumper off) as the USB JTAG function using USB connector J5 is typically in use. To use the J3 JTAG pod flat cable connector, remove the J5 USB cable and install a jumper on 2-pin header J38.

Clock Generation

The SP701 board provides an I2C programmable (10 MHz – 810 MHz) Si570 oscillator (U45) to source the 200 MHz default SYSCLK. The U45 (I2C address `0x5D`) I2C02_SYSOSC bus is connected to U23 TCA9548A main I2C0 bus switch channel 1. The U45 Si570 LVDS output is connected to FPGA U1 bank 33 MRCC pins AE8 (P) and AE7 (N). See the I2C Bus Topology section for U45 programming setup information.

The following table lists the clock types on the SP701 board.

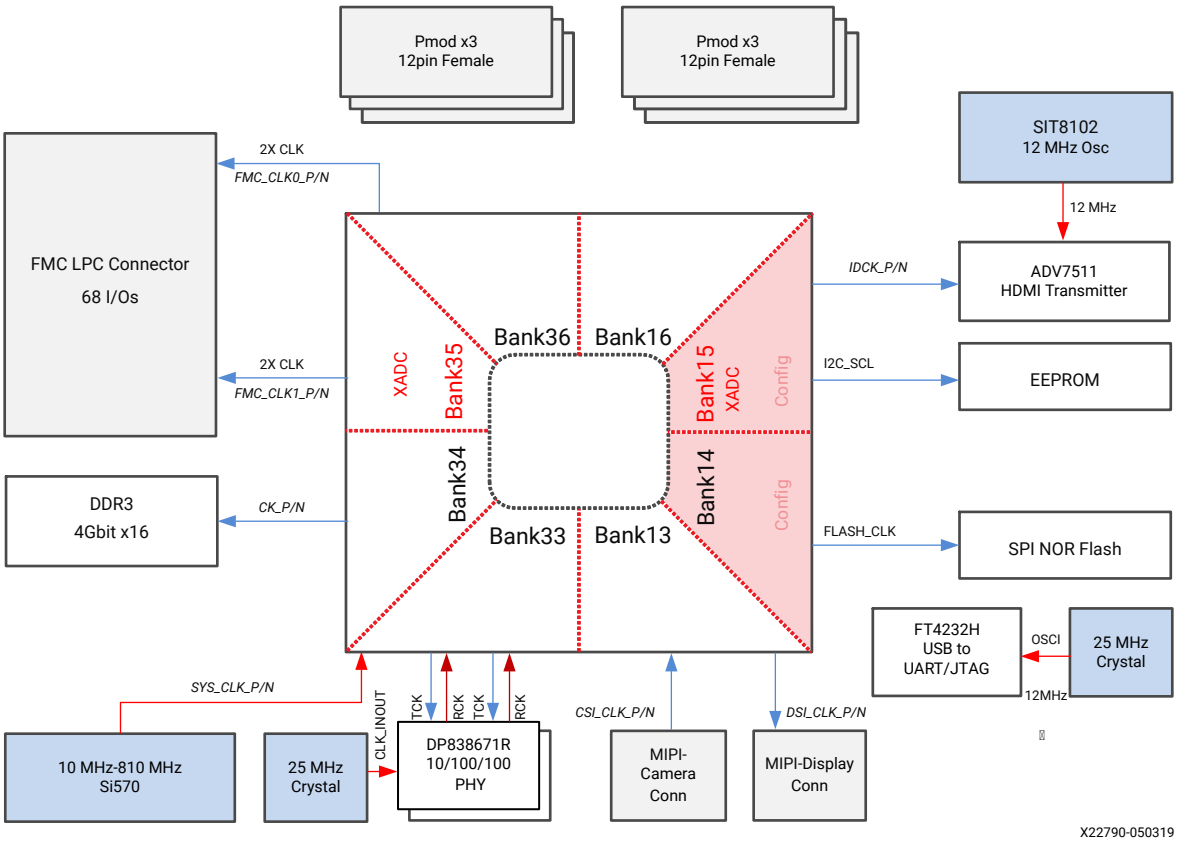
Table 8: **SP701 Clocks**

Clock	Direction	Frequency	I/O Standard	Bank
SYS_CLK	In to FPGA from Si570	33.3333 MHz	LVDS	Bank 33, MRCC
DDR3L CK	Out from FPGA to DDR3L	400 MHz - 800 MHz	DIFF_SSTL15	Bank 34, DQS
ETH1/2_GTX_CLK	Out from FPGA to DP83867IR	125 MHz	LVCMOS_33	Bank 33, SE I/O
ETH1/2_RX_CLK	In to FPGA from DP83867IR	125 MHz	LVCMOS_25	Bank 33, SRCC/MRCC
MIPI_CSI_CLK	In to FPGA from PCAM	672 MHz	LVDS_25	Bank 33, SRCC/MRCC
MIPI_DSI_CLK	Out from FPGA to LCD	TBD	HSTL_18	Bank 13, Diff I/O
FMC_CLK0_M2C	FMC LPC to FPGA	Variable	LVDS_25/HSTL_18	Bank 36, MRCC
FMC_CLK1_M2C	FMC LPC to FPGA	Variable	LVDS_25/HSTL_18	Bank 35, MRCC
FMC_LA00_CC	Out/In by FPGA for FMC LPC	Variable	LVDS_25/HSTL_18	Bank 36, SRCC
FMC_LA01_CC	Out/In by FPGA for FMC LPC	Variable	LVDS_25/HSTL_18	Bank 35, SRCC
6x of PMOD_CLK	Out from FPGA to 6x PMOD connectors	Variable	LVCMOS_33	Bank 16, SE I/O
HDMI_CLK	Out from FPGA to ADV7511	25 MHz - 165 MHz	LVCMOS_33	Bank 15, SE I/O

The detailed FPGA connections for the clocks described in the table above are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints. For more Si570 information, see the data sheet at the Silicon Laboratories, Inc. website.

The following figure shows the SP701 board clocking diagram.

Figure 7: **SP701 Clocking Diagram**



USB UART Interface

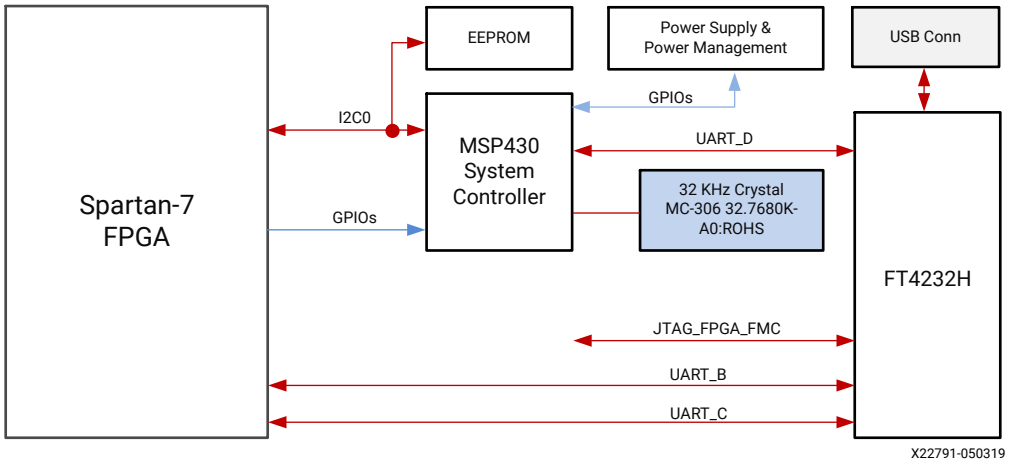
[Figure 2, callout 13]

The FT4232HQ U6 multifunction USB-UART on the SP701 board provides two level-shifted UART connections through the single micro-AB USB connector J5.

- Channel ADBUS is configured in JTAG mode to support the JTAG chain
- Channel ACBUS implements 4-wire FT4232_B_UART (level-shifted) FPGA U1 bank 14 connections
- Channel BDBUS implements 4-wire FT4232_C_UART (level-shifted) FPGA U1 bank 13 connections
- Channel BCBUS implements 2-wire FT4232_D_UART MSP430 U25 connections

The USB UART interface circuit is shown in the following figure.

Figure 8: **FTDI USB UART Circuit**



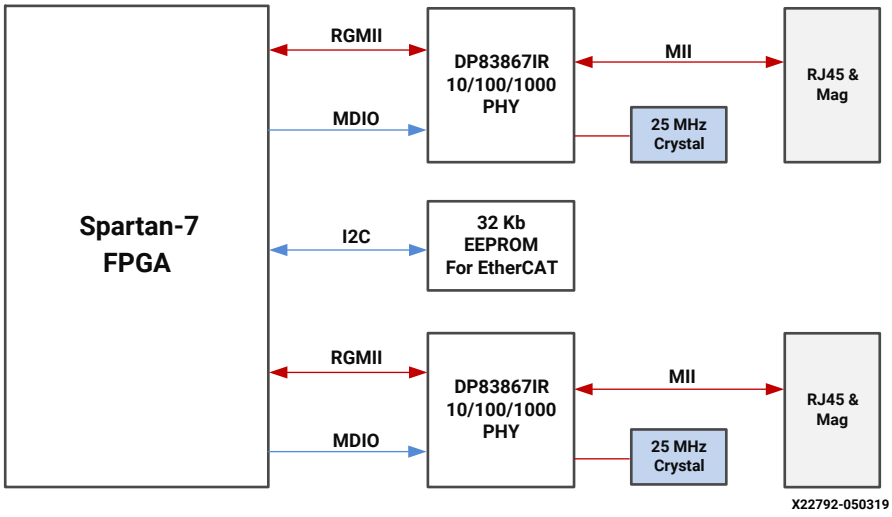
The FTDI FT4232HQ data sheet is available on the Future Technology Devices International Ltd. website. The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

10/100/1000 Mb/s Tri-speed Ethernet PHY (RGMII)

[Figure 2, callouts 8, 9]

A BECKHOFF IP ET1815, ET1816 MAC can be used to implement a 10/100/1000 Mb/s Ethernet interface (supports EtherCAT for Industrial Ethernet applications) in Spartan-7 FPGA, shown in the figure below, that connects to an external TI DP83867IRPAP Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector. The associated EEPROM has 12-byte reserved for the board serial number on start location of 0x14 and 6-byte reserved for the Ethernet MAC ID on start location of 0x35.

Figure 9: **SP701 Dual Ethernet**



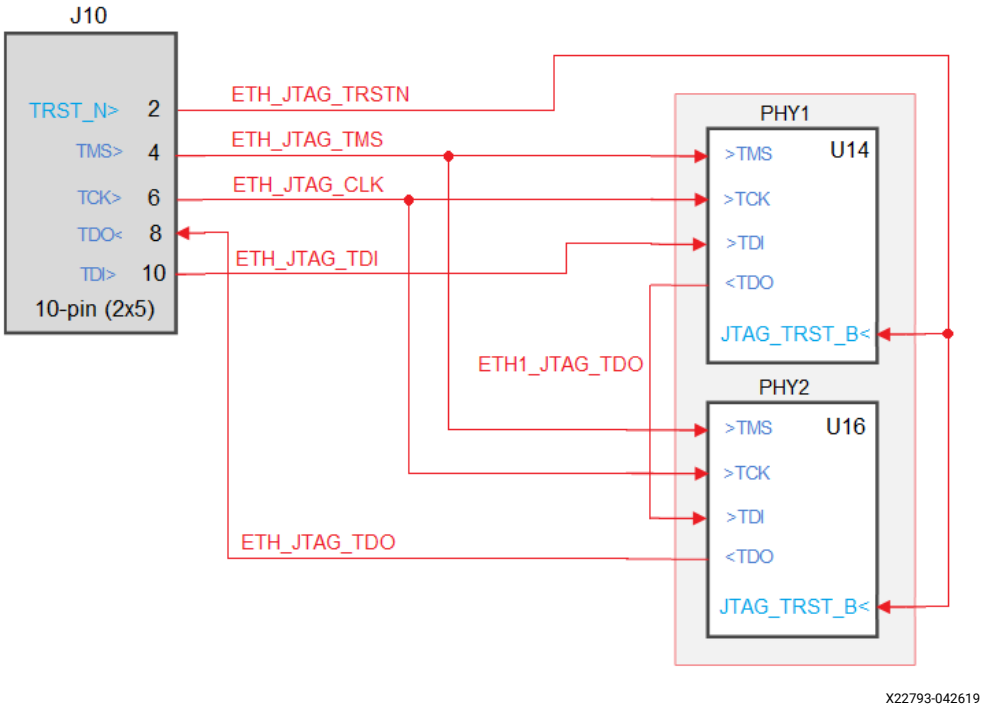
The SP701 evaluation board uses dual TI PHY device DP83867IRPAP (U14, U16) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board only supports the RGMII mode. Each PHY connects to a user-provided Ethernet cable through RJ-45 connector (J9, J11), Wurth 7499111221A with built-in magnetics, and status LEDs. On power-up, or on reset, the PHY are configured to operate in the RGMII mode with the PHY addresses set by hardware strap settings:

- PHY1 U14 PHY_ADDR[4:0] = 0001
- PHY2 U16 PHY_ADDR[4:0] = 0010

The TI DP83867IRPAP data sheet is on the Texas Instruments website.

The Ethernet PHY components have their own JTAG chain connected to 2x5 male pin header J10 as shown in the following figure.

Figure 10: **Ethernet JTAG**



The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Ethernet PHY Status LEDs

Figure 2, callouts 8, 9

Each Ethernet PHY is connected to a RJ-45 connector with status LEDs integrated into the metal frame of the connector. The two PHY status LEDs are visible within the frame of each RJ45 Ethernet jack as shown in the following figure. As viewed from the front opening, the left green LED is the link activity indicator and the right green LED is the 1000BASE-T link mode indicator.

Figure 11: **Ethernet PHY Status LEDs**

For each Ethernet PHY, a separate discrete LED indicates that a link has been established, as described in the following list:

- PHY1 DP83867IRPAP U14 RJ-45 J9, link established DS2, near item 25 in Figure 2.
- PHY2 DP83867IRPAP U16 RJ-45 J11, link established D2, near item 9 in Figure 2.

Details about the Tri-Mode Ethernet MAC core are provided in the *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051).

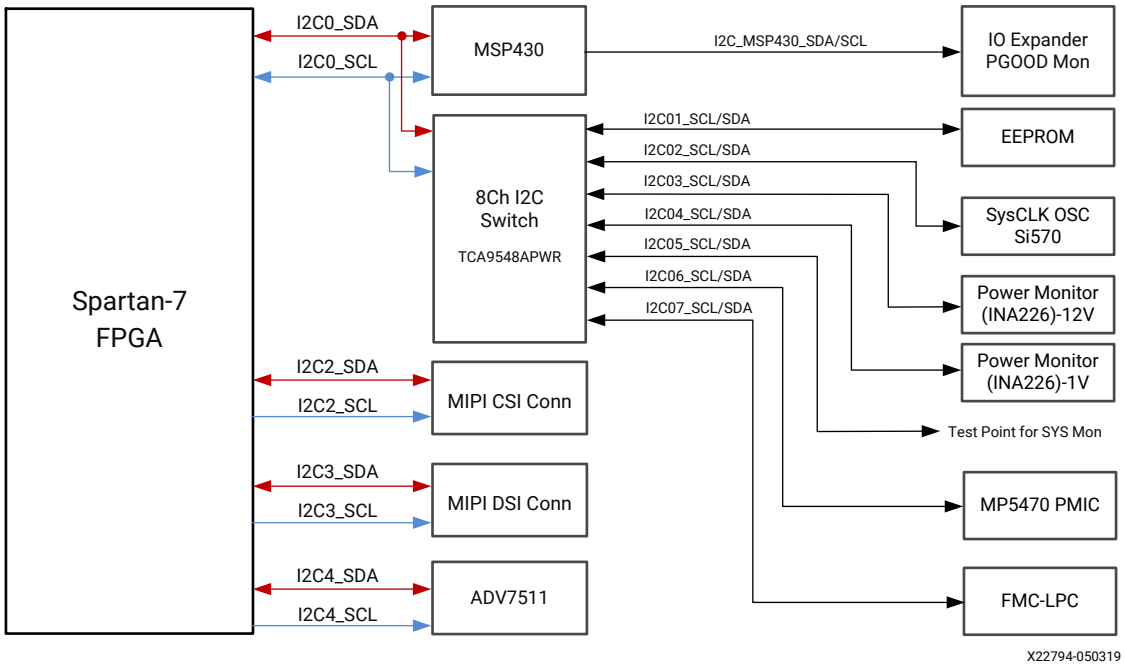
I2C Bus Topology

[Figure 2, callout 17]

The SP701 evaluation board I2C bus implementation consists of bus I2C0, shared by the FPGA U1 HP bank 16 and the MSP430 system controller U25. The I2C bus is routed to a TCA9548A 1-to-8 bus switch U23 (address 0x74). Seven of the eight bus switch channels are used. The bus switch can operate at speeds up to 400 kHz.

The SP701 evaluation board I2C bus topology is shown in the following figure.

Figure 12: **SP701 I2C Topology**



The following table lists the XC7S100 U1 FPGA I2C bus connectivity.

Table 9: **XC7S100 U1 FPGA I2C Bus Connectivity**

I2C0 Bus	I2C Switch Position	I2C Address		Target Device
		Binary Format	Hex Format	
TCA9548 8-Chan. Switch U23	N/A	0b1110100	0x74	U23 TCA9548A
I2C01_EEPROM_SDA/SCL	0	0b1010000	0x50	U27 M24C32
I2C02_SYSOSC_SDA/SCL	1	0b1010101	0x55	U45 SI570
I2C03_12VMON_SDA/SCL	2	0b1000001	0X41	U32 INA226
I2C04_1VMON_SDA/SCL	3	0b1000100	0x44	U33 INA226
I2C05_SYSMON_SDA/SCL	4	N/A	N/A	TP10/TP11 TEST POINT
I2C06_MP5470_SDA/SCL	5	0b1101000	0x68	U34 MP5470GL PMIC
I2C07_FMC_SDA/SCL	6	0b1010000	0x50	J21 FMC LPC
NOT USED	7	N/A	N/A	N/A
XC7S100 FPGA U1 BANK 33 I2C Port				
I2C2_CAM_SDA/SCL	U1.AE13/AD13	0b1101000	0x78	J8 MIPI-CSI
XC7S100 FPGA U1 BANK 13 I2C Port				
I2C3_DSI_SDA/SCL	U1.AB24/AC26	0bTBD	0xTBD	J20 MIPI-DSI
XC7S100 FPGA U1 BANK 15 I2C Port				
I2C4_HDMI_SDA/SCL	U1.K23/J24	0b1100010	0x72	U18 ADV7511 HDMI
MSP430 U25 PORT P4_1, P4_2 I2C_MSP430_SDA/SCL Bus				
TCA6416 Dual 8-bit I/O Port U24	N/A	0b0100000	0x40	U24 TCA6416A

The MSP430 system controller U25 has a local I2C_MSP430_SDA/SCL bus connected to a dual 8-bit port TI TCA6416A I/O expander U24 (address 0x40). The I/O expander is used for control outputs and status inputs as listed in the following table.

Table 10: **MSP430 TCA6416A U24 I/O Expander Connections**

TCA6416A U24 I/O Expander Addr. 0b0100000, 0x40			
Port #	**Schematic Net Name**	**DIR**	**Connected Device**
P00	EN_1V35	IN	U35 MPM3620A VCCO_1V35 regulator
P01	EN_1V1_ETH	IN	U38 MPM3805G 1V1_VDD regulator
P02	EN_5V	IN	U36 MPM3606A 5V regulator
P03	EN_3V3_EXT	IN	U39 MP8756G 3V3_EXT regulator
P04	EN_VADJ	OUT	U40 MP8756G VADJ regulator
P05	EN_1V_1V8_2V5_3V3	IN	U34 MP5470G VCCINT_1V, VCCO_1V8, VCCO_2V5, VCCO_3V3 multi-output regulator
P06	VSEL0_VADJ	OUT	Q17 FB_VADJ_VSEL0 U40 MP8756G VADJ regulator feedback adjusting switch
P07	VSEL1_VADJ	OUT	Q18 FB_VADJ_VSEL1 U40 MP8756G VADJ regulator feedback adjusting switch
P10	12VCURSNS_ALERT	IN	U32 INA226 POWER MONITOR ON INPUT 12V

Table 10: **MSP430 TCA6416A U24 I/O Expander Connections** *(cont'd)*

TCA6416A U24 I/O Expander Addr. 0b0100000, 0x40			
Port #	**Schematic Net Name**	**DIR**	**Connected Device**
P11	1VCURSNS_ALERT	IN	U33 INA226 POWER MONITOR ON VCCINT_1V
P12	NOT USED	IN	N/A
P13	M0_0	IN	U1 FPGA CONFIG. BANK 0 MODE M0
P14	M1_0	IN	U1 FPGA CONFIG. BANK 0 MODE M1
P15	M2_0	IN	U1 FPGA CONFIG. BANK 0 MODE M2
P16	FMC_PRSNT_M2C_LT	IN	J21 FMC LPC
P17	PGOOD_VADJ	IN	U40 MP8756G VADJ regulator

The TI TCA9548 and TCA6416 data sheets are on the Texas Instruments website. The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints

HDMI Video Output

[Figure 2, callout 12]

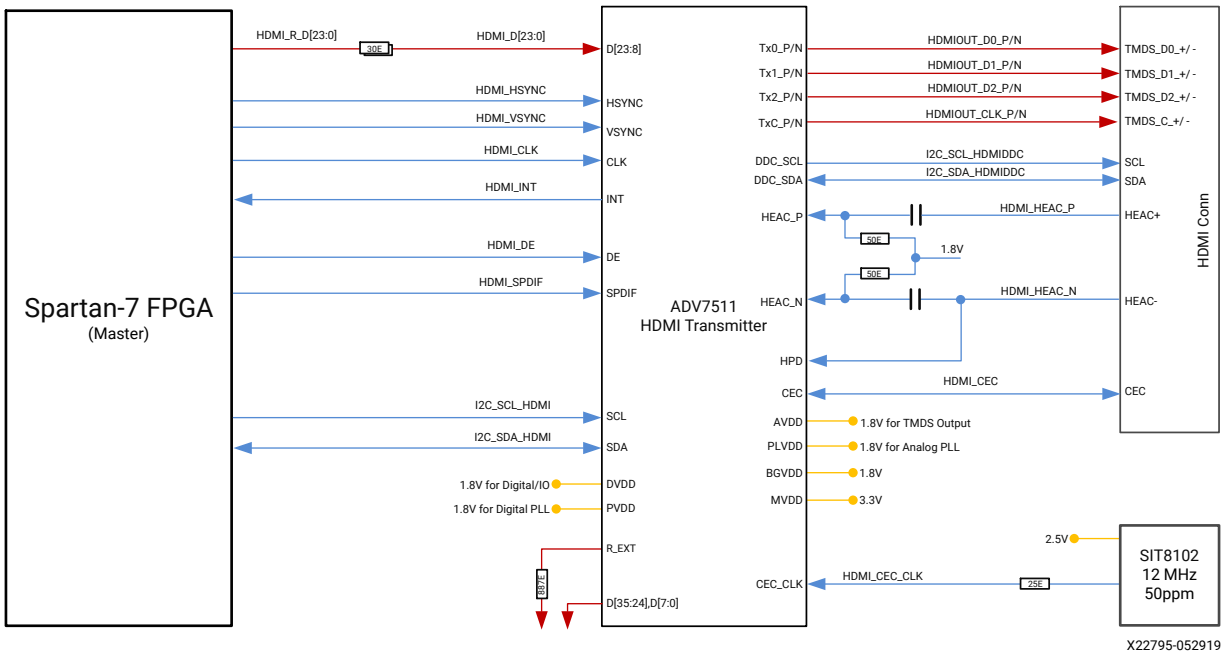
The SP701 board provides a HDMI video output using the Analog Devices ADV7511KSTZ-P HDMI transmitter (U18). The HDMI output is provided on a Molex 47151-1001 HDMI type-A connector (J13). The ADV7511 is wired to support 1080P 60 Hz, YCbCr 4:2:2 encoding using 24-bit input data mapping.

The SP701 board supports the following HDMI device interfaces:

- 24 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt Out Pin to FPGA
- I2C
- SPDIF

The HDMI output interface is shown in the following figure.

Figure 13: **HDMI Output Interface**



For more details, see the ADV7511KSTZ-P data sheet at the Analog Devices website. The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

MIPI-CSI and MIPI-DSI

[Figure 2, callout 10, 11]

The mobile industry processor interface (MIPI) is a serial communication interface specification promoted by the MIPI Alliance. An FPGA MIPI implementation provides a standard connection medium for cameras and displays referred to as a camera serial interface (CSI) or a display serial interface (DSI). Both interface standards use the PHY specification known as D-PHY. The D-PHY specification provides a flexible, low-cost, high-speed serial interface solution for communication interconnection between components inside mobile devices.

FPGAs do not have I/O standards that can natively support D-PHY. Connecting MINI-equipped camera and display components requires implementing the D-PHY hardware specification with discrete components outside the FPGA.

See the *D-PHY Solutions* (XAPP894) application note for more information about:

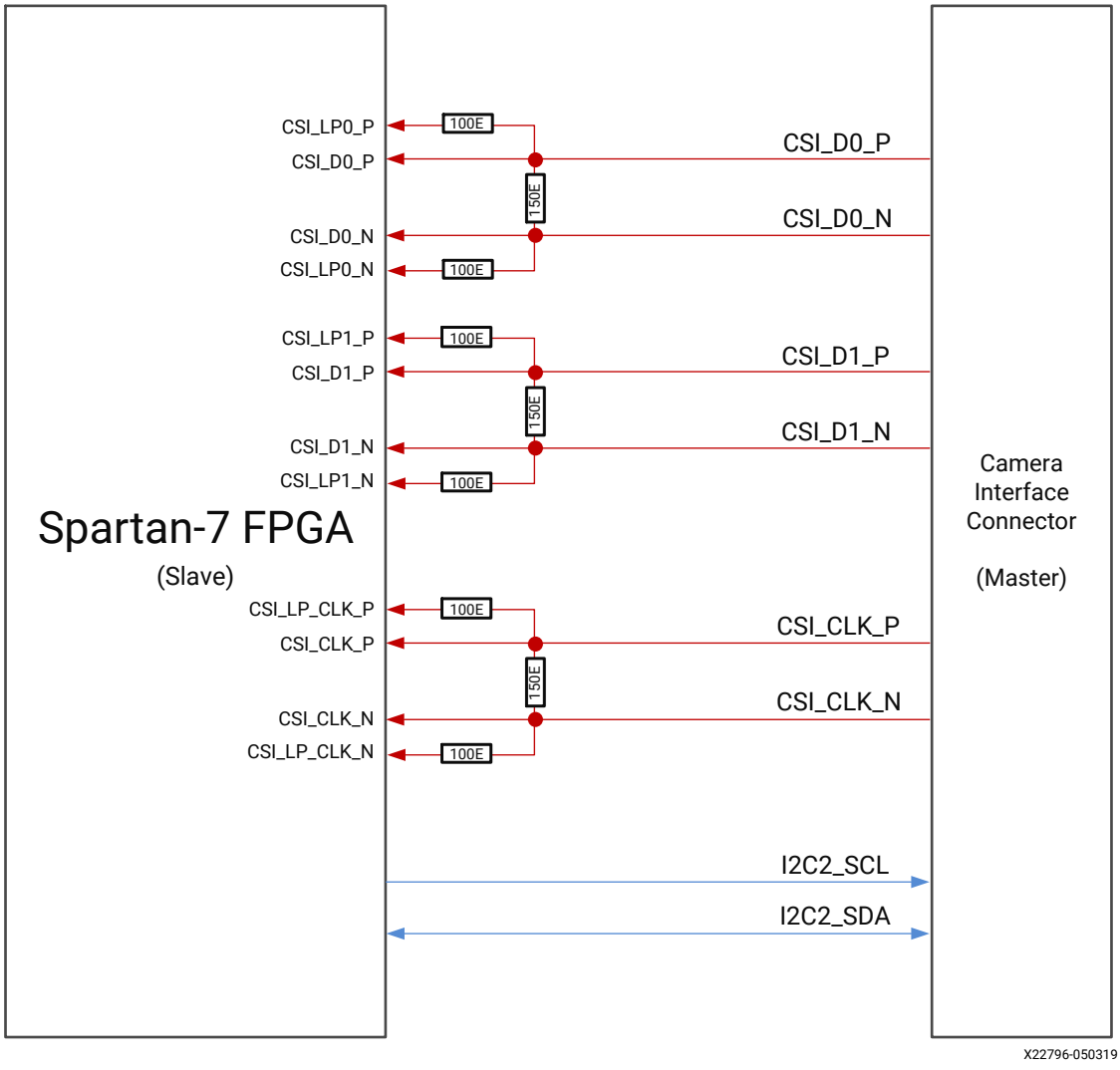
- MIPI-CSI (input) scalable low-voltage signaling (SLVS) conditioning to FPGA LVDS25.
- MIPI-DSI (output) FPGA differential HSTL18 conditioning to SLVS.

The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

MIPI-CSI

The SP701 board supports MIPI-CSI. The Digilent PCAM module has been tested with this board. MIPI-CSI interface is connected to AMP/TE Connectivity 1-1734248-5 15-pin connector J8. MIPI-CSI interface is shown in the following figure.

Figure 14: **MIPI-CSI Interface**

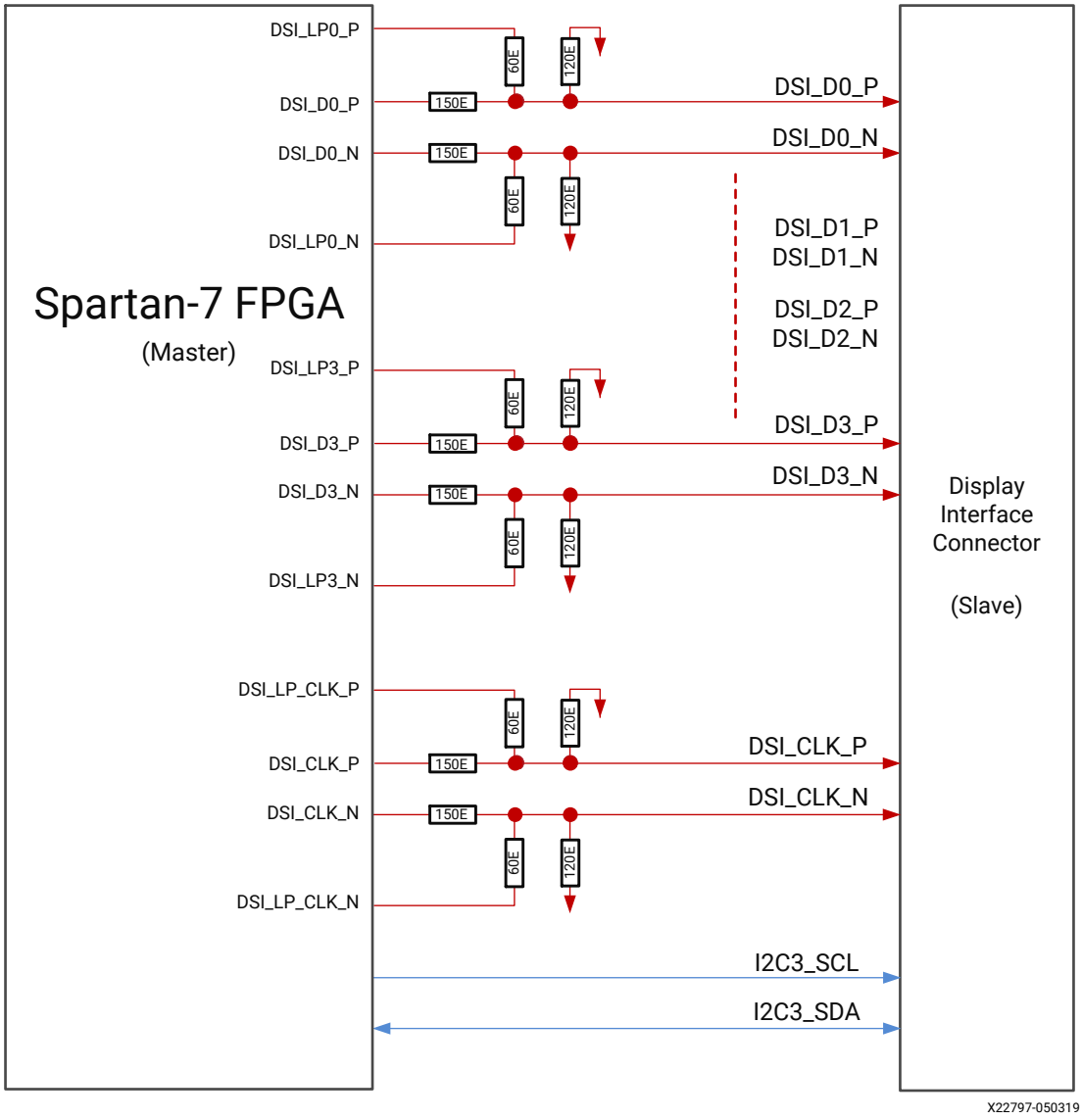


See the Digilent website for information about Pcam 5.

MIPI-DSI

The SP701 board provides MIPI DSI (display serial interface) support. The MIPI-DSI interface is connected to Hirose FH34SJ-34S-0.5SH 34-pin connector J20. The MIPI-DSI interface is shown in the following figure.

Figure 15: **MIPI-DSI Interface**



For more information about MIPI, see the MIPI Alliance website.

Power and Status LEDs

[Figure 2, callout 20]

The following table lists the SP701 power, user, and status LEDs.

Table 11: **SP701 Power, User, and Status LEDs**

Reference Designator	Description (Green Unless Otherwise Noted)
DS1	DONE (blue)
D4	MSP430_LED0
D5	MSP430_LED1
D6	GPIO_LED0
D7	GPIO_LED1
D8	GPIO_LED2
D9	GPIO_LED3
D10	GPIO_LED4
D11	GPIO_LED5
D12	GPIO_LED6
D13	GPIO_LED7
D14	12V On (red)
DS2	ETH1_LED1
D2	ETH2_LED1

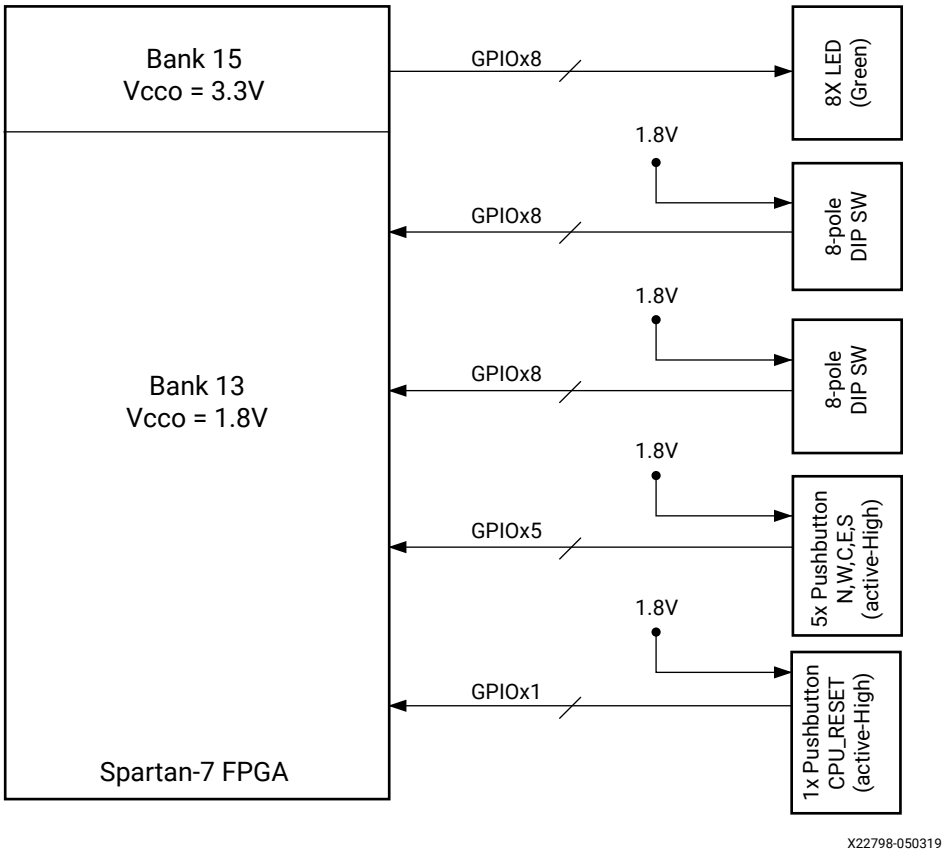
User I/O

[Figure 2, callout 20]

The SP701 board provides these user and general purpose I/O capabilities:

- Eight user LEDs, active-High (callout 20)
  - GPIO_LED[0:7]: D6, D7, D8, D9, D10, D11, D12, D13
- 2x 8-position user DIP switch, active-High (callout 23)
  - GPIO_DIP_SW_B[0:7]: SW12
  - GPIO_DIP_SW_B[8:16]: SW10
- Five user PB (geographical) and CPU reset PB, active-High (callouts 21 and 22)
  - GPIO_SW_[NWCES]: SW4, SW5, SW6, SW7, SW9
  - CPU_RESET: SW8

Figure 16: **User GPIO**



The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

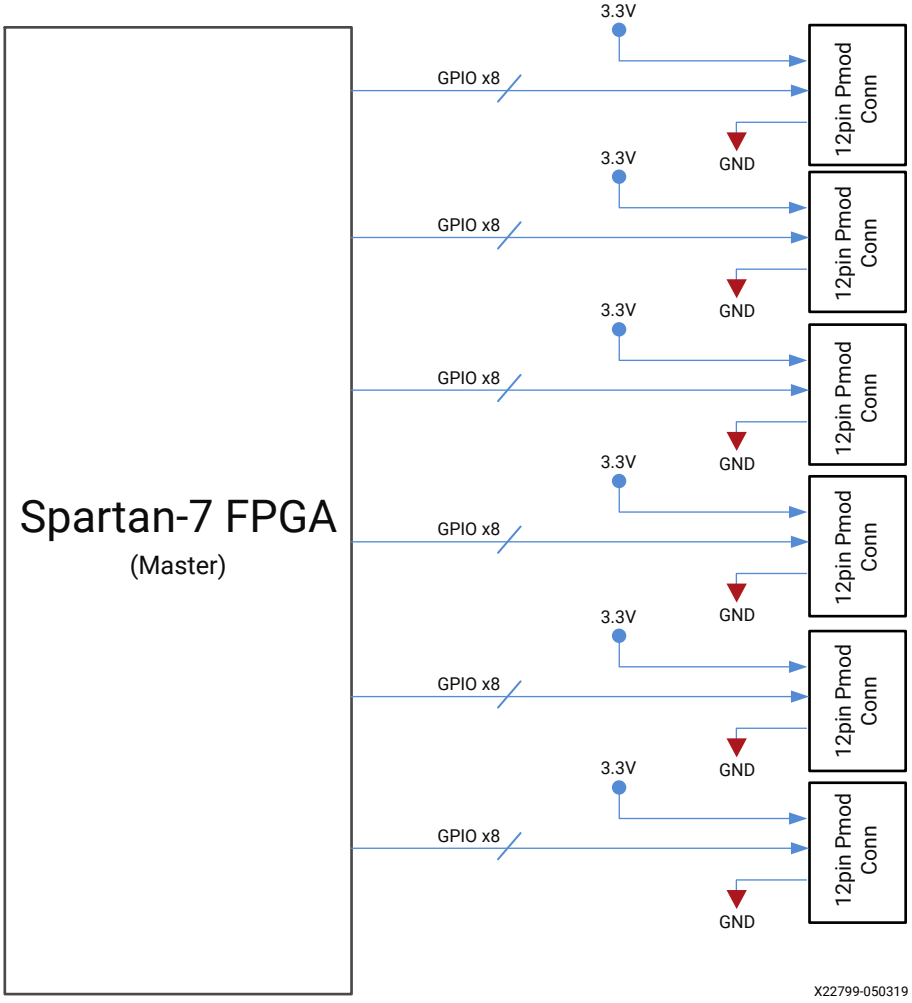
User PMOD GPIO Connectors

[Figure 2, callout 20, 21]

The SP701 evaluation board implements six right-angle PMOD GPIO receptacles J14-J19. The 3.3V PMOD nets are wired to the XC7S100 FPGA 3.3V bank 16. For more information about PMOD connector compatible PMOD modules, see the Digilent Inc. website.

The following figure shows the GPIO PMOD connectors.

Figure 17: **6x PMOD RA Receptacles**



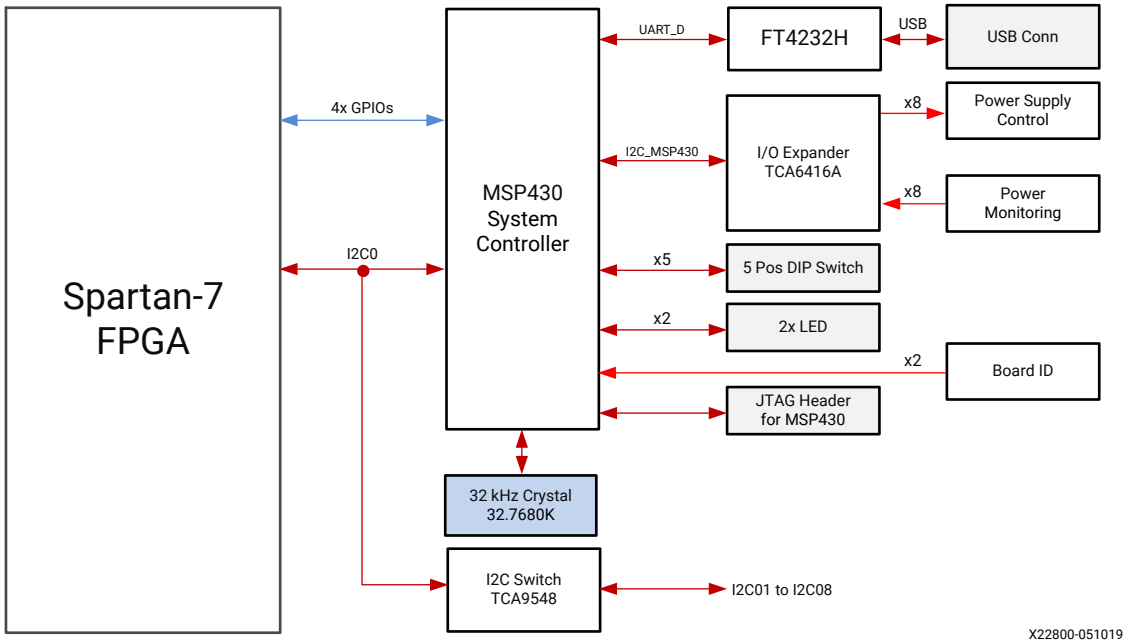
The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

System Controller MSP430

[Figure 2, callout 14]

The SP701 evaluation board implements an on-board system controller (MSP430F5342 U25) accessible from the FT4232H USB-UART BCBUS Port D.

Figure 18: **MSP430 Block Diagram**

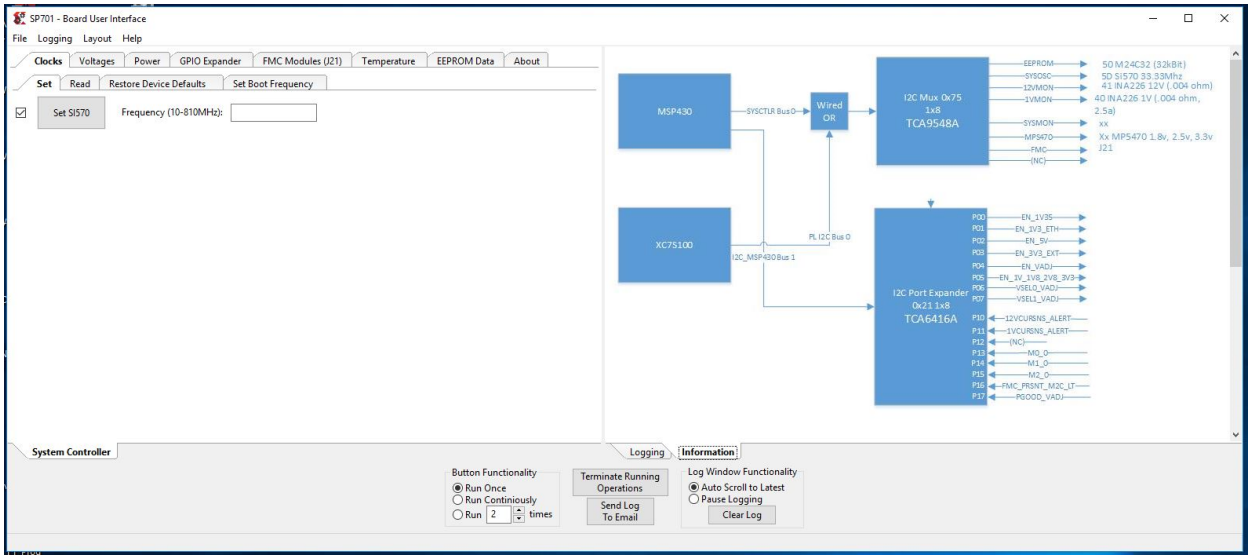


A host PC resident system controller user interface (SCUI) is provided on the SP701 website. This GUI enables you to query and control select programmable features such as clocks, FMC functionality, and power systems parameters. The SP701 documentation also includes a tutorial on the SCUI, SP701 System Controller Tutorial (XTP551), and a SP701 Software Install and Board Setup Tutorial (XTP552). The instructions are summarized as follows.

1. Ensure that the Silicon Labs VCP USB-UART drivers are installed. See *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033).
2. Download the SCUI host PC application.
3. Connect a USB cable between your PC and the SP701 USB micro-AB connector (J5).
4. Power-cycle the SP701.
5. Ensure that SYSCTLR LED0 (D4) blinks and LED1 D5 is illuminated.
6. Launch the SCUI.

The SCUI GUI is shown in the following figure.

Figure 19: **SCUI Graphical User Interface**



On the first use of the SCUI, go to the **FMC → Set VADJ → Boot-up tab** and click **USE FMC EEPROM Voltage**. The SCUI buttons are grayed out during command execution and return to their original appearance when ready to accept a new command. See the SP701 System Controller Tutorial (XTP551) and the SP701 Software Install and Board Setup Tutorial (XTP552) for more information on installing and using the System Controller utility.

For more details, see the MSP430F5342 data sheet on the Texas Instruments website. The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

FPGA Mezzanine Card Interface

[Figure 2, callout 7]

The SP701 evaluation board supports the VITA 57.1 FPGA mezzanine card (FMC) specification by providing a low pin count (LPC) FMC connector at J21. LPC connectors use a 10 x 40 form factor that is partially populated with 160 pins. The connector is keyed so that a mezzanine card, when installed in the FMC LPC connector on the SP701 evaluation board, faces away from the board. The FMC LPC connector pinout is shown in the Appendix A: VITA 57.1 FMC Connector Pinouts.

FMC LPC Connector J21

[Figure 2, callout 7]

The 160-pin connector J21 implements partial FMC LPC connectivity (refer to schematic 0381874 and the XDC file for details).

- 68 single-ended, or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 2 differential user clocks
- 2 I2C
- 5 JTAG
- 2 state flags
- 61 ground and 10 power connections

The SP701 board FMC VADJ voltage for LPC connector J21 is determined by the MSP430 system controller adjusting the Monolithic Power Systems MP8756GD U40 voltage regulator as described in Board Power System. Valid values for the VADJ_FMC rail are 1.8V, 2.5V, and 3.3V.

The detailed FPGA connections for the feature described in this section are documented in the SP701 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Power On/Off Slide Switch

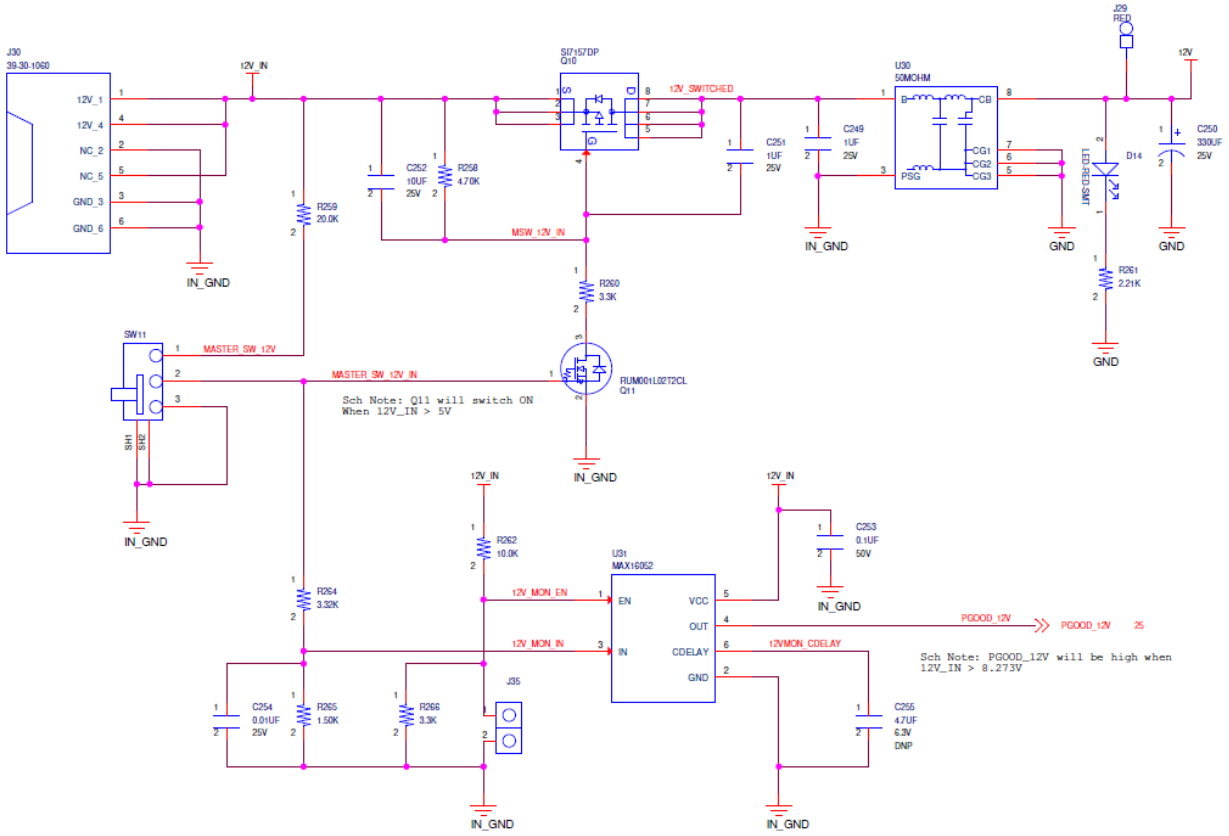
[Figure 2, callout 28]

The SP701 board power switch is SW11. Sliding the switch actuator from the off to the on position applies 12V power from J30, a 6-pin mini-fit connector. Red LED D14 illuminates when the SP701 board power is on. See Board Power System for details on the on-board power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the SP701 board power connector J30. The ATX 6-pin connector has a different pin-out than J30. Connecting an ATX 6-pin connector into J30 damages the SP701 board and voids the board warranty.*

The following figure shows the power connector J30, power switch SW11, and LED indicator D14.

Figure 20: **SP701 Power Input**



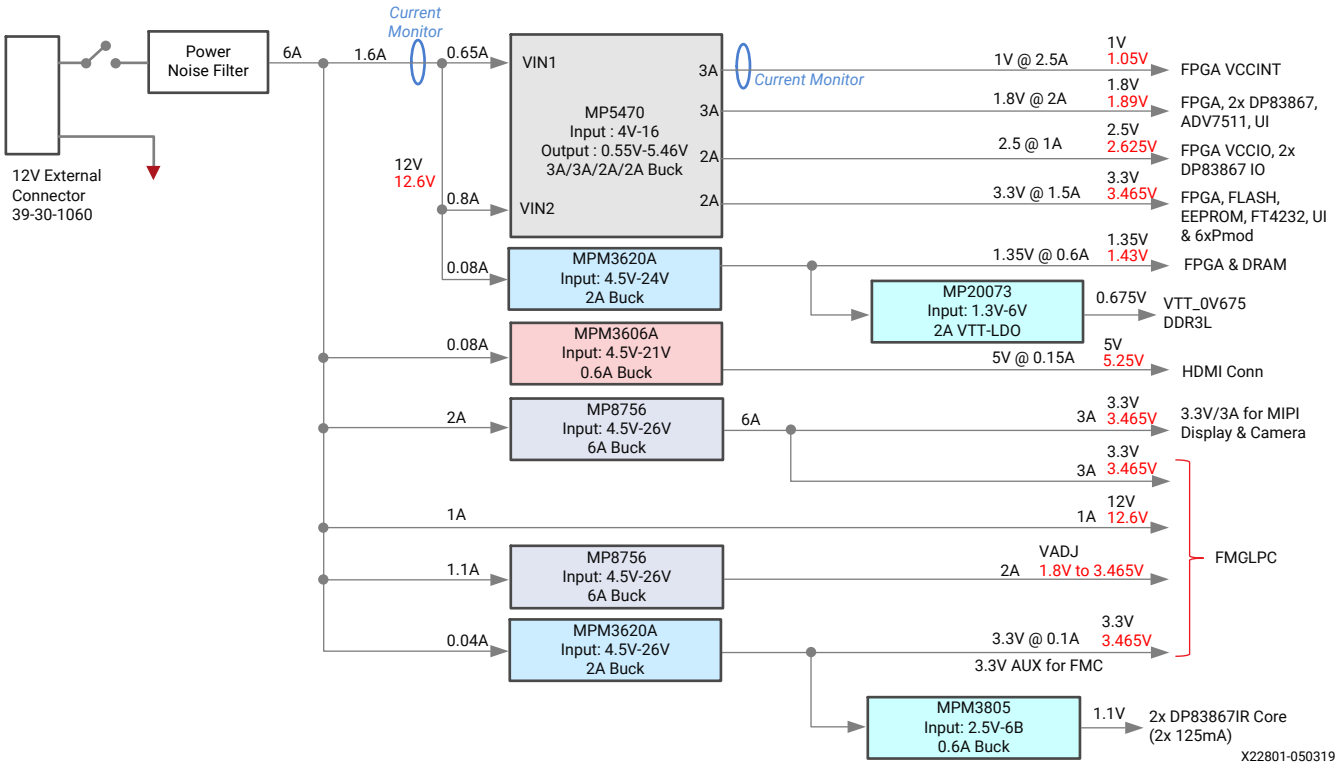
Board Power System

[Figure 2, callout 29]

The SP701 power system is comprised of monolithic power systems components. The four outputs (VCCINT, VCCO_1V8, VCCO_2V5, and VCCO_3V3) of the MP5470 U34 regulator are adjustable through its I2C bus connection accessible from the FPGA U1 Bank 16 and the MSP430 system controller.

The following figure shows the SP701 power system block diagram.

Figure 21: **Power System Block Diagram**



The following table lists the SP701 power system voltage regulators.

Table 12: **SP701 Power System**

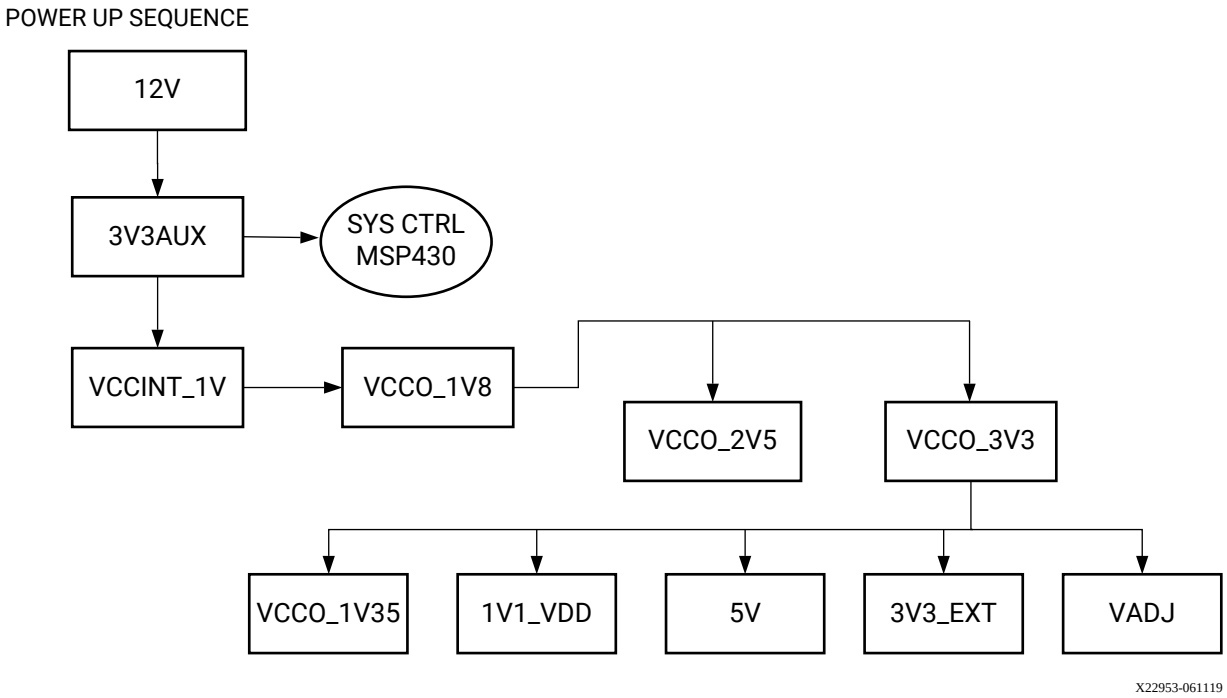
Device Type	Ref. Des.	I2C Address	Description	O/P	Power Rail Net Name	Power Rail Voltage	Max. Current	Schematic Page
INA226AIDGS	U32	0x41	Current and power monitor	N/A	12V	N/A	N/A	24
MP5470GL	U34	0x68	Four-output PMIC	SW1	VCCINT_1V	1.00V	3A	24
				SW2	VCCO_1V8	1.80V	2A	
				SW3	VCCO_2V5	2.50V	2A	
				SW4	VCCO_3V3	3.30V	2A	
INA226AIDGS	U33	0x44	Current and power monitor	N/A	VCCINT_1V	N/A	N/A	24
MPM3620A	U35	N/A	Synchronous step-down converter	OUT	VCCO_1V35	1.35V	2A	25
MPM3606A	U36	N/A	Synchronous step-down converter	OUT	5V	5.0V	0.6A	25
MPM3805GQB	U38	N/A	Synchronous step-down converter	OUT	1V1_VDD	1.10V	0.6A	25

Table 12: **SP701 Power System** *(cont'd)*

Device Type	Ref. Des.	I2C Address	Description	O/P	Power Rail Net Name	Power Rail Voltage	Max. Current	Schematic Page
MPM3620A	U37	N/A	Synchronous step-down converter	OUT	3V3AUX	3.30V	2A	25
MP8756GD	U39	N/A	POL switching regulator	SW	3V3_EXT	3.30V	6A	26
MP8756GD	U40	N/A	POL switching regulator	SW	VADJ	1.80V	6A	26
MP20073DH	U13	N/A	DDR memory termination regulator	VTTREF	VTTREF	0.675V	2A	6

The following figure shows the SP701 power system sequencing diagram.

Figure 22: **Power System Sequence**



The options for VADJ are 1.8V, 2.5V, and 3.3V. They can be selected using the System Controller (MSP430) I2C connected TCA64164A I/O expander U24 ports P06 VSEL0_VADJ and P07 VSEL1_VADJ pins. The VADJ regulator can similarly be powered ON/OFF by the TCA64164A I/O expander U24 port P04 pin.

Table 13: **SP701 Power System VADJ**

VADJ	VSEL0_VADJ (U24.10)	VSEL1_VADJ (24.11)
3.3V	1	1
2.5V	0	1
1.8V	0	0

XADC Header

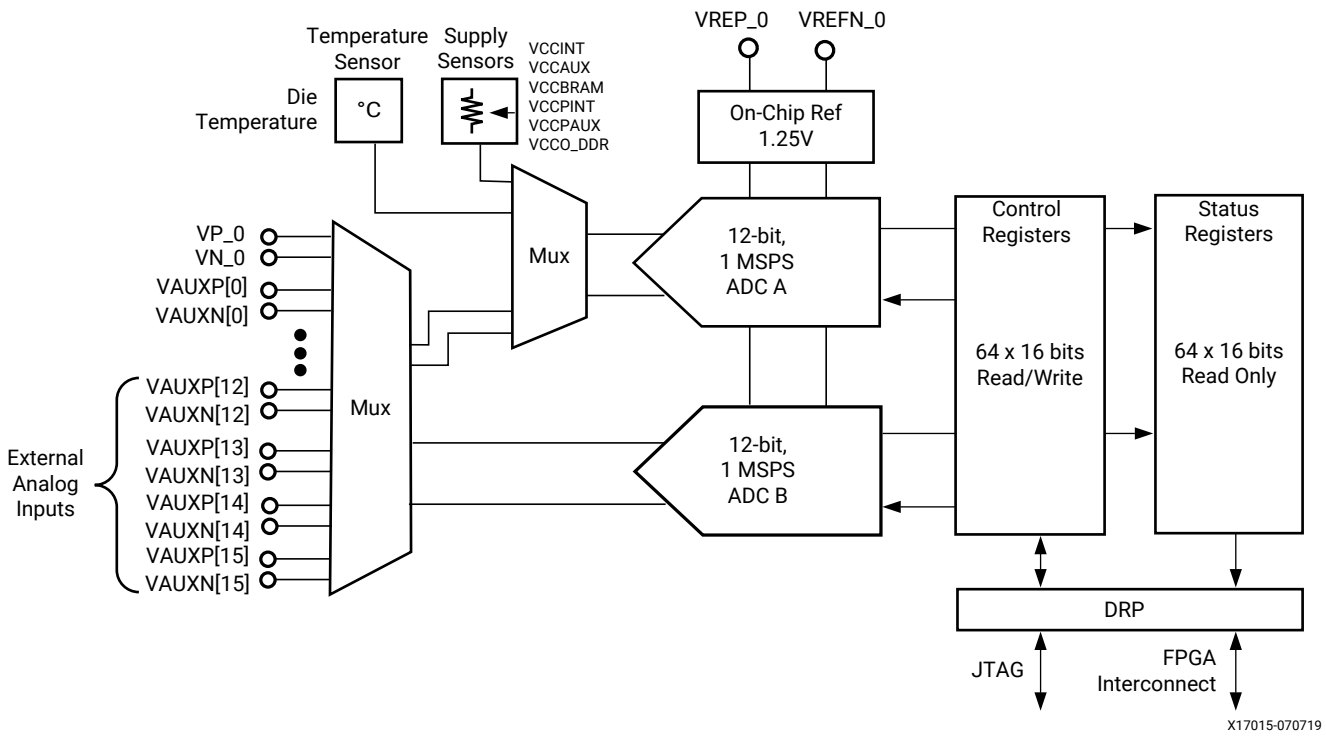
[Figure 2, callout 34]

The Xilinx® System Monitor (SYSMON) technology enables monitoring the physical environment via on-chip power supply, temperature sensors, and external analog inputs. SYSMON is a key part of the power management infrastructure for the board, providing telemetry information for the supplies for the Xilinx device and the various other on-board supplies.

The analog mixed signal (AMS) block present in Xilinx 7 series FPGAs is called XADC (includes SYSMON function). Apart from the SYSMON function, the ADCs provide a general-purpose, high-precision analog interface for a range of applications. The following figure shows the block diagram of the single XADC block available in the Spartan-7 family. The interface can be JTAG, DRP, and AXI to the XADC/SYSMON block.

See the *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for details on the capabilities of the analog front end.

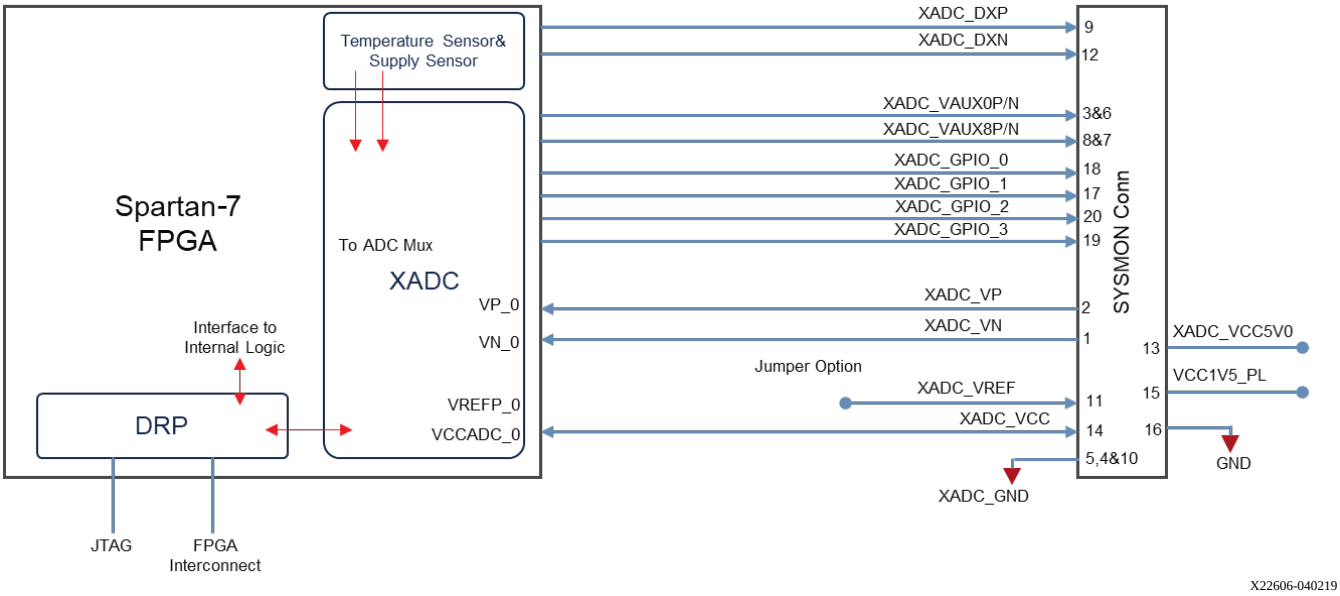
Figure 23: **XADC (SYSMON) Block Diagram**



It is not necessary to instantiate the XADC in a design to access the on-chip monitoring capability. However, if the XADC is not instantiated in a design, the only way to access this information is through the JTAG test access port (TAP). To allow access to the status registers (measurement results) from the FPGA logic, the XADC must be instantiated.

The following figure shows the SYSMON implementation and SYSMON header J24, a 2x10 shrouded male pin header. Jumper J26 is provided to select internal reference or external reference.

Figure 24: **XADC (SYSMON) Interface**



See the SP701 schematic 0381874 for detailed SYSMON header J24 and XADC_VREF option details.

VITA 57.1 FMC Connector Pinouts

The following figure shows the pinout of the FPGA mezzanine card (FMC) low pin count (LPC) connector defined by the VITA 57.1 FMC specification. For a description of how the SP701 evaluation board implements the FMC specification, see FPGA Mezzanine Card Interface and FMC LPC Connector J21.

Figure 25: **FMC LPC Connector Pinout**

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

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Appendix B

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the SP701 board provides for designs targeting the SP701 evaluation board. Net names in the constraints file correlate with net names on the latest SP701 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.

The FMC LPC connector J21 is connected to FPGA banks powered by the variable voltage V_{ADJ} (1.8V nominal). Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT! *See the SP701 board website documentation tab (Board Files check box) for the XDC file.*

Appendix C

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

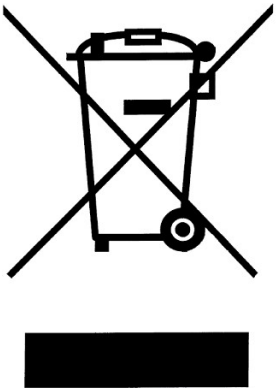
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

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Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the SP701 board and its documentation is available on the following websites.

- SP701 Evaluation Kit
- SP701 Evaluation Kit Master Answer Record 72092

These documents provide supplemental material useful with this guide:

1. *7 Series FPGAs Data Sheet: Overview* (DS180)
2. *Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS189)
3. *Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions* (UG586)
4. *7 Series FPGAs Memory Resources User Guide* (UG473)
5. *7 Series FPGAs Configuration User Guide* (UG470)
6. *7 Series FPGAs Packaging and Pinout Product Specification* (UG475)
7. *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
8. *7 Series FPGAs PCB Design Guide* (UG483)
9. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
10. *Vivado Design Suite User Guide: Using Constraints* (UG903)
11. *D-PHY Solutions* (XAPP894)
12. SP701 System Controller Tutorial (XTP551)
13. SP701 Software Install and Board Setup Tutorial (XTP552)

    Documents associated with other devices used by the SP701 board are available at these vendor websites:

14. Micron Technology: www.micron.com (MT25QL01GBBBESF-0SIT, MT41K256M16TW-107:P)
15. Analog Devices: www.analog.com/en/index (ADV7511KSTZ-P)
16. Samtec: www.samtec.com (SEAF series connectors)
17. VITA FMC Marketing Alliance: www.vita.com/fmc (FPGA Mezzanine Card (FMC) VITA 57.1, 57.4 specifications)
18. Silicon Labs: www.silabs.com (Si570)
19. Texas Instruments: www.ti.com (TCA9548A, TCA6416A, DP83867IRP, ADP123)
20. Future Technology Devices International Ltd.: www.ftdichip.com (FT4232HQ)

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