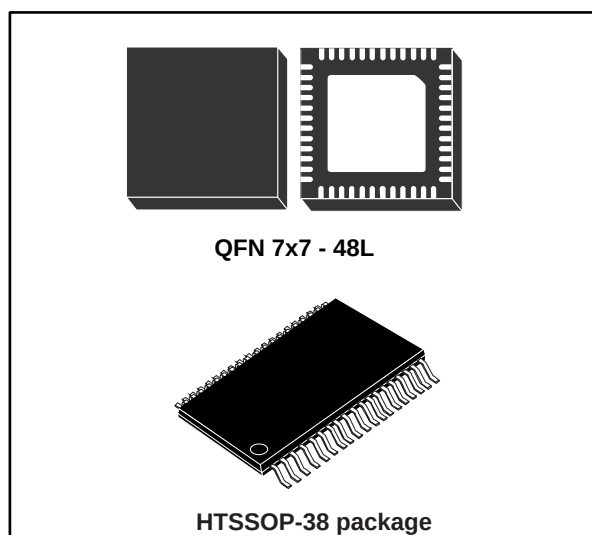


## High speed digital input current limiter with digital filter

Datasheet - production data



### Applications

- Programmable logic controller and remote input modules
- High speed protected termination for digital input with serialized SPI output
- IEC61131-2 type 1, 2 and 3

### Description

The SCLT3 series provides an 8-line protected digital input termination with serialized state transfer.

This device enhances the I/O module density by cutting the dissipation (78 mW per input) and reducing the count of opto-transistors.

An adjustable digital filter and an LED driver are embedded in each type 3 input section. Its 2 MHz SPI peripheral output serializes the input state transfer to the I/O module controller.

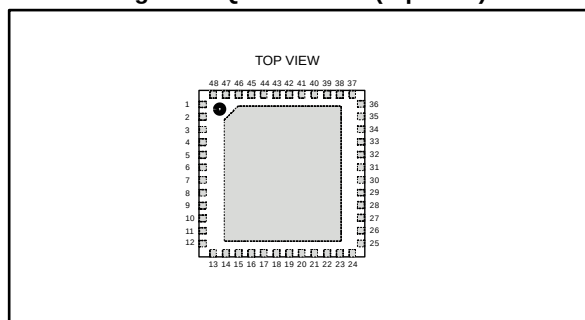
### Features

- 8 inputs - 8-bit SPI output
- High side input with common ground
- 5 V voltage regulator
- Package: QFN 7x7 - 48L or HTSSOP-38
- 35 V reverse polarity capable
- Adjustable current limiters
- LED output for visual status
- Optional: 16-bit mode with parity check, temperature and voltage alarms
- Daisy chain capable
- Input digital filter with adjustable delay: 20  $\mu$ s to 3 ms
- Power dissipation: 78 mW per channel

### Complies with the following standards

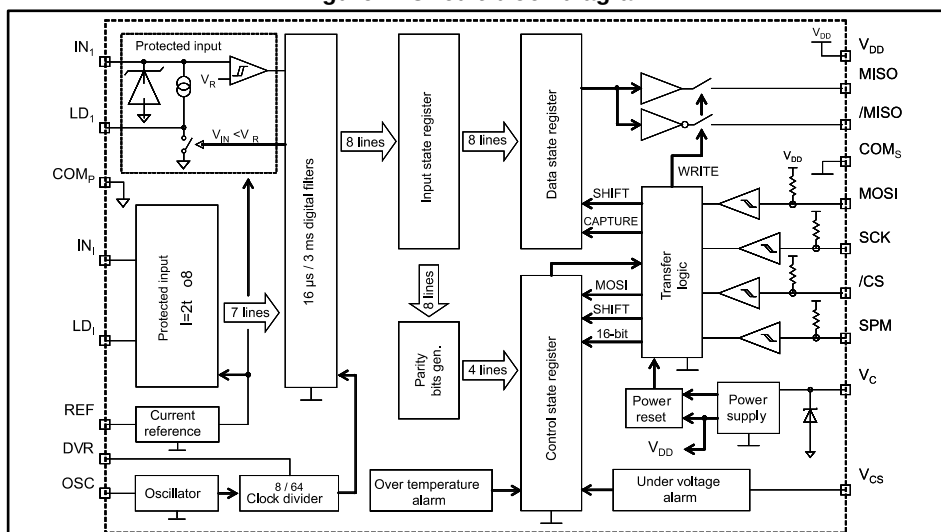
- IEC 61000-4-2
  - $\pm 8$  kV contact discharge
  - $\pm 15$  kV air discharge
- IEC 61000-4-4
  - Input:  $\pm 1$  kV
  - Power supply:  $\pm 2.5$  kV

Figure 1: QFN 7x7-48L (top view)

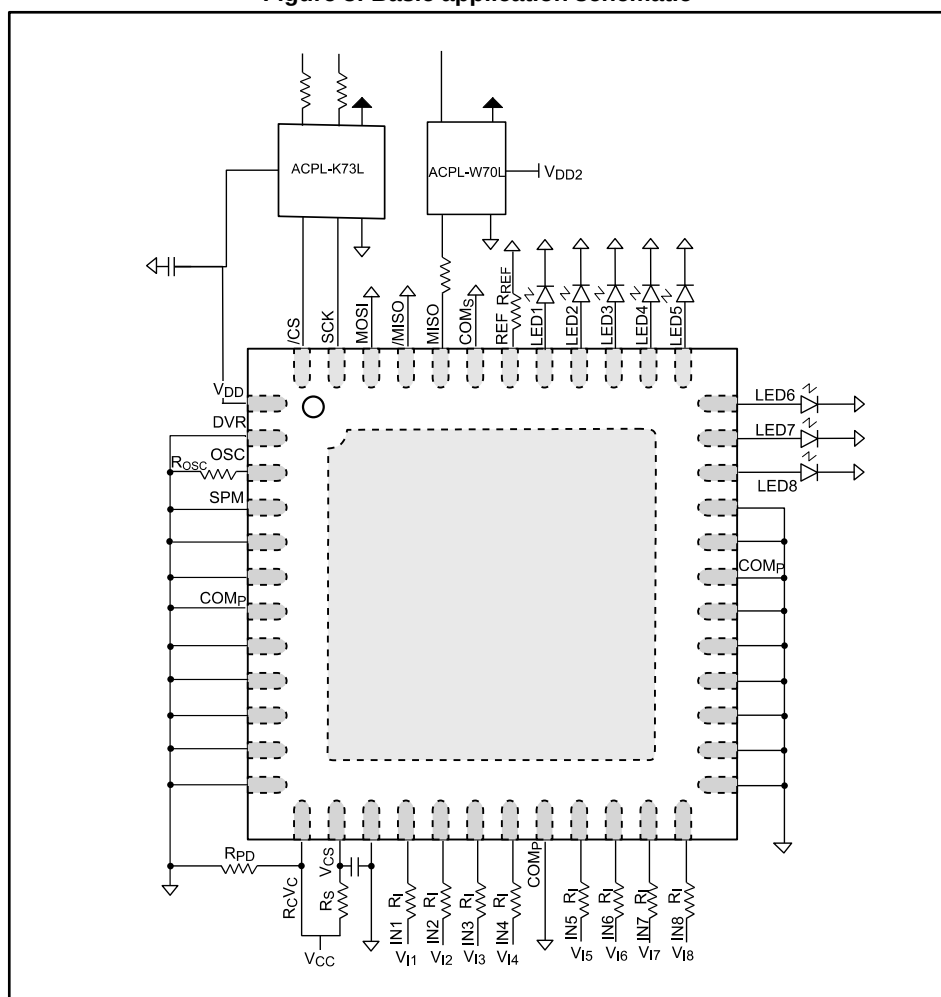


## 1 Circuit block diagrams

**Figure 2: Circuit block diagram**



**Figure 3: Basic application schematic**



## 1.1 I/O pin description

Table 1: I/O pin description

| Symbol           | Parameter    |                                                                                                    | Pin #<br>SCLT3-8BQ7                                    | Pin #<br>SCLT3-8BT8 |
|------------------|--------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------|---------------------|
| IN <sub>I</sub>  | Power input  | Logic input with current limitation, I = 1 to 8                                                    | 16, 17, 18, 19, 21, 22, 23, 24                         | 8 to 11, 13 to 16   |
| LD <sub>I</sub>  | Power output | LED output driver with current regulation, I = 1 to 8                                              | 34, 35, 36, 37, 38, 39, 40, 41                         | 20 to 27            |
| V <sub>C</sub>   | Power input  | 24 V sensor powersupply                                                                            | 13                                                     | 5                   |
| V <sub>CS</sub>  | Signal input | 24 V sensor power supply sensing input                                                             | 14                                                     | 6                   |
| COM <sub>P</sub> | Ground       | Power ground of power sensor supply                                                                | 7, 15, 20, 31                                          | 4, 7, 12, 17        |
| V <sub>DD</sub>  | Power output | 5 V logic power supply                                                                             | 1                                                      | 38                  |
| COM <sub>S</sub> | Ground       | Signal ground of logic / output section                                                            | 43                                                     | 30                  |
| REF              | Signal input | Input current limiter reference setting                                                            | 42                                                     | 29                  |
| SPM              | Signal input | SPI shift register length selector:<br>• SPM to GND = 16 bits<br>• SPM to V <sub>DD</sub> = 8 bits | 4                                                      | 3                   |
| /CS              | Logic input  | SPI chip Select signal                                                                             | 48                                                     | 35                  |
| SCK              | Logic input  | SPI serial clock signal                                                                            | 47                                                     | 34                  |
| MOSI             | Logic input  | SPI serial data input signal                                                                       | 46                                                     | 33                  |
| DVR              | Logic input  | Divider ratio selector of the digital input filters (8 or 64 steps)                                | 2                                                      | 1                   |
| OSC              | Signal input | Delay setting of the digital input filters                                                         | 3                                                      | 2                   |
| MISO             | Logic output | SPI serial data output signal                                                                      | 44                                                     | 31                  |
| /MISO            | Logic output | Inverting SPI serial data output signal                                                            | 45                                                     | 32                  |
| TAB              | Substrate    | Exposed pad: connected to die substrate, to be connected to COM <sub>P</sub>                       | TAB                                                    | Expose pad          |
| NC               |              | Not connected (or to be connected to COM <sub>P</sub> )                                            | 5, 6, 8, 9, 10, 11, 12, 25, 26, 27, 28, 29, 30, 32, 33 | 18, 19, 28, 36, 37  |

Figure 4: Pinout description of the QFN 7x7-48L and HTSSOP-38 versions (top view)

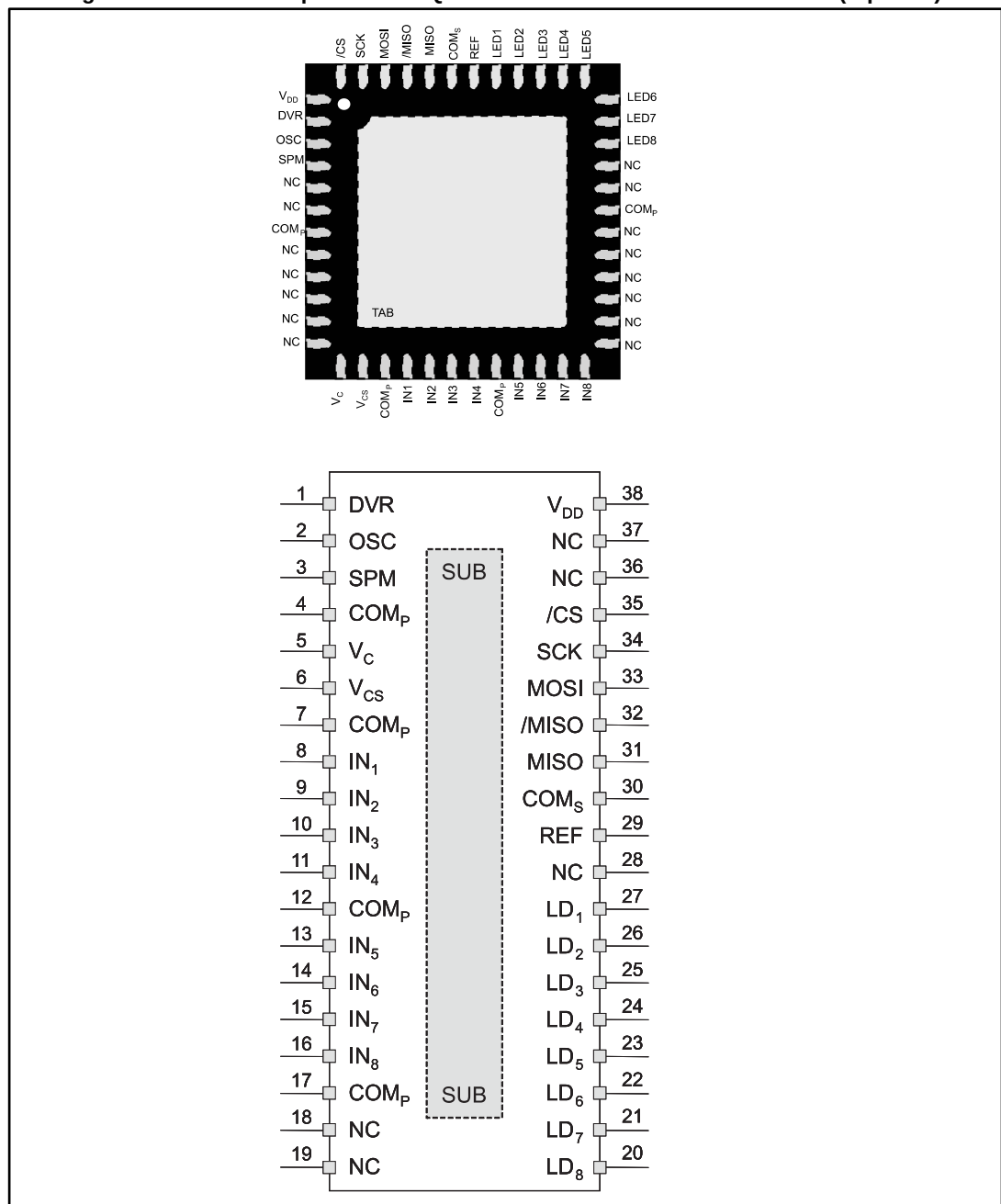
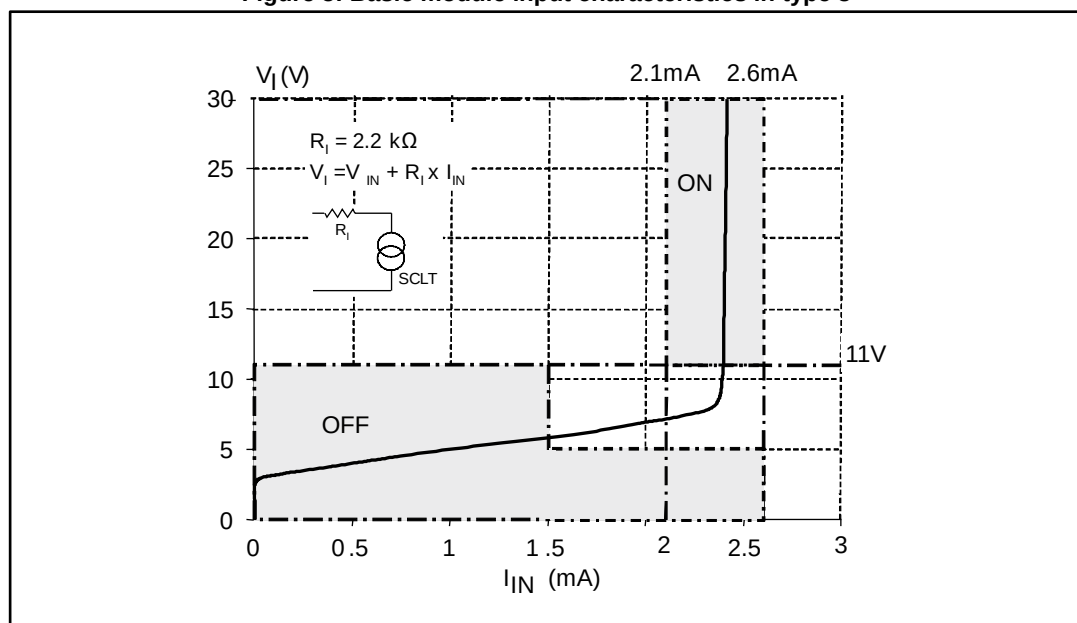


Figure 5: Basic module input characteristics in type 3



## 2 Characteristics

Table 2: Absolute maximum ratings

| Symbol           | Pin                | Parameter name                         | Conditions                      | Value                                   | Unit |
|------------------|--------------------|----------------------------------------|---------------------------------|-----------------------------------------|------|
| V <sub>CC</sub>  | V <sub>C</sub>     | Bus power supply DC voltage            | 500 Ω < R <sub>C</sub> < 2.2 kΩ | -35 <sup>(1)</sup> to 35 <sup>(2)</sup> | V    |
| V <sub>C</sub>   | V <sub>C</sub>     | Power supply voltage                   | R <sub>C</sub> = 0 kΩ           | -0.3 to 30                              | V    |
| I <sub>CC</sub>  | V <sub>C</sub>     | Maximum bus power supply current       |                                 | 15                                      | mA   |
| V <sub>CS</sub>  | V <sub>CS</sub>    | Sensing bus power supply voltage       |                                 | -0.3 to 6                               | V    |
| I <sub>DD</sub>  | V <sub>DD</sub>    | Maximum output power supply current    | R <sub>C</sub> = 500 Ω          | 12                                      | mA   |
| V <sub>I</sub>   | IN <sub>I</sub>    | Input steady state voltage, I = 1 to 8 | R <sub>I</sub> = 2.2 kΩ         | -35 to 35                               | V    |
| I <sub>IN</sub>  | IN <sub>I</sub>    | Input forward current range            |                                 | -20 to 10                               | mA   |
| I <sub>osc</sub> | OSC                | Maximum sourced oscillator current     |                                 | 120                                     | μA   |
| LV <sub>I</sub>  | SCK<br>/CS<br>MOSI | Logic input voltage                    |                                 | -0.3 to 6                               | V    |
| T <sub>stg</sub> |                    | Storage temperature range              |                                 | -40 to 150                              | °C   |
| T <sub>j</sub>   |                    | Ambient temperature range              |                                 | -40 to 105                              | °C   |

**Notes:**

<sup>(1)</sup>A reverse polarization diode must be placed on V<sub>CC</sub> in order to avoid leakage when -35 V is applied

<sup>(2)</sup>70 mm<sup>2</sup> of 35 μm thick copper is required for single layer FR4 PCB to have a low enough R<sub>th</sub> and therefore keep SCLT3 device below its T<sub>j</sub>(max)

Table 3: Operating conditions

| Symbol              | Pin                                 | Parameter name                            | Conditions                                               | Value                   | Unit |
|---------------------|-------------------------------------|-------------------------------------------|----------------------------------------------------------|-------------------------|------|
| V <sub>CC</sub>     | V <sub>C</sub>                      | Bus power supply DC voltage               | R <sub>C</sub> > 500 Ω                                   | 15 to 35 <sup>(1)</sup> | V    |
| V <sub>DD</sub>     | V <sub>DD</sub>                     | Internal logic power supply voltage       |                                                          | 5                       | V    |
| I <sub>DD</sub>     | V <sub>DD</sub>                     | Internal logic power supply voltage       | R <sub>C</sub> > 500 Ω                                   | 10                      | mA   |
| V <sub>I</sub>      | IN                                  | Input repetitive steady state voltage     | R <sub>I</sub> = 2.2 kΩ <sup>(2)</sup>                   | -30 to 35               | V    |
| V <sub>LD</sub>     | LD <sub>I</sub>                     | Maximum LED output voltage,<br>I = 1 to 8 |                                                          | 2.7                     | V    |
| F <sub>INmax</sub>  | IN                                  | Maximum single input frequency            | 8-bit mode                                               | 20                      | kHz  |
| F <sub>SCKmax</sub> |                                     | Maximum SPI clock frequency               |                                                          | 0.1 to 2                | MHz  |
| R <sub>OSC</sub>    | OSC                                 | Filter oscillator resistance range        |                                                          | 15 k to 1.5 M           | Ω    |
| LV                  | SCK<br>/CS<br>MOSI<br>MISO<br>/MISO | Logic input / output voltage              |                                                          | 0 to 5.5                | V    |
| T <sub>amb</sub>    | All                                 | Operating ambient temperature range       | V <sub>CC</sub> ≤ 30 V                                   | -40 to 85               | °C   |
|                     |                                     |                                           | V <sub>CC</sub> ≤ 24 V<br>R <sub>th(j-a)</sub> = 70 °C/W | -40 to 105              |      |
| T <sub>j</sub>      |                                     | Operating junction temperature range      |                                                          | -40 to 150              | °C   |

**Notes:**<sup>(1)</sup>32 V in DC; 35 V during 0.5 s max<sup>(2)</sup>V<sub>I</sub> = V<sub>IN</sub> + R<sub>I</sub> × I<sub>IN</sub>

Table 4: DC electrical characteristics based on figure 2 application environment

| Symbol                   | Pin             | Name                                                   | Conditions                 | Min.                  | Typ. | Max.                 | Unit |
|--------------------------|-----------------|--------------------------------------------------------|----------------------------|-----------------------|------|----------------------|------|
| Input current limitation |                 |                                                        |                            |                       |      |                      |      |
| I <sub>LIM</sub>         | IN              | V <sub>IN</sub> = 5.5 to 26 V, R <sub>I</sub> = 2.2 kΩ |                            | 2.1                   | 2.35 | 2.6                  | mA   |
| I <sub>ON</sub>          | LD <sub>I</sub> | On state LED current                                   | V <sub>I</sub> = 11 V      | 2                     |      |                      | mA   |
| Input digital filter     |                 |                                                        |                            |                       |      |                      |      |
| T <sub>OSC</sub>         | OSC             | Oscillator period                                      | R <sub>OSC</sub> = 51 kΩ   | 1.13                  |      | 1.37                 | μs   |
|                          |                 |                                                        | R <sub>OSC</sub> = 1200 kΩ | 20                    |      | 28                   | μs   |
| R <sub>OSC</sub>         | OSC             | Oscillator resistance                                  |                            | 51                    |      | 1200                 | kΩ   |
| t <sub>CKF</sub>         |                 | CKF period                                             | DVR = V <sub>DD</sub>      | 64 × T <sub>OSC</sub> |      |                      |      |
|                          |                 |                                                        | DVR = COM <sub>S</sub>     | 8 × T <sub>OSC</sub>  |      |                      |      |
| t <sub>FT</sub>          | IN              | Filtering time                                         |                            | 2 × t <sub>CKF</sub>  |      | 3 × t <sub>CKF</sub> |      |

**Table 5: SPI electrical characteristics ( $T_j = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 24\text{ V}$ ,  $V_{DD} = 5\text{ V}$  respect to COM ground pin; unless otherwise specified)**

| Symbol           | Pin            | Name                       | Conditions                                             | Min. | Typ. | Max. | Unit |
|------------------|----------------|----------------------------|--------------------------------------------------------|------|------|------|------|
| $F_{CK}$         | SCK            | Clock frequency            |                                                        |      |      | 2    | MHz  |
| $T_S$            | MOSI           | Data setup time            | MOSI toggling to SCK rising                            | 25   |      |      | ns   |
| $T_D$            | MISO           | Write out propagation time | SCK falling to MISO toggling, $C_{OUT} = 10\text{ pF}$ |      |      | 50   | ns   |
| $T_{LD}$         | SCK            | Enable lead time           | /CK falling to SCK rising                              | 80   |      |      | ns   |
| $T_{HC}$         | SCK            | Clock hold time            | SCK falling to /CS rising                              | 160  |      |      | ns   |
| $T_{DT}$         | /CS            | Transfer delay time        | /CS rising to /CS falling                              |      |      | 150  | ns   |
| $T_H$            | MOSI           | Data hold time             | SCK rising to MOSI toggling                            | 25   |      |      | ns   |
| $T_{DIS}$        | MISO           | Data output disable time   | /CS rising to MISO disabled                            |      |      | 200  | ns   |
| $LV_{IH}$        | MOSI, SCK, /CS | Logic input high voltage   | Share of $V_{DD}$                                      |      |      | 70   | %    |
| $LV_{IL}$        |                | Logic input low voltage    | Share of $V_{DD}$                                      | 30   |      |      | %    |
| $LV_{OH}$        | MISO, /MISO    | Logic output high voltage  | $I_{OH} = 3\text{ mA}$                                 | 4    | 4.75 |      | V    |
| $LV_{OL}$        |                | Logic output low voltage   | $I_{OL} = 3\text{ mA}$                                 |      | 0.25 | 1    | V    |
| $T_{RO}, T_{FO}$ | MISO, /MISO    | MISO signal fall/rise time | $I_{MISO} = 3\text{ mA}$                               |      | 20   |      | ns   |
| $T_A$            | MISO           | Output access time         | /CS falling to MISO toggling                           |      | 40   | 80   | ns   |
| $DuCy$           | SCK            | Clock duty cycle           |                                                        | 25   |      | 75   | %    |

**Figure 6: Time diagram**

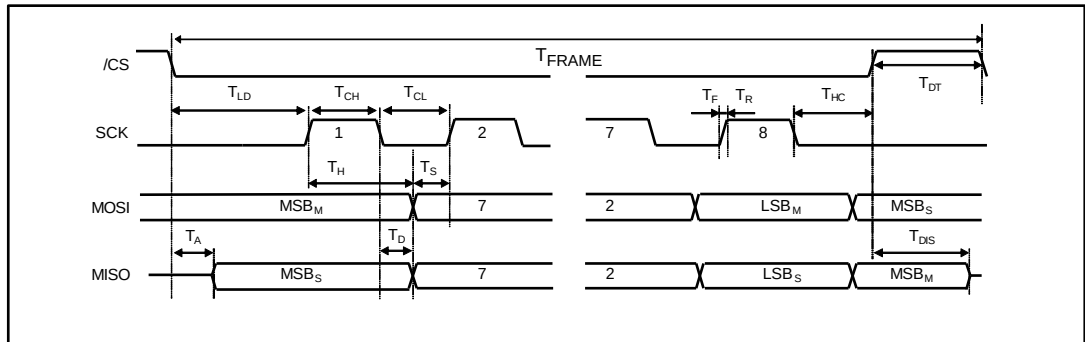




Table 6: Electromagnetic compatibility ratings

| Symbol           | Pin             | Parameter name <sup>(1)</sup>                               | Value   | Unit |
|------------------|-----------------|-------------------------------------------------------------|---------|------|
| V <sub>PPB</sub> | V <sub>I</sub>  | Peak pulse voltage burst, IEC61000-4-4 <sup>(2)</sup>       | 4       | kV   |
| V <sub>PP</sub>  | V <sub>I</sub>  | Peak pulse voltage surge, IEC61000-4-5                      | 1       | kV   |
| V <sub>PP</sub>  | V <sub>CC</sub> | Peak pulse voltage surge, IEC61000-4-5                      | 2.5     | kV   |
| V <sub>ESD</sub> | V <sub>IN</sub> | ESD protection, IEC 61000-4-2, per input:<br>Air<br>Contact | 15<br>8 | kV   |

**Notes:**

<sup>(1)</sup> Test set-up, see application

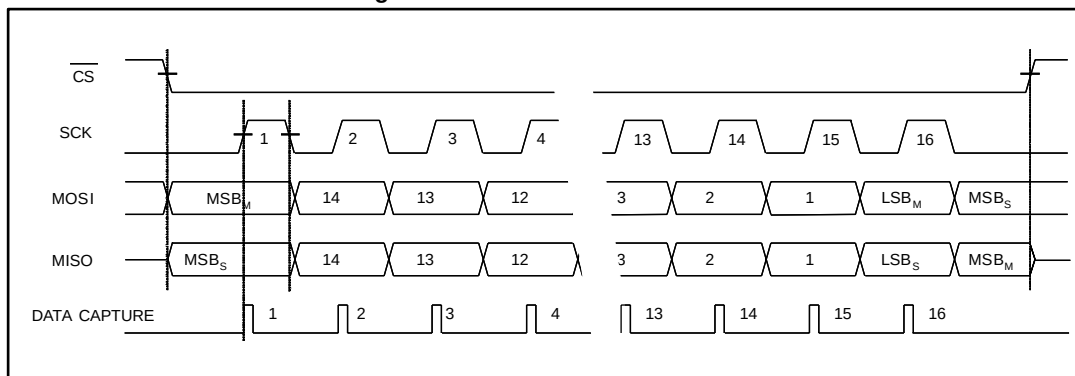
<sup>(2)</sup> See [AN3031](#).

## 3 Functional description

### 3.1 Operation of the SCLT3 with SPI bus ( $C_{POL} = 0$ , $C_{PHA} = 0$ )

The SPI bus master controller manages the data transfer with the chip select signal /CS and controls the data shift in the register with the clock SCK signal.

Figure 7: Serial data format frame



The transfer of the SCLT3 input states in the SPI registers starts when the chip select /CS signal falls and ends when this /CS is rising back.

The transfer of data out of the SCLT3 slave MISO output starts immediately when the chip select /CS goes low.

Then, the input MOSI is captured and presented to the shift register on each rising edge of the clock SCK. And the data are shifted in this register on each falling edge of the serial clock SCK, the data bits being written on the output MISO with the most significant bit first.

#### 3.1.1 The serial data Input MOSI

This input signal MOSI is used to shift external data bits into the SCLT3 register from the most significant MSB bit to the lower significant one LSB. The data bits are captured by the SCLT3 on the rising edge of the serial clock signal SCK.

### 3.2 The input digital filter

Depending on the biasing of the SPM pin, the data frame is 8-bits or 16-bits.

A digital filter is implemented between the input state comparator and the input state register. It consists of a 2-step sampling circuit that is controlled by an oscillator as shown on Figure 7.

The filtering time  $t_{FT}$  is set by the external oscillator resistor and is a function of the oscillator period  $t_{CKF}$ :

- $2 \times t_{CKF} < t_{FT} < 3 \times t_{CKF}$
- $t_{CKF} = \text{Divider ratio} \times t_{OSC} (R_{OSC})$

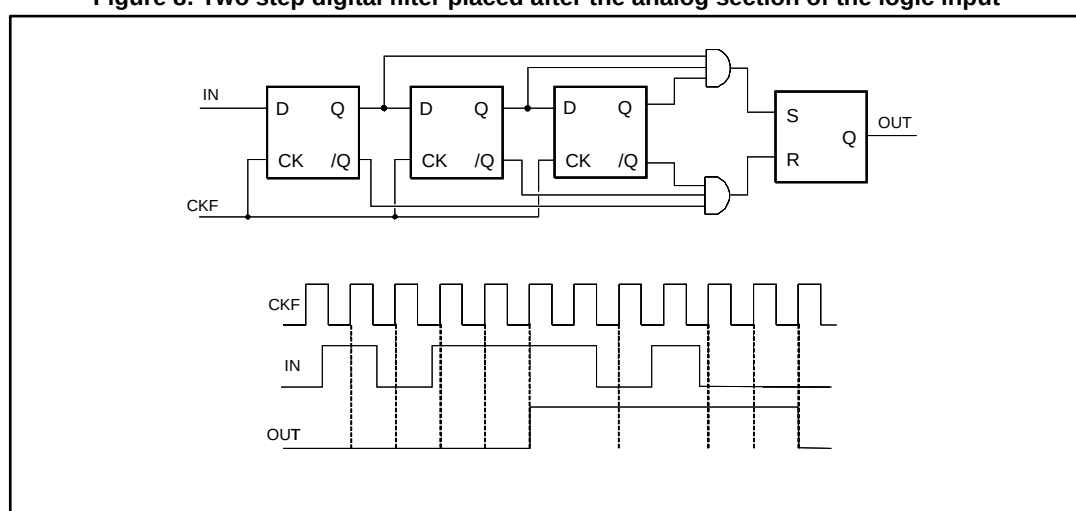
This period can be adjusted between 20  $\mu\text{s}$  and 3000  $\mu\text{s}$  as shown on [Table 6: "Electromagnetic compatibility ratings"](#).

Table 7: Typical setting of the digital filter timings

| Input speed                          | Fast             |                  | Medium          | Slow            |
|--------------------------------------|------------------|------------------|-----------------|-----------------|
| Input frequency (kHz)                | 60               | 20               | 5               | 0.3             |
| Min. filter time $t_{FT}$ ( $\mu$ s) | 20               | 50               | 230             | 3000            |
| OSC resistance (k $\Omega$ )         | 51               | 150              | 82              | 1300            |
| CKF period $t_{CKF}$ ( $\mu$ s)      | 10               | 25               | 115             | 1500            |
| DVR connection                       | COM <sub>S</sub> | COM <sub>S</sub> | V <sub>DD</sub> | V <sub>DD</sub> |
| Divider ratio                        | 8                | 8                | 64              | 64              |

Being placed in the front end of the module, this filter increases the transient immunity of the SCLT and its SPI logic circuitry. It also simplifies the input management software task of the ASIC controller.

Figure 8: Two step digital filter placed after the analog section of the logic input



### 3.3 The SPI data transfer operation

#### 3.3.1 The SPI data frame

Depending on the biasing of the SPM pin, the data frame is 8-bits or 16-bits. The selected structure of the SPI is a 16-bit word in order to be able to implement the input state data and some control bits such as the UVA alarm, the 4 checksum bits and the two low and high state stop bits.

#### 3.3.2 The SPI data transfer

The SCLT3 transfers its 16 data bits through the SPI within one chip select Hi-Lo-Hi sequence. So, this length defines the minimum length that the shift register of the SPI master controller is able to capture: 16 bits.

The Table 8 shows the 16-bit mode way the data are transferred starting from the data bits, the control bits and ending by a stop bit.

Table 8: SPI data transfer organization versus CLT input states with SPM = 0

| Bit #   | LSB                 | Bit 1 | Bit 2  | Bit 3  | Bit 4  | Bit 5  | Bit 6  | Bit 7               |
|---------|---------------------|-------|--------|--------|--------|--------|--------|---------------------|
| Control | High <sup>(1)</sup> | Low   | PC4    | PC3    | PC2    | PC1    | /OTA   | /UVA                |
| Bit #   | Bit 8               | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | MSB                 |
| Data    | IN 1                | IN 2  | IN 3   | IN 4   | IN 5   | IN 6   | IN 7   | IN 8 <sup>(2)</sup> |

**Notes:**<sup>(1)</sup>Last OUT<sup>(2)</sup>First OUT

### 3.4 Control bit signals of the SPI transferred data frame

#### 3.4.1 The power bus voltage monitoring

The UVA circuit generates the alarm /UVA that is active low when the power bus voltage is lower than the activation threshold  $V_{CON}$ , 17 V typical, and it is disabled high when the power bus voltage rises above the threshold  $V_{COFF}$ , 18 V typical.

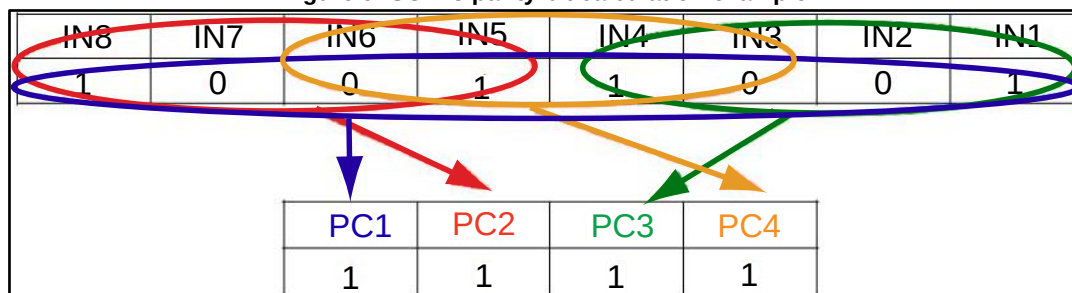
#### 3.4.2 The over temperature alarm

The alarm signal /OTA is enabled, low state active, when the junction temperature is higher than the activation threshold  $T_{ON}$ , 150 °C typical, and it is disabled when the junction temperature falls below the threshold  $T_{OFF}$ , 140 °C typical.

#### 3.4.3 The parity checksum bits calculation and transfer

The aim of the parity checksum bit is to detect one error in the transferred SPI word. Several parity checksum bits are generated and transmitted through the SPI on the control bit #2 to #5. In order to calculate parity bit, "exclusive NOR" operations are performed as follow:

Figure 9: SCLT3 parity bit calculation example



### 3.5 Loss of VCC power supply

The operation of the SCLT3 is extended below the levels required in the IEC 61131-2 standard to allow the implementation of the under voltage alarm UVA as described the SPI control bit section.

If there is no more power feeding on the  $V_{CC}$  input, the SCLT3 chip goes to sleep mode, and the MISO output is forced in low state during SPI transfer attempt. The last SPI control data bit is a stop bit placed normally in high state all time: the loss of power supply is detected by checking its state: if low, the output is disabled by the internal power reset POR.

This POR signal is active in low state when  $V_C$  is less than 9 V or the internal power supply  $V_{DD}$  is less than 3.25 V.

**Table 9: Logic state of the SPI output versus the power loss signal POR and the SPI chip select /CS**

| POR | /CS | MISO | /MISO | SPI status                            |
|-----|-----|------|-------|---------------------------------------|
| 1   | 1   | Z    | Z     | Normal with no communication          |
| 1   | 0   | 1    | 0     | Normal with communication             |
| 1   | 0   | 0    | 1     | Normal with communication             |
| 0   | 1   | Z    | Z     | Power loss with no communication      |
| 0   | 0   | 0    | 1     | Power loss with communication attempt |

**Figure 10: Logic status of the SCLT3 power supply**

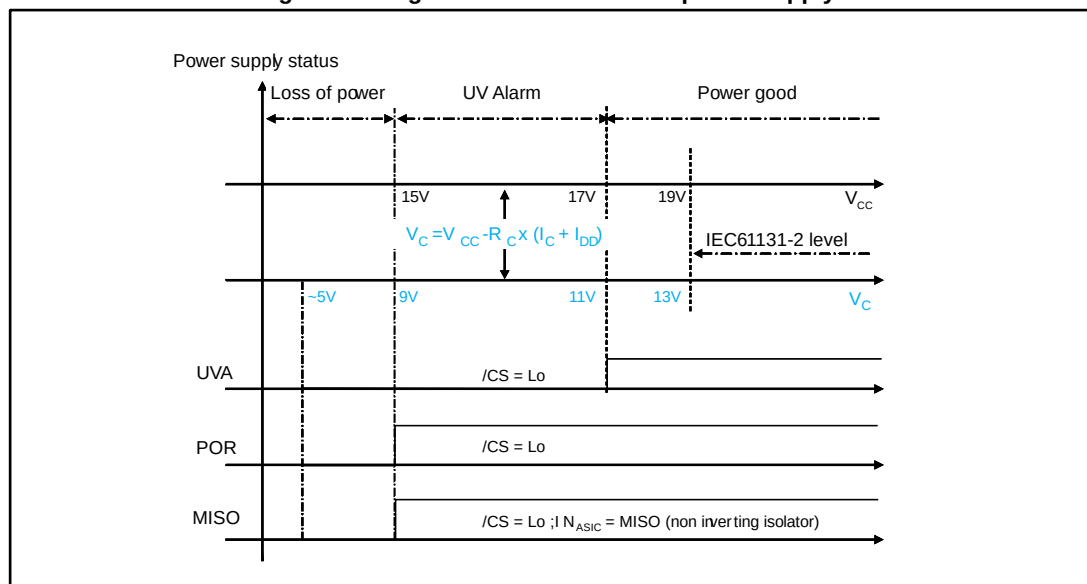


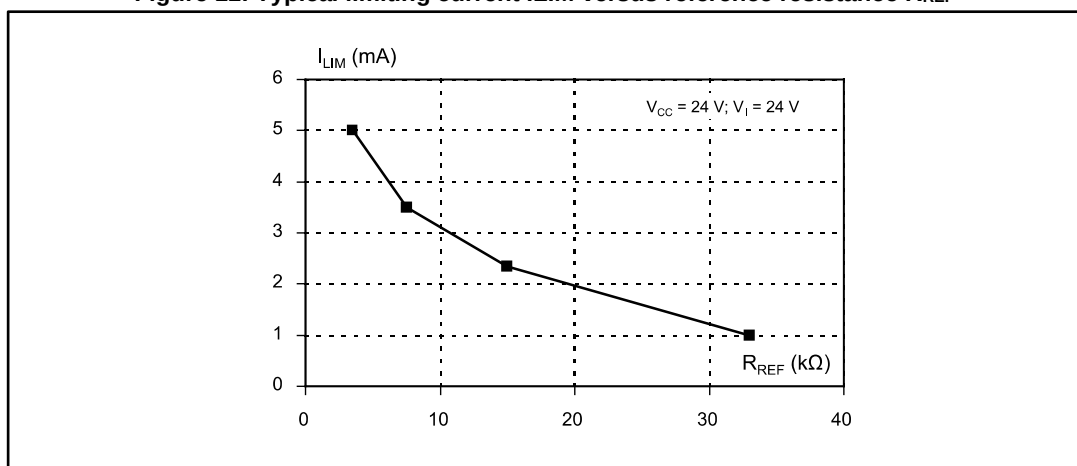
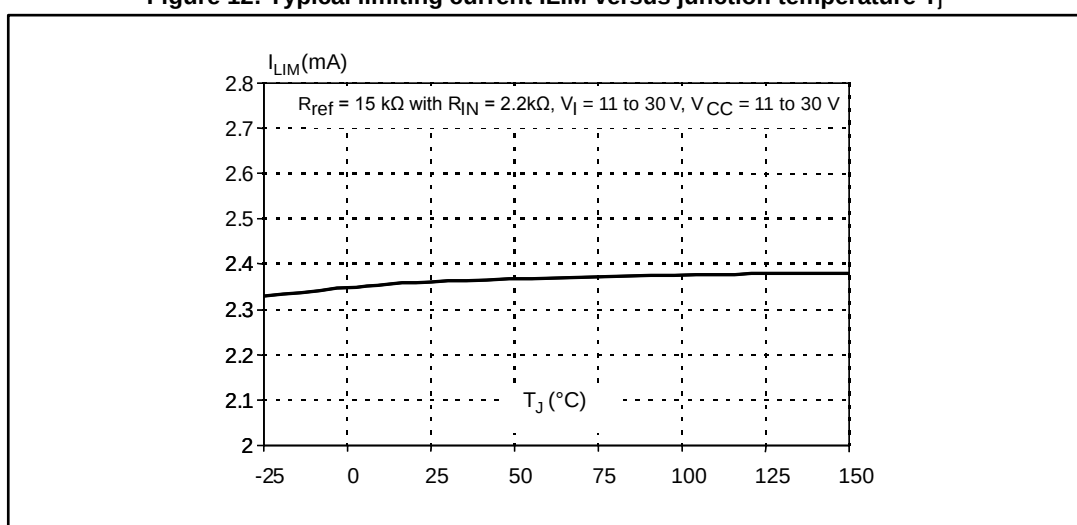
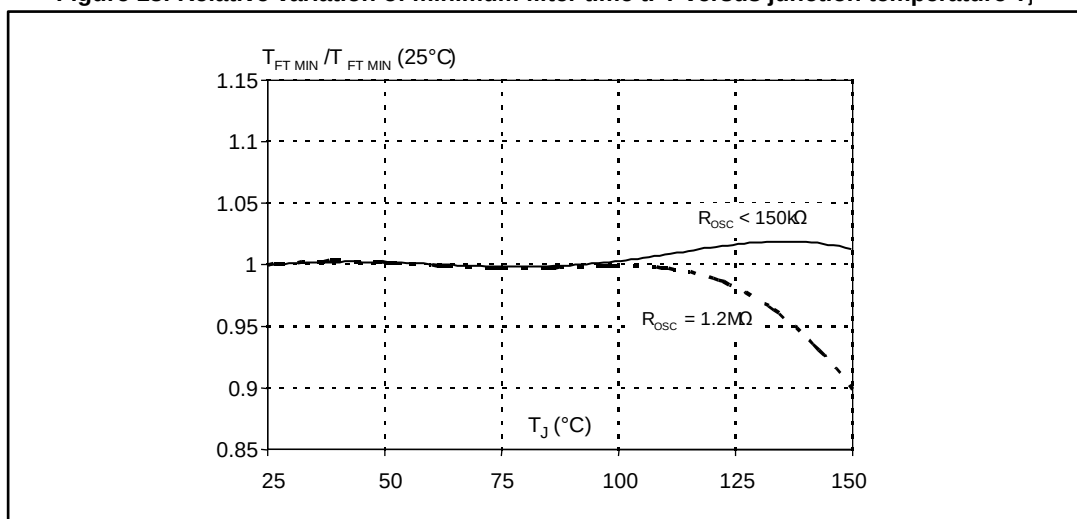
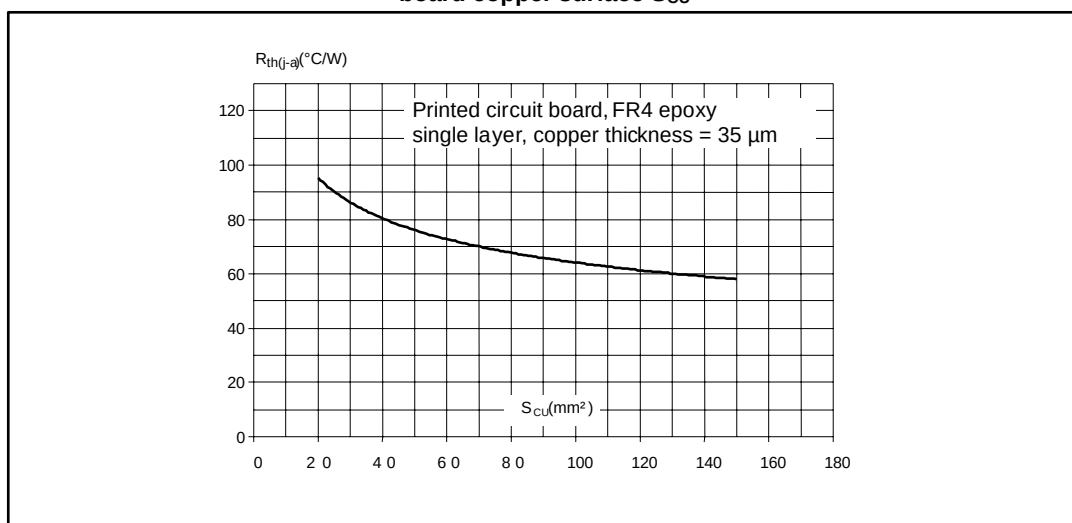
Figure 11: Typical limiting current  $I_{LIM}$  versus reference resistance  $R_{REF}$ Figure 12: Typical limiting current  $I_{LIM}$  versus junction temperature  $T_J$ Figure 13: Relative variation of minimum filter time  $t_{FT}$  versus junction temperature  $T_J$ 

Figure 14: Variation of junction to ambient thermal resistance  $R_{th(j-a)}$  versus printed circuit board copper surface  $S_{Cu}$



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 QFN 7X7-48 L package information

Figure 15: QFN 7X7-48 L package outline

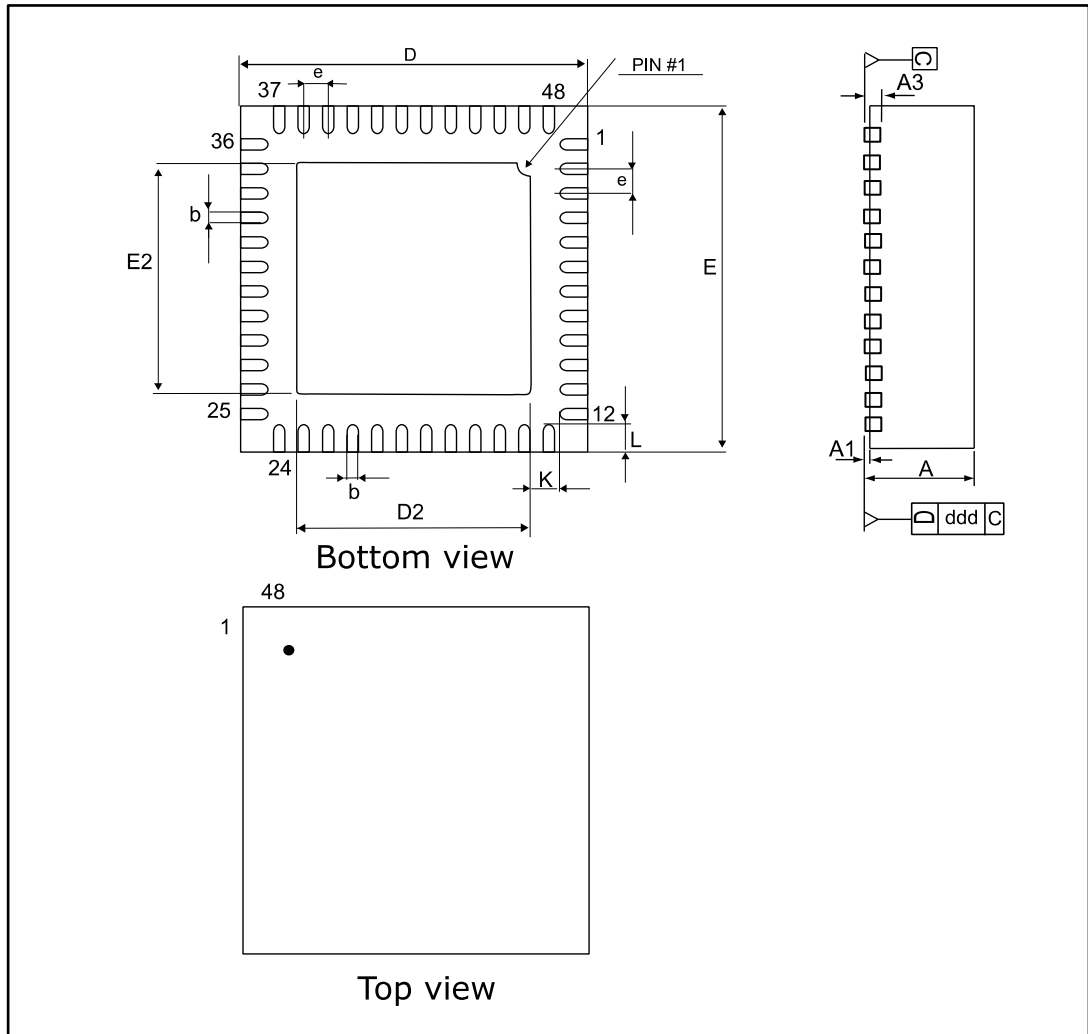




Table 10: QFN 7X7-48 L package mechanical data

| Ref. | Dimensions  |       |      |                       |        |        |
|------|-------------|-------|------|-----------------------|--------|--------|
|      | Millimeters |       |      | Inches <sup>(1)</sup> |        |        |
|      | Min.        | Typ.  | Max. | Min.                  | Typ.   | Max.   |
| A    | 0.80        | 0.90  | 1.00 | 0.0315                | 0.0354 | 0.0394 |
| A1   |             | 0.02  | 0.05 |                       | 0.0008 | 0.0020 |
| A3   |             | 0.203 |      |                       | 0.008  |        |
| b    | 0.18        | 0.25  | 0.30 | 0.0071                | 0.0100 | 0.0118 |
| D    |             | 7.00  |      |                       | 0.275  |        |
| E    |             | 7.00  |      |                       | 0.275  |        |
| e    |             | 0.50  |      |                       | 0.019  |        |
| D2   | 5.00        | 5.15  | 5.25 | 0.197                 | 0.203  | 0.206  |
| E2   | 5.00        | 5.15  | 5.25 | 0.197                 | 0.203  | 0.206  |
| K    | 0.20        |       |      | 0.008                 |        |        |
| L    | 0.30        | 0.40  | 0.50 | 0.011                 | 0.015  | 0.019  |

**Notes:**

<sup>(1)</sup>Values in inches are converted from mm and rounded to 4 decimal digits.

## 4.2 HTSSOP-38 package information

Figure 16: HTSSOP-38 package outline

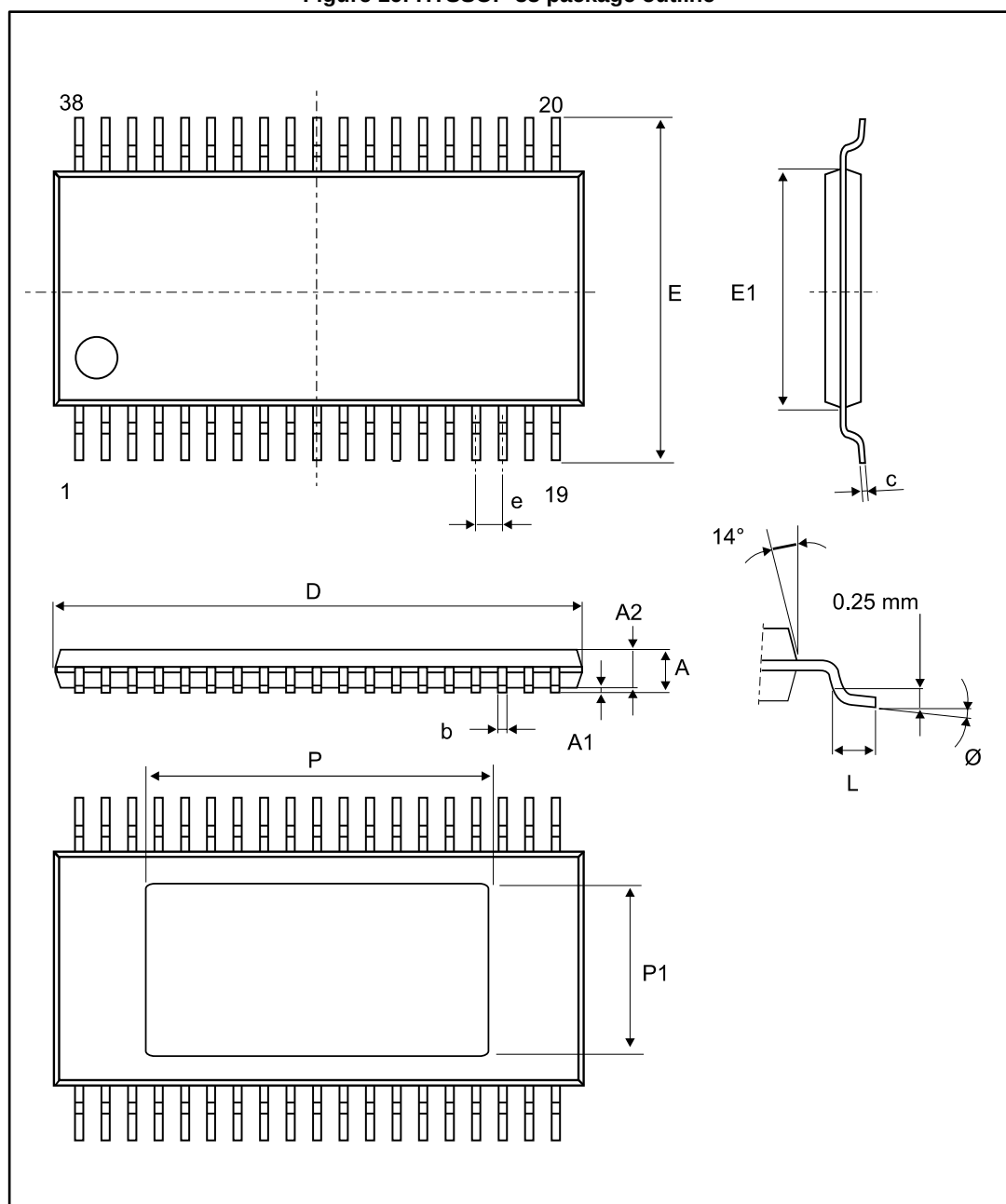
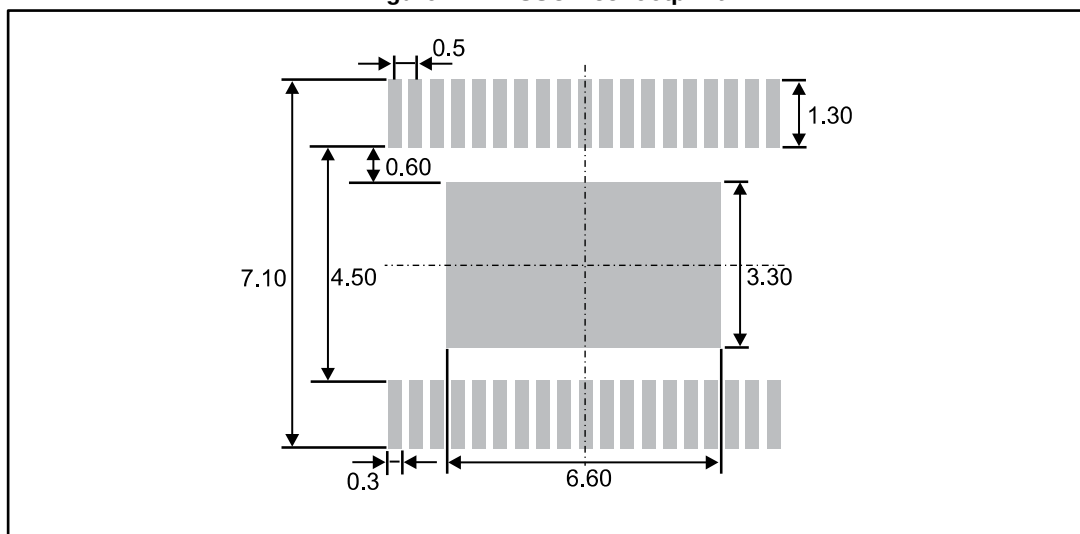


Table 11: HTSSOP-38 package mechanical data

| Ref. | Dimensions  |      |      |        |       |       |
|------|-------------|------|------|--------|-------|-------|
|      | Millimeters |      |      | Inches |       |       |
|      | Min.        | Typ. | Max. | Min.   | Typ.  | Max.  |
| A    |             |      | 1.10 |        |       | 0.043 |
| A1   | 0.05        |      | 0.15 | 0.002  |       | 0.006 |
| A2   | 0.85        | 0.90 | 0.95 | 0.033  | 0.035 | 0.037 |
| b    | 0.17        |      | 0.27 | 0.007  |       | 0.011 |
| c    | 0.09        |      | 0.20 | 0.003  |       | 0.008 |
| D    | 9.60        | 9.70 | 9.80 | 0.378  | 0.382 | 0.386 |
| E1   | 4.30        | 4.40 | 4.50 | 0.169  | 0.173 | 0.177 |
| e    |             | 0.50 |      |        | 0.020 |       |
| E    |             | 6.40 |      |        | 0.252 |       |
| L    | 0.50        | 0.60 | 0.70 | 0.020  | 0.024 | 0.027 |
| P    | 6.40        | 6.50 | 6.60 | 0.252  | 0.256 | 0.260 |
| P1   | 3.10        | 3.20 | 3.30 | 0.122  | 0.126 | 0.130 |
| Ø    | 0°          |      | 8°   | 0°     |       | 8°    |

Figure 17: HTSSOP-38 footprint



## 5 Ordering information

Figure 18: Ordering information scheme

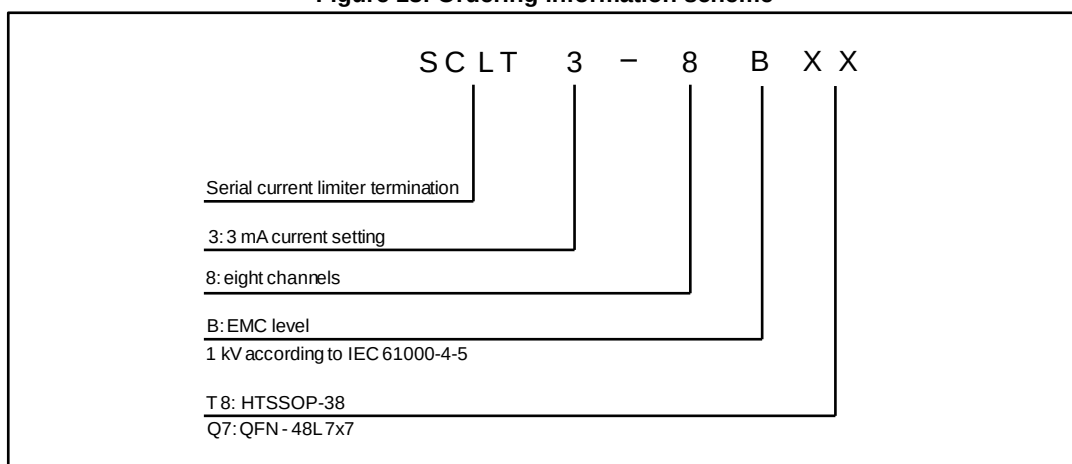


Table 12: Ordering information

| Order code    | Marking    | Package    | Weight | Base qty. | Delivery mode |
|---------------|------------|------------|--------|-----------|---------------|
| SCLT3-8BT8-TR | SCLT3-8BT8 | HTSSOP-38  | 114 mg | 2500      | Tape and reel |
| SCLT3-8BQ7-TR | SCLT3-8BQ7 | QFN7x7-48L | 130 mg | 2500      | Tape and reel |

## 6 Revision history

Table 13: Document revision history

| Date        | Revision | Changes                                                                                                              |
|-------------|----------|----------------------------------------------------------------------------------------------------------------------|
| 29-Jul-2016 | 1        | Initial release.                                                                                                     |
| 12-Nov-2015 | 2        | Updated <i>Table 4</i> .                                                                                             |
| 05-Dec-2016 | 3        | Added part number previously included in the datasheet DocID15191. Updated document accordingly. Minor text changes. |

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