

## DIFFERENTIAL VIDEO AMPLIFIER

### FEATURES

- Adjustable Gain to 400 (Typ)
- No Frequency Compensation Required
- Low Noise . . . 3-mV  $V_n$  (Typ)

### DESCRIPTION

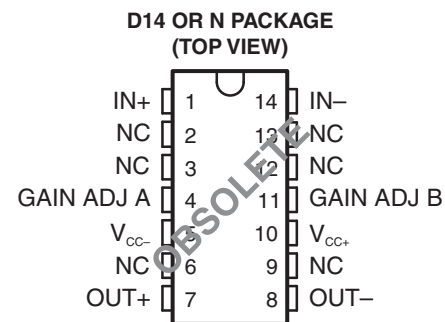
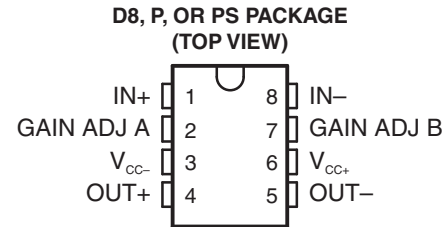
This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted for near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

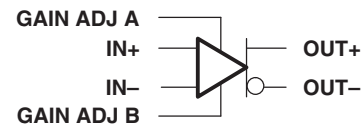
The TL592B is characterized for operation from 0°C to 70°C.



NC – No internal connection

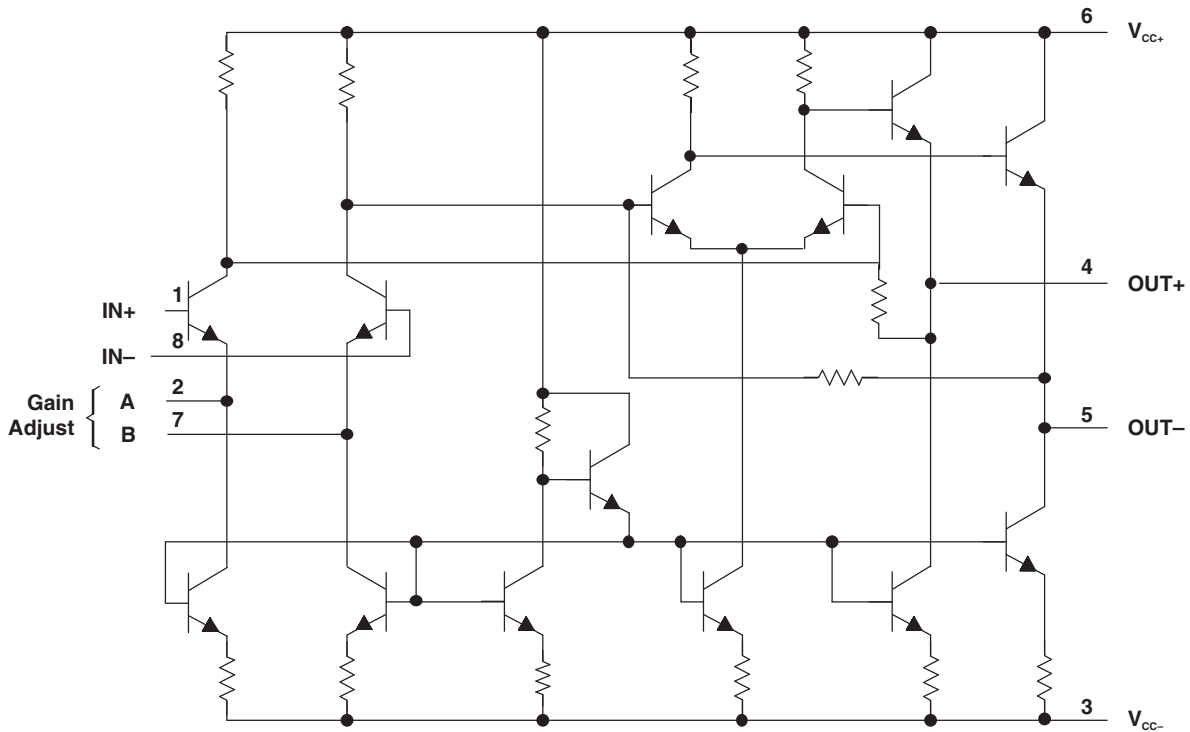
Note: D8 and D14 are the codes to differentiate the 8-pin and 14-pin versions, respectively.

### SYMBOL



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**SCHEMATIC**



NOTE: Pin numbers shown are for D, P, and PS packages.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

$V_{CC+}$	Positive supply voltage	8 V
$V_{CC-}$	Negative supply voltage	-8 V
$V_{DI}$	Differential input voltage	$\pm 5$ V
$V_I$	Voltage range, any input	$V_{CC+}$ to $V_{CC-}$
$I_O$	Output current	10 mA
$P_D$	Continuous total power dissipation	See Dissipation Rating Table
$T_A$	Operating free-air temperature range	0°C to 70°C
$T_{stg}$	Storage temperature range	-65°C to 150°C
$T_{lead}$	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential input voltages are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .

**DISSIPATION RATINGS**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE $T_A$	$T_A = 70^\circ\text{C}$ POWER RATING
D8	530 mW	5.8 mW/°C	59	464 mW
D14	530 mW	N/A	N/A	530 mW
N	530 mW	N/A	N/A	530 mW
P	530 mW	N/A	N/A	530 mW
PS	530 mW	N/A	N/A	530 mW

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{CC+}$	Positive supply voltage	3	6	8	V
$V_{CC-}$	Negative supply voltage	-3	-6	-8	V
$T_A$	Operating free-air temperature	0		70	°C

## ELECTRICAL CHARACTERISTICS

 at specified free-air temperature,  $V_{CC\pm} = \pm 6$  V,  $R_L = 2$  k $\Omega$  (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS <sup>(1)</sup>	$T_A$	MIN	TYP	MAX	UNIT
$A_{VD}$	1	$V_{OPP} = 3$ V, $R_L = 2$ k $\Omega$	25°C	300	400	500	V/V
			0°C to 70°C	250		600	
			25°C		13		
BW	2	$V_{OPP} = 1$ V, $R_{AB} = 0$	25°C		50		MHz
$I_{IO}$			25°C		0.4	5	$\mu$ A
			0°C to 70°C			6	
$I_{IB}$			25°C		9	30	$\mu$ A
			0°C to 70°C			40	
$V_{ICR}$	3		25°C	$\pm 1$			V
			0°C to 70°C	$\pm 1$			
$V_{OC}$	1	$R_L = \infty$	25°C	2.4	2.9	3.4	V
$V_{OO}$	1	$V_{ID} = 0$ , $R_{AB} = \infty$ , $R_L = \infty$	25°C		0.35	0.75	V
			0°C to 70°C			1.5	
$V_{OPP}$	1	$R_L = 2$ k $\Omega$ , $R_{AB} = 0$	25°C	3	4		V
			0°C to 70°C	2.8			
$r_i$		$V_{OD} = 1$ V, $R_{AB} = 0$	25°C		4		k $\Omega$
			0°C to 70°C			3.6	
$r_o$			0°C to 70°C			30	$\Omega$
$C_i$			0°C to 70°C		5		pF
CMRR	3	$V_{IC} = \pm 1$ V, $R_{AB} = 0$	25°C	60	86		dB
					60		
			0°C to 70°C	50			
					60		
$k_{SVR}$	4	$\Delta V_{CC+} = \pm 0.5$ V, $\Delta V_{CC-} = \pm 0.5$ V, $R_{AB} = 0$	25°C	50	70		dB
			0°C to 70°C	50			
$V_n$	4	BW = 1 kHz to 10 MHz	25°C		3		$\mu$ V
$t_{pd}$	2	$\Delta V_O = 1$ V	25°C		7.5		ns
$t_r$	2	$\Delta V_O = 1$ V	25°C		10.5		ns
$I_{sink(max)}$		$V_{ID} = 1$ V, $V_O = 3$ V		3	4		mA
$I_{CC}$		No load, No signal	25°C		18	24	mA
			0°C to 70°C			27	

(1)  $R_{AB}$  is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.

PARAMETER MEASUREMENT INFORMATION

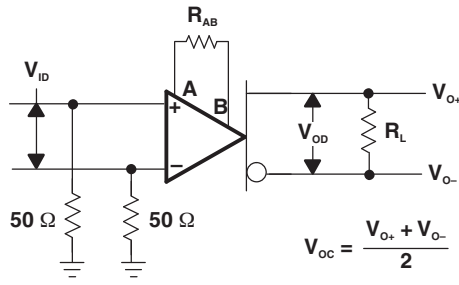


Figure 1.

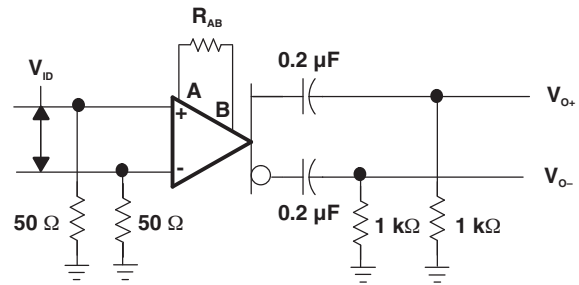


Figure 2.

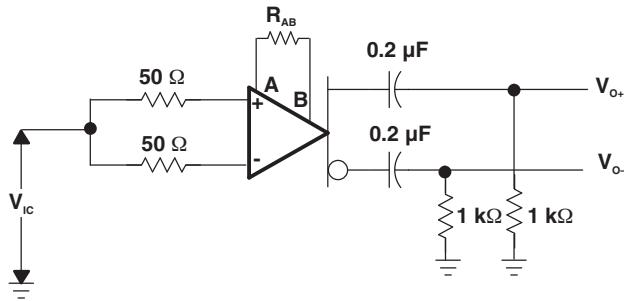


Figure 3.

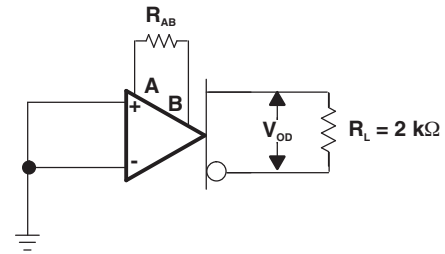


Figure 4.

TYPICAL CHARACTERISTICS

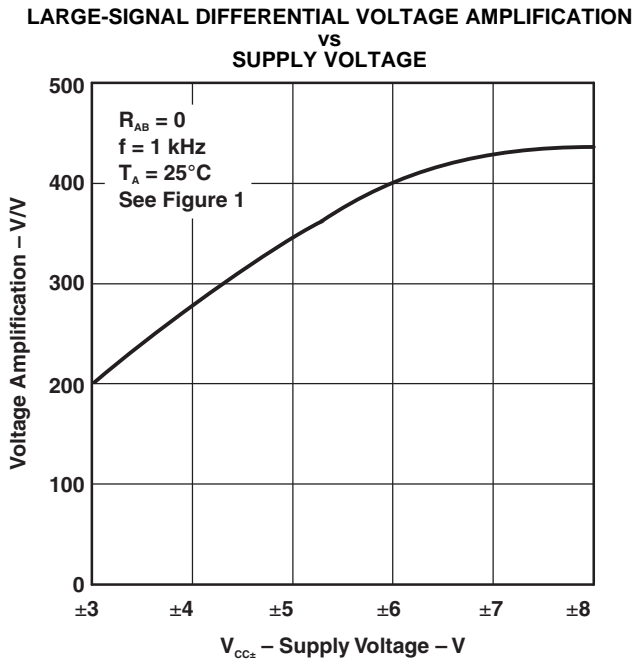


Figure 5.

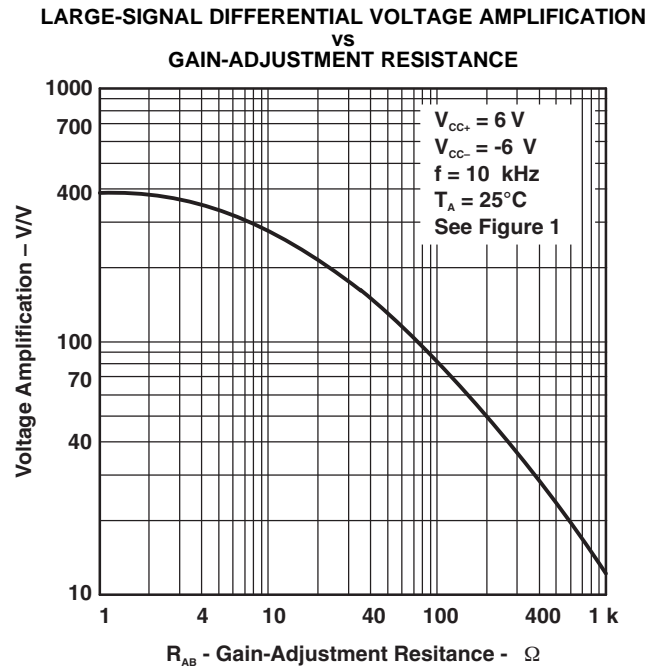


Figure 6.

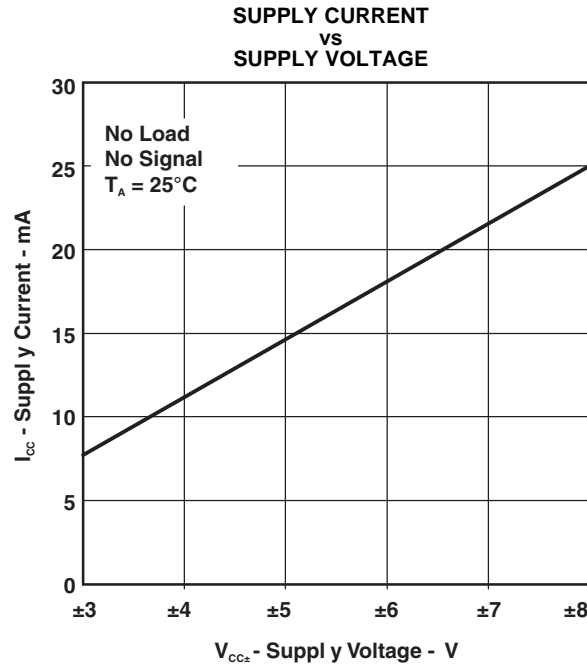


Figure 7.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL592B-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL592B	<a href="#">Samples</a>
TL592B-8DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL592B	<a href="#">Samples</a>
TL592BP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL592BP	<a href="#">Samples</a>
TL592BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T592B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL592B-8DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL592B-8DR	SOIC	D	8	2500	340.5	338.1	20.6



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4212188/A 09/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated