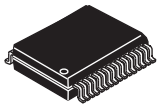
Document Number: MC33395
Rev 4.0, 2/2007

Three-Phase Gate Driver IC

33395
33395T

THREE-PHASE GATE DRIVER IC



DWB SUFFIX
EW SUFFIX (Pb-FREE)
98ARH99137A
32-PIN SOICW

The 33395 simplifies the design of high-power BLDC motor control design by combining the gate drive, charge pump, current sense, and protection circuitry necessary to drive a three-phase bridge configuration of six N-channel power MOSFETs. Mode logic is incorporated to route a pulse width modulation (PWM) or a complementary PWM output signal to either low-side or high-side MOSFETs of the bridge.

Detection and drive circuitry are also incorporated to control a reverse battery protection high-side MOSFET switch. PWM frequencies up to 28 kHz are possible. Built-in protection circuitry prevents damage to the MOSFET bridge as well as the drive IC and includes overvoltage shutdown, overtemperature shutdown, overcurrent shutdown, and undervoltage shutdown.

The device is parametrically specified over ambient temperature range of -40°C ≤ T_A ≤ 125°C and 5.5 V ≤ V_{IGN} ≤ 24 V supply.

Features

- Drives Six N-Channel Low $R_{DS(ON)}$ Power MOSFETs
- Built-In Charge Pump Circuitry
- Built-In Current Sense Comparator and Output Drive Current Limiting
- Built-In PWM Mode Control Logic
- Built-In Circuit Protection
- Designed for Fractional to Integral HP BLDC Motors
- 32-Pin SOIC Wide Body Surface Mount Package
- 33395 Incorporates a <5.0 µs Shoot-Through Suppression Timer
- 33395T Incorporates a <1.0 µs Shoot-Through Suppression Timer
- Pb-Free Packaging Designated by Suffix Code EW

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33395DWB/R2	-40°C to 125°C	32 SOICW
MC33395EW/R2		32 SOICW (Pb-Free)
MCZ33395EW/R2		
MC33395TDWB/R2		32 SOICW
MC33395TEW/R2		32 SOICW (Pb-Free)

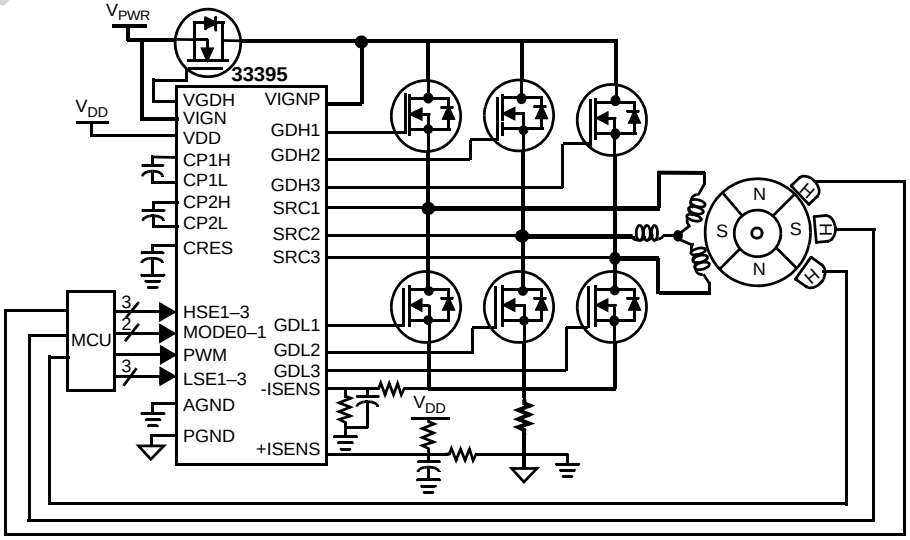


Figure 1. 33395 Simplified Application Diagram

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* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

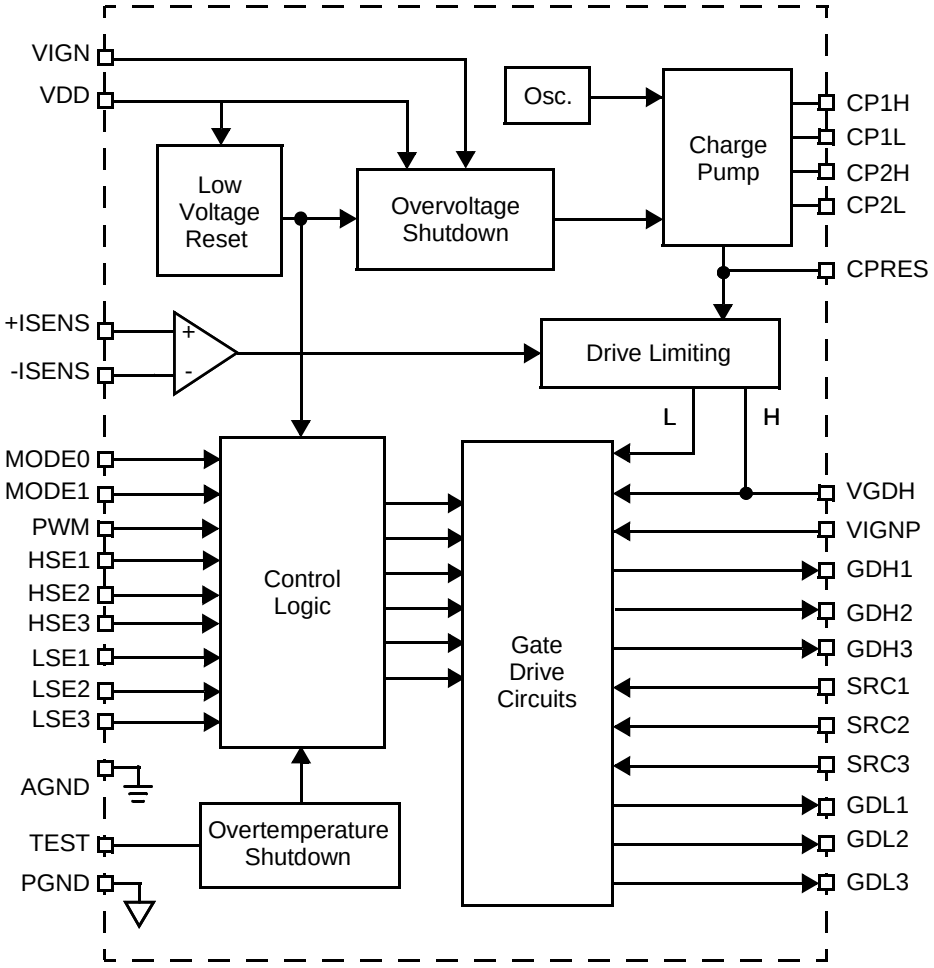


Figure 2. 33395 Simplified Internal Block Diagram

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PIN CONNECTIONS

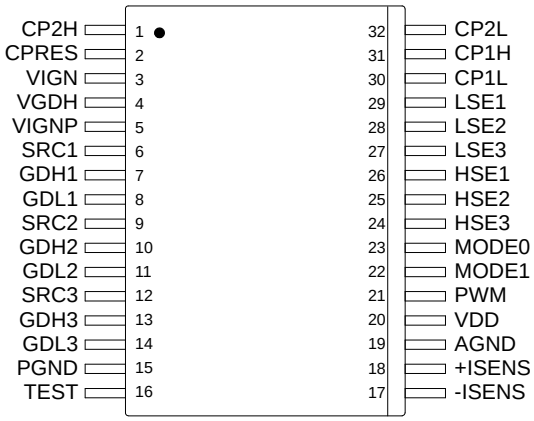


Figure 3. 33395 Pin Connections

Table 1. 33395 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 9.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	CP2H		Charge Pump Cap	High potential pin connection for secondary charge pump capacitor
2	CPRES	Input	Charge Pump Reserve Cap	Input from external reservoir capacitor for charge pump
3	VIGN	Input	Input Voltage	Input from ignition level supply voltage for power functions
4	VGDH	Output	High-Side Gate Voltage	Output full-time gate drive for auxiliary high-side power MOSFET switch
5	VIGNP	Input	Input Voltage Protected	Input from protected ignition level supply for power functions
6	SRC1	Sensor	High-Side Sense	Sense for high-side source voltage, phase 1
7	GDH1	Output	Gate Drive High	Output for gate high-side, phase 1
8	GDL1	Output	Output for Gate	Output for gate drive low-side, phase 1
9	SRC2	Sensor	High-Side Sense	Sense for high-side source voltage, phase 2
10	GDH2	Output	Gate Drive High	Output for gate high-side, phase 2
11	GDL2	Output	Output for Gate	Output for gate drive low-side, phase 2
12	SRC3	Sensor	High-Side Sense	Sense for high-side source voltage, phase 3
13	GDH3	Output	Gate Drive High	Output for gate drive high-side, phase 3
14	GDL3	Output	Gate Drive Low	Output for gate drive low-side, phase 3
15	PGND	Ground	Power Ground	Ground pins for power functions
16	Test	N/A	Test Pin	This should be connected to ground or left open
17	-ISENS	Input	IS Minus	Inverting input for current limit comparator
18	+ISENS	Input	IS Plus	Non-inverting input for current limit comparator
19	AGND	Ground	Analog Ground	Ground pin for logic functions
20	VDD	Power	Logic Supply Voltage	Supply voltage for logic functions
21	PWM	Input	Pulse Width Modulator	Input for pulse width modulated driver duty cycle

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Table 1. 33395 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 9.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
22	MODE1	Input	Mode Control Bit 1	Input for mode control selection
23	MODE0	Input	Mode Control Bit 0	Input for mode control selection
24	HSE3	Input	High-Side Enable	Input for high-side enable logic, phase 3
25	HSE2	Input	High-Side Enable	Input for high-side enable logic, phase 2
26	HSE1	Input	High-Side Enable	Input for high-side enable logic, phase 1
27	LSE3	Input	Low-Side Enable	Input for low-side enable logic, phase 3
28	LSE2	Input	Low-Side Enable	Input for low-side enable logic, phase 2
29	LSE1	Input	Low-Side Enable	Input for low-side enable logic, phase 1
30	CP1L	Input	External Pump Capacitor	Input from external pump capacitor for charge pump and secondary pins
31	CP1H	Input	External Pump Capacitor	Input from external pump capacitor for charge pump and secondary pins
32	CP2L	Input	Charge Pump Capacitor	Input from external reservoir, external pump capacitors for charge pump, and secondary pins

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ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
VIGN Supply Voltage	V_{IGN}	-15.5 to 40	VDC
VIGNP Load Dump Survival	$V_{IGNP_{LD}}$	-0.3 to 65	VDC
VDD Logic Supply Voltage (Fail Safe)	V_{DD}	-0.3 to 7.0	VDC
Logic Input Voltage (LSEn, HSEn, PWM, and MODEn)	V_{IN}	0.3 to 7.0	VDC
Start Up Current V_{IGNP}	$I_{VIGNSTARTUP}$	100	mA
ESD Voltage (1) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±500 ±200	V
Storage Temperature	T_{STG}	-65 to 160	°C
Operating Ambient Temperature	T_A	-40 to 125	°C
Operating Case Temperature	T_C	-40 to 125	°C
Maximum Junction Temperature	T_J	150	°C
Power Dissipation (T_A = 25°C)	P_D	1.5	W
Peak Package Reflow Temperature During Reflow (2), (3)	T_{PPRT}	Note 3	°C
Thermal Resistance, Junction-to-Ambient	$R_{\Theta JA}$	65	°C/W

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

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STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions -40°C ≤ T_A ≤ 125°C, 5.5 V ≤ V_{IGNP} ≤ 24 V unless otherwise noted. Typical values reflect approximate parameter mean at T_A = 25°C under normal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
V_{IGN} Current @ 5.5 V–24 V, V_{DD} = 5.5 V	I_{IGN}	–	0.2	1.0	mA
V_{IGNP} Current @ 5.5 V–24 V, V_{DD} = 5.5 V	I_{IGNP}	–	–	100	mA
V_{IGNP} Overvoltage Shutdown	$V_{IGNP_{SD}}$	25	33	36.5	V
V_{IGNP} Voltage	V_{IGNP}	5.5	–	24	V
V_{DD} Current @ 5.5 VDC, 5.5 V ≤ V_{IGNP} ≤ 24 V	$I_{V_{DD}}$	–	1.8	4.0	mA
V_{DD} Low-Voltage Reset Level	$V_{DD(RESET)}$	2.5	3.2	4.0	V
V_{DD} One-Time Fuse (Logic Supply)	–	7.0	–	–	V
INPUT/OUTPUT					
Input Current at V_{DD} = 5.5 V LSEn, HSEn, PWM, and MODEn = 3.0 V	I_{IN}	5.0	12	25	µA
Input Threshold at V_{DD} = 5.5 V LSEn, HSEn, PWM, and MODEn (4)	V_{TH}	1.0	2.0	3.0	V
V_{SCRn} Source Sense Voltage SRC1, SRC2, SRC3	V_{SCRn}	-0.3	V_{IGNP}	24	V
Comparator Input Offset Voltage	$V_{INP(OFFSET)}$	5.0	14	20	mV
Comparator Input Bias Current	$V_{INP(BIAS)}$	-500	-170	500	nA
Comparator Input Offset Current	$I_{INP(OFFSET)}$	-300	-3.0	300	nA
Common Mode Voltage (5)	V_{CMR}	0	–	V_{DD}-2.0	V_{DC}
Comparator Differential Input Voltage (5)	$V_{INPdiff}$	-V_{DD}	–	+V_{DD}	V
Charge Pump Voltage V_{IGN} (6)	V_{CRES}-V_{IGNP}				V
V_{IGNP} = 5.5 V, I_{CRES} = 1.0 mA		4.0	6.0	18	
V_{IGNP} = 9.0 V, I_{CRES} = 1.0 mA		4.0	7.5	18	
V_{IGNP} = 12 V, I_{CRES} = 5.0 mA		4.5	10	18	
V_{IGNP} = 24 V, I_{CRES} = 1.0 mA		8.0	16	18	
V_{IGNP} = 24 V, I_{CRES} = 5.0 mA		4.5	12	18	
V_{GDH} Output Voltage with GDHn in ON State	$V_{GDHn(on)}$-V_{SRCn}				V
V_{IGNP} = 5.5 V, I_{GDHn} = 1.0 mA		4.0	5.2	18	
V_{IGNP} = 12 V, I_{GDHn} = 5.0 mA		4.0	9.0	18	
V_{IGNP} = 24 V, I_{GDHn} = 5.0 mA		4.5	11	18	
V_{GDH} Output Voltage with GDHn in OFF State V_{IGNP} = SRCn = 14 V, I_{GDHn} = 1.0 mA	$V_{GDHn(off)}$	-1.0	0.6	1.0	V

Notes

4. Logic inputs LSEn, HSEn, PWM, and MODEn have internal 20 µA internal sinks.
5. Guaranteed by design and characterization. Not production tested.
6. The Charge Pump has a positive temperature coefficient. Therefore the Min's occur at -40°C, Typ's at 25°C, and Max's at 125°C.

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Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40°C ≤ T_A ≤ 125°C, 5.5 V ≤ V_{IGNP} ≤ 24 V unless otherwise noted. Typical values reflect approximate parameter mean at T_A = 25°C under normal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT/OUTPUT (CONTINUED)					
V_{GDL} Low-Side Output Voltage GDHn in ON State	$V_{GDL(on)}$				V
V_{IGNP} = 5.5 V, I_{GDLn} = 1.0 mA		5.0	8.0	18	
V_{IGNP} = 12 V, I_{GDLn} = 5.0 mA		8.0	14	18	
V_{IGNP} = 24 V, I_{GDLn} = 0.0 mA		8.0	17	19	
V_{IGNP} = 24 V, I_{GDLn} = 5.0 mA		8.0	16	19	
V_{GDL} Output Voltage GDHn in OFF State	$V_{GDL(off)}$				V
V_{IGNP} = 14 V, I_{GDLn} = 1.0 mA		-1.0	0.3	1.0	
Thermal Shutdown (7)	T_{LIM}	160	–	190	°C

Notes

7. Guaranteed by design and characterization. Not production tested.

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DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions -40°C ≤ T_A ≤ 125°C, 5.5 V ≤ V_{IGNP} ≤ 24 V unless otherwise noted. Typical values reflect approximate parameter mean at T_A = 25°C under normal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
High-Side (GDHn) and Low-Side Drivers (GDHn) Rise Time (25% to 75%), C_{ISS} Value = 2000 pF [8]	t_{RH}	–	0.35	1.5	µs
High-Side (GDHn) and Low-Side Drivers (GDHn) Fall Time (75% to 25%), C_{ISS} Value = 2000 pF [8]	t_{FH}	–	0.25	1.5	µs
Shoot-Through Suppression Time Delay (33395) [8], [9] 33395 33395T	t_{D1}, t_{D2}	 1.0 0.2	 3.0 0.65	 5.5 1.0	µs
Current Limit Time Delay [10]	$t_{ILIMDELAY}$	1.5	2.8	5.0	µs

Notes

8. See Figure 4, page 8.
9. Shoot-Through Suppression Time Delay is provided to prevent directly connected high- and low-side MOSFETs from being on simultaneously.
10. Current Limit Time Delay: The internal comparator places the device in the current limit mode when the comparator output goes LOW and sets an internal logic bit. This takes a finite amount of time and is stated as the Current Limit Time Delay.

TIMING DIAGRAM

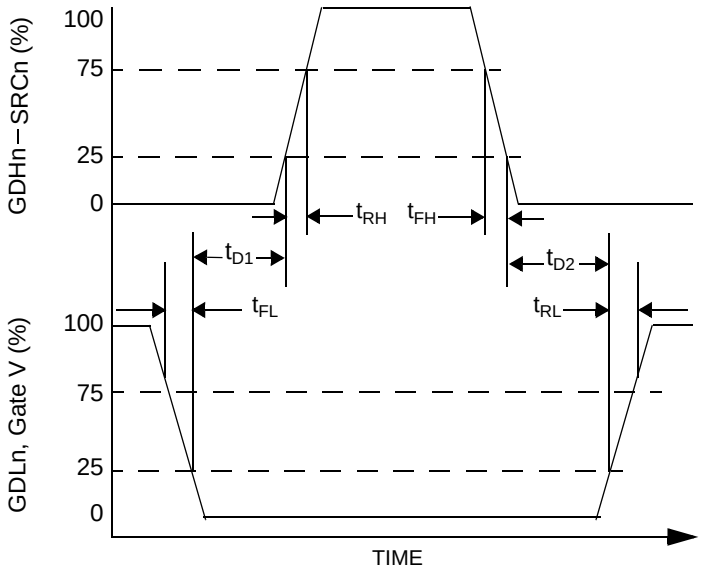


Figure 4. Shoot-Through Suppression

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FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33395 and 33395T devices are designed to provide the necessary drive and control signal buffering and amplification to enable a DSP or MCU to control a three-phase array of power MOSFETs such as would be required to energize the windings of powerful brushless DC (BLDC) motors. It contains built-in charge pump circuitry so that the MOSFET array may consist entirely of N-Channel MOSFETs. It also contains feedback sensing circuitry and control circuitry to provide a robust overall motor control design.

FUNCTIONAL PIN DESCRIPTION

CHARGE PUMP CAPACITOR (CP2H)

High potential pin connection for secondary charge pump capacitor

CHARGE PUMP RESERVE CAPACITOR (CPRES)

Input from external reservoir capacitor for charge pump

INPUT VOLTAGE (VIGN)

Input from ignition level supply voltage for power functions

HIGH-SIDE GATE VOLTAGE (VGDH)

Output full-time gate drive for auxiliary high-side power MOSFET switch

INPUT VOLTAGE PROTECTED (VIGNP)

Input from protected ignition level supply for power functions

HIGH-SIDE SENSE (SRC1, SRC2, SRC3)

Sense for high-side source voltage, phase 1/2/3

GATE DRIVE HIGH (GDH1, GDH2, GDH3)

Output for gate high-side, phase 1/2/3

OUTPUT FOR GATE (GDL1, GDL2, GDL3)

Output for gate drive low-side, phase 1

POWER GROUND (PGND)

Ground pins for power functions

TEST PIN (TEST)

This should be connected to ground or left open

IS MINUS (-ISENS)

Inverting input for current limit comparator

IS PLUS (+ISENS)

Non-Inverting input for current limit comparator

ANALOG GROUND (AGND)

Ground pin for logic functions

LOGIC SUPPLY VOLTAGE (VDD)

Supply voltage for logic functions

PULSE WIDTH MODULATOR (PWM)

Input for pulse width modulated driver duty cycle

MODE CONTROL BIT 1 (MODE1)

Input for mode control selection

MODE CONTROL BIT 0 (MODE0)

Input for mode control selection

HIGH-SIDE ENABLE (HSE3, HSE2, HSE1)

Input for high-side enable logic, phase 1/2/3

LOW-SIDE ENABLE (LSE3, LSE2, LSE1)

Input for low-side enable logic, phase 1/2/3

EXTERNAL PUMP CAPACITOR (CP1L, CP1H)

Input from external pump capacitor for charge pump and secondary pins

CHARGE PUMP CAPACITOR (CP2L)

Input from external reservoir, external pump capacitors for charge pump, and secondary pins

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FUNCTIONAL INTERNAL BLOCK DESCRIPTION

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GATE DRIVE CIRCUITS

The gate drive outputs (GDH1, GDH2, etc.) supply the peak currents required to turn ON and hold ON the MOSFETs, as well as turn OFF and hold OFF the MOSFETs.

CHARGE PUMP

The current capability of the charge pump is sufficient to supply the gate drive circuit's demands when PWMing at up to 28 kHz. Two external charge pump capacitors and a reservoir capacitor are required to complete the charge pump's circuitry.

Charge reservoir capacitance is a function of the total MOSFET gate charge (Q_G) gate drive voltage level relative to the source (V_{GS}) and the allowable sag of the drive level during the turn-on interval (V_{SAG}). C_{RES} can be expressed by the following formula:

$$C_{RES} = \frac{Q_G \times V_{GS}}{2 \times V_{GS} \times V_{SAG} - V_{SAG}^2}$$

For example, for Q_G = 60 nC, V_{GS} = 14 V, V_{SAG} = 0.2 V:

$$C_{RES} = \frac{(60\ nC) \times (14\ V)}{2 \times (14\ V) \times (0.2\ V) - (0.2)^2} = 0.15\ \mu F$$

Proper charge pump capacitance is required to maintain, and provide for, adequate gate drive during high demand turn-ON intervals. Use the following formula to determine values for C_{P1} and C_{P2}:

For example, for the above determination of C_{RES} = 0.15 µF:

$$\frac{C_{RES}}{20} \leq C_{P1} = C_{P2} \leq \frac{C_{RES}}{10}$$

By averaging these two values, the proper C_{Pn} value can be determined:

$\frac{0.15\ \mu F}{20}$ = 0.075 µF, lower limit; and $\frac{0.15\ \mu F}{10}$ = .015 µF, upper lim

C_{P1} and C_{P2} =(0.0075 µF + 0.015 µF) ÷ 2 = 0.01 µF

THERMAL SHUTDOWN FUNCTION

The device has internal temperature sensing circuitry which activates a protective shutdown function should the die reach excessively elevated temperatures. This function effectively limits power dissipation and thus protects the device.

OVERVOLTAGE SHUTDOWN FUNCTION

When the supply voltage (V_{IGN}) exceeds the specified over- voltage shutdown level, the part will automatically shut down to protect both internal circuits as well as the load. Operation will resume upon return of V_{IGN} to normal operating levels.

LOW VOLTAGE RESET FUNCTION

When the logic supply voltage (V_{DD}) drops below the minimum voltage level or when the part is initially powered up, this function will turn OFF and hold OFF the external MOSFETs until the voltage increases above the minimum voltage level required for normal operation.

CONTROL LOGIC

The control logic block controls when the low-side and high-side drivers are enabled. The logic implements the Truth Table found in the specification and monitors the M0, M1, PWM, CL, OT, OV, LSE, and HSE pins. Note that the drivers are enabled 3 µs after the PWM edge. During complimentary chop mode the high-side and low-side drives are alternatively enabled and disabled during the PWM cycle. To prevent shoot-through current, the high-side drive turn-on is delayed by t_{D1}, and the low-side drive turn on is delayed by t_{D2} (see Figure 4, page 8).

Note that the drivers are disabled during an overtemperature or overvoltage fault. A flip-flop keeps the drive off until the following PWM cycle. This prevents erratic operation during fault conditions. The current limit circuit also uses a flip-flop for latching the drive off until the following PWM cycle.

Note PWM must be toggled after POR, Thermal Limit, or overvoltage faults to re-enable the gate drivers.

VGDH

The VGDH pin is used to provide a gate drive signal to a reverse battery protection MOSFET. If reverse battery protection is desired, V_{IGN} would be applied to the source of an external MOSFET, and the drain of the MOSFET would then deliver a "protected" supply voltage (V_{IGNP}) to the three phase array of external MOSFETs as well as the supply voltage to the V_{IGNP} pin of the IC.

In a reverse polarity event (e.g., an erroneous installation of the system battery), the V_{GDH} signal will not be supplied to the external protection MOSFET, and the MOSFET will remain off and thus prevent reverse polarity from being applied to the load and the VIGNP supply pin of the IC.

HIGH-SIDE GATE DRIVE CIRCUITS

Outputs GDH1, GDH2, and GDH3 provide the elevated drive voltage to the high-side external MOSFETs (HS1, HS2, and HS3; see Figure 5, page 13). These gate drive outputs supply the peak currents required to turn ON and hold ON the high-side MOSFETs, as well as turn OFF the MOSFETs. These gate drive circuits are powered from an internal charge pump, and therefore compensate for voltage dropped across the load that is reflected to the source-gate circuits of the high-side MOSFETs.

LOW-SIDE GATE DRIVE CIRCUITS

Outputs GDL1, GDL2, and GDL3 provide the drive voltage to the low-side external MOSFETs (LS1, LS2, and LS3; see

Figure 5). These gate drive outputs supply the peak currents required to turn ON and hold ON the low-side MOSFETs, as well as turn OFF the MOSFETs.

V_{DD} FUSE

The V_{DD} supply of the 33395 IC has an internal fuse, which will blow and set all outputs of the device to OFF, if the V_{DD} voltage exceeds that stated in the maximum rating section of the data sheet. When this fuse blows, the device is permanently disabled.

I_{SENS} INPUTS

The +Isens and -Isens pins are inputs to the internal current sense comparator. In a typical application, these would receive a a low-pass filtered voltage derived from a current sense resistor placed in series with the ground return of the three-phase output bridge. When triggered by the comparator, the CL (current limit) bit of the internal error register is set, and the output gate drive pairs (i.e., GDH1 and GDL1, GDH2 and GDL2, GDH3 and GDL3), are controlled such that current will cease flowing through the load (refer to Table 5, Truth Table, page 12).

OVERTEMPERATURE AND OVERVOLTAGE SHUTDOWN CIRCUITS

Internal monitoring is provided for both over temperature conditions and over voltage conditions. When any of these conditions presents itself to the IC, the corresponding internally set bits of the error register are set, and the output gate drive pairs (i.e., GDH1 and GDL1, GDH2 and GDL2, GDH3 and GDL3), are controlled such that current will cease flowing through the load (refer to Table 5).

LSE AND HSE INPUT CIRCUITS

The low-side enable input pins (LSE1, LSE2, LSE3) and high-side enable input pins (HSE1, HSE2, HSE3) form the input pairs (HSE1 and LSE1, HSE2 and LSE2, HSE3 and LSE3) which set the logic states of the output gate drive pairs (i.e., GDH1 and GDL1, GDH2 and GDL2, GDH3 and GDL3) in accordance with the logic set forth in the Truth Table (page 12). Typically these inputs are supplied from an MCU or DSP to provide the phasing of the currents applied to a brushless dc motor's stator coils via the output MOSFET pairs.

PWM INPUT

The pulse width modulation input provides a single input pin to accomplish PWM modulation of the output pairs in accordance with the states of the Mode 0 and Mode 1 inputs as set forth in the Truth Table (page 12).

MODE SELECTION INPUTS

The mode selection inputs (Mode 0 and Mode 1) determine the PWM implementation of the output pairs in accordance with the logic set forth in the Truth Table (page 12). PWMing can thus be set to occur either on the high-side MOSFETs or the low-side MOSFETs, or can be set to occur on both the high-side and low-side MOSFETs as "complementary chopping".

TEST PIN

This pin should be grounded or left floating (i.e., do not connect it to the printed circuit board). It is used by the automated test equipment to verify proper operation of the internal overtemperature shut down circuitry. This pin is susceptible to latch-up and therefore may cause erroneous operation or device failure if connected to external circuitry.

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FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

Table 5. Truth Table

The logic state of each output pair, GDLn and GDHn (n = 1, 2, 3), is a function of its corresponding input pair, LSEn and HSEn (n = 1, 2, 3), along with the logic states of the MODEn and PWM inputs and the internally set overtemperature shutdown (OT), overvoltage (OV), and current limit (CL) bits provided in this table.

NORMAL OPERATION

Switching Modes		Internally Set Bits			Input Pairs (e.g., LSE2 and HSE2)		Output Pairs (e.g., GDL2 and GDH2)	
MODE1	MODE0	OT	OV	CL	LSEn	HSEn	GDLn	GDHn
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	1
0	0	0	0	0	1	0	PWM	0
0	0	0	0	0	1	1	0	0
0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	1
0	1	0	0	0	1	0	PWM	$\overline{\text{PWM}}$
0	1	0	0	0	1	1	0	0
1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	PWM
1	0	0	0	0	1	0	1	0
1	0	0	0	0	1	1	0	0
1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	1	$\overline{\text{PWM}}$	PWM
1	1	0	0	0	1	0	1	0
1	1	0	0	0	1	1	0	0

FAULT MODE OPERATION

Switching Modes		Internally Set Bits			Input Pairs (e.g., LSE2 and HSE2)		Output Pairs (e.g., GDL2 and GDH2)	
MODE1	MODE0	OT	OV	CL	LSEn	HSEn	GDLn	GDHn
0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	1	0	1
0	0	0	0	1	1	0	0	0
0	0	0	0	1	1	1	0	0
0	1	0	0	1	0	0	0	0
0	1	0	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1
0	1	0	0	1	1	1	0	0
1	0	0	0	1	0	0	0	0
1	0	0	0	1	0	1	0	0
1	0	0	0	1	1	0	1	0
1	0	0	0	1	1	1	0	0
1	1	0	0	1	0	0	0	0
1	1	0	0	1	0	1	1	0
1	1	0	0	1	1	0	1	0
1	1	0	0	1	1	1	0	0
x	x	x	1	x	x	x	0	0
x	x	1	x	x	x	x	0	0

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TYPICAL APPLICATIONS

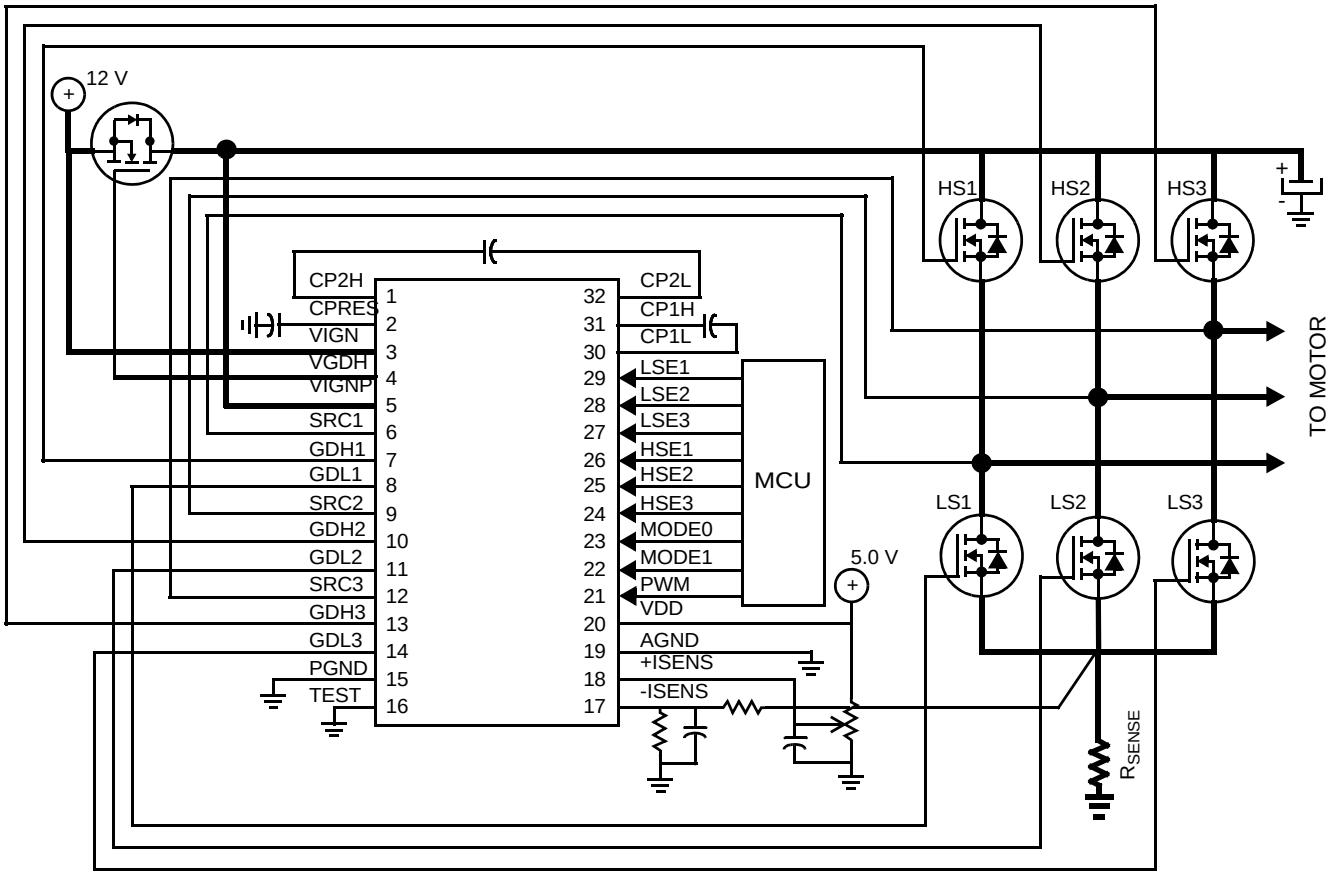


Figure 5. Typical Application Diagram

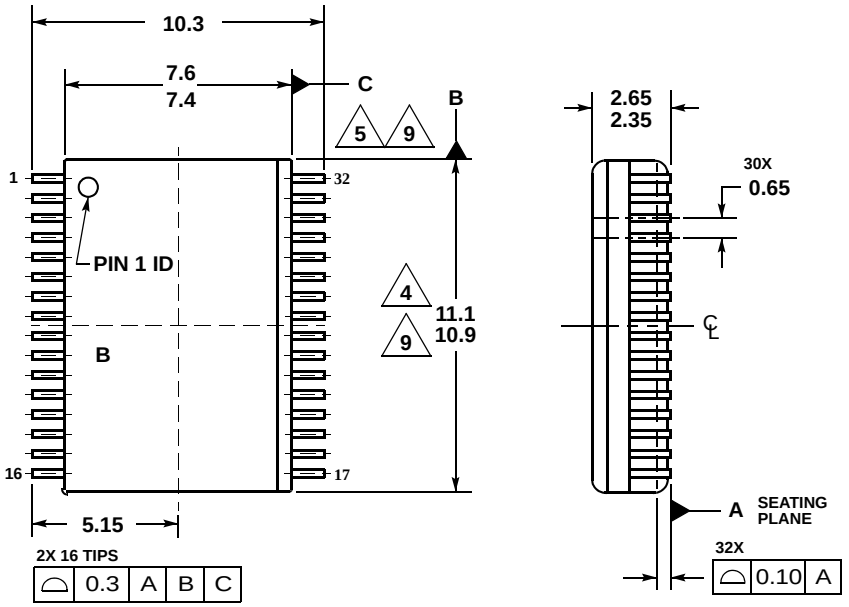
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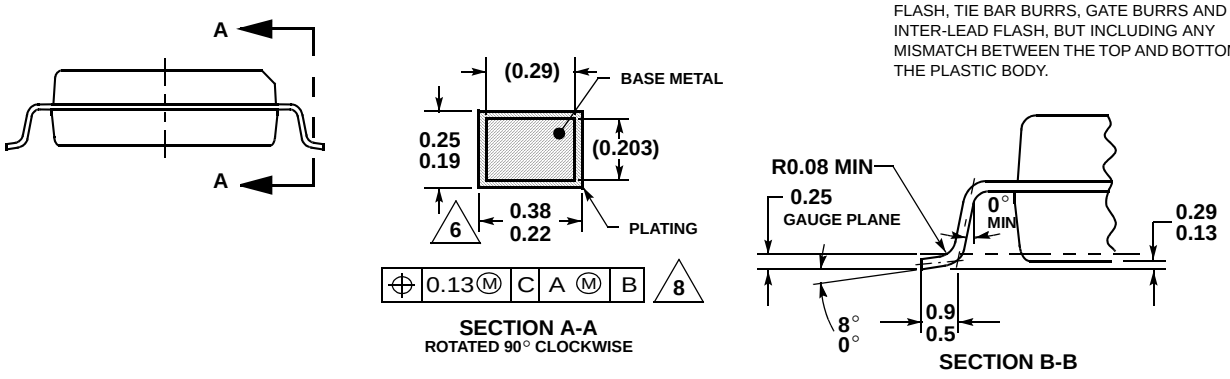
PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98ARH99137A listed below.



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 MM PER SIDE. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.



DWB SUFFIX
EW SUFFIX (PB-FREE)
32-PIN
PLASTIC PACKAGE
98ARH99137A
ISSUE A

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	7/2005	• Implemented Revision History page • Converted to Freescale format • Added Pin Definitions
4.0	2/2007	• Updated Freescale data sheet form and style • Added MCZ33395EW/R2 to the Ordering Information block • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter and added notes (2) and (3) to Maximum Ratings on page 5

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