CD40162B and CD40163B were not acquired from Harris Semiconductor.

TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS103C – Revised July 2003

CD40160B, CD40161B, CD40162B, CD40163B Types

CMOS Synchronous Programmable 4-Bit Counters

High-Voltage Types (20-Volt Rating)

CD40160B – Decade with Asynchronous Clear
CD40161B – Binary with Asynchronous Clear
CD40162B – Decade with Synchronous Clear
CD40163B – Binary with Synchronous Clear

■ CD40160B, CD40161B, CD40162B, and CD40163B are 4-bit synchronous programmable counters. The CLEAR function of the CD40162B and CD40163B is synchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160B and CD40161B is asynchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$, or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

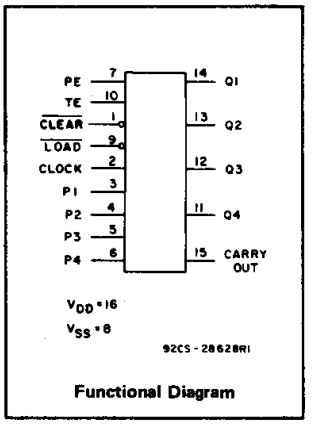
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (C_{OUT}). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

The CD40160B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix). The CD40161B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

The CD40160B through CD40163B types are functionally equivalent to and pin-compatible with the TTL counter series 74LS160 through 74LS163 respectively.

Features:

- **Internal look-ahead for fast counting**
- **Carry output for cascading**
- **Synchronously programmable**
- **Clear asynchronous input (CD40160B, CD40161B)**
- **Clear synchronous input (CD40162B, CD40163B)**
- **Synchronous load control input**
- **Low-power TTL compatibility**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**



Functional Diagram

Applications:

- **Programmable binary and decade counting**
- **Counter control/timers**
- **Frequency dividing**

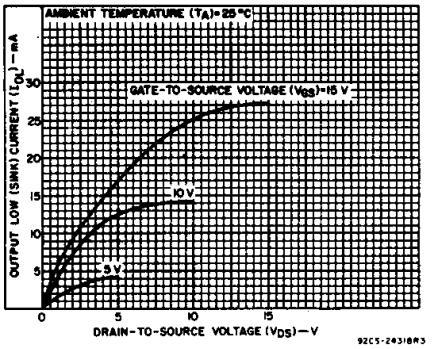


Fig. 1– Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

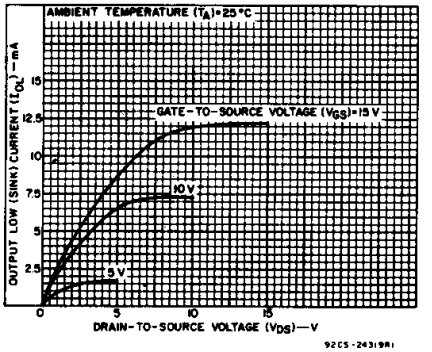


Fig. 2– Minimum output low (sink) current characteristics.

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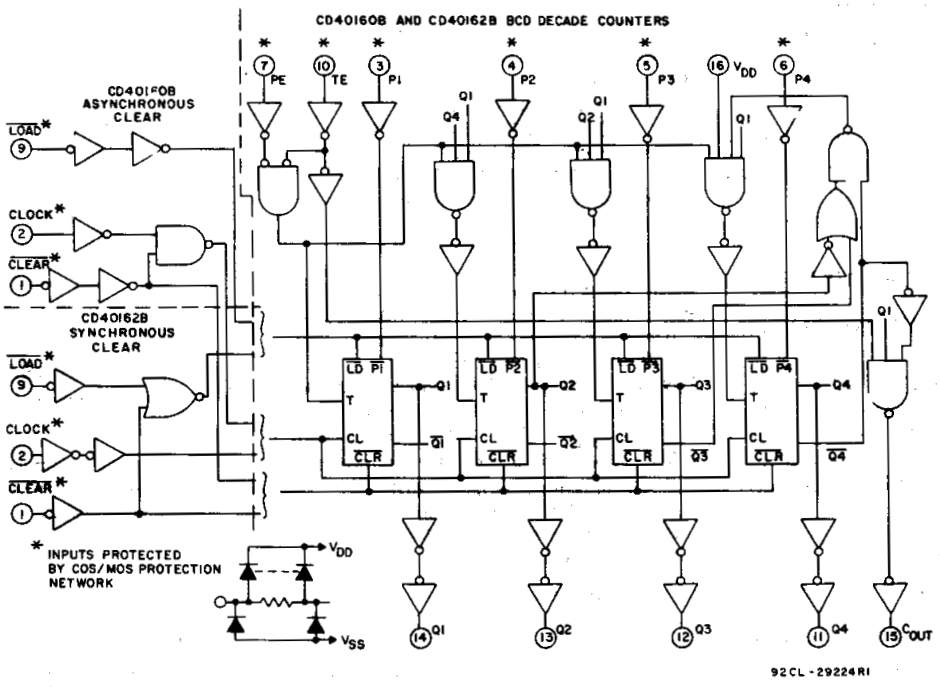


Fig. 3— Logic diagrams for CD40160B and CD40162B BCD decade counters.

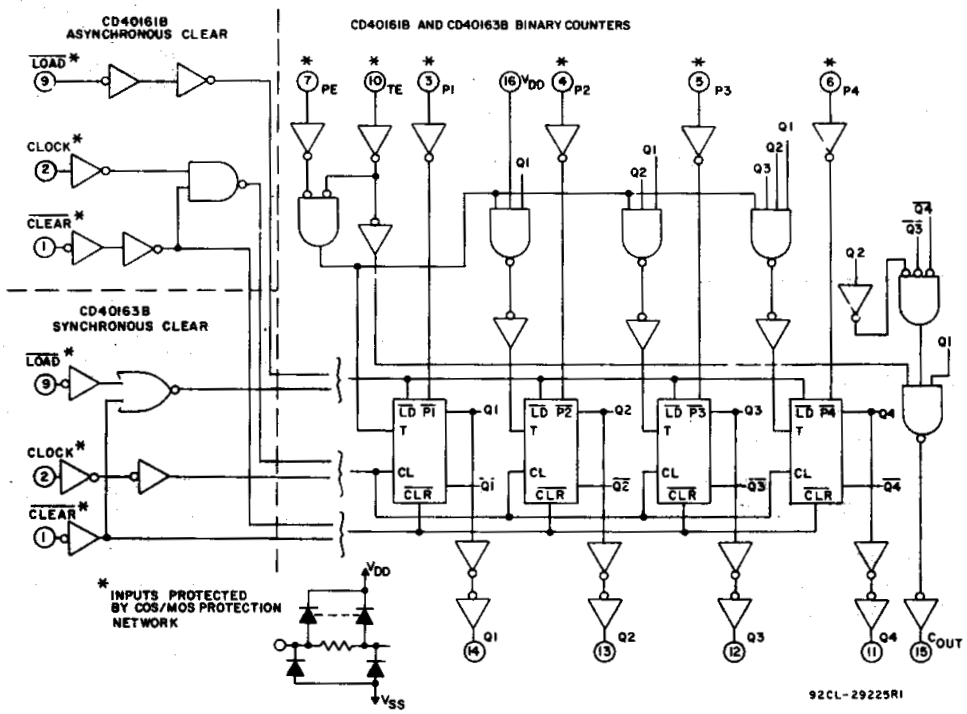


Fig. 4— Logic diagrams for CD40161B and CD40163B binary counters.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range (Full T_A = Full Package-Temperature Range)	–	3	18	V
Setup Time: t_{SU} Data to Clock	5	240	–	ns
	10	90	–	
	15	60	–	
$\overline{\text{Load}}$ to Clock	5	240	–	ns
	10	90	–	
	15	60		
PE or TE to Clock	5	340	–	ns
	10	140	–	
	15	100	–	
$\overline{\text{Clear}}$ to Clock (CD40162B, CD40163B)	5	340	–	ns
	10	140	–	
	15	100		
All Hold Times, t_H	5	0	–	ns
	10	0	–	
	15	0	–	
$\overline{\text{Clear}}$ Removal Time, t_{rem} (CD40160B, CD40161B)	5	200	–	ns
	10	100	–	
	15	70	–	
$\overline{\text{Clear}}$ Pulse Width, t_{WL} (CD40160B, CD40161B)	5	170	–	ns
	10	70	–	
	15	50	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	5.5	
	15	–	8	
Clock Pulse Width, t_W	5	170	–	ns
	10	70	–	
	15	50	–	
Clock Rise or Fall Time, t_rCL or t_fCL	5	–	200	μs
	10	–	70	
	15	–	15	

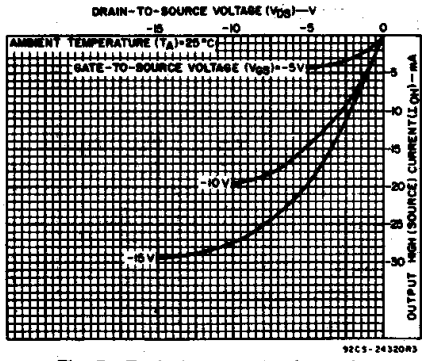


Fig. 5— Typical output high (source) current characteristics.

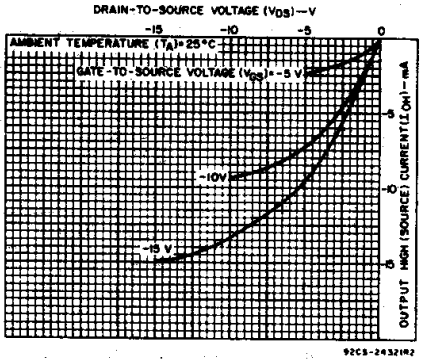


Fig. 6— Minimum output high (source) current characteristics.

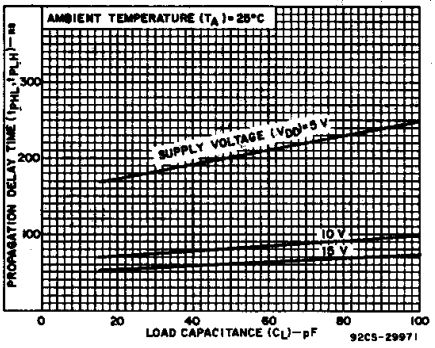


Fig. 7— Typical propagation delay time as a function of load capacitance (CLOCK to Q).

TRUTH TABLE

CLOCK	$\overline{\text{CLR}}$	$\overline{\text{LOAD}}$	PE	TE	OPERATION
↑	1	0	X	X	PRESET
↑	1	1	0	X	NC
↑	1	1	X	0	NC
↑	1	1	1	1	COUNT
X	0	X	X	X	RESET (CD40160B, CD40161B)
↑	0	X	X	X	RESET (CD40162B, CD40163B)
↓	1	X	X	X	NC (CD40162B, CD40163B)

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE NC = NO CHANGE

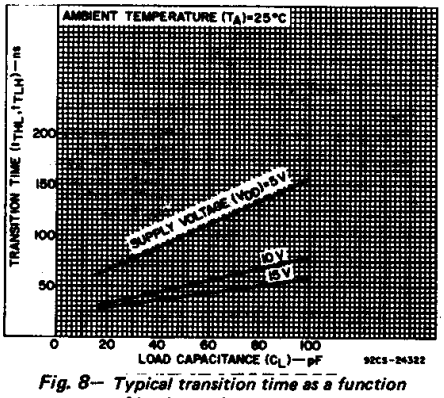


Fig. 8— Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

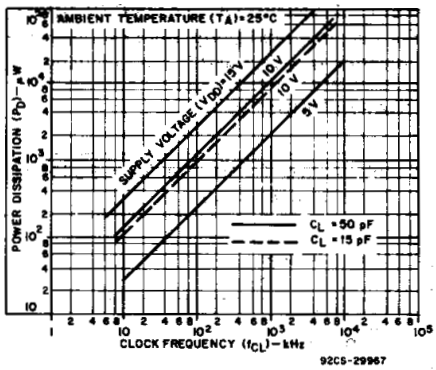


Fig. 9— Typical power dissipation as a function of CLOCK frequency.

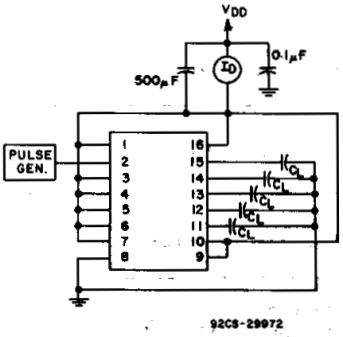


Fig. 10— Dynamic power dissipation test circuit.

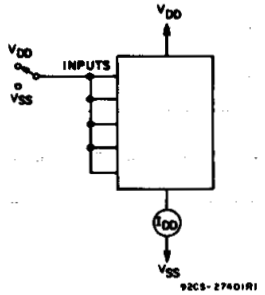


Fig. 11— Quiescent-device-current test circuit.

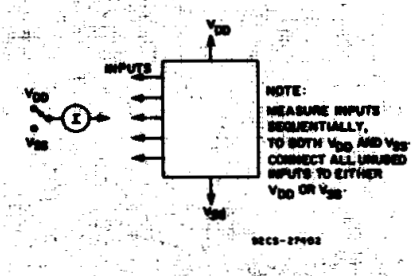


Fig. 12— Input-current test circuit.

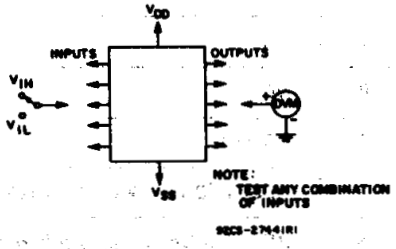
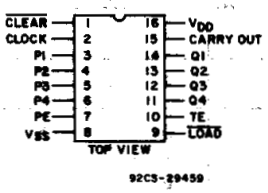


Fig. 13— Input-voltage test circuit.

TERMINAL ASSIGNMENT



DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS ALL TYPES* Min.	Typ.	Max.	UNITS
CLOCK OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Q	5	–	200	400	ns
	10	–	80	160	
	15	–	60	120	
Clock to C_{OUT}	5	–	225	450	ns
	10	–	95	190	
	15	–	70	140	
TE to C_{OUT}	5	–	125	250	ns
	10	–	55	110	
	15	–	40	80	
Minimum Setup Time, t_{SU} Data to Clock	5	–	120	240	ns
	10	–	45	90	
	15	–	30	60	
$\overline{\text{Load}}$ to Clock	5	–	120	240	ns
	10	–	45	90	
	15	–	30	60	
PE to TE to Clock	5	–	170	340	ns
	10	–	70	140	
	15	–	50	100	
Minimum Hold Time, t_H	5	–	–	0	ns
	10	–	–	0	
	15	–	–	0	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, t_W	5	–	85	170	ns
	10	–	35	70	
	15	–	25	50	
Maximum Clock Frequency, f_{CL}	5	2	3	–	MHz
	10	5.5	8.5	–	
	15	8	12	–	
Maximum Clock Rise or Fall Time,† t_rCL, t_{fCL}	5	200	–	–	μs
	10	70	–	–	
	15	15	–	–	
CLEAR OPERATION					
Propagation Delay Time, t_{PHL} (CD40160B, CD40161B) $\overline{\text{Clear}}$ to Q	5	–	250	500	ns
	10	–	110	220	
	15	–	80	160	
Minimum Setup Time, t_{SU} (CD40162B, CD40163B) $\overline{\text{Clear}}$ to Clock	5	–	170	340	ns
	10	–	70	140	
	15	–	50	100	
Minimum Hold Time, t_H (CD40162B, CD40163B) $\overline{\text{Clear}}$ to Clock	5	–	–	0	ns
	10	–	–	0	
	15	–	–	0	
Minimum $\overline{\text{Clear}}$ Removal Time, t_{rem} (CD40160B, CD40161B)	5	–	100	200	ns
	10	–	50	100	
	15	–	35	70	
Minimum $\overline{\text{Clear}}$ Pulse Width, t_{WL} (CD40160B, CD40161B)	5	–	85	170	ns
	10	–	35	70	
	15	–	25	50	

* Except as noted.
† If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

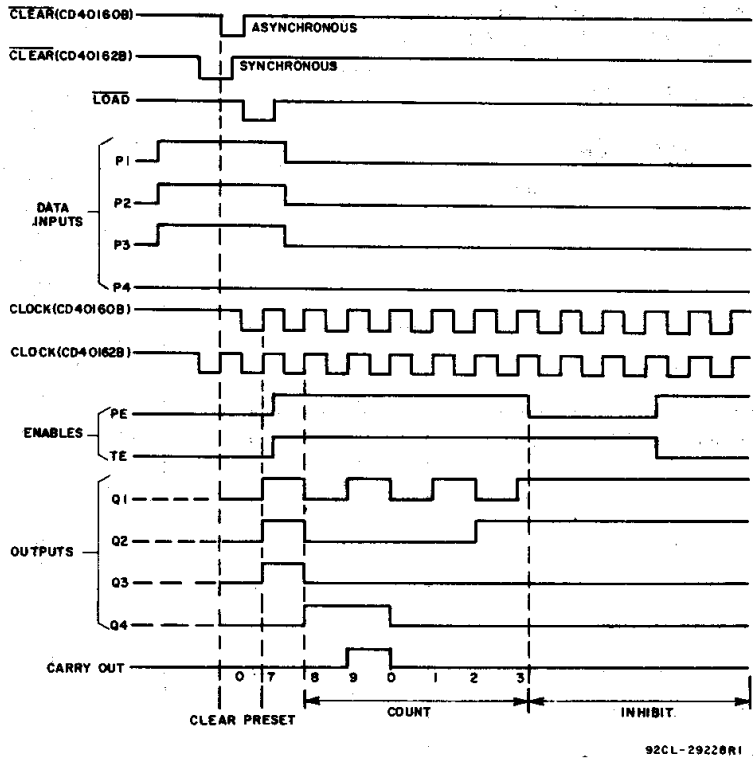


Fig. 14— Timing diagram for CD40160B, CD40162B.

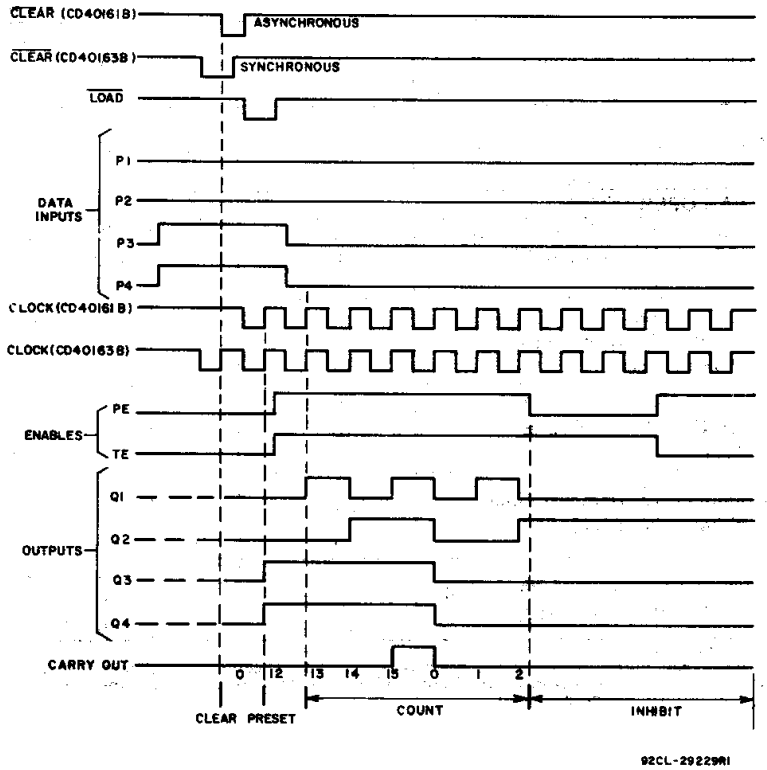


Fig. 15— Timing diagram for CD40161B, CD40163B.

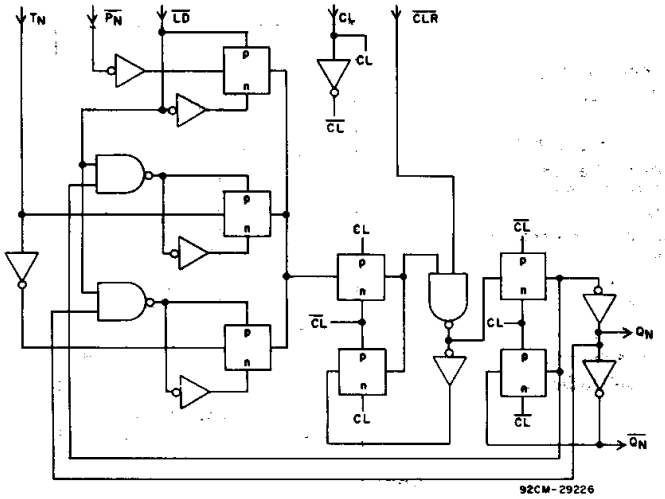
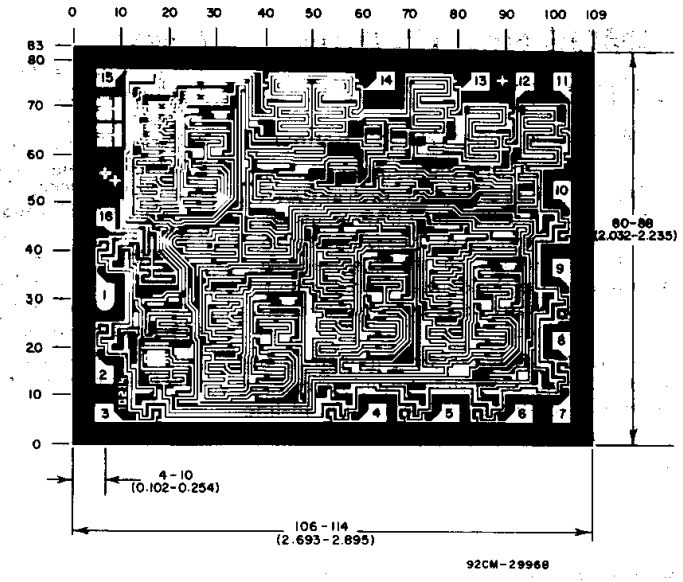


Fig. 16– Detail of flip-flops of CD40160B and CD40161B (asynchronous clear).



Dimensions and pad layout for CD40160BH. Dimensions and pad layout for CD40161BH, CD40162BH, and CD40163BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

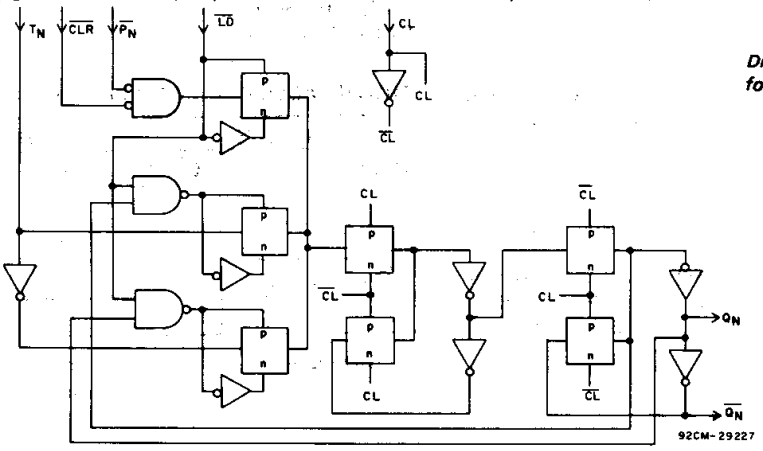


Fig. 17– Detail of flip-flops for CD40162B and CD40163B (synchronous clear).

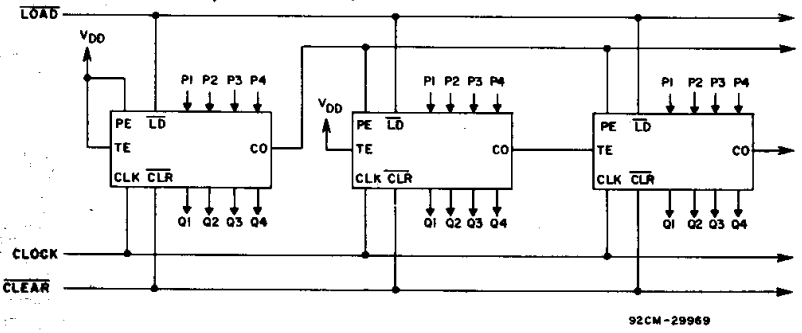


Fig. 18 – Cascaded counter packages in the parallel-clocked mode.

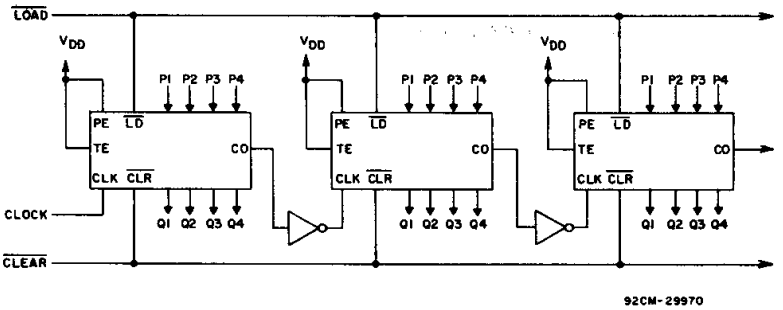


Fig. 19 – Cascaded counter packages in the ripple-clocked mode.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40160BF3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD40160BF3A	Samples
CD40161BE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD40161BE	Samples
CD40161BF3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD40161BF3A	Samples
CD40161BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40161B	Samples
CD40161BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0161B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40161B, CD40161B-MIL :

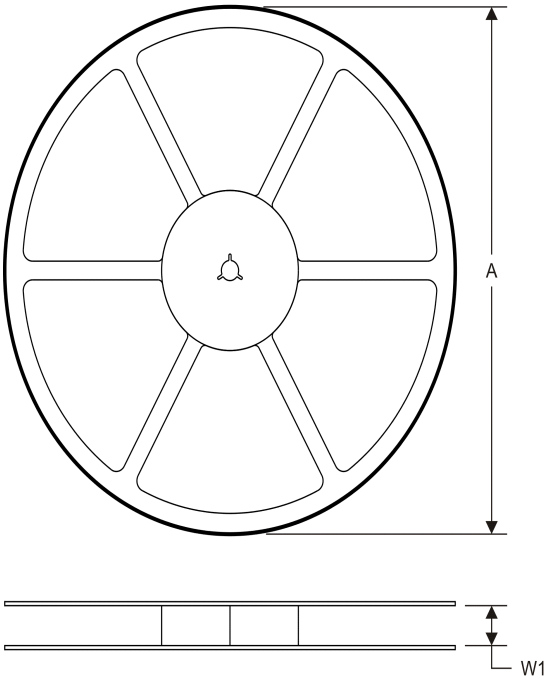
- Catalog: CD40161B
- Military: CD40161B-MIL

NOTE: Qualified Version Definitions:

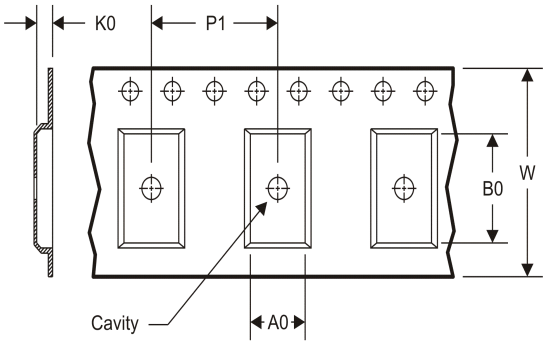
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



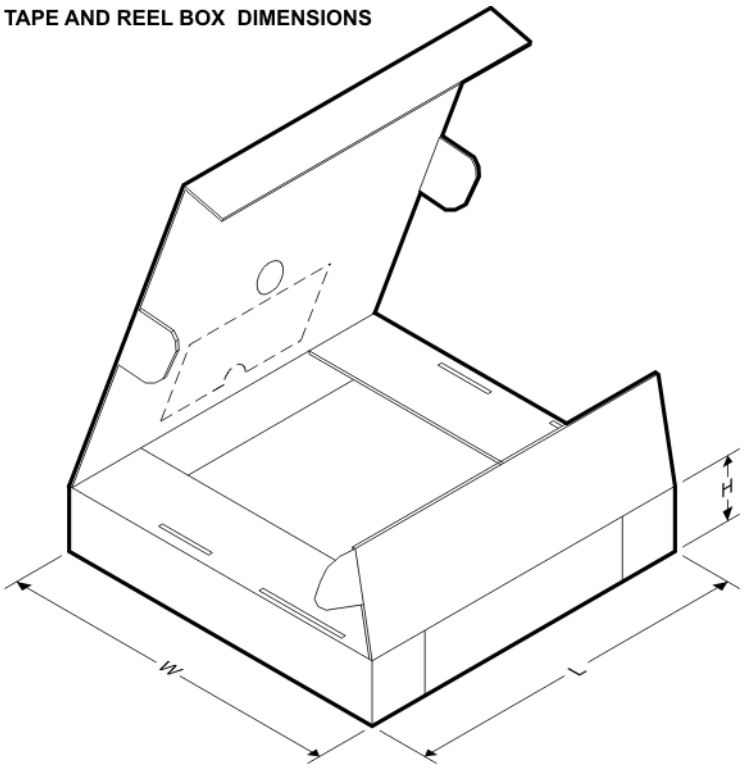
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40161BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40161BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



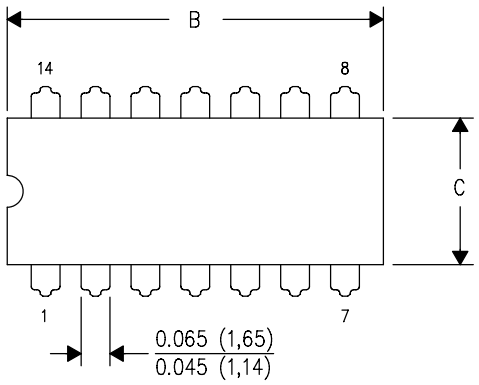
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40161BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD40161BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

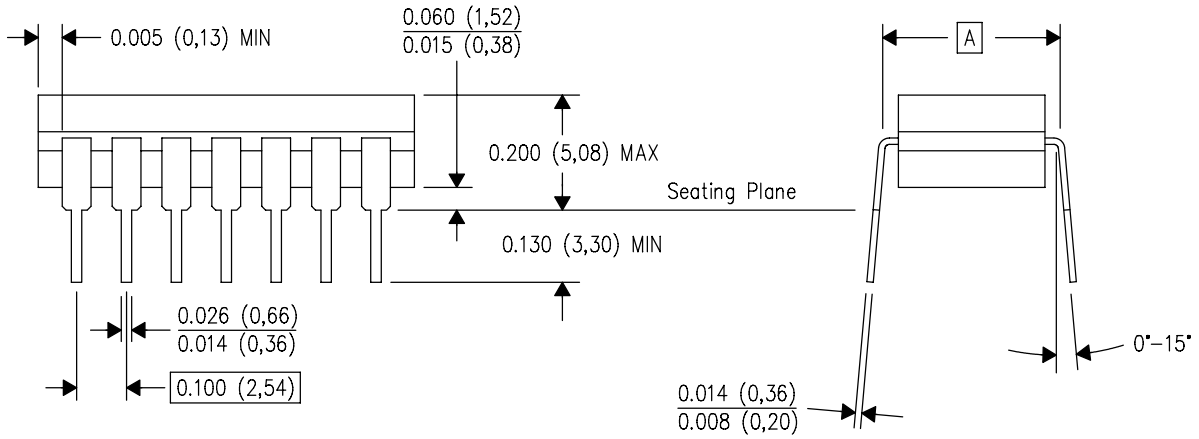
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



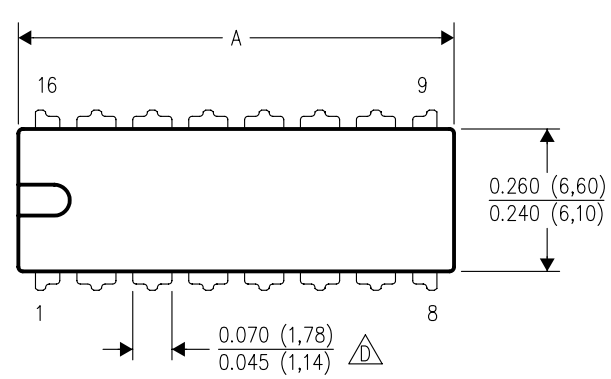
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

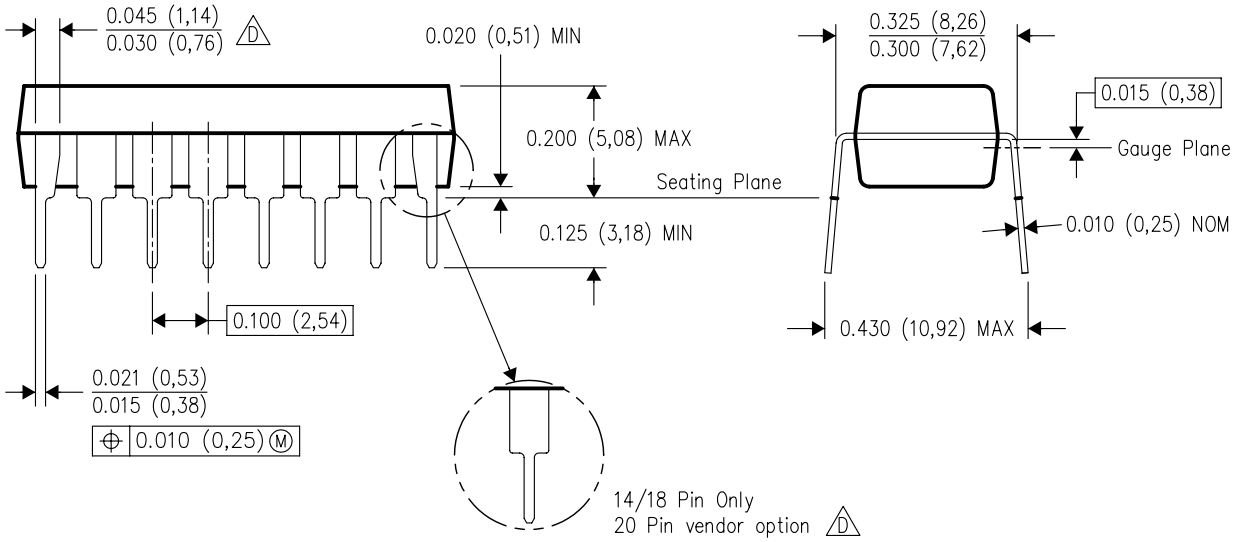
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

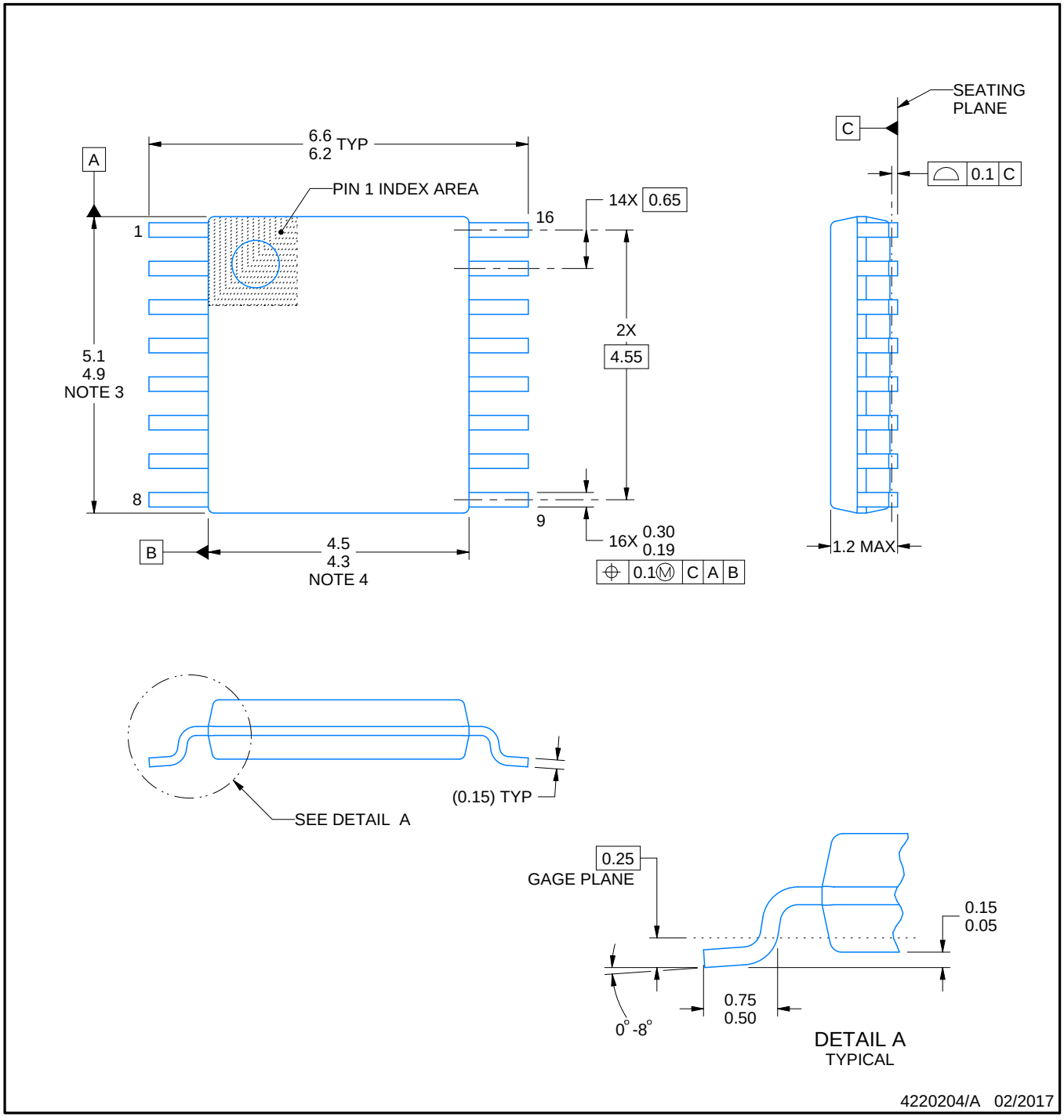
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0016A

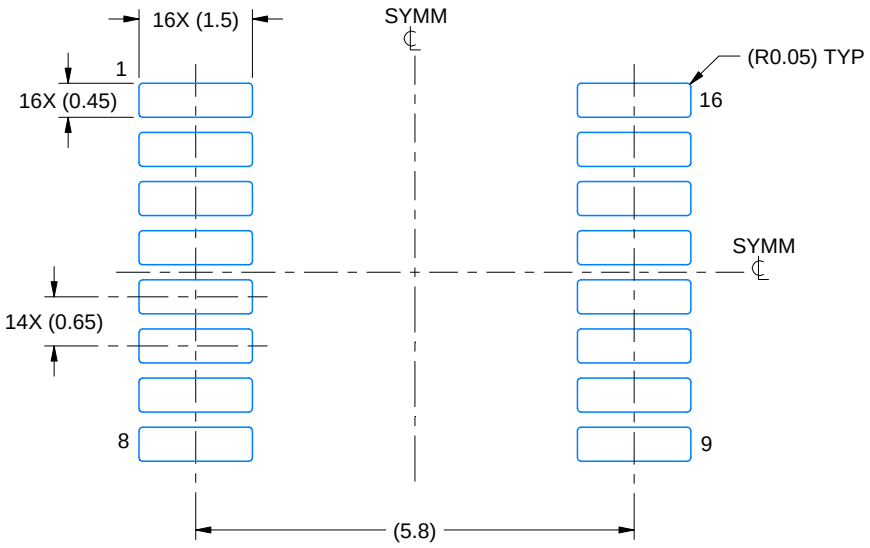
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

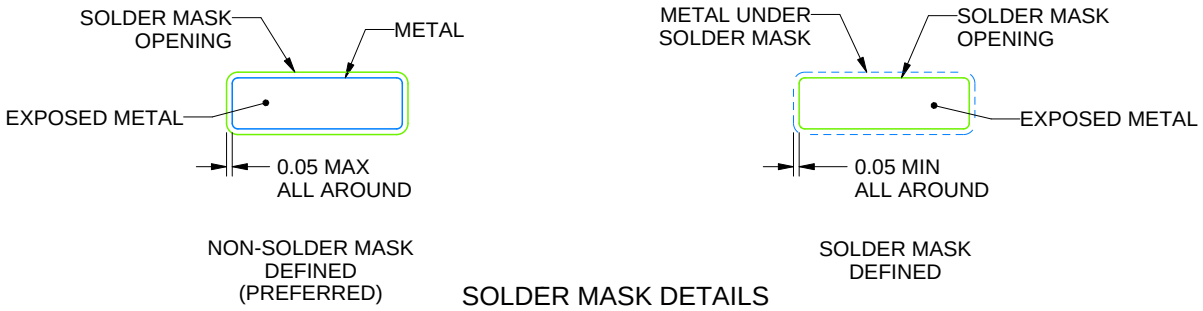


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

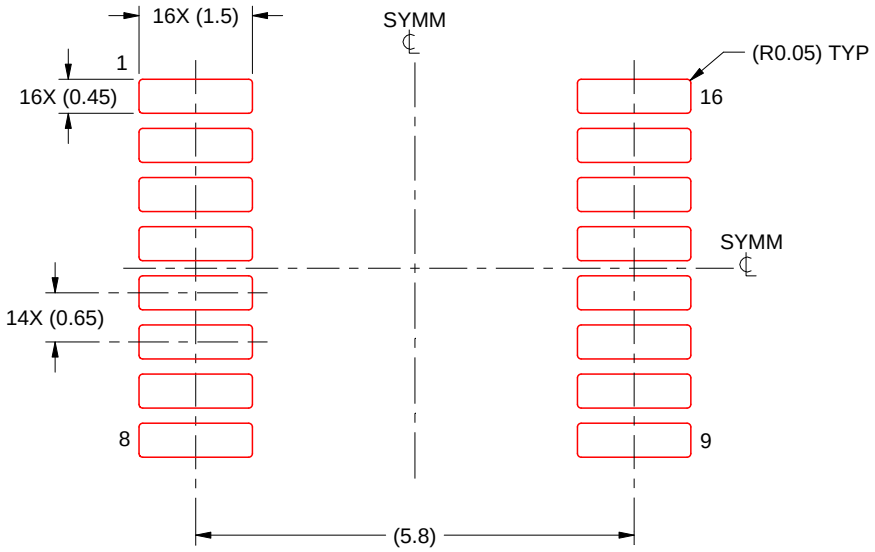


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

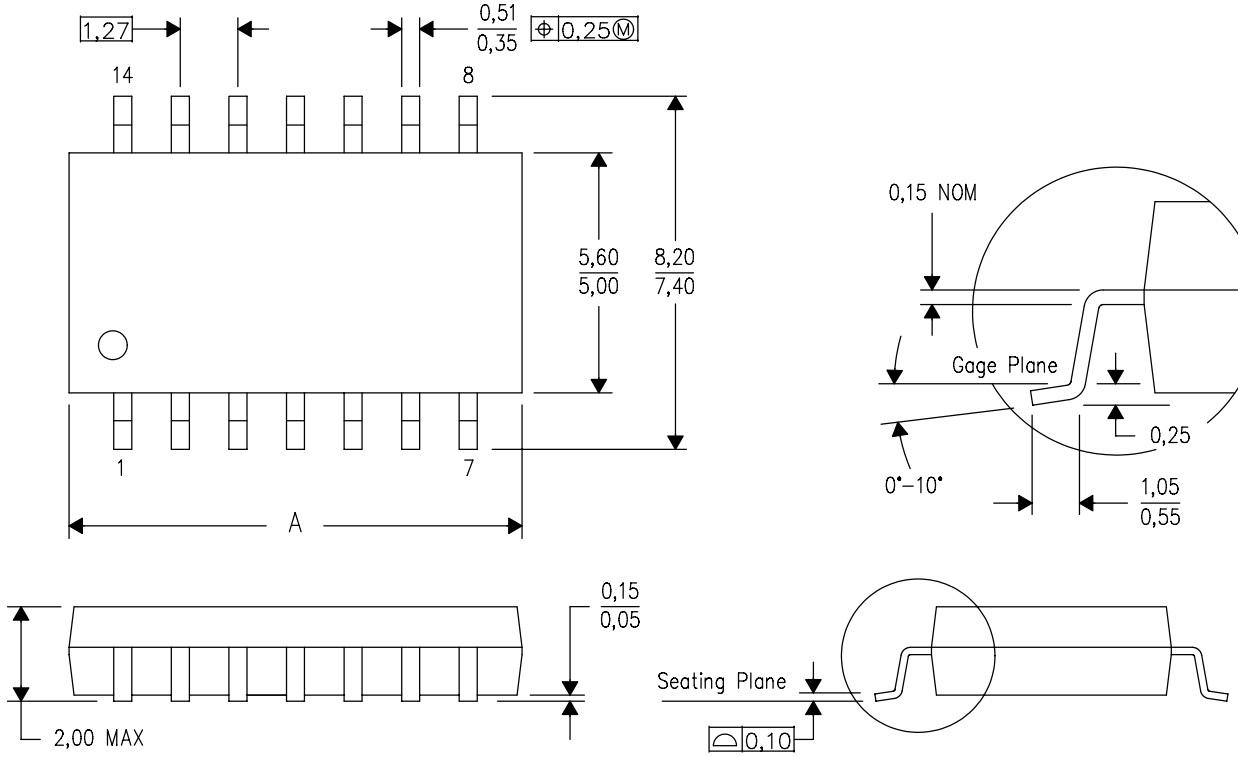
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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