DEMO MANUAL DC043
Micropower A/D Demo Board

LTC1286 Micropower 12-Bit A/D Converter Demo Board

DESCRIPTION

The LTC®1286 is a micropower, 12.5ksps, sampling 12-bit A/D converter which draws only 1.25mW from a single 5V supply. The LTC1286 demo board provides the user with a way to evaluate the LTC1286 A/D converter. In addition, the LTC1286 demo board is intended to illustrate the layout and bypassing techniques required to obtain optimum performance from this part. The LTC1286 demo board is designed to be easy to use and requires only a 7V to 15V supply, a clock signal and an analog input signal. As shown in the Board Photo, the LTC1286 is a very space efficient solution for A/D users. By combining a micropower 12-bit A/D, sample-and-hold, serial port and auto shutdown circuit into a single 8-pin SOIC package, all the data acquisition circuitry including the bypass caps can be placed into an area of only 0.1 square inch.

This manual shows how to use the demo board. Included are timing diagrams, power supply requirements and analog input range information. Additionally, a schematic, parts list, drawings and dimensions of all the PC board layers are included. An explanation of the layout and bypass strategies used in this board is also included so that anyone designing a PC board using the LTC1286 will be able to get the maximum performance from the device.

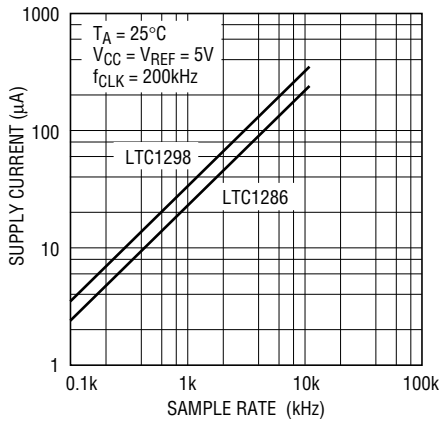
FEATURES

- Proven µPower 12-Bit ADC Surface Mount Layout
- Actual ADC Footprint Only 0.1 Inch^2 Including Bypass Capacitors
- 71dB SINAD, 84dB THD and ±0.25LSB DNL
- Gerber Files for This Circuit Board Are Available. Call the LTC Factory.

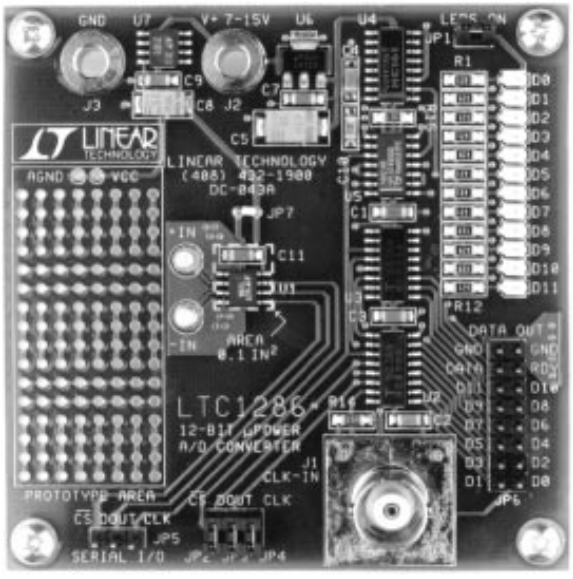
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TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Supply Current vs Sample Rate



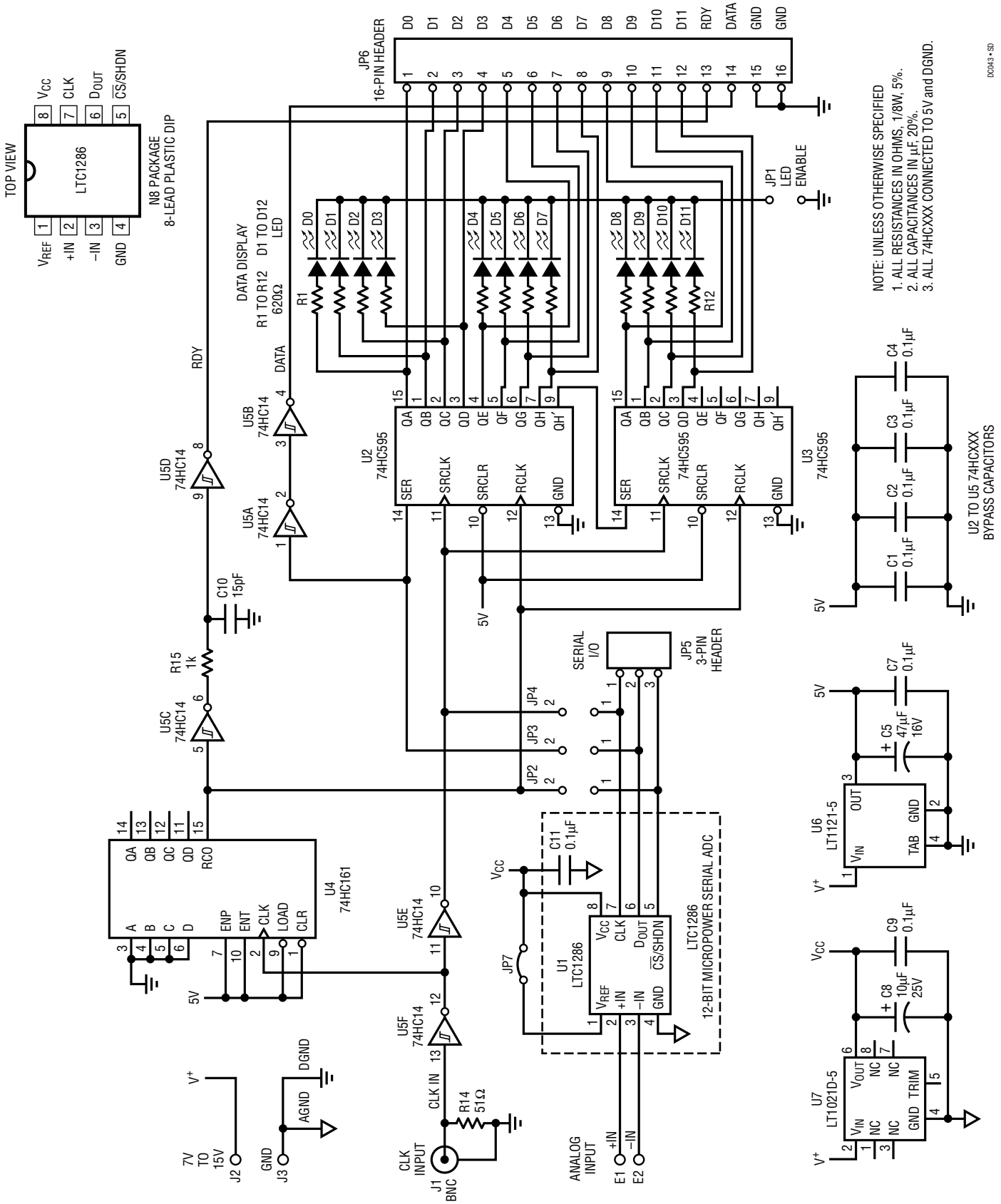
LT1286/98 G03



DC043 • BP01

Actual Size

SCHEMATIC DIAGRAM



PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1 to C4, C7, C9, C11	7	12065C104KATMA	0.1µF 50V 10%, X7R Capacitor	AVX	(803) 946-0362
C5	1	TAJD476K016R	47µF 16V 10%, Tantalum Capacitor	AVX	(207) 282-5111
C8	1	TAJC106K025R	10µF 25V 10%, Tantalum Capacitor	AVX	(207) 282-5111
C10	1	1206CG150J9BB2	15pF 50V 10%, X7R Capacitor	Philips	(407) 744-4200
D0 to D11	12	LN1251C	2.1V 45mW SMT Red LED	Panasonic	(201) 348-5217
E1, E2	2	1502-02	0.094" Turrent Terminal	Keystone	(718) 956-0666
JP1 to JP4	4	TSW-1-2-07-G-S	0.100cc 2-Pin 0.025-SQR Jumper	Samtec	(800) 726-8329
JP5	1	TSW-1-3-07-G-S	0.100cc 3-Pin 0.025-SQR Header	Samtec	(800) 726-8329
JP6	1	TSW-1-8-07-G-D	0.100cc 16-Pin 2-Row Header	Samtec	(800) 726-8329
JP7	1	JL-100-25-T	Jumper Link (0.100 Wire)	Samtec	(800) 726-8329
J1	1	227699-3	50Ω Vert. PC-MNT BNC CON	AMP	(717) 564-0100
J2, J3	2	575-4	0.175-ID Low-Pro Banana Jack	Keystone	(718) 956-0666
R1 to R12	12	CR32-621J-T	620Ω 1/8W 5% Chip Resistor	AVX	(803) 448-9411
R14	1	9C12063A51R0JM	51Ω 1/8W 5% Chip Resistor	Philips	(817) 325-7871
R15	1	CR32-102J-T	1k 1/8W 5% Chip Resistor	AVX	(803) 448-9411
U1	1	LTC1286CS8	12-Bit SER ADC I.C.	LTC	(408) 432-1900
U2, U3	2	MC74HC595AD	8-Bit SHFT REG I.C.	Motorola	(602) 655-3005
U4	1	MC74HC161D	4-Bit BIN CNTR I.C.	Motorola	(602) 655-3005
U5	1	MC74HC14AD	HEX Inverter	Motorola	(602) 655-3005
U6	1	LT1121CST-5	5V Regulator	LTC	(408) 432-1900
U7	1	LT1021DCS8-5	5V Reference	LTC	(408) 432-1900
	4	SNT-100-BK-T	0.100cc Shunt	Samtec	(800) 726-8329
	4	HTSP-3	#4-40 × 1/2" F/F Plastic Standoff	Micro Plastic	(501) 453-8861
	4	Any	#4-40, 3/8" Phillips Pan Head Screw		

OPERATION

OPERATING THE BOARD

Powering the Board

To use the demo board, apply a 7V to 15V power source capable of supplying ≥100mA to the banana jacks (J2 and J3). Be careful to observe the correct polarity. Internal regulators provide 5V to the V_{CC} and V_{REF} pin of the LTC1286. A LT1121-5 regulator provides 5V for the digital circuitry.

Applying the Analog Input

Analog signals are applied to the LTC1268 demo board using turret terminals +IN and –IN. The analog signal input range is 0V to 5V. Optimum performance is achieved using a signal source that has low output impedance, is low noise and has low distortion. Signal generators such as the B & K Type 1051 sine generator give excellent results.

Applying the Clock Signal

The clock signal is applied to BNC connector J1 and the $\overline{CS}$ signal is generated on the board. The clock input uses TTL or CMOS levels. The maximum clock frequency is 200kHz. After applying the clock signal and while it is active, a high-to-low logic level transition on the LTC1286's $\overline{CS}$ input initiates a conversion and data transfer as shown in Figure 1.

OPERATION

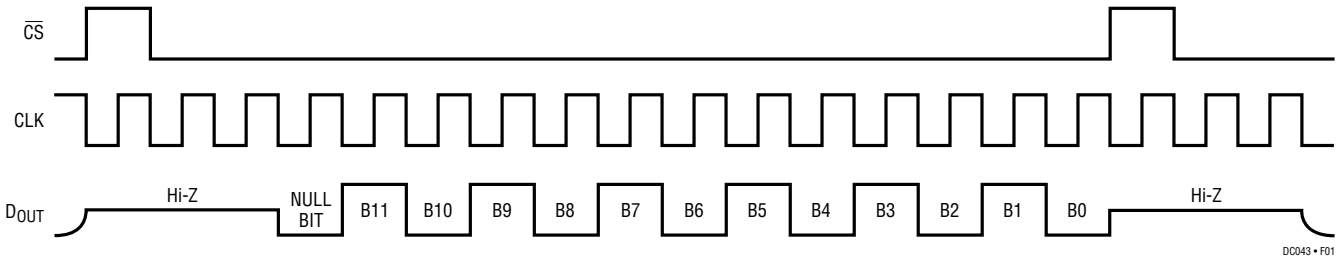


Figure 1. Timing Diagram

Reading the Output Data

The ADC serial data outputs are buffered by the two 74HC595 latches and are available as a parallel output on connector JP6. The latches are used to drive the LEDs and connector (Refer to the LTC1286 data sheet for details on different digital interface modes).

The LTC1286 output data is in unipolar format. A Data Ready line, RDY, (JP6 pin 13) is provided to latch the data. Data is valid on the rising edge of RDY. Connector JP6 has two ground pins (JP6 pin 15 and JP6 pin 16). These pins should be connected to the digital ground of a data receiving system.

The LTC1286 data word can be acquired with a logic analyzer. By using a logic analyzer that has a PC-compatible floppy drive, (such as an HP1663A), conversion data can be stored on a disk and easily transferred to a PC. Once the data is transfered to a PC, programs such as Mathcad or Excel can be used to calculate FFTs. The FFTs can be used to obtain LTC1286 AC specifications such as signal-to-noise ratio and total harmonic distortion.

LEDs D0 to D11 provide a visual display of the LTC1286 digital output word. D0 is the LSB and D11 is the MSB. Jumper JP1 can be removed to disable the LEDs reducing supply consumption by up to 56mA.

Driving $\overline{CS}$ and CLK

Jumpers for $\overline{CS}$, CLK, and D_{OUT} (JP2 to JP4) are shorted for normal operation. The jumpers can be removed and $\overline{CS}$ and CLK lines can be externally driven if desired. See the LTC1286 data sheet for details on driving these lines.

LAYOUT

The use of separate analog and digital ground planes is a good practice for a well designed PC board using the LTC1286. The proper way to make the analog and digital ground planes can be seen by examining the solder side of the PCB layout. The two ground planes are completely isolated except for one connection near the top of the board. The two ground planes follow the same path on the component and solder sides of the board to reduce coupling between the ground planes. Further, any trace that opens a portion of the ground plane may reduce the ground plane's efficiency. Therefore, ensure that the analog ground plane's solder side has a limited number of plane-breaking traces within it. The analog and digital traces do not cross each other (whether on the board's top or bottom side) or run adjacent to each other.

BYPASSING

It is important that the supply and reference bypass capacitors for the LTC1286 be placed as close as possible to the supply and reference pins. The ground side of the capacitors should have very short paths to analog ground. The V_{CC} and V_{REF} pins should be bypassed with high quality ceramic capacitors of at least 0.1µF.

OPERATION

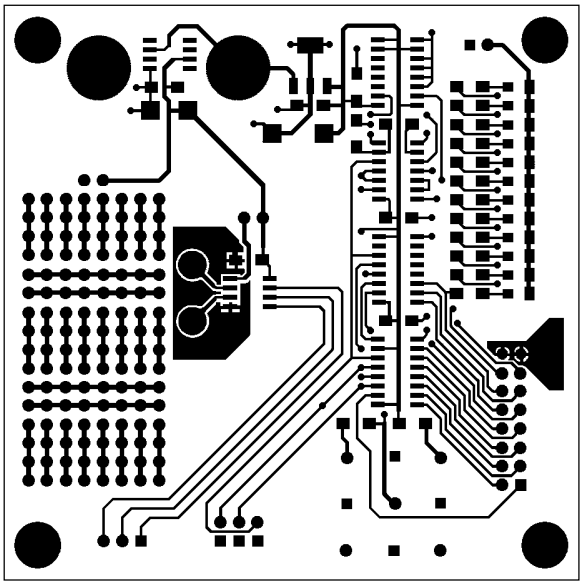
Table 1.

JUMPER	JUMPER NAME	JUMPER CONNECTION
JP1	LED Enable	Shorted to enable LEDs. Open to disable the LEDs.
JP2	$\overline{CS}$	Shorted for normal operation. If open, the $\overline{CS}$ line can be driven externally to select or deselect the LTC1286.
JP3	D_{OUT}	Shorted for normal operation. If open, the D_{OUT} line can drive a scope probe.
JP4	CLK	Shorted for normal operation. If open, the CLK line can be driven externally to clock the LTC1286.

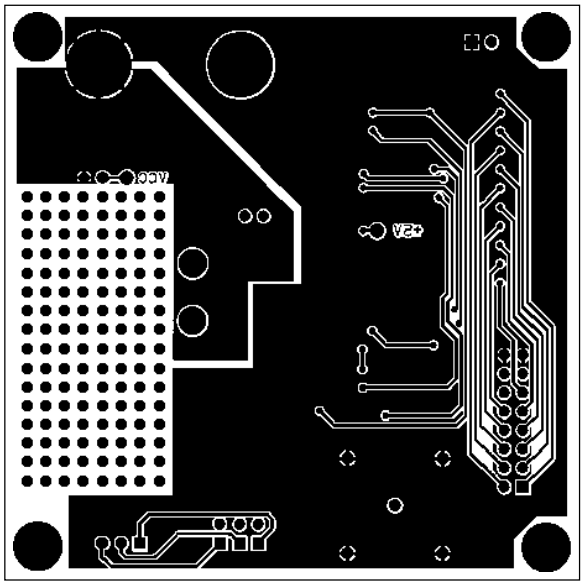
Table 2.

INPUT/OUTPUT PIN	FUNCTION
J1	Clock Input
J2	7V to 15V at ≥100mA
J3	Ground
+IN	Positive Analog Input
–IN	Negative Analog Input
JP6-1	D0 (LSB)
JP6-2	D1
JP6-3	D2
JP6-4	D3
JP6-5	D4
JP6-6	D5
JP6-7	D6
JP6-8	D7
JP6-9	D8
JP6-10	D9
JP6-11	D10
JP6-12	D11 (MSB)
JP6-13	RDY. Can be used by an external system to latch the ADC's output. Latch data on the rising edge.
JP6-14	Data. Serial data output of the ADC
JP6-15 JP6-16	Ground. Connect to the digital ground of a data receiving system.

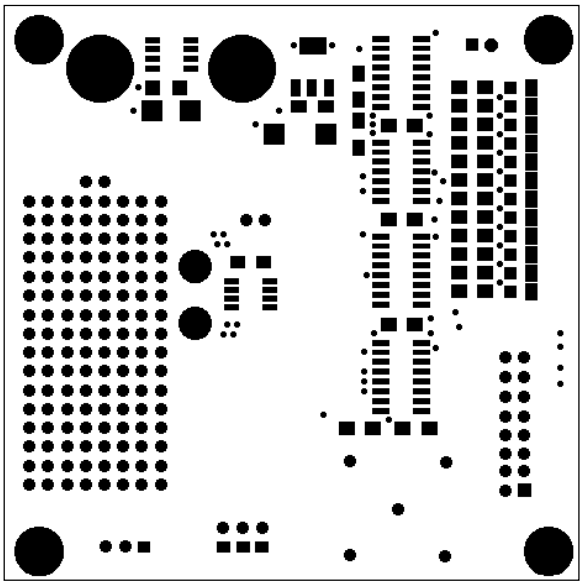
PCB LAYOUT AND FILM



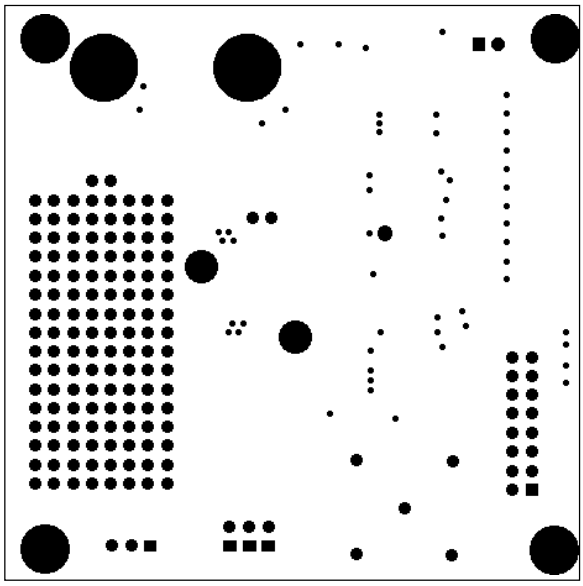
Circuit: Component Side



Circuit: Solder Side

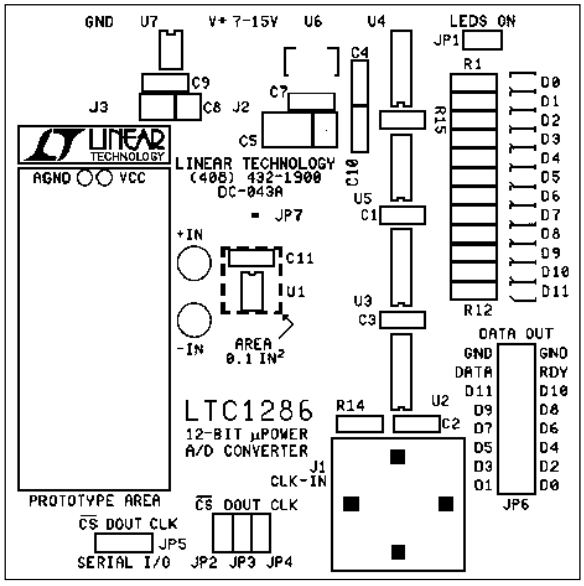


Component Side Solder Mask



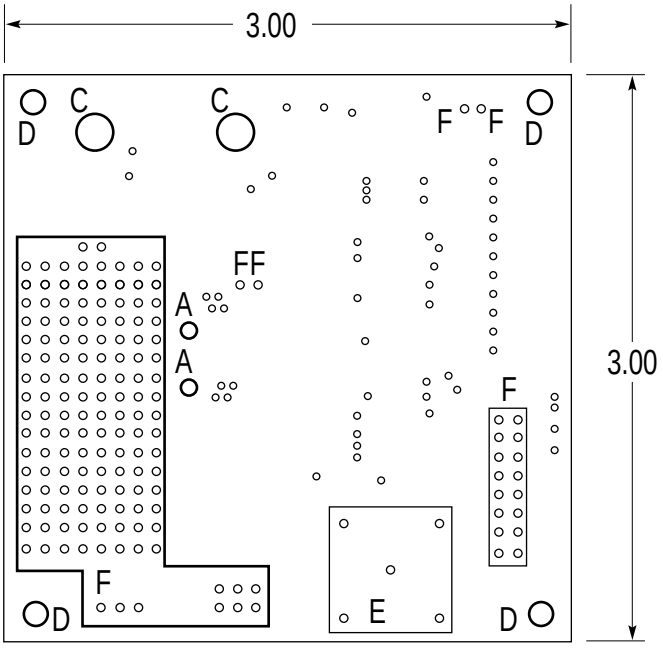
Solder Side Solder Mask

PCB LAYOUT AND FILM



Component Side Silkscreen

PC FAB DRAWING



NOTES:

1. MATERIAL IS FR4, 0.062″ THICK WITH 2 OUNCE COPPER.
2. PCB WILL BE DOUBLE-SIDED WITH PLATED THROUGH-HOLES.
3. HOLE SIZES ARE AFTER PLATING. PLATED THROUGH HOLE WALL THICKNESS MINIMUM 0.0014″ (1OZ.).
4. USE PADMASTER PROCESS.
5. SOLDER MASK BOTH SIDES WITH PC401 USING FILM PROVIDED.
6. SILKSCREEN COMPONENT SIDE USING FILM PROVIDED. USE WHITE, NON-CONDUCTIVE INK.
7. ALL DIMENSIONS ARE IN INCHES.

SYMBOL	DIAMETER	# OF HOLES
A	0.094	2
C	0.210	2
D	0.120	4
E	0.043	5
F	0.039	159
UNMARKED	0.020	57
	TOTAL HOLES	229

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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