UCC2863x, High-Power Flyback Controller with Primary-Side Regulation and Peak-Power Mode

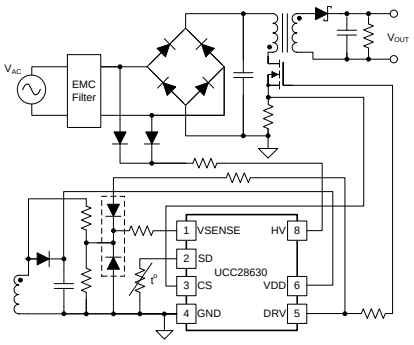
1 Features

- High-Power, Primary-Side CV/CC Regulation
- Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) Operation
- Built-In 700-V Start-Up Current Source
- Active X-Capacitor Discharge (UCC28630 and UCC28633)
- Adjustable Constant-Current (CC) Mode Limiting (except for UCC28630)
- High Gate Drive Current 1-A Source and 2-A Sink
- Low Power Modes for <30-mW System Standby
- Best-In-Class Light Load (10%) Efficiency >85%
- PSR design with no opto-coupler - can meet high CM isolation & surge requirements
- VDD OVP for independent indirect output OV under open-feedback fault conditions
- Peak-Power Mode for Transient Overload
- Shutdown Pin Interface for External NTC
- Protections: Overvoltage, Overcurrent, Over-Temperature, Overload Timer (UCC28630), AC Line UV, Brownout and Pin Protections
- Frequency Dither to Ease EMI Compliance (except the UCC28632)
- Create a Custom Design Using the UCC2863x With the WEBENCH® Power Designer

2 Applications

- AC-DC Adapters for Notebook, Game Consoles, Printers
- Open Frame SMPS for Industrial, Printer, White Goods, LCD Monitors
- Energy Efficient AC-DC Supplies for Nominal Power 10-W to 65-W, (with up to 200% transient peak power)

Simplified Schematic



3 Description

The UCC2863x targets high-power, primary-side regulated flyback converters. The ability to operate in both CCM and DCM make the device suitable for applications with a wide power range. The peak power mode allows transient peak power delivery up to 200% of nominal rating, with only a 25% peak current increase, maximizing transformer utilization.

The transformer bias winding is used to sense output voltage for regulation, and for low-loss input voltage sensing. Advanced sampling techniques allow CCM operation, and deliver excellent output voltage regulation performance for opto-coupler-less designs at power levels of 100 W and above.

A high-voltage current source enables fast and efficient start-up. Advanced light-load modes are deployed to reduce both controller and system power consumption at no load and light load. These modes enable potential system designs to meet 30-mW no-load power for power designs up to 30 W nominal, 60 W peak.

The device has been designed for ease-of-use and incorporates many features to enable a wide range of designs. Extensive protection features are included to simplify system design.

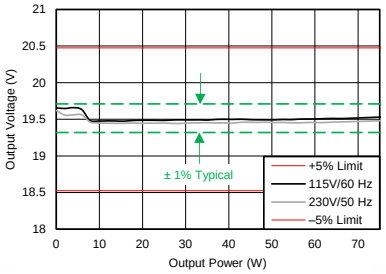
See the Device Comparison Table for details.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
UCC28630	SOIC (7)	4.90 mm x 3.90 mm
UCC28631		
UCC28632		
UCC28633		
UCC28634		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Measured Regulation



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (March 2015) to Revision D **Page**

- Added UCC28634 initial release. ... 1
- Deleted text "for 65-W Nominal Power Design" ... 1
- Added text "PSR design with no opto-coupler - can meet high CM isolation & surge requirements" ... 1
- Added text "VDD OVP for independent indirect output OV under open-feedback fault conditions" ... 1
- Added Webench links. ... 1
- Added Device Comparison Table details. ... 1
- Added UCC28634 to the Device Information Table. ... 1
- Added UCC28634 to the Device Comparison Table. ... 5
- Added UCC28634 to Thermal Information ... 7
- Added UCC28634 to Electrical Characteristics ... 8
- Added UCC28634 to Electrical Characteristics ... 8
- Changed picture to represent added UCC28634 ... 10
- Added UCC28634 ... 13
- Added UCC28634 ... 15
- Added UCC28634 ... 16
- Changed to correct picture link ... 19
- Changed to fix equation typo ... 21
- Added UCC28634 ... 41
- Changed to correct typo ... 41
- Changed to correct typo, changed from 4.7 to 47 ... 41
- Added paragraph to clarify the fault protection. ... 41
- Added UCC28634 ... 42
- Added text "For UCC28634, all pin-faults are non-latching." ... 43
- Added UCC28634 to the table ... 52
- Changed equation to fix typo ... 67

Changes from Revision B (March 2014) to Revision C **Page**

- Changed "No" to "Yes" in Device Comparison Table for Part# UCC28633D, "ACTIVE-X CAPACITOR DISCHARGE" column ... 5
- Changed "Handling Ratings" table to "ESD Ratings" table. Moved Storage Temperature and Lead Temperature to Abs Max Ratings table. ... 6
- Revised Figure 40 ... 47

Changes from Revision A (January 2014) to Revision B **Page**

- Added parts UCC28631, UCC28632 and UCC28633 to the datasheet. ... 1
- Added Active X-Capacitor Discharge Function reference to the UCC28630 and UCC28633. ... 1
- Added Adjustable Constant-Current (CC) Mode Limiting bullet. ... 1
- Added Overload Timer reference to the UCC28630 only. ... 1
- Added Frequency Dither to Ease EMI Compliance exception for the UCC28632. ... 1
- Added UCC28631D, UCC28632D and UCC28633D to the Device Information Section. ... 1
- Added Device Comparison Table. ... 5
- Added UCC28632 Frequency dither range exception. ... 8
- Added UCC28632 Dither repetition period exception. ... 8

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- Added UCC28633 Wake-up level (rising) exception. 8
- Added UCC28633 SD $V_{WAKE(rise)}$ vs. Temperature exception. 12
- Added text to the, "The controller operates in either DCM and CCM..." paragraph. 13
- Changed the "Supply the device bias power during latched fault mode" bullet. 15
- Added UCC28630 and UCC28633 only exception to the "AC sense input for X-capacitor discharge detect" bullet. 15
- Changed HV Pin Connection diagram. 15
- Added sentence, "In the UCC28631 and the UCC28632, the HV pin can connect to either the AC or DC side of the bridge." 16
- Added VIN(avg) definition. 16
- Added (UCC28630 and UCC28633 only) to the Active X-Capacitor Discharge section. 19
- Added UCC28633 to the Improved Performance with UCC28630 section. 20
- Added UCC28631, UCC28632 and the UCC28633 $I_{OUT(lim)}$ adjustment note. 37
- Added UCC28630 only note to the Primary-Side Overload Timer section. 38
- Added UCC28630 only note added to the Overload Timer Adjustment section. 40
- Added CC-Mode $I_{OUT(lim)}$ Adjustment section. 41
- Added UCC28631, UCC28632 and the UCC28633 to the Fault Sources and Associated Responses table. 42
- Added The fault response (latching or auto recovery) depends on the device variant, per Table 3. 44
- Added The fault response (latching or recovery) depends on the device variant, per Table 3. 44
- Added UCC28633 exception to the External SD Pin Wake Input section. 45
- Added External Wake Input at VSENSE Pin (UCC28633 Only) section. 46
- Added UCC28632 exception to the Frequency Dither For EMI section. 51
- Added External Wake Pulse Calculation at VSENSE Pin (UCC28633 Only) section. 66

Changes from Original (January 2014) to Revision A **Page**

- Changed marketing status from Product Preview to Production Data. 1

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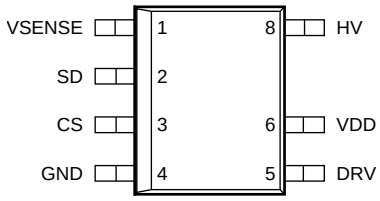
5 Device Comparison Table

ORDER NUMBER	FEATURES				
	ACTIVE-X CAPACITOR DISCHARGE	OVERLOAD TIMER	ADJUSTABLE CC LIMIT	FREQUENCY DITHER	SECONDARY-SIDE WAKE UP
UCC28630D	Yes	Yes	No	Yes	SD Pin
UCC28631D	No	No	Yes	Yes	SD Pin
UCC28632D	No	No	Yes	No	SD Pin
UCC28633D	Yes	No	Yes	Yes	VSENSE Pin
UCC28634D	No	No	Yes	Yes	SD Pin

6 Pin Configuration and Functions

7-Pin SOIC
Package D
(Top View)



PIN Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	3	I	Current sense input
DRV	5	O	Output drive pin for the external flyback MOSFET
GND	4	G	Ground reference connection for all signals
HV	8	P	High-voltage connection to the internal high-voltage start-up current source
SD	2	I	Latching fault shutdown input pin. May be connected to an external temperature sensor
VDD	6	P	Bias supply input pin to the device. Decoupled with a 1-µF ceramic bypass capacitor, connect directly across pins 6-4. Connect an additional hold-up capacitor charged from the transformer auxiliary bias winding to this pin.
VSENSE	1	I	Sense pin for the flyback transformer bias and sense winding for output feedback regulation, output OVP, and input voltage sense/UV protection

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Start-up pin voltage	HV		700	V
Bias supply voltage	VDD		20	
Current sense input voltage	CS	–0.3	1.5	
All other input pins	VSENSE	–0.3	VDD	
	SD	–0.3	VDD	
Operating junction temperature range, T_J		–40	125	°C
Storage temperature, T_{stg}		-65	125	
Lead temperature			260	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. All voltages are with respect to GND. These ratings apply over the junction operating temperature ranges unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
CS input	0		1.0	V
All other inputs (except HV, CS)	0		VDD	
SD pin external capacitance	0		1	nF
R_{HV}, external resistor on HV pin, see Figure 15	180	200	220	kΩ
R_P, external pull-up resistor on VSENSE pin, see Figure 21	3.8	3.9	4.0	

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7.4 Thermal Information (UCC28630, UCC28631)

THERMAL METRIC(1)		UCC28630	UCC28631	UNIT
		D	D	
		7 PINS	7 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	128.5	128.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	57.3	57.3	
θ_{JB}	Junction-to-board thermal resistance	83.4	83.4	
ψ_{JT}	Junction-to-top characterization parameter	12.3	12.3	
ψ_{JB}	Junction-to-board characterization parameter	82.1	82.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information (UCC28632, UCC28633, (UCC28630, UCC28634)

THERMAL METRIC(1)		UCC28632	UCC28633	UCC28634	UNIT
		D	D	D	
		7 PINS	7 PINS	7 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	128.5	128.5	128.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	57.3	57.3	57.3	
θ_{JB}	Junction-to-board thermal resistance	83.4	83.4	83.4	
ψ_{JT}	Junction-to-top characterization parameter	12.3	12.3	12.3	
ψ_{JB}	Junction-to-board characterization parameter	82.1	82.1	82.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.6 Electrical Characteristics

over operating junction temperature range (unless otherwise noted) and VDD = 12 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
START-UP CURRENT SOURCE						
I_{VDD0}	VDD pin short-circuit charging current	VDD = 0.2 V, V_{HV} = 100 V	0.6	0.9	1.2	mA
I_{VDD1}	VDD pin final charging current	VDD = 11.9 V, V_{HV} = 100 V	1.1	4.0	7.6	mA
I_{LEAK}	HV current source leakage current	VDD = 18 V, V_{HV} = 100 V HV, current source off, T_A = 25°C		0.1	0.5	µA
SUPPLY VOLTAGE MONITORING						
$V_{DD(start)}$	VDD start-up voltage	VDD increasing	13.00	14.75	16.50	V
$V_{DD(stop)}$	VDD minimum operating voltage after start-up	VDD decreasing after start-up	7.3	8.0	8.5	V
$V_{DD(hyst)}$	VDD start – VDD stop level			6.5		V
$V_{DD(reset)}$	VDD reset restart level		3.5	5.0	6.5	V
$V_{DD(ovp)}$	VDD over-voltage protection level	VDD increasing after start-up, UCC28630, UCC28631, UCC28632, UCC28633	16.5	17.5	18.3	V
		VDD increasing after start-up, UCC28634 only	14.0	14.85	15.55	V
$I_{DD(run)}$	Supply current during normal operation	V_{SENSE} = 0.45 V, CS = 0 V See (1) C_{LOAD} = 700 pF on DRV	6.0	9.0	13.0	mA
$I_{DD(sleep)}$	Supply current during sleep mode, between switching pulses	V_{SENSE} = 8.0 V, V_{CS} = 1.0 V, light-load mode at 200 Hz, T_A = 25°C		90	110	µA
OSCILLATOR						
$f_{SW(max)}$	Maximum switching frequency	V_{SENSE} = 0.45 V, V_{CS} = 0 V	110	120	130	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{SENSE} = 8.0 V, V_{CS} = 1.0 V, light-load mode	0.18	0.20	0.22	kHz
D_{MAX}	Maximum Duty Cycle	V_{SENSE} = 0.45 V, V_{CS} = 0 V		70%		
$t_{ON(min)}$	Minimum On time	V_{SENSE} = 8.0 V, V_{CS} = 1.0 V, light-load mode	550	600	650	ns
$f_{SW(dith)}$	Frequency dither range	Except UCC28632		± 6.7%		
t_{DITH}	Dither repetition period	Except UCC28632		6.0		ms
SHUTDOWN (SD) PIN (EXTERNAL FAULT INPUT)(2)						
I_{PULLUP}	Internal pull-up current source	See (2), (3), (4)	185	210	235	µA
$V_{TRIP(rise)}$	Fault ok level (rising)	See (2), (3), (4) , UCC28630, UCC28631, UCC28632,UCC28633	3.2	3.5	3.8	V
		See (2), (3), (4) , UCC28634 only	2.2	2.5	2.8	V
$V_{TRIP(fall)}$	Fault trip level (falling)	See (2), (3), (4)	1.7	2.00	2.3	V
$V_{TRIP(hyst)}$		See (2), (3), (4)		1.5		V
$V_{WAKE(rise)}$	Wake-up level (rising)	See (2), (3), (4)Except UCC28633	1.8	2.2	2.6	V
t_{WAKE}	Wake delay time	Delay to first DRV pulse		10		µs

(1) C_{LOAD} = 700 pF included on DRV pin.
(2) The SD pin functions as an NTC input pin (with internal pull-up) during normal operation. The internal pull-up is clamped to 4 V. At start-up, the external temperature sensor (NTC) must be cool enough that the SD pin pulls up above the $V_{TRIP(rise)}$ start level. After start-up, if this pin is pulled below $V_{TRIP(fall)}$ level, this activates external over-temperature shut-down.
(3) During low power modes (when $F_{SW} < F_{SMP(max)}$), the internal SD pin pull-up is disabled, and the pin functions as a transient wake-up input. In this case, if the pin is raised above $V_{WAKE(rise)}$ level, the device wakes from low power sleep mode (rather than waiting for the scheduled timer-based wake). This is useful for applications that require a response to load transients from zero or near-zero load, where a wake-up signal can be appropriately coupled to the SD pin from the secondary-side.
(4) A decoupling capacitor on the SD pin should not be required; if used, it must not exceed 1 nF.

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Electrical Characteristics (continued)

over operating junction temperature range (unless otherwise noted) and VDD = 12 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSENSE Pin (MAGNETIC SENSE)						
$V_{OUT(ref)}$	Internal output voltage sense reference level	Required positive voltage at VSENSE pin during off-time (at 25°C)	7.425	7.500	7.575	V
$t_{OUT(smp)}$	Vsense sample delay for V_{OUT}	Measured w.r.t. DRV falling edge		1.7		µs
$V_{OUT(ovp)}$	Internal output voltage sense OVP level	Measured w.r.t. regulation level, tracking		120%		
CURRENT SENSE (CS) Pin						
$V_{CS(max)}$	Peak CS pin voltage level	At maximum modulator demand		800		mV
$V_{CS(min)}$	Peak CS pin voltage level	At minimum modulator demand		172		mV
V_{SLOPE}	Slope compensation ramp			30		mV/µs
OVER TEMPERATURE PROTECTION						
$TEMP_{TRIP}$	Thermal protection shutdown temperature	Default internal setting, latch-off protection			125	°C
$TEMP_{HYST}$	Thermal protection hysteresis			10		°C
GATE DRIVE OUTPUT (DRV)						
R_{OH}	High level source resistance	I_{OH} = 100 mA		22	35	Ω
R_{OL}	Low level sink resistance	I_{OL} = –100 mA		1.2	2.5	Ω

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7.7 Typical Characteristics

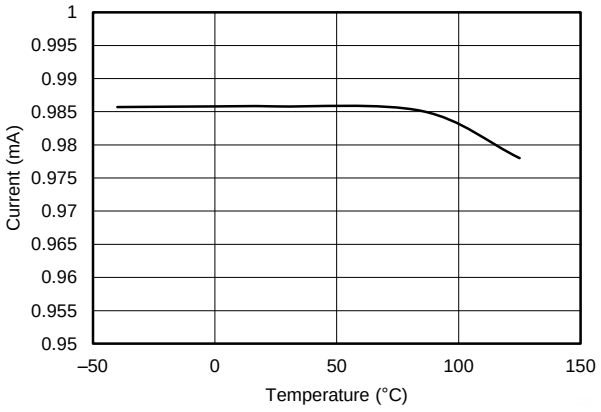

Figure 1. I_{VDD0} Charging Current vs. Temperature

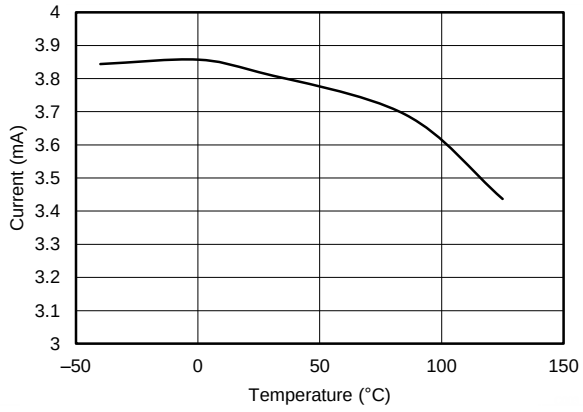

Figure 2. I_{VDD1} Charging Current vs. Temperature

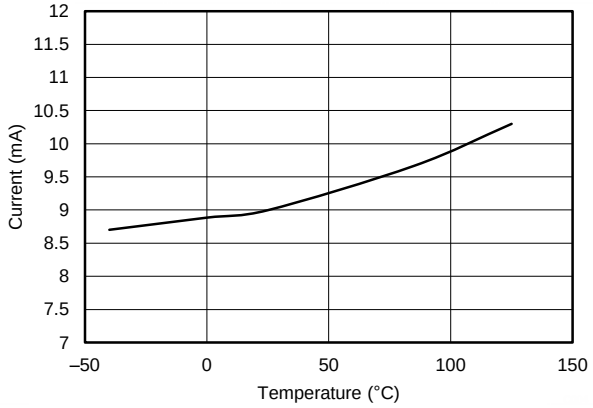

Figure 3. $I_{DD(run)}$ Current vs. Temperature

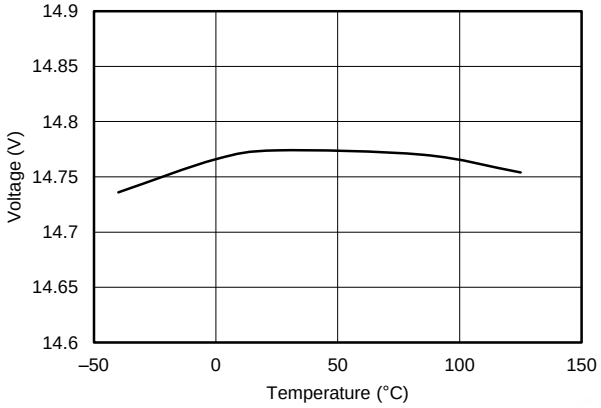

Figure 4. $V_{DD(start)}$ Threshold vs. Temperature

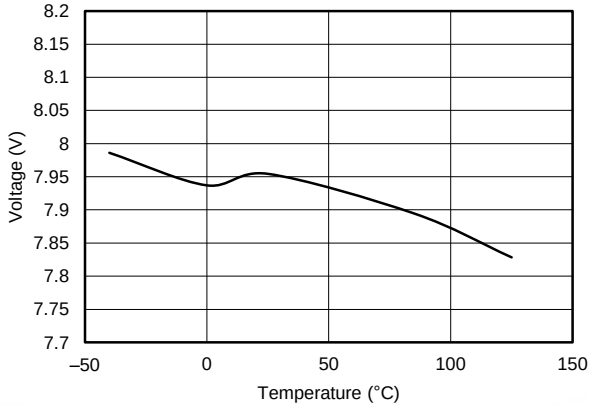

Figure 5. $V_{DD(stop)}$ Threshold vs. Temperature

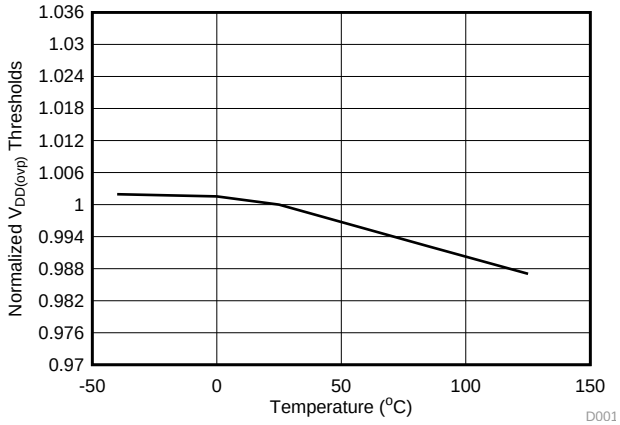

Figure 6. Normalized $V_{DD(ovp)}$ Threshold vs. Temperature

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Typical Characteristics (continued)

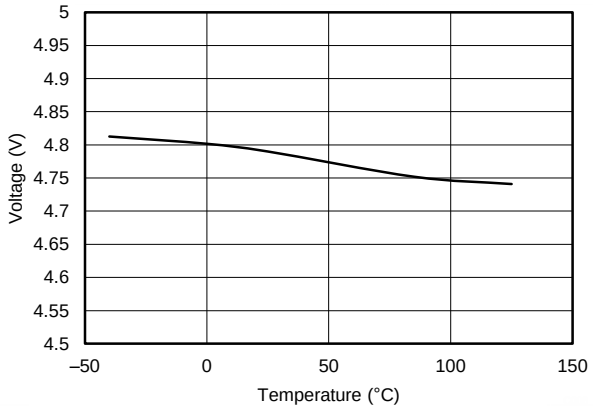

Figure 7. $V_{DD(reset)}$ Threshold vs. Temperature

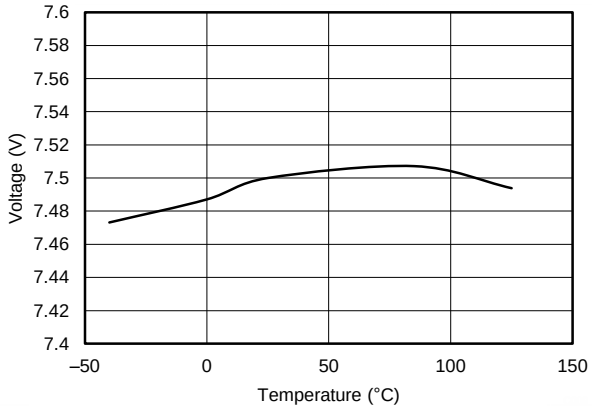

Figure 8. $V_{OUT(ref)}$ vs. Temperature

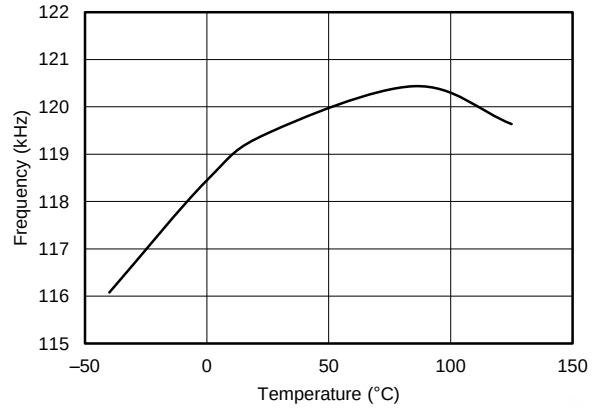

Figure 9. $F_{SW(max)}$ vs. Temperature

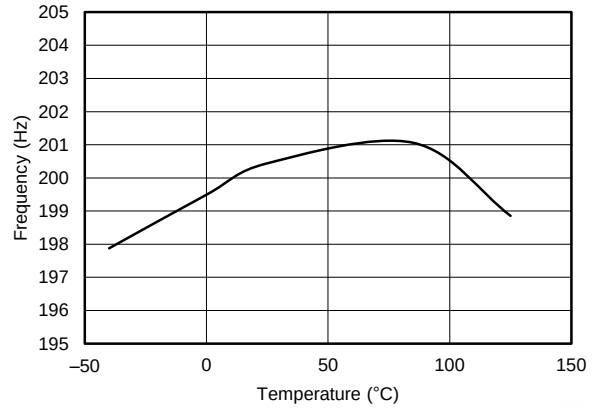

Figure 10. $F_{SW(min)}$ vs. Temperature

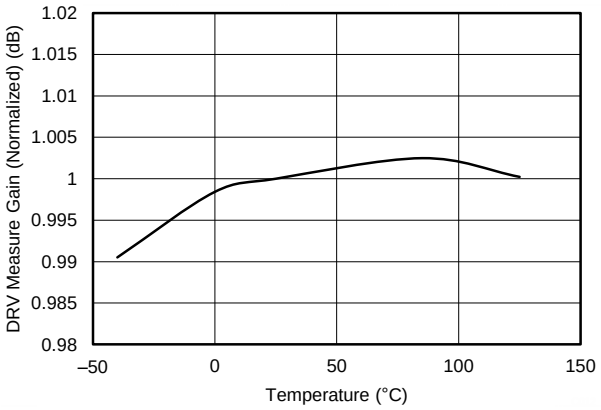

Figure 11. DRV Programming Current Measure vs. Temperature

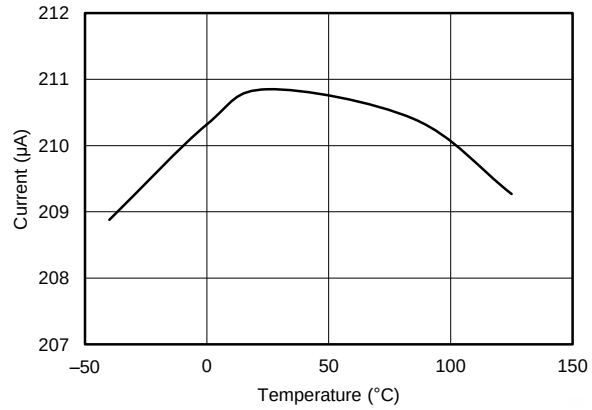

Figure 12. SD Pull-Up vs. Temperature

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Typical Characteristics (continued)

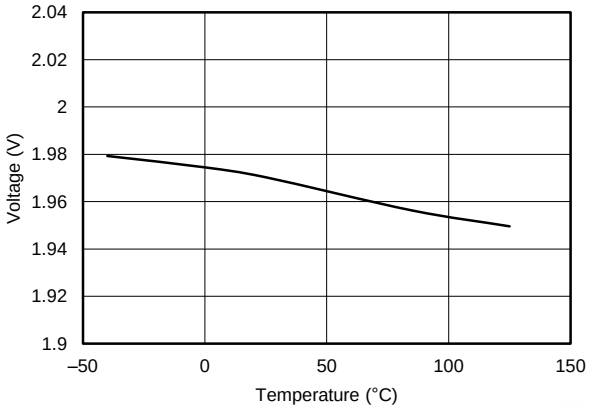

Figure 13. SD $V_{TRIP(fall)}$ vs. Temperature

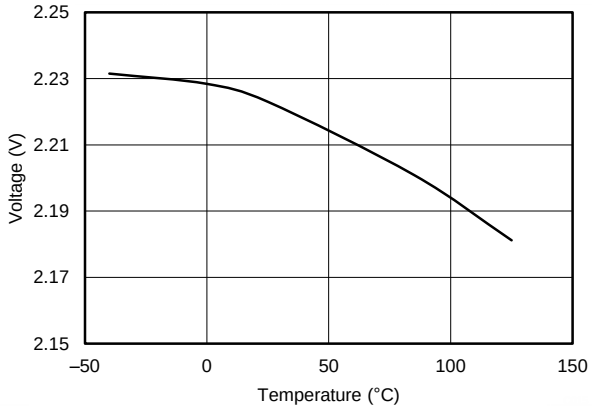

Figure 14. SD $V_{WAKE(rise)}$ vs. Temperature (except UCC28633)

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8 Detailed Description

8.1 Overview

The UCC28630, UCC28631, UCC28633, UCC28633 and UCC28634 family of devices are highly-integrated, primary-side-regulated (PSR) flyback controllers. The device supports magnetically-sensed output voltage regulation via the transformer bias winding. This feature eliminates the need for a secondary-side reference, error amplifier and opto-isolator. The device employs an advanced internal control algorithm that offers accurate static output voltage regulation against line and load. The fixed-point, magnetic-sampling scheme allows operation in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Additionally, the device achieves accurate constant-current (CC) control of the output current limit using only primary-side, current sensing. Uniquely, this CC function operates seamlessly as the operating mode changes between DCM and CCM operation.

The controller includes an internal, high-voltage (HV) start-up current-source, and employs low-power sleep modes and switching frequency reduction, to improve light-load efficiency and standby power. The device typically achieves standby power levels between 0.05% and 0.1% of peak output power.

The controller operates in either DCM and CCM, using a mix of peak current-mode PWM (AM) and switching-frequency modulation (FM) schemes. The control approach improves performance (efficiency, size and cost) and can reduce transformer size and cost by allowing operation in CCM with FM during peak overload conditions. Extensive protection features are incorporated, including output overvoltage protection (OVP), bias rail overvoltage and undervoltage (OV/UV), active X-capacitor discharge, line undervoltage and brownout protection, overcurrent overload timer, open- and short-circuit pin protections, peak current adjustment with line and frequency dither for system EMI reduction. The various devices in the UCC2863x family offer a different mix of features to suit a wide range of applications and requirements.

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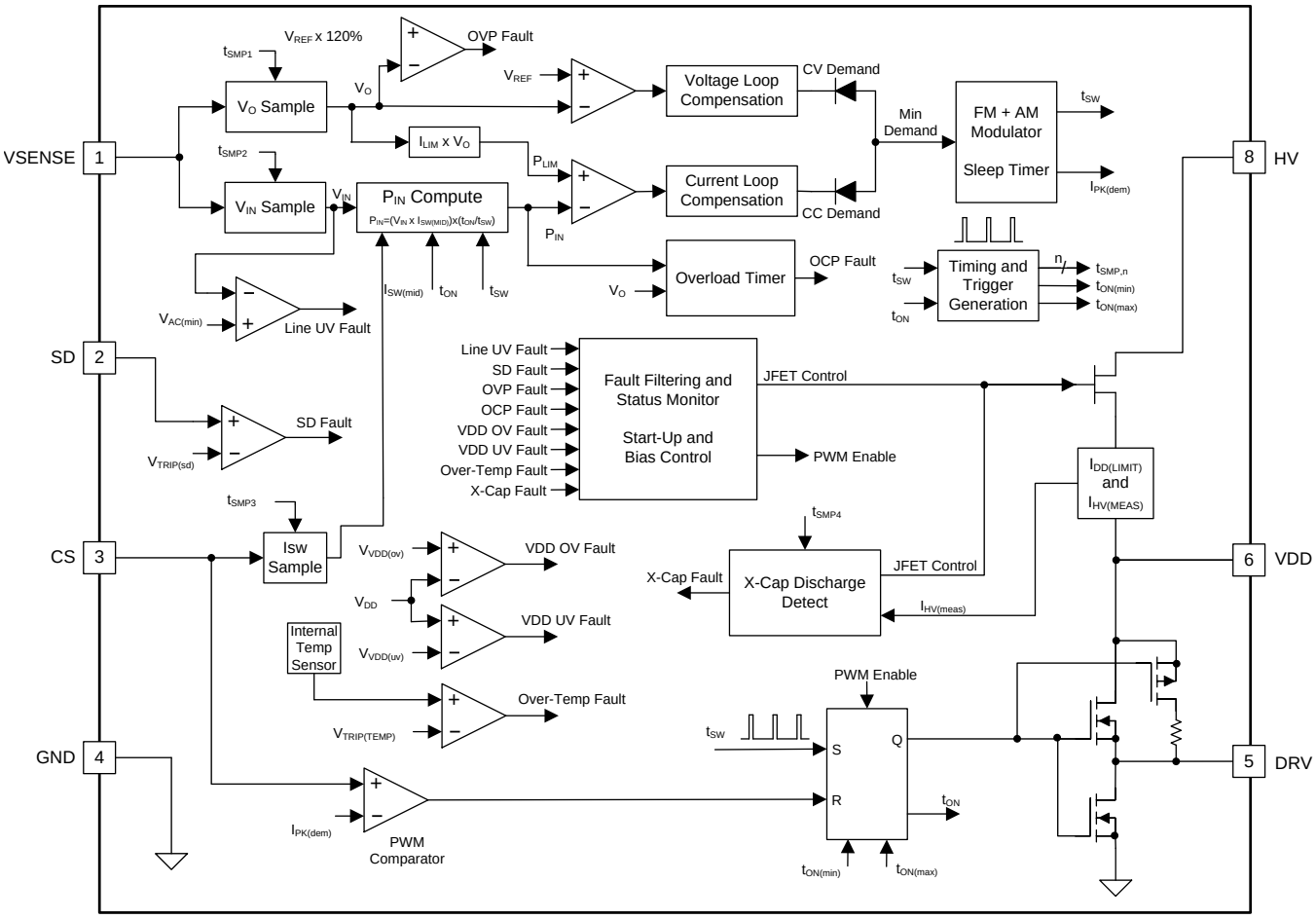
8.2 Functional Block Diagram



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8.3 Feature Description

The application designer requires some key device internal parameters in order to calculate the required power stage components and values for a given design specification. Table 6 summarizes the key parameters.

8.3.1 High-Voltage Current Source Start-Up Operation

The controller includes a switched, high-voltage, current source on the HV pin to allow fast start-up, and eliminates the static power dissipation in a conventional resistive start-up approach. This feature reduces standby power consumption.

The HV pin has three major functions:

- Supply the device start-up current
- Supply the device bias power during latched fault mode
- AC sense input for X-capacitor discharge detect (UCC28630 and UCC28633 only)

The UCC28630 and UCC28633 input supply to the HV start-up pin must be connected to the AC side of the bridge rectifier as shown in Figure 15, in order to support X-capacitor discharge. More details are given in Active X-Capacitor Discharge (UCC28630 and UCC28633 only), below. Connection to the AC side of the bridge also allows faster detection of AC mains removal under latched fault conditions, allowing prompt reset of latched faults for fast restart.

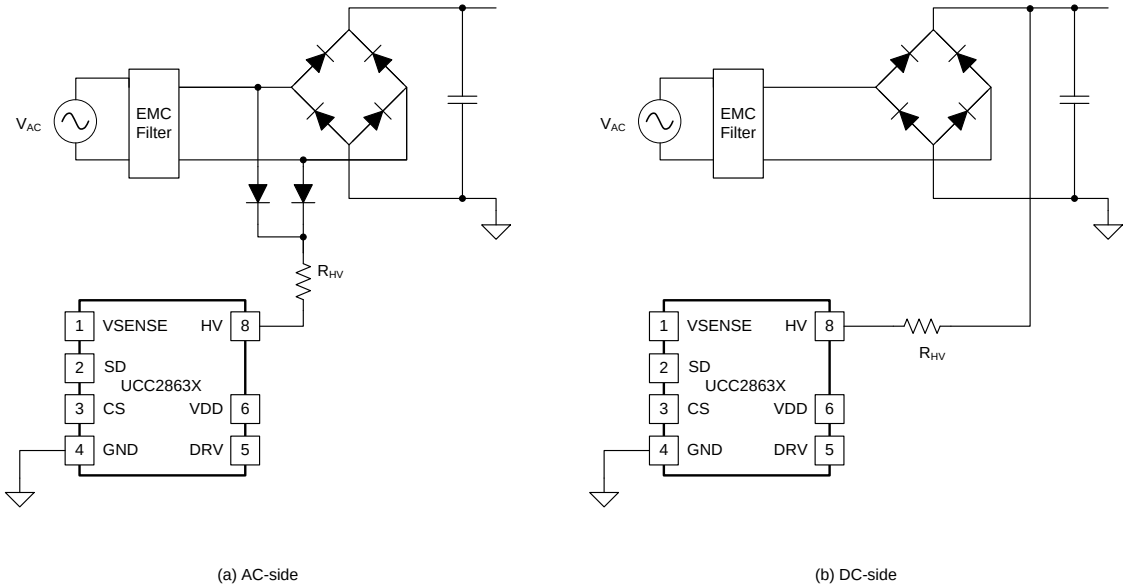

Figure 15. HV Pin Connection: (a) AC-side, (b) DC-side (UCC28631, UCC28632 and UCC28634 only)

Feature Description (continued)

In the UCC28631, UCC28632 and UCC28634, the HV pin can connect to either the AC or DC side of the bridge. The addition of the 200-kΩ external HV resistance (required for X-capacitor discharge sensing) limits the available charging current for the external bias supply input capacitor. However, for typical values of between 22 µF and 33 µF of input capacitance, start-up bias times of less than 1.5 s are achievable at 90 V_{AC}. Start-up time can be estimated using Equation 1.

$$t_{START} = R_{HV} \times C_{VDD} \times \ln\left(\frac{V_{IN(avg)}}{V_{IN(avg)} - V_{DD(start_max)}}\right)$$

where

- $V_{IN(avg)} = V_{RMS} \times \frac{2 \times \sqrt{2}}{\pi}$ for AC connection and $V_{IN(avg)} = V_{RMS} \times \sqrt{2}$ for DC connection (1)

For 90 V_{AC}, if C_{VDD} = 22 µF and worst case $V_{DD(start_max)}$ = 16.5 V, then t_{START} is 1.002 s.

Figure 16 illustrates the start-up behavior of the controller. The HV current source has built-in short-circuit protection that limits the initial charge current out of the bias voltage pin until the bias voltage reaches $V_{DD(sc)}$. This limits the power dissipated in the HV current source in the event of a short circuit on the VDD pin. Thereafter, the HV current source switches to full available current. The controller remains in a low-power, start-up mode until the bias voltage reaches $V_{DD(start)}$, after which the HV current source is turned off and the controller initiates a start-up sequence.

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Feature Description (continued)

The bias voltage decays during the start-up sequence at a rate dependent on the size of the energy storage capacitor connected to the VDD pin. The VDD storage capacitor must be sized appropriately to ensure adequate energy storage to supply both the controller bias power and MOSFET drive power during start-up, until the VDD rail can be supplied through the transformer bias winding. If the bias voltage falls below $V_{DD(stop)}$ (due to bias winding fault or an inadequate VDD storage capacitance), the controller stops switching, and transitions into low-power mode for a time delay of $t_{RESET(long)}$, or until the bias voltage falls to the $V_{DD(reset)}$ level, whichever is shorter. See VDD Capacitor Selection for required VDD capacitor sizing. Once the time delay elapses, the bias voltage rapidly discharges to the $V_{DD(reset)}$ level, followed by turn-on of the internal HV current source, and a normal restart attempt follows.

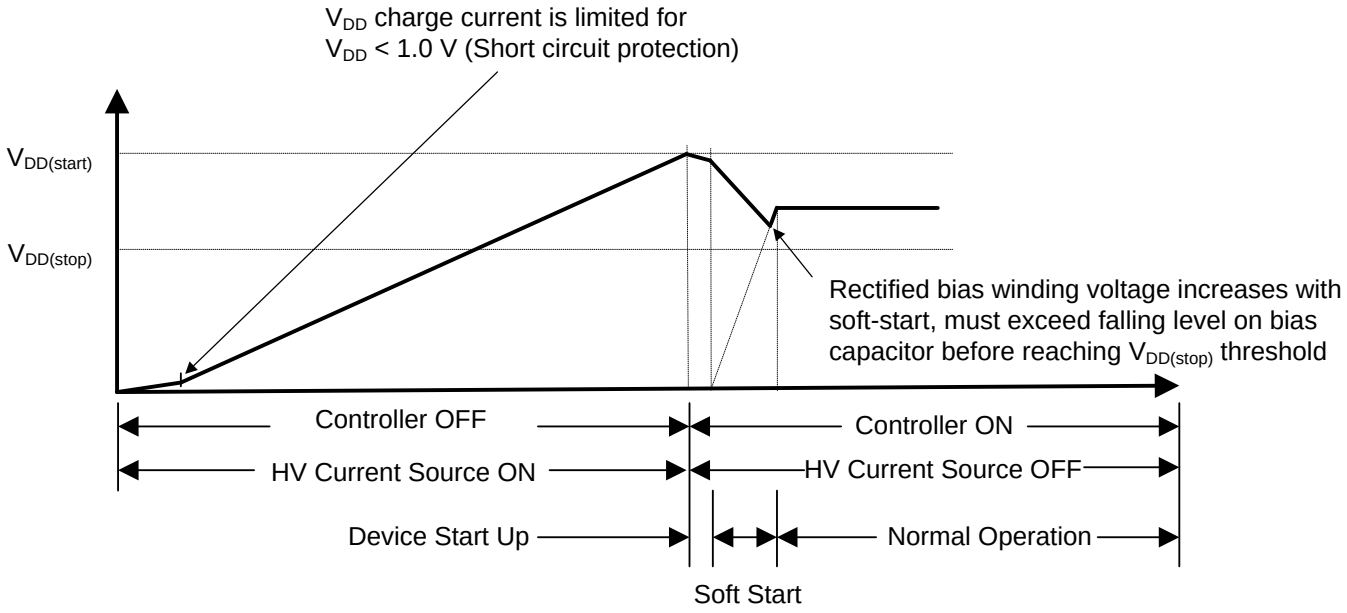

Figure 16. Normal Start-Up Sequence, (assuming V_{AC} > UV start threshold)

Feature Description (continued)

8.3.2 AC Input UVLO / Brownout Protection

At start-up, once the VDD pin has reached the $V_{DD(start)}$ level, the internal start-up current source is turned off. The controller tests the voltage across the bulk capacitor to determine if the level is high enough to allow the power stage to start, if it has exceeded the rising AC_{ON} level. Because there is no load across the bulk capacitor at this stage, the bulk voltage can be used as a proxy for the peak of the AC line. In order to measure the bulk voltage in a low-loss fashion, the controller generates a sequence of three exploratory switching pulses at a frequency of $f_{SW(uv)}$, at minimum peak-current demand level $V_{CS(min)}$ to avoid audible noise, and to deliver minimum energy to the output of the power stage.

Based on the magnetic sampling information determined via the bias winding during these switching pulses, if the output voltage is greater than the output overvoltage threshold, the pulsing stops immediately, and the controller transitions into latched-fault mode. If, however, there is no overvoltage condition detected at the output, the pulse-set completes. If the sensed line voltage is above the line AC_{ON} start threshold, then the controller starts up normally, and begins to generate the PWM drive pulses that charge and regulate the output voltage. Alternatively, if the sensed bulk level is below the AC_{ON} threshold, then the controller enters low power mode for the reset period ($t_{RESET(short)}$). It then depletes the VDD rail to the $V_{DD(reset)}$ level. At this point, the start-up sequence repeats, and the device generates another set of exploratory switching pulses. This sequence repeats indefinitely until the AC input is increased to a sufficient level that the bulk voltage exceeds the AC_{ON} level.

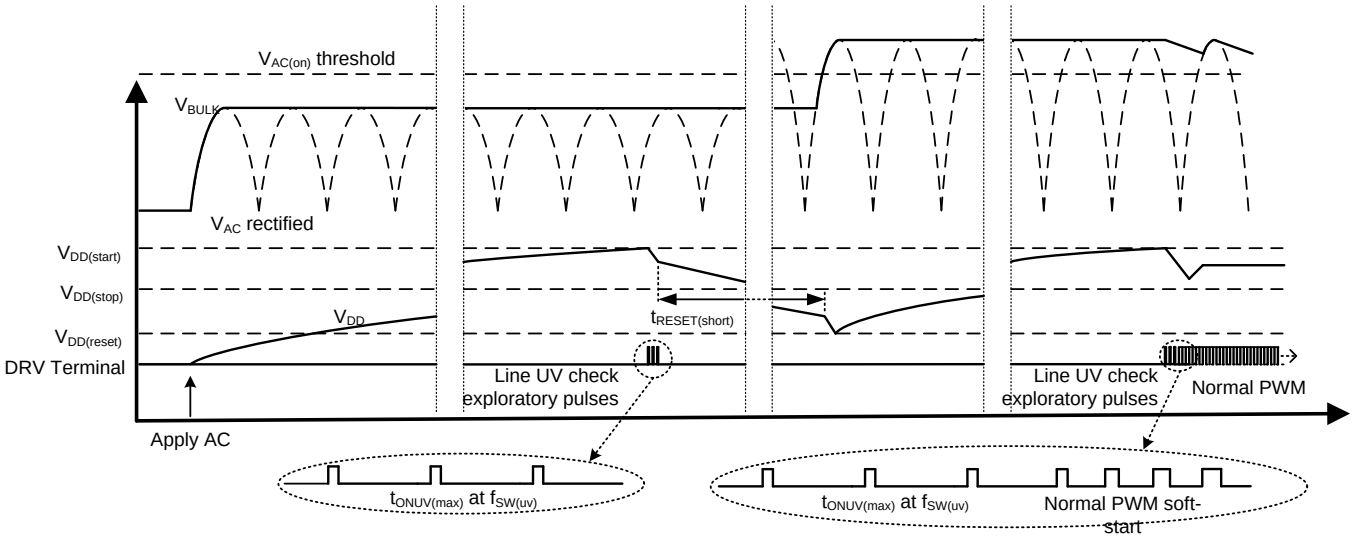

Figure 17. AC Input UVLO Detection and Start Up

Once started, the controller regularly monitors the bulk capacitor voltage. Because the ripple on the bulk capacitor depends on the load level, the device determines the maximum bulk level every 11 ms (approprite for minimum AC frequency of 47 Hz), so the AC peak can be determined. The controller provides input undervoltage protection based on the sensed AC peak level. Once the peak drops below the AC_{OFF} level for the delay period ($t_{UV(delay)}$), the PWM switching halts, and the controller enters low-power mode for the reset period ($t_{RESET(short)}$). The device then discharges the bias voltage to the $V_{DD(reset)}$ level, followed by a restart sequence. The controller cycles through the AC_{ON}, monitoring (detailed above) indefinitely until the AC input again rises above the AC_{ON} level.

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Feature Description (continued)

8.3.3 Active X-Capacitor Discharge (UCC28630 and UCC28633 only)

Safety standards such as EN60950 require that any X-capacitors in EMC filters on the AC side of the bridge rectifier quickly discharge to a safe level when AC is disconnected. This discharge requirement ensures that any high-voltage level present at the pins of the AC plug does not present an electric shock hazard. The standards require that the voltage across the X-capacitor decay with a maximum time constant of 1 second. Typically, this requirement is achieved by including a resistive discharge element in parallel with the X-capacitor. However, this resistance causes a continuous power dissipation that impacts the standby power performance. The power dissipation in the discharge resistors depends on the X-capacitor value. Assuming that the discharge resistor meets the 1-second time-constant requirement, (in other words, the R-C product is 1 second) the dissipation is described in Equation 2.

$$P_X = V_{AC}^2 \times C_X \tag{2}$$

Thus at 230 V_{AC}, the discharge resistor causes 5.3-mW dissipation for every 100 nF of X-capacitance – for a typical 470-nF X-capacitor value, that causes 25 mW to be lost in the discharge resistors.

The safety standard does not mandate that the X-capacitor is fully discharged to zero within one second. It simply requires the discharge rate to exhibit a 1-s time constant. Figure 18 shows the discharge characteristic (for a 1-s discharge time constant) versus time, for disconnection at the peak of 90 V_{AC}, 115 V_{AC}, 230 V_{AC} and 264 V_{AC}. For AC inputs above 115 V_{AC}, with 1-s discharge time constant, the voltage does not drop below the Safety-Extra-Low-Voltage (SELV) 60-V level until 1 s or longer. In fact, at 264 V_{AC}, 1.83 seconds elapse before reaching 60 V.

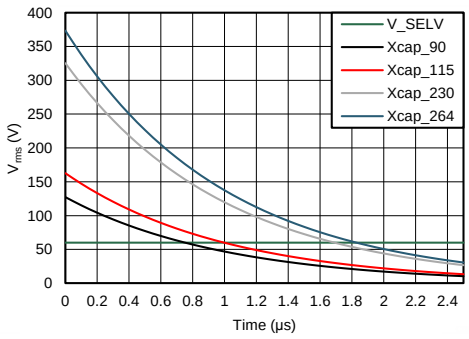

Figure 18. X-Capacitor Discharge with 1-s Time Constant, for Various Voltages

Feature Description (continued)

8.3.3.1 Improved Performance with UCC28630 and UCC28633

In order to reduce standby power and eliminate the standing loss associated with the conventional discharge resistors, the UCC28630 and the UCC28633 devices incorporate active X-capacitor discharge circuitry. This circuit periodically monitors the voltage across the X-capacitor to detect any possible DC-condition (which would indicate that AC mains disconnection has occurred), and then discharges the voltage across the X-capacitor using the internal HV current source. The X-capacitor discharge function discharges the X-capacitor to the SELV 60-V level in 1 s (as long as the design considerations discussed in this section are followed).

The device internally monitors the current into the HV pin to determine if the voltage across the X-capacitor in the EMI filter has a sufficient AC ripple component. If insufficient AC content is detected, then a DC condition is internally flagged. This causes the controller to enter low-power mode for the reset period ($t_{RESET(short)}$), followed by bias voltage discharge to the reset level ($V_{DD(reset)}$) , and then the start-up HV current source turns on again to effectively discharge the X-capacitor by transferring charge to the VDD reservoir capacitor.

Because the device monitors the HV pin to detect a DC condition on the X-capacitor, the system cannot operate with DC input to the HV pin. Instead, the HV pin must be connected to an AC source only. The device interprets any DC input on the HV pin as DC across the X-capacitor, indicating an AC-disconnect event. This causes a repeating cycle of start-up and shutdown. The device requires an external 200-kΩ of resistance on the HV pin, to limit the current to a level below the saturation point of the internal HV current source. This limit produces a HV input current that is approximately proportional to AC line, so that the AC content can be sensed.

The size of the X-capacitor that can be discharged depends on the VDD energy storage capacitor. Assuming the worst case, a maximum X-capacitor disconnect voltage could be at the peak of 264 V_{RMS}, and assuming that it should be discharged down to 60-V SELV level, the minimum allowed VDD capacitor can be sized based on the worst case $V_{DD(reset)}$ and $V_{DD(start)}$ levels as described in Equation 3.

$$C_{VDD} \geq C_X \times \left(\frac{V_{AC(pk)} - V_{SELV}}{V_{DD(start_min)} - V_{DD(reset_max)}} \right) = C_X \times \left(\frac{373 - 60}{13.0 - 6.5} \right) = C_X \times (48.15) \quad (3)$$

For example, for a 330-nF X-capacitor value, the required VDD capacitor is 15.9 µF, so a 22-µF capacitor suffices.

$$C_{VDD} \geq 330\ \text{nF} \times (48.15) = 15.9\ \mu\text{F} \quad (4)$$

In order to reduce the power consumption from the high voltage AC line, the device pulses current into the HV pin at a low frequency with very low duty-cycle. The HV current source on-time ($t_{ON(HV)}$) , repeats at intervals of $t_{SMP(HV)}$. Moreover, the pulsing occurs in bursts, with a time delay between bursts. The sampling occurs in bursts of 21, at intervals of $t_{SMP(HV)}$, with a wait time of $t_{WAIT(HV)}$ between bursts. This reduces the effective average duty-cycle to a very low value (approximately 0.2%), and minimizes the overhead of X-capacitor sampling current and device bias consumption overhead to approximately 2 mW of extra standby consumption at high-line 230 V_{AC}.

The device enables the X-capacitor monitor in latched fault mode, and in light-load regions where the power level is below $P_{LL(\%)}$, as a percentage of the nominal rated level. Above the $P_{LL(\%)}$ level, the X-capacitor monitor is disabled. At this load level the bulk capacitor discharges at a rate that is sufficient to also discharge the X-capacitor, which appears in parallel with the bulk capacitor once the bulk voltage drops far enough to forward bias the bridge rectifier diodes. In this case ensure that the bulk capacitance value is not too large for the power level desired, which in-turn ensures that the bulk capacitor discharge rate is fast enough to discharge the X-capacitor to meet the 1-s discharge target. This can be calculated in Equation 5.

$$C_{BULK} \leq \frac{2\left(\frac{P_{NOM} \times P_{LL\%}}{\eta}\right) \times t_{XCAP(dis)}}{\left(V_{AC(pk)}{}^2 - V_{SELV}{}^2\right)} \quad (5)$$

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Feature Description (continued)

Assuming a worst case AC disconnect at the peak at 264 V_{RMS} (373 V_{PK}), and a requirement to discharge to SELV level of 60 V in $t_{XCAP(dis)}$ of 1 s, for a P_{NOM} of 65 W at 87% efficiency, this is calculated in Equation 6.

$$C_{BULK} \leq \frac{2 \times \left[\frac{(65 \times 0.125)}{0.87}\right] \times 1}{(373^2 - 60^2)} = 138\ \mu F \tag{6}$$

Once the bulk capacitance value is chosen, also ensure that when the bulk capacitor has been discharged down to the line UV AC_{OFF} threshold, that it continues to discharge to an acceptable level during the line UV persistence delay time ($t_{UV(delay)}$) as shown in Equation 7.

$$C_{BULK} \leq \frac{2 \times \left(\frac{P_{NOM} \times P_{LL\%}}{\eta}\right) \times t_{UV(delay)}}{2 \times AC_{OFF}^{\ 2} - V_{SELV}^{\ 2}} \tag{7}$$

Again, taking the example above:

$$C_{BULK} \leq \frac{2 \times \left(\frac{(65 \times 0.125)}{0.87}\right) \times 0.04}{(2 \times 65^2 - 60^2)} = 154\ \mu F \tag{8}$$

Once the first constraint is satisfied, the second one is also automatically met.

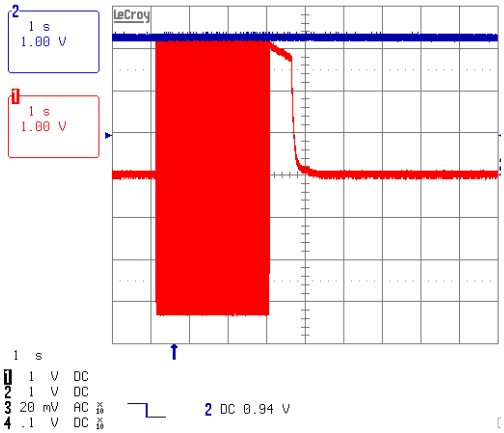

Figure 19. X-Capacitor Discharge Activation, at 230 V_{AC}, No Load (red = X-capacitor, blue = bulk-capacitor, both 100 V/div)

Feature Description (continued)

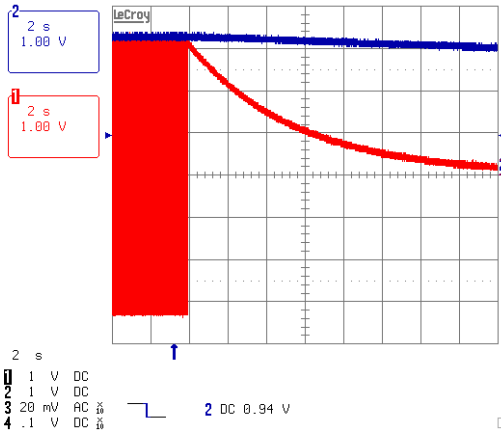

Figure 20. X-Capacitor Decay Rate Without Active Discharge (time constant dominated by 20-MΩ probe impedance) (red = X-capacitor, blue = bulk-capacitor, both 100 V/div)

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Feature Description (continued)

8.3.4 Magnetic Input and Output Voltage Sensing

A sense winding on the transformer is used to measure the input voltage and output voltage of the power stage. This winding is typically the converter bias winding. The sense winding should be interfaced to the VSENSE pin as shown in Figure 21. This interface requires that the voltage across the winding be scaled with a resistor divider R_A / R_B, and then offset with a switched, pull-up resistor R_P (in series with a diode) connected to the gate drive pin DRV.

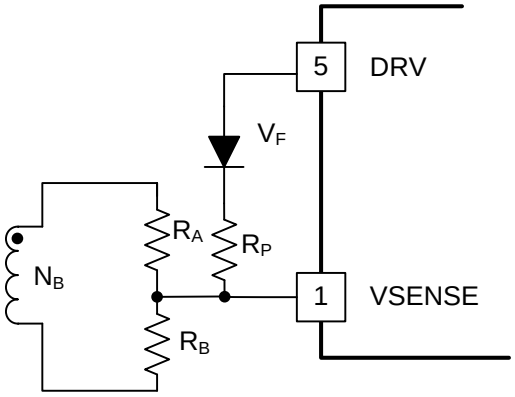

Figure 21. VSENSE Pin Interface Arrangement

During the off-time portion of the switching cycle (also referred to as the flyback interval), the resistor divider (R_B / (R_A + R_B)) scales the positive voltage swing at the VSENSE pin for output voltage regulation, as shown in Figure 22. During this interval, since the DRV output is low, the diode in series with R_P is reverse-biased, and so R_P is out-of-circuit.

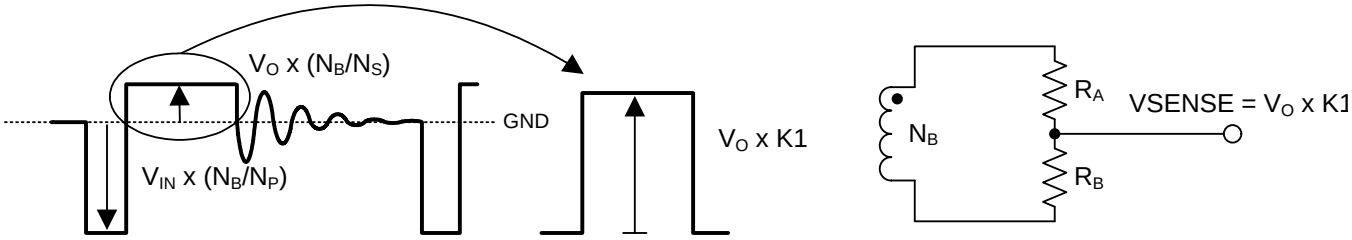

Figure 22. V_{OUT} Sense Using the Positive Swing on the Sense Winding

Feature Description (continued)

During the on-time portion of the switching cycle, when the DRV pin goes high (should swing very close to the value at the VDD pin), the switched pull-up R_P allows the negative swing on the winding to be level-shifted positive, and thus also be sensed at the VSENSE pin, as shown in Figure 23. In this way the bias winding may be used to sense both line input voltage and output voltage.

NOTE

The input voltage sensed by the transformer bias winding is actually the voltage across the bulk capacitor, not the AC input voltage, because the bulk capacitor voltage appears across the primary winding when the flyback switch turns on

Uses of the sensed bulk and output voltages:

- Input AC mains UVLO
- Input brownout
- Line-dependent peak-current adjustment
- Accurate output-current regulation
- Output-voltage regulation
- Output over-voltage protection (OVP)

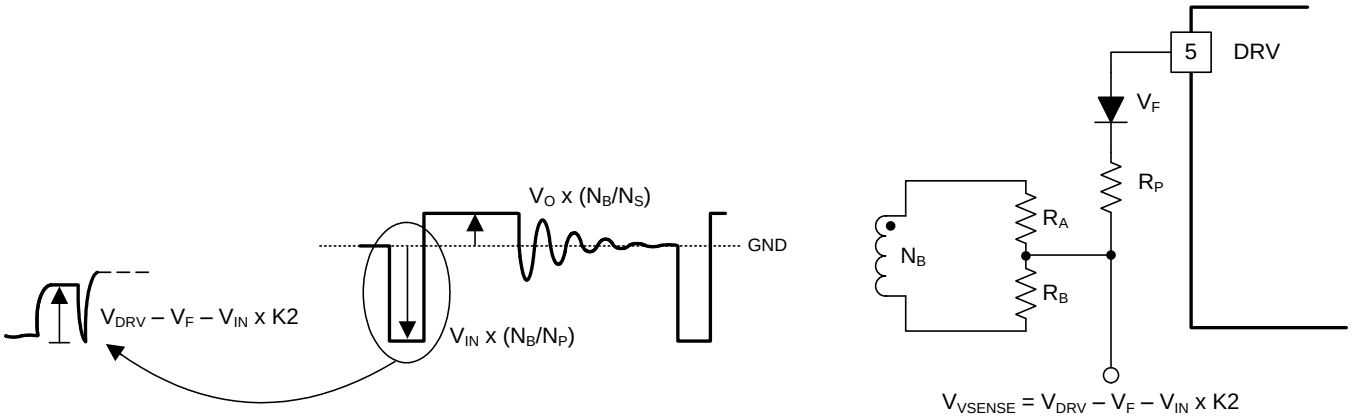

Figure 23. Line Input Sense by Offsetting the Negative Swing on the Sense Winding

In order to protect the VSENSE pin from excessive negative current in the event of a manufacturing fault (such as an open circuit on R_P), use a series limiting resistor and clamping diode on the VSENSE pin. Combine the clamping diode and DRV pull-up diode into a single-package common-cathode diode to reduce the component count of the system. This is illustrated in Figure 24.

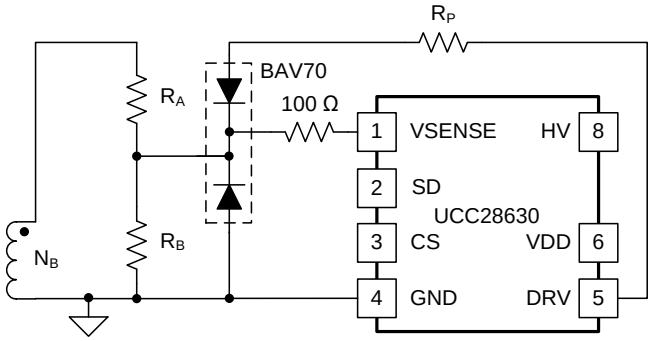

Figure 24. VSENSE Pin Protection and Interface to Bias Winding

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Feature Description (continued)

The device continually adjusts the input voltage sample delay, measuring the sample half-way through the on-time interval, to ensure the cleanest signal. The device uses same mid-point sample trigger when measuring the main MOSFET switch current (I_{SW}). Sampling MOSFET switch current in the middle of the on-time automatically measures the average current during the on-time, $I_{SW(on_avg)}$, which is required for the current limit and overload timer block.

The output voltage sample point is always time relative to the turn-off instant. Internally, the device uses the CS pin to determine the cycle end, rather than the PWM falling edge on the DRV pin. The device bases this determination on the instant that the MOSFET switch current drops below the demanded peak current level (I_{PEAK}) at the peak current mode comparator. Some delay always occurs from the falling edge on DRV to the point when the external power MOSFET turns off. This internal timing method ensures a more accurate measure of $I_{SW(on_avg)}$, and also ensures that the output voltage sample point is not measured too early, before the leakage ringing has subsided. The effect of the gate turn-off delay and the adjustment of the output voltage sample point is illustrated in Figure 25.

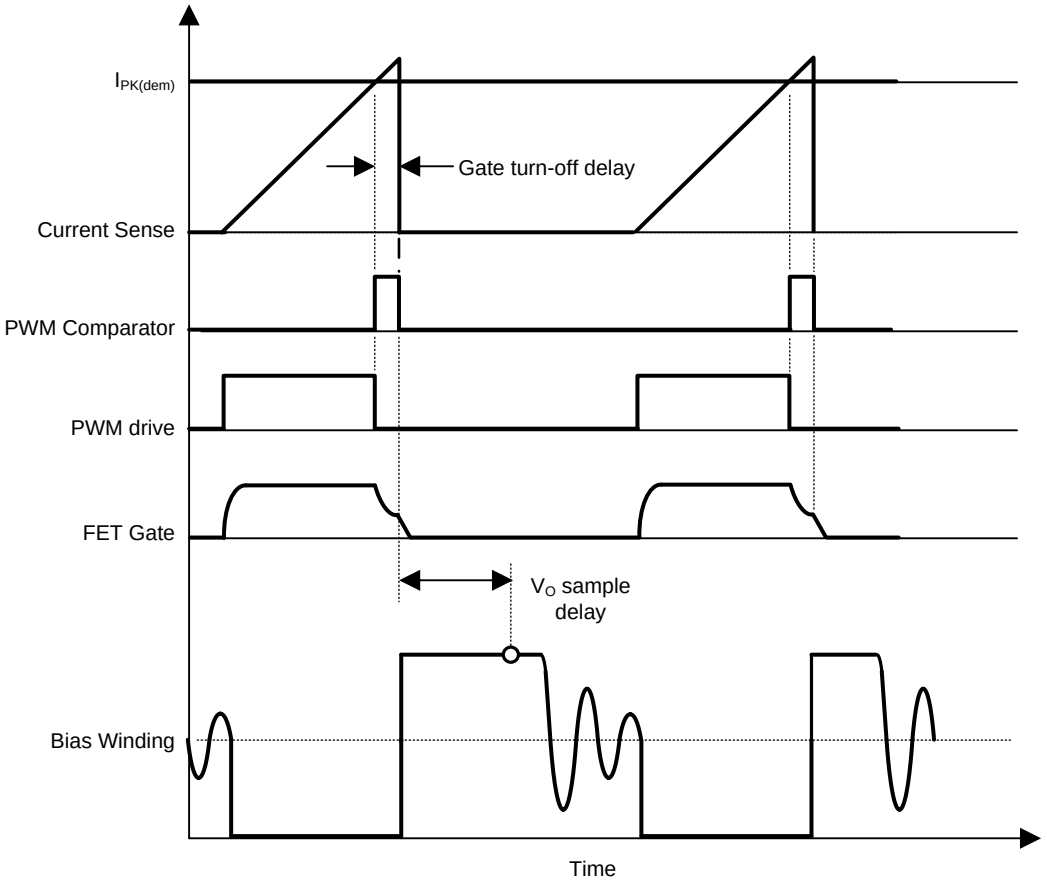

Figure 25. V_{OUT} Sample Adjust for External Gate Delay

Feature Description (continued)

The sampling of the input voltage and output voltage signals on the bias winding must be synchronized to the on-time and off-time flyback intervals respectively, because the signals occur during only those intervals in the switching cycle. Typical waveforms and timing are illustrated in Figure 26.

More conventional *knee-point* detection schemes, where the sample is measured at the end of the flyback interval when the secondary-side current has decayed to zero, inherently always operate in discontinuous conduction mode (DCM). However, the fixed sample-point scheme used on the UCC2863x has the advantages of being able to operate in regions of fixed frequency, and being able to operate in continuous conduction mode (CCM). Fixed sample-point schemes conventionally suffer poorer regulation than *knee-point* schemes, because there is always current flowing at the sample instant. This current produces a sensing error as a result of the voltage drop produced across the secondary-side resistance and leakage inductance. This parasitic voltage drop varies with output voltage, line and load, thus influencing the regulation. The UCC2863x devices uses a novel internal compensation scheme to adjust for this parasitic voltage drop, and can deliver excellent static line and load regulation, even when operating heavily in CCM.

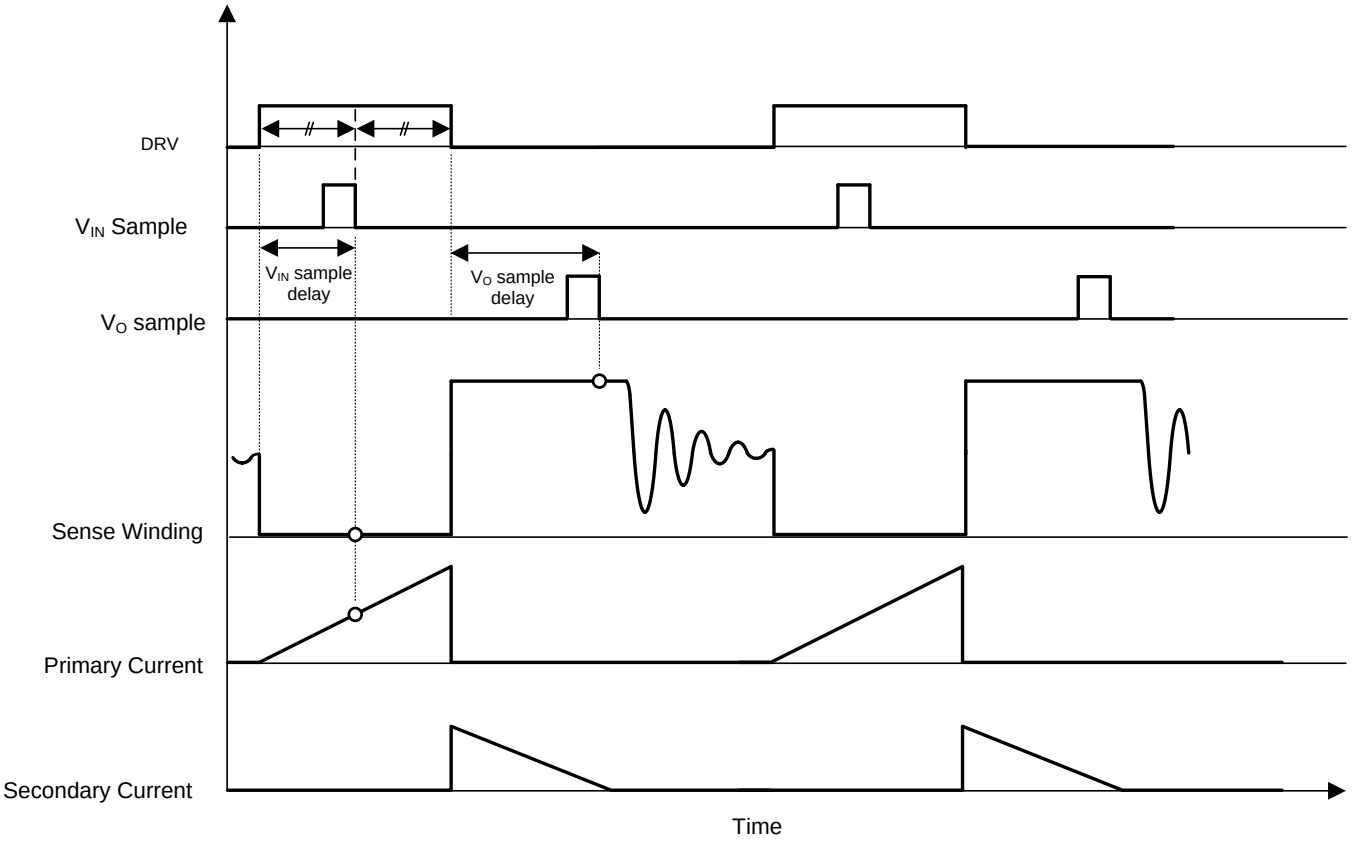

Figure 26. V_{IN} and V_{OUT} Sample Trigger Timing

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Feature Description (continued)

8.3.5 Fixed-Point Magnetic Sense Sampling Error Sources

To support operation in CCM, and allow operation at fixed frequency over a large percentage of the load range, the UCC2863x uses fixed-point sampling rather than *knee-point* detection. When conventionally used, fixed-point sampling typically suffers from poorer regulation performance. This poor performance results from the voltage drops across the secondary-side parasitic resistance R_{SEC}, and the secondary-side leakage inductance from secondary-side to bias $L_{LK(sec_bias)}$, as a consequence of the fact that current remains flowing on the secondary-side when the device measures the output voltage. As shown in Figure 27, the secondary-side pin voltage that gets reflected to the bias winding is detailed in Equation 9.

$$V_{SEC} = V_{OUT} + V_{RECT} + V_{R(sec)} - V_{L(leak)} + V_{RC(esr)} \tag{9}$$

Equation 9 can be expanded and rearranged into Equation 10.

$$V_{SEC} = V_{OUT} \times \left(1 - \frac{L_{LK(sec\ bias)}}{L_{SEC}}\right) + V_{RECT} + I_{SEC} \times \left(R_{SEC} + R_{C(esr)}\right) - \left(I_{LOAD} \times R_{C(esr)}\right) \tag{10}$$

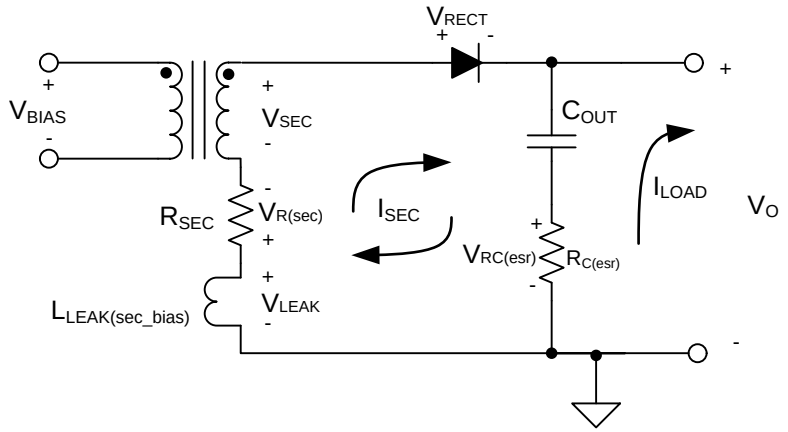

Figure 27. Secondary-Side Pin Voltage Contributors with Secondary-Side Current Flow

Feature Description (continued)

Many elements contribute errors to the sensed secondary-side pin voltage, when measured across the bias winding:

- **$V_{L(leak)}$:** Negative voltage drop across the sec-bias leakage inductance $L_{LK(sec_bias)}$; assuming constant regulated output voltage, this voltage drop is fixed constant offset, because V_{OUT}/L_{SEC} is constant as long as the output is in regulation.
- **V_{RECT}:** Positive voltage drop across the output rectifier (assuming use of a conventional diode). This voltage drop varies with load current and temperature. However, a constant nominal voltage drop can usually be used, because the increasing forward voltage drop with increasing load current is largely cancelled by the decrease in forward drop as a result of the temperature rise that results.
- **$V_{R(sec)}$:** This is the drop across the secondary-side winding resistance. This value depends on loading, and varies in proportion to the primary peak current demand that is set by the modulator.
- $V_{RC(esr)}$**:** This is the drop across the output capacitor equivalent series resistance (esr). This value depends on the difference between the secondary-side winding current and the DC load current being drawn.

Typically, the peak secondary-side winding current I_{SEC} is many times larger than the load current, and the secondary-side winding resistance is typically larger than the output capacitor esr. Thus, the last term in Equation 10 involving I_{LOAD} can typically be neglected.

The leakage inductance and secondary-side rectifier terms represent quasi-constant offset terms, so do not affect regulation to a significant extent. Thus, the quasi-constant offset terms can be accounted for in the calculation of the required scaling resistors to produce the desired setpoint voltage.

The remaining term that dominates the regulation error in Equation 10 is the drop across the secondary-side winding resistance and capacitor esr at the sample instant, $\{I_{SEC} \times (R_{SEC} + R_{C(esr)})\}$. The controller internally adjusts the control loop reference in proportion to the primary peak current demand in order to null the I_{SEC} related error term in the sampled bias winding voltage. Since the peak secondary-side current $I_{SEC(pk)}$ is the primary peak current $I_{PRI(pk)}$ scaled by the transformer turns ratio, the internal control loop reference effectively varies in approximate proportion to I_{SEC}, resulting in dramatically improved regulation performance.

This improved regulation performance allows the use of primary-side regulation in a wider range of applications, and at unprecedented power levels, operating in both CCM and DCM.

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Feature Description (continued)

8.3.6 Magnetic Sense Resistor Network Calculations

Because the device uses the VSENSE pin to measure both V_{OUT} and V_{IN} of the power stage, it is important to calculate the resistor values correctly. The step-by-step design process is outlined in this section.

8.3.6.1 Step 1

Depending on the power level, choice of transformer size, and required trade-offs between primary MOSFET and secondary-side rectifier ratings, the transformer turns N_P, N_S and N_B will be chosen first. The controller can support a wide range of turns ratios.

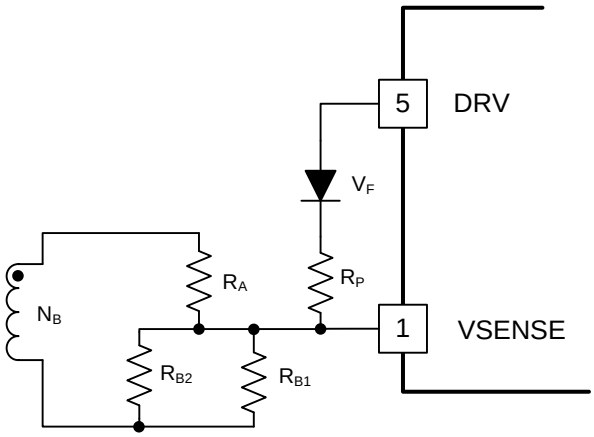

Figure 28. Practical Magnetic Sense Setup with Extra Resistor R_{B2} for Setpoint Fine Adjust

8.3.6.2 Step 2

Once N_P, and N_B are known, the required value of R_A in Figure 28 is calculated using Equation 11.

$$R_A = R_P \times \left(\frac{N_B}{N_P}\right) \times K_{LINE} \quad (11)$$

In this equation, the internal controller gain K_{LINE} is 49.25 (see Table 6 for key internal controller parameters), and the internal gains are designed for a fixed value for R_P, (i.e. R_P MUST be 3.9 kΩ).

Feature Description (continued)

8.3.6.3 Step 3

Once N_S, target V_{OUT}, output rectifier drop V_{RECT}, and the secondary-side-to-bias leakage inductance $L_{LK(sec_bias)}$ are known, the required value for R_B can be calculated. Referring to Equation 10, $L_{LK(sec_bias)}$ can be approximated as a percentage of the secondary-side-referred magnetizing inductance L_{SEC}. (See Magnetic Sense Resistor Network Selection for details).

$$R_B = \frac{R_A}{\left(\frac{\left(V_{OUT} \times \left(1 - \%L_{LK(sec_bias)}\right) + V_{RECT}\right) \times \left(\frac{N_B}{N_S}\right)}{V_{OUT(ref)}} - 1\right)} \quad (12)$$

In this case, R_B may need to be empirically adjusted to achieve the required exact output set-point, especially if V_{RECT} varies or is not known precisely. For this reason, it is recommended that R_B should be implemented on the system PCB as two parallel resistors R_{B1} and R_{B2} as shown in Figure 28, to allow easier fine-tuning of set-point. For set-point tuning, only R_B should be adjusted. R_A should never be adjusted, because to do so would affect the line sense gain and introduce errors into the line voltage measurement.

8.3.6.4 Step 4

Verify that the equivalent Thevenin resistance R_{TH} of the R_A/R_B combination falls in the required range of 10 kΩ to 20 kΩ.

$$R_{TH} = \frac{R_A \times R_B}{R_A + R_B} \quad (13)$$

$$10\ k\Omega < R_{TH} < 20\ k\Omega \quad (14)$$

If the Thevenin resistance is outside of that range, then the original choice of turns ratio must be adjusted, and design steps repeated until a valid value for R_{TH} is determined. This is unlikely to occur in practice, unless an extreme turns ratio is chosen. If R_{TH} is outside this range, it triggers the VSENSE pin open or short pin-check at start-up.

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Feature Description (continued)

8.3.7 Magnetic Sensing: Power Stage Design Constraints

Because the controller employs fixed-point sampling for output voltage sensing, there are some transformer design constraints that must be observed. The minimum magnetizing volt-seconds during the on-time interval occurs at the minimum CS pin voltage, $V_{CS(min)}$, under light-load conditions. This minimum should be the case at all line voltages, because the controller compensates for line-dependent peak-current overshoot during turn-off delay. The choice of transformer turns ratio, transformer inductance (L_{PRI}), and current sense resistance (R_{CS}) must ensure that the corresponding reset volt-seconds during the flyback interval are sufficient that a valid output sample is available at the sample point, $t_{OUT(smp)}$. This constraint is summarized in Equation 15.

$$\frac{R_{CS}}{L_{PRI}} \leq \frac{V_{CS(min)}}{t_{OUT(smp)}} \times \frac{N_S}{N_P} \times \frac{1}{(V_{OUT} + V_{RECT})} \quad (15)$$

where

- V_{RECT} is the voltage drop across the output rectifier

Additionally, the device requires a minimum on-time, $t_{ON(min)}$, to ensure enough time for the system input voltage (V_{IN}) and switch current (I_{SW}) to be measured. To meet the minimum on-time requirement at maximum line, and minimum load, the ratio of current sense resistance (R_{CS}) to transformer inductance (L_{PRI}) must meet the constraint shown in Equation 16.

$$\frac{R_{CS}}{L_{PRI}} \leq \frac{1}{V_{IN(pk_max)}} \times \frac{V_{CS(min)}}{t_{ON(min)}} \quad (16)$$

Equation 15 or Equation 16 sets the limit for the ratio of R_{CS} to L_{PRI}, but both need to be verified. See Typical Application for more details.

Feature Description (continued)

8.3.8 Magnetic Sense Voltage Control Loop

Because the output voltage feedback is inherently a sampled signal obtained from the bias winding, the internal voltage control loop is most naturally implemented digitally. The internal control loop implements the equivalent of a PID loop in digital form. Because the output can be sampled only at certain intervals in each switching cycle, the sample rate is naturally tied to the switching frequency, and the sample rate increases with increasing frequency. However, the device clamps the sample rate at a normalized maximum rate, $f_{SMP(max)}$. But because the device must always synchronize to the next available switching cycle to obtain a new sample of the output voltage, the effective sample rate varies somewhat around this value.

The digital control loop compensator block diagram is shown in Figure 29. A new sample of output voltage is supplied to the compensator at the normalized maximum clock rate ($f_{SMP(max)}$) , or f_{SW}, whichever is lower. An updated output voltage demand signal, y_k, is produced at the same clock rate. This voltage loop demand represents the required operating point on the modulator curves to keep the output voltage in regulation. The modulator sets the appropriate switching frequency and peak current demand depending on the load power.

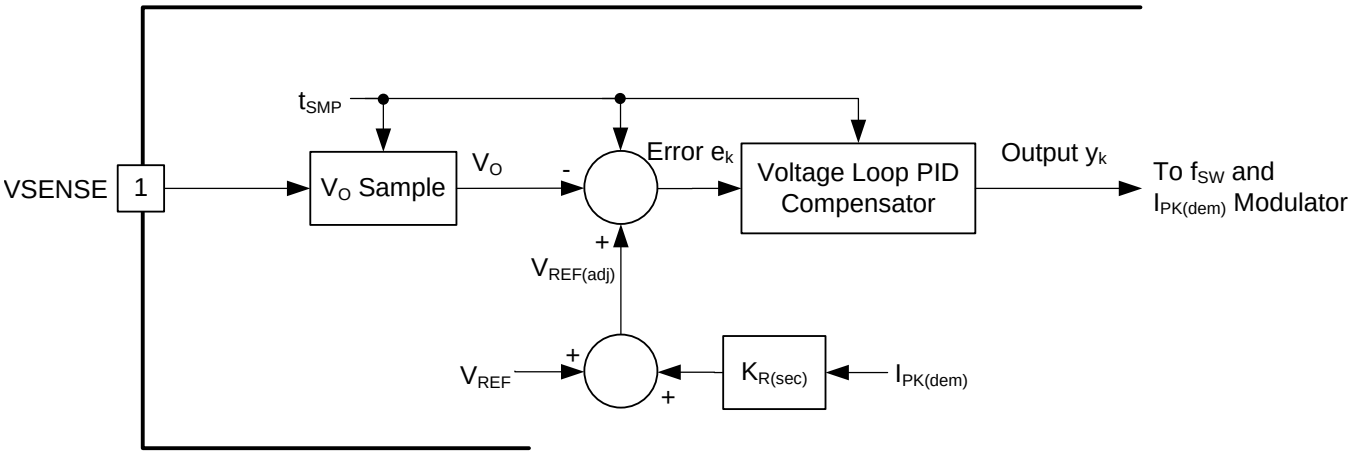

Figure 29. Digital Voltage Control Loop Simplified Block Diagram

The control loop PID gain factors are internally fixed values, optimized for flyback power stages in the range between 20 W and 130 W. The loop is designed to work with magnetizing inductance values in the range between 200 µH and 1500 µH. Assuming that the output capacitance value is chosen based on required ripple current rating, then loop stability is not a problem. Adding extra output capacitance does not degrade the loop performance and the resulting extra output hold-up improves transient response.

The Typical Application section includes gain-phase measurements taken using the 65-W UCC28630EVM-572 evaluation module.

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Feature Description (continued)

8.3.9 Peak Current Mode Control

The controller operates in peak current mode. The primary-side switch (MOSFET) current is sensed by a shunt resistor (R_{CS1}) connected in series with the source of the FET as shown in Figure 30. The voltage that is developed across the sense resistor is connected to the CS pin of the controller. The device uses the current sense signal at the CS pin to terminate the PWM pulse according to the peak current demand of the modulator. The device automatically applies slope compensation as soon as the duty cycle of the DRV pin pulse exceeds 50%. This compensation provides stable operation up to maximum DRV duty cycle. The device applies this slope compensation as a downslope on the demand signal at the PWM comparator, so is not measureable at the CS pin. The device synchronizes the slope compensation signal to the PWM and is active only between 50% and 70% duty cycle, as shown in Figure 31.

Normal operating range for the CS pin is between 0 mV and 800 mV. The R_{CS1} resistor should be scaled such that the peak current at maximum peak load and minimum bulk capacitor voltage produces a signal of approximately 800 mV peak at the CS pin. This resistor value is calculated in conjunction with the calculation of the required primary magnetizing inductance, as outlined in Notebook Adapter, 19.5 V, 65 W, section.

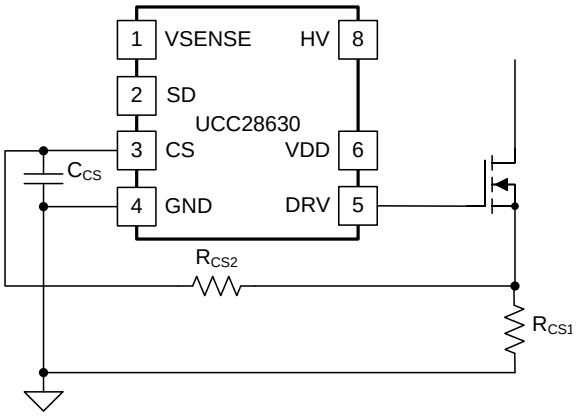

Figure 30. Primary-Side Current Sensing

Feature Description (continued)

A nominal 100 ns of filtering that is internal to the CS pin helps filter the leading turn-on spike of current. Depending on PCB layout, an RC filter (R_{CS2} and C_{CS}) may be required on the CS pin as shown in Figure 30 to filter noise and spikes. The capacitor C_{CS} should be positioned as close as possible to pins 3 and 4 and tracked directly to the pins. Series resistor R_{CS2} should also be located close to pin 3 to minimize noise pick-up. R_{CS2} value should not exceed 20 kΩ, because a larger value could be detected as a possible open circuit on the CS pin during the start-up pin-fault checks. The R-C filter time constant should not be excessive (timing between 100 ns and 200 ns is typical). Otherwise the filter reduces the measured peak current, and allows greater actual peak current to flow versus the modulator demand level. Such effects force the regulation loop to reduce the switching frequency to compensate, and at highest line, no load, this can lead to regulation difficulties if the control loop attempts to drop the frequency so far that it reaches the f_{MIN} limit.

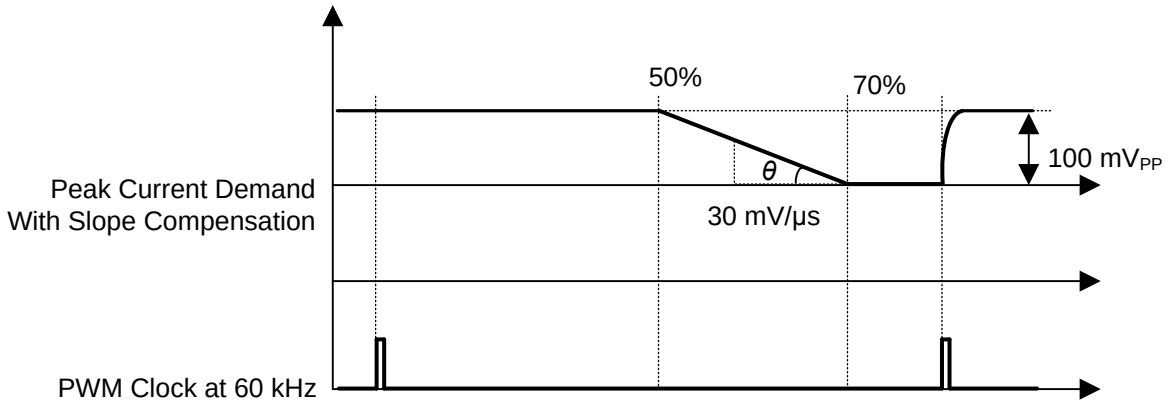

Figure 31. Peak Current Demand with Slope Compensating Downslope

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Feature Description (continued)

8.3.10 I_{PEAK} Adjust vs. Line

The controller applies a line-dependent reduction in the peak-current demand to correct for the current overshoot due to the PWM and gate drive propagation delay, with the aim of delivering a constant peak current versus line at a given power level. This maintains approximately constant switching frequency versus line for a given power level (until the operation enters into CCM), improves regulation, reduces audio noise, and allows lower standby power at high line. If not corrected, the current overshoot could become significant at high line, where the inductor current di/dt is higher. This overshoot would cause a pronounced increase in transferred power per switching cycle at high line, because power is proportional to I_{PK}^2. The effect of the delay on the peak-current overshoot is illustrated in Figure 32.

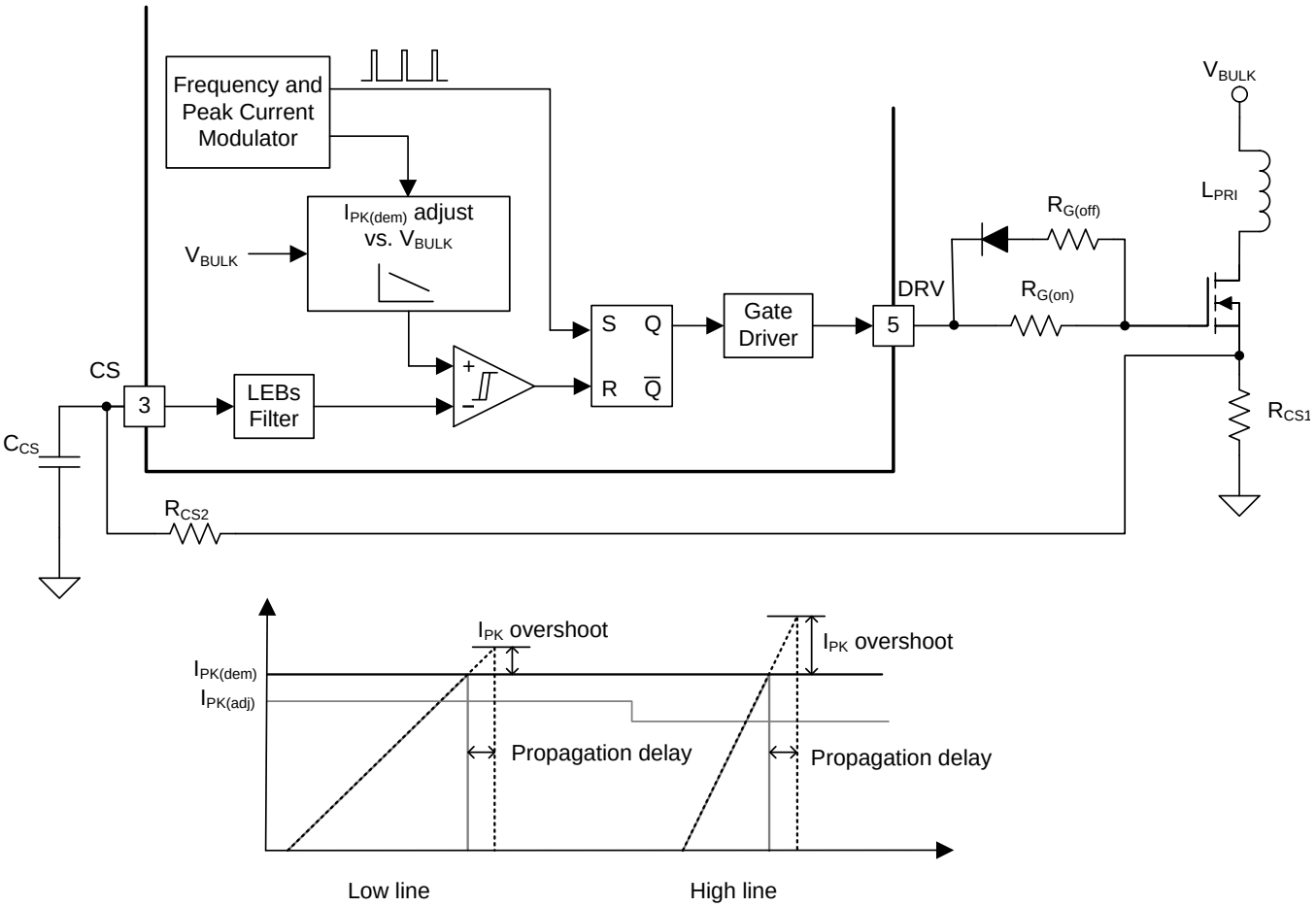

Figure 32. Peak-Current Demand Adjustment vs V_{BULK} to Correct Prop Delay Overshoot

For different power stage designs, the combination of primary magnetizing inductance L_{PRI}, current sense resistance R_{CS} and external MOSFET gate turn-off delay $t_{OFF(ext)}$, must be verified against Equation 17, to ensure that the internal peak-current compensation gain range is satisfied. The $K_{LINE(adj)}$ factor should be within the range indicated. If the external turn-off delay is too long, then the internal I_{PEAK} adjustment factor is too low, and the adjustment at high line is not able to achieve the required level of over-shoot compensation. As noted previously, this could result in regulation difficulties at no-load, and may cause poor line and load regulation, or require an increase in output pre-load power.

$$K_{LINE(adj)} = \left(\frac{R_{CS}}{L_{PRI}} \times \left(t_{PROP(gate)} + t_{OFF(ext)}\right)\right) > 120\ \mu \text{ and} < 350\mu \quad (17)$$

where

- where $t_{PROP(gate)}$ is the internal controller gate-drive turn-off propagation delay, given in Table 6.

Feature Description (continued)

8.3.11 Primary-Side Constant-Current Limit (CC Mode)

In addition to the peak-current mode PWM function, the device also uses sensed current at the CS pin to estimate the secondary-side load current. The device samples the CS pin voltage and measures it in the middle of the on-time, which is effectively the average switch current during the on time, $I_{SW(avg_on)}$. This measurement scheme is the case during both DCM and CCM operational modes. The average switch current during the on time is scaled by the PWM duty cycle to give the $I_{IN(avg)}$ of the power stage. The power stage input power, P_{IN}, can then be estimated as the product of (V_{IN} x $I_{IN(avg)}$). The CC mode operation regulates P_{IN} to track ($I_{OUT(lim)}$ x V_{OUT}), if P_{IN} increases to reach $P_{IN(lim)}$, thereby achieving a regulated constant current as shown in Equation 18.

$$P_{IN} = V_{IN} \times I_{IN(avg)} = \frac{V_{OUT} \times I_{OUT(lim)}}{\eta} = P_{IN(lim)} \tag{18}$$

$$I_{OUT} = \frac{V_{IN} \times I_{IN(avg)} \times \eta}{V_{OUT}} = \frac{P_{IN(lim)} \times \eta}{V_{OUT}} = I_{OUT(lim)} \tag{19}$$

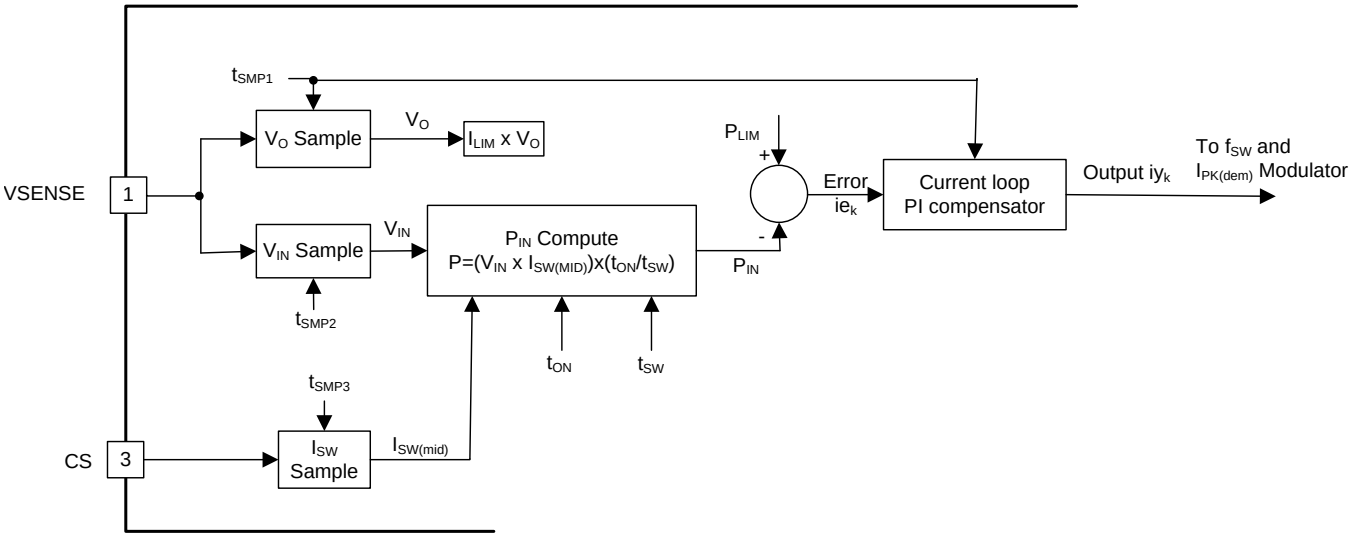

Figure 33. Digital Current Control Loop Simplified Block Diagram

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Feature Description (continued)

Assuming that the power stage efficiency does not change significantly with operating point, by regulating the input power in inverse proportion to output voltage, this regulates output current. This achieves a *brick-wall* CC characteristic, where the output current is regulated as the input voltage changes and as the output voltage rolls off, regardless of power stage operating mode (CCM or DCM). The CC mode protection eliminates the characteristic load current *tail-out* that is typically seen with peak-current mode control as output voltage collapses and operation goes deeper into CCM mode.

NOTE

As the output voltage decreases in CC mode, the VDD level also decreases. If the overload is severe, the drop in output voltage causes VDD to drop below the $V_{DD(stop)}$ UV level. This drop causes a shutdown for $t_{RESET(long)}$, as given in Table 6, followed by a restart attempt.

The constant-current mode output current limit level ($I_{OUT(lim)}$) is a function of both the R_{CS1} resistor and the transformer turns ratio. The device uses an internal reference and gain for the CC loop, K_{CC1} and K_{CC2}, that set the CC $I_{OUT(lim)}$ point as a function of the chosen turns ratio, output voltage and current sense resistance as shown in Equation 20.

$$I_{OUT(lim)} = \frac{1}{R_{CS1}} \times \frac{N_P}{N_S} \times \frac{K_{CC1}}{K_{CC2} + V_{OUT} \times \frac{N_P}{N_S}} \quad (20)$$

For the UCC28631, UCC28632 and the UCC28633 devices, the $I_{OUT(lim)}$ can be adjusted to be a percentage of the maximum value calculated by equation Equation 20. see CC-Mode $I_{OUT(lim)}$ Adjustment for more details.

Feature Description (continued)

8.3.12 Primary-Side Overload Timer (UCC28630 only)

The internal overload timer in the UCC28630 uses the same output load current measurement that is used by the CC loop. This measurement tracks the power stage thermal stress, and protects the power stage against output overload. If the output is overloaded for too long such that the power stage would be over-stressed, then the PWM shuts down, and enters low-power mode for a time period of $t_{RESET(long)}$; thereafter the device discharges VDD to the $V_{DD(reset)}$ level and initiates a hiccup mode restart.

The overload timer operates by taking an estimate of output current, squaring it (assuming the power stage losses are dominated by resistive I^2 losses) to produce ($K \times I^2_{OUT}$), where K is a scaling gain factor. The overload timer is constantly running at every load level, and accumulates at a rate dependent on the difference between ($K \times I^2_{OUT}$) and the previous level of the timer. If ($K \times I^2_{OUT}$) is greater than the previous timer level, the timer level continues to increase; if ($K \times I^2_{OUT}$) is less than the previous timer level, then the timer level decreases. At any steady load, the overload timer level eventually settles at a level proportional to I^2_{OUT}. Because the overload timer level adjusts at a rate dependent on the difference between ($K \times I^2_{OUT}$) and the previous level, the timer initially reacts faster to larger differences, but over time settles exponentially at a level proportional to ($K \times I^2_{OUT}$).

As shown in Figure 34, in both the first and second examples, the initial steady load allows the timer to integrate and settle at a level proportional to the load. The margin to the over-load trip level depends on the historical loading, lower prior average loading results in greater future over-load capability, and vice versa. The rate at which the timer reacts to different load steps is set by the chosen time constant (or response rate) per Table 1.

The overload timer can cope with pulsed loads and loads with a complex waveform. Because the rate of increase and decrease also depends on the load change from the previous load, it also times out faster for bigger overloads, or allows a smaller overload to run for much longer. The overload timer operates in both normal CV mode and overload CC mode, or a dynamic mix of both modes.

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Feature Description (continued)

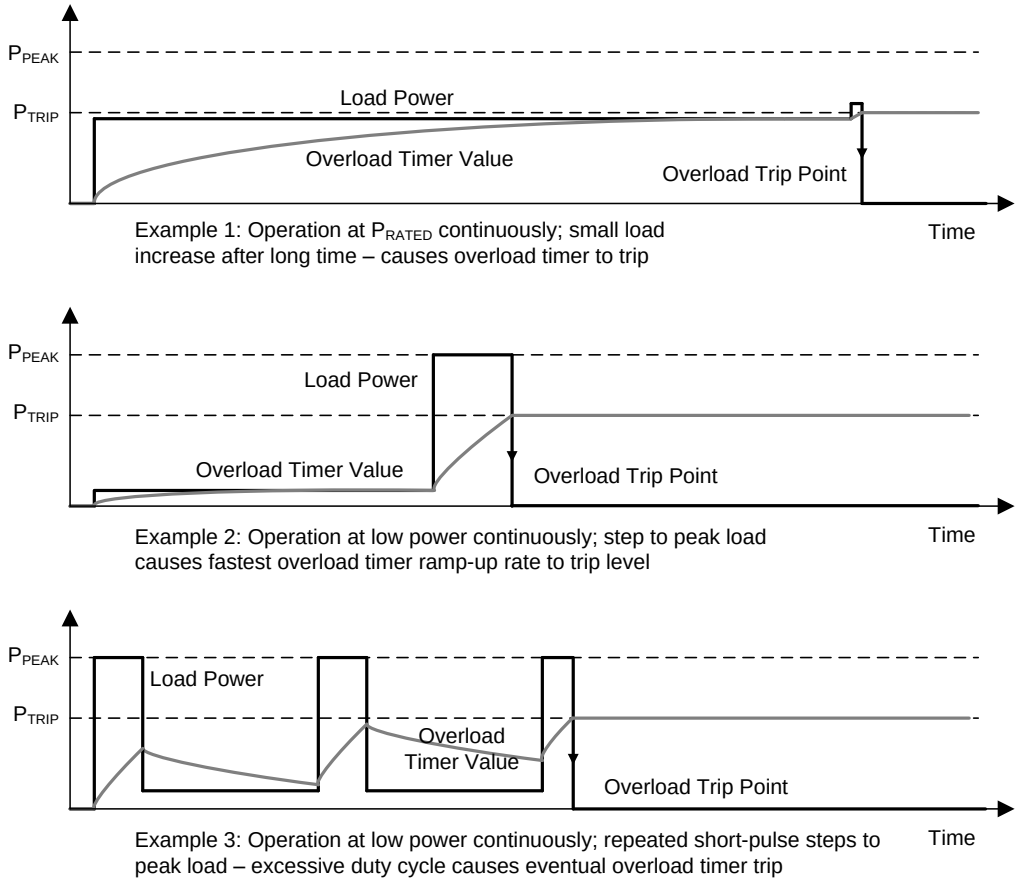

Figure 34. Overload Timer Example Waveforms Under Various Load Scenarios

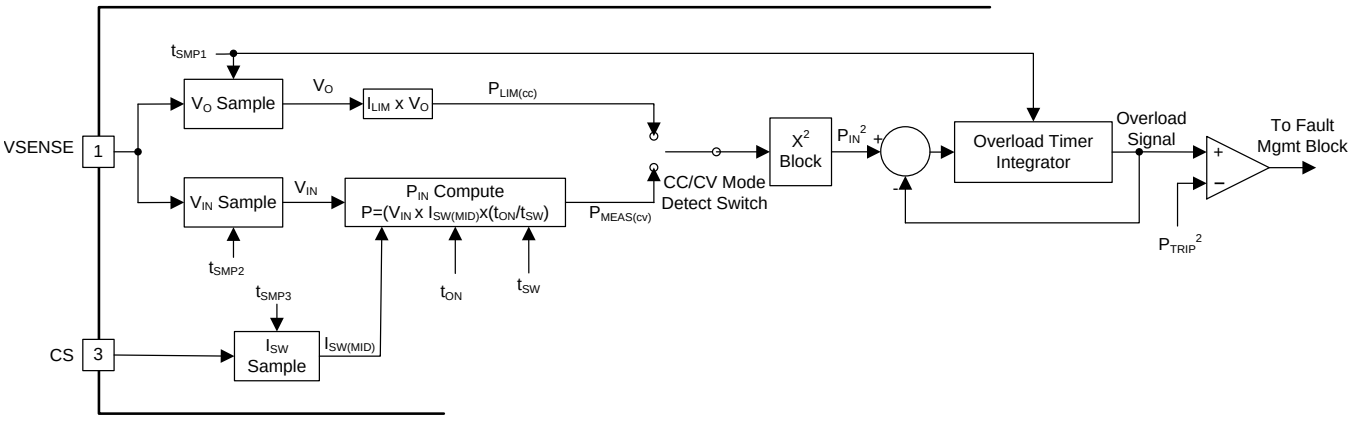

Figure 35. Overload Timer Block Diagram

Feature Description (continued)

8.3.13 Overload Timer Adjustment (UCC28630 only)

The UCC28630 overload timer trip level and time constant are both selectable from a defined list of combinations. The user can select the overload timer trip level as a percentage of the rated continuous nominal power, P_{NOM} (see Figure 41), and the timer response speed. The available choices are detailed in Table 1.

Table 1. Overload Timer Adjustment

R_{PROG} PROGRAMMING RESISTOR (kΩ) (E96 series values)	TIMER CONTINUOUS OPERATION P_{TRIP}/P_{NOM} (%)	TIME CONSTANT AT 200% of P_{NOM} OR IN CC MODE (ms)
Open, or > 47	160	1000
20.0	160	500
12.7	160	150
9.31	135	1000
7.32	135	500
6.04	135	150
5.11	110	1000
4.42	110	500
3.92	110	150

The desired pull-down resistance on the DRV pin sets the required overload parameters, as shown in Figure 36. The controller measures the resistance value on the DRV pin at start-up using a low-level test voltage (400 mV to ensure it is well below the lowest possible power MOSFET gate threshold voltage) and sensing the current that flows. Thus, based on the resistance R_{PROG}, the required set of timer parameters can be chosen.

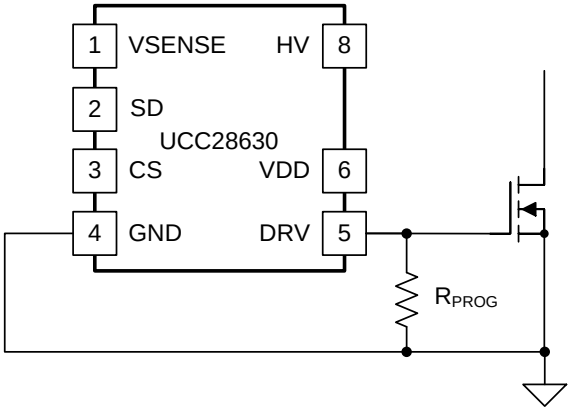

Figure 36. Overload Timer Setting Adjustment (with programming pull-down resistor on DRV pin)

To ensure that the sensed current does not sit close to an interval boundary, the resistor values listed in Table 1 (or the closest value possible) should be used. These recommended resistor values position the test current in the center of each interval.

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8.3.14 CC-Mode $I_{OUT(lim)}$ Adjustment

For the UCC28631, UCC28632, UCC28633 and UCC28634, the pull-down programming resistor on the DRV pin, as shown in Figure 36, sets the desired CC-Mode limit. The available CC-Mode levels are listed in Table 2, where the CC limit is given as a percentage of the maximum allowed value from Equation 20.

Table 2. CC-Mode Levels

R_{PROG} (kΩ)	CC LIMIT
Open or > 47	100%
20	90%
12.7	80%
9.31	75%
7.32	70%
6.04	65%
5.11	60%
4.43	55%
3.92	50%

8.3.15 Fault Protections

The controller has several built-in fault protections. Most faults are subject to internal persistence filtering to avoid false-tripping due to noise or spurious glitches from external events. When a fault is detected and persists for the corresponding filter delay time, the device terminates and disables the PWM drive signal. No PWM activity occurs if the fault (pin faults for example) is detected at start-up . Table 3 lists all fault sources, persistence delays and the associated response (latching or auto-restart).

In the case of auto-restart (sometimes called hiccup-mode) faults, the device enters low-power mode for a time period of $t_{RESET(long)}$ (or $t_{RESET(short)}$ in the case of AC line UV fault and X-capacitor discharge), then discharges the VDD pin to the $V_{DD(reset)}$ level, followed by a restart attempt. The device continues in a repeating shutdown-delay-restart loop until the fault is removed. Once the fault clears, the controller restarts automatically, there is no need to remove and re-apply AC input voltage to the system.

Latching faults do not allow any PWM restart attempts until the AC input voltage is removed. In this case the controller enters low-power mode. During low-power mode, the device regulates the VDD pin between two levels $V_{DD(latch_hi)}$ and $V_{DD(latch_lo)}$, as given in Table 6, using the start-up HV current source. This regulation keeps the controller biased to maintain the latched fault condition as long as AC voltage is present at the input. When the device loses AC input voltage during latched-fault mode, the controller resets, and restarts when the AC input is re-applied.

If there is an open-feedback fault due to an open or short on the VSENSE pin or associated external resistor divider on the aux winding, the output voltage is protected against an over-voltage condition. If the open-feedback fault occurs before power-up, the fault will be detected by VSENSE pin- fault protection (see next section 9.3.16), and the controller will not generate any PWM drive signal. This prevents any possible output OV due to this open-feedback fault condition. If the open-feedback occurs after power-up, when the power stage is already operating, the open-feedback condition can cause Vout to increase. In this case, the VDD level will also increase in proportion to Vout (they will track based on the Flyback transformer turns ratio). When the VDD rail reaches the $V_{DD(ovp)}$ protection threshold, the PWM will be disabled, and the controller will go to fault mode, as described above. The $V_{DD(ovp)}$ protection is used as an indirect back-up OV protection mechanism for the main output under running open-feedback fault conditions. The level of output OV depends on the ratio of the normal VDD regulation level to the $V_{DD(ovp)}$ level. Note that UCC28630/1/2/3 use $V_{DD(ovp)}$ trip level of 17.5 V nominal, whereas the UCC28634 uses a lower $V_{DD(ovp)}$ of 14.85 V nominal, to ensure a lower/tighter level of output OV under VSENSE open-feedback conditions. As a result, the user must be careful to choose the number of turns in the transformer aux winding to ensure that the normal VDD regulation is below the $V_{DD(ovp)}$ protection level, to avoid false-triggering of the $V_{DD(ovp)}$ protection.

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Table 3. Fault Sources and Associated Responses

FAULT TYPE	TYPICAL CAUSE	FILTER DELAY TIME	RESPONSE		
			UCC28630	UCC28631, UCC28632, UCC28633	UCC28634
VDD OV	Excessive transformer leakage; system board fault	125 µs (1)	Latching	Auto-restart	Auto-restart
VDD UV	Insufficient VDD capacitor; system board fault	125 µs (1)	Auto-restart	Auto-restart	Auto-restart
AC brownout	AC voltage removal or extended dip	40 ms	Auto-restart	Auto-restart	Auto-restart
OverTemp	Internal $T_{J(max)}$ reached	125 µs (1)	Latching	Auto-restart	Auto-restart
SD pin low	External NTC over-temperature event	125 µs (1)	Latching	Auto-restart	Auto-restart
Overload timer	Excessive load power for too long	Programmable (2)	Auto-restart	N/A	N/A
Output OV	System board fault; system output voltage back-driven excessively	125 µs (1)	Latching	Auto-restart	Auto-restart
VSENSE pin	Short or open detected at start-up	No filter (3)	Latching	Latching	Auto-restart
DRV pin	Short detected at start-up	No filter (3)	Latching	Latching	Auto-restart
CS pin	Short or open detected at start-up	No filter (3)	Latching	Latching	Auto-restart
Internal fault	Internal chip diagnostics fault detected	No filter (3)	Latching	Latching	Auto-restart

(1) The filter delay time is either 125 µs or 2 PWM periods, whichever is longer.
(2) The overload timer delay can be programmed as shown in Table 1.
(3) Because these faults are only identified before PWM commences, noise filtering is not required.

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8.3.16 Pin-Fault Detection and Protection

The controller includes protection against most practical pin faults. These faults include open pins, pins shorted to adjacent pins, pins shorted to GND and pins shorted to VDD. The device performs pin fault checking at start-up, before the PWM is enabled. Table 4 summarizes the response to pin faults. Most faults cause either a latched shut-down, or failure to start-up. For UCC28634, all pin-faults are non-latching.

A short-circuit from the HV pin (pin 8) to the VDD pin (pin 6) is unlikely to occur, because pin 7 is not included in the package. The HV pin and tracking requires additional PCB spacing in any event to meet creepage requirements. However, if such a fault does occur, the device continues to charge the VDD capacitor through the HV pin external series resistor, and the power supply starts up and appears to operate normally. But because the HV and VDD pins are shorted, the internal HV current source cannot switch-out the external HV resistor, so it always dissipates power. This condition results in a large increase in no-load standby power. A 200-kΩ external HV resistor, dissipates 66 mW at 115 V_{AC}, and 265 mW at 230 V_{AC}. At load levels where the X-capacitor discharge function is operational, the short to VDD appears to be an AC-disconnect event, and causes the device to cycle on and off.

Table 4. Pin Faults and Associated Responses

PINS		OPEN	ADJACENT SHORT	GND SHORT	VDD SHORT
NAME	NO.				
VSENSE	1	Latched fault	Latched fault	Latched fault	No start-up
SD	2	Normal operation	Latched fault	Latched fault	Latched fault
CS	3	Latched fault	Latched fault	Latched fault	No start-up
GND	4	Device fails, power supply damaged	Latched fault	N/A	No start-up
DRV	5	Hiccup fault	No start-up	Latched fault	No start-up
VDD	6	No start-up	No start-up	No start-up	N/A
no pin	7	N/A	N/A	N/A	N/A
HV	8	No start-up	N/A	No start-up	Fault not detected/Hiccup fault

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8.3.17 Over-Temperature Protection

The controller has built-in thermal protection. If the controller junction enters an over-temperature condition, the controller shuts down. The fault response (latching or auto recovery) depends on the device variant, per Table 3. There is 10°C hysteresis in the over-temperature trip point, the controller only restarts if the junction temperature has dropped by at least 10°C below the trip level.

8.3.18 External Fault Input

An external fault input signal may be applied to the controller SD (shutdown) pin. This signal forces the controller into fault mode. To trigger the fault, the voltage on this pin should be pulled below the fault trip threshold. A typical application is shown in Figure 37, where this pin is used to shut down the controller in the event of an over-temperature event as detected by a NTC (negative temperature coefficient) thermistor. The device pulls up the SD pin internally using a current source. As temperature rises, the external NTC resistance decreases, reducing the voltage on the pin. When the pin voltage drops to the fault trip threshold, the controller enters fault mode. The fault response (latching or recovery) depends on the device variant, per Table 3.

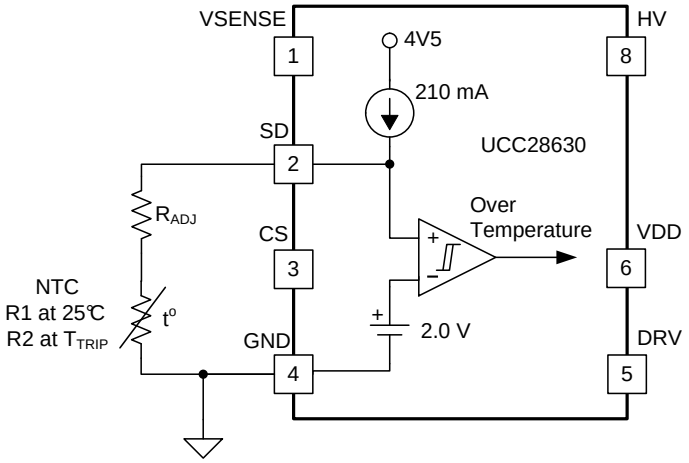

Figure 37. Fault Interface to SD Pin

The required trip resistance can be calculated from the internal trip voltage and pull-up current source. Nominally, this is 9.5 kΩ. Choose the NTC should so that it can achieve this value of resistance at the desired hot-spot trip temperature. If the NTC resistance is too low at the required trip temperature, connect a standard chip resistor in series to bring the total resistance up to 9.5 kΩ.

The device internally filters the SD pin with persistence delay as listed in Table 3. An external filter capacitor is not normally necessary. However, if an application uses an external filter capacitor, the value should be limited to 1 nF maximum. A larger value may impact the useful life of the controller.

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8.3.19 External SD Pin Wake Input (except UCC28633)

During low-power modes (when $f_{SW} < f_{SMP(max)}$), the device disables the internal pull-up on the SD pin. This action allows the pin voltage to fall to GND, and the SD pin then functions as a transient wake-up input. In this case, if the pin rises above the wake threshold while the device is in low-power sleep mode, the device wakes and starts PWM pulses immediately. This feature is useful for applications that require a faster response to load transients from zero or near-zero load, where a wake-up signal can be appropriately coupled to the SD pin from the secondary side.

Figure 38 describes a typical secondary-side wake circuit and coupling of the wake signal to the controller on the primary side. This circuit uses a TL103W component which is an integrated reference plus two op-amps in a convenient SOIC-8 package. Both op-amps are connected to the same internal 2.5-V TL431 type reference, with a 3-resistor divider chain allowing each op-amp to monitor a different level. The upper op-amp output is low as long as the device is regulating the output voltage normally. If a sufficiently large load transient occurs while the primary-side controller is in sleep mode, the output voltage drops below a transient wake level. The upper op-amp output goes high, driving current through the low-cost wake signal opto-coupler. On the primary side, the wake opto-coupler pulls up the SD pin above the wake threshold and forces PWM switching as a reaction to the load transient.

The lower op-amp section monitors the output voltage and its output goes low only when the output voltage is above a minimum enable threshold for the secondary-side wake-up monitor. This action is necessary so that under certain conditions, such as a start-up sequence or short-circuit condition (when the output voltage is already below the transient wake level) that the secondary-side circuit does not continually drive the wake opto-coupler, which could activate an SD pin fault during pin-fault checking at start-up.

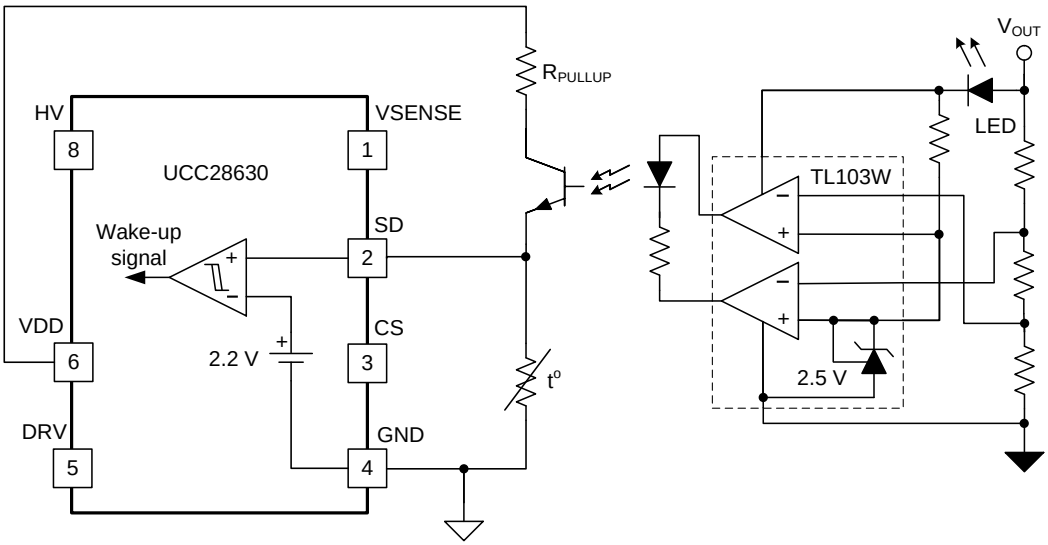

Figure 38. Typical Secondary-Side Voltage Monitor and Wake-Up Circuit for Interfacing to the SD Pin

8.3.20 External Wake Input at VSENSE Pin (UCC28633 Only)

The UCC28633 device variant supports fast PSR transient response via the VSENSE pin. When the loop demand drives the modulator frequency below approximately $f_{SMP(max)}$, the controller enters a low-power sleep mode for a portion of the switching cycle. The sleep interval varies, depending on the switching frequency commanded. The sleep interval is longer for lower switching frequency, and longest at $f_{SW(min)}$. For conventional PSR controllers, if a load transient occurs during this sleep interval, the controller will not react until the next timed wake-up, during which the output voltage can drop significantly, depending on the size of the load step and the amount of output capacitance.

The UCC28633 can respond to fast transient *wake* signal coupled to the VSENSE pin. If the wake signal exceeds an internal pin threshold $V_{SENSE(wake)}$ while the controller is in sleep mode, the sleep interval is terminated and PWM activity commences within a typical delay time of t_{WAKE}. This dramatically improves the response to heavy load transients from zero load, or very light load. If the switching frequency is above $f_{SMP(max)}$, the controller never enters sleep mode, so wake response on the VSENSE pin never enabled. The commencement of any sleep interval in the controller is delayed until the resonant ringing on the VENSE pin has decreased below the $V_{SENSE(wake)}$ threshold for at least 2 µs. Once the ringing has decreased, the wake response is enabled, and the sleep interval commences.

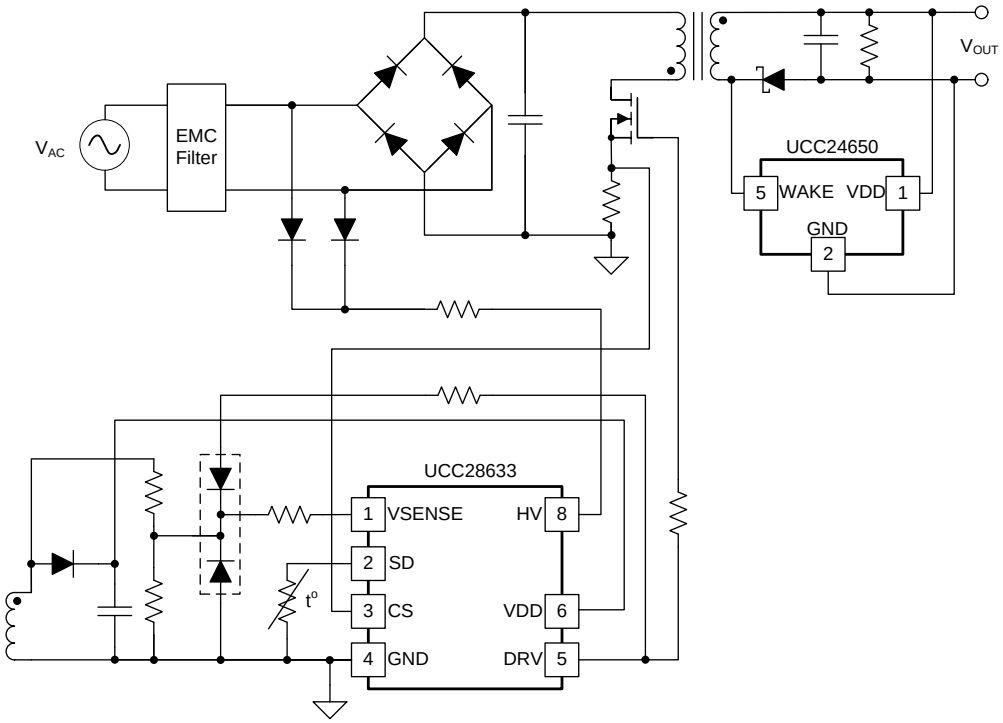

Figure 39. UCC24650 Secondary-Side Voltage Monitor and Wake-Up Circuit

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The wake signal at the VSENSE pin can be generated using a secondary side low power voltage monitor such as UCC24650, as shown in Figure 39. Further details can be found in the datasheet for UCC24650. This secondary-side monitor uses the switching activity on the secondary winding to trigger refresh of an internal sample-and-hold circuit to measure and record the system output voltage at the VDD pin. Thereafter, if the actual output voltage, sensed at the VDD pin, drops by ΔWAKE% (see UCC24650 detailed datasheet specifications) of the previously sampled value, the WAKE pin is internally pulled low through a current-limited open-drain switch. As shown in Figure 39, the main output rectifier diode is positioned at the return side of the secondary winding, so that the GND-referenced UCC24650 WAKE function can be deployed. In effect, the WAKE pin shorts out the rectifier diode for a short interval (see UCC24650 detailed datasheet specifications), to draw some current from the output capacitor through the transformer secondary winding. This sets up a low-level pulse of current that then rings resonantly in the power circuit magnetizing inductance and parasitic capacitance. The ringing causes a similar ringing voltage waveform on all transformer windings, including the bias/sense winding, which interfaces to the VSENSE pin. If the initial pulse of current drawn by the secondary WAKE pin is sufficient, then the ringing voltage at the VSENSE pin is large enough to exceed the $V_{SENSE(wake)}$ threshold.

The UCC24650 datasheet Application Information section includes details of how to estimate the amplitude of the wake-pulse ringing at the WAKE pin. In some cases, especially at higher rated output power, the transformer magnetizing inductance is lower, while the total switch node capacitance tends to be higher. This reduces the transformer impedance, and can also result in reduced wake pulse amplitude. In these cases, the UCC24650 WAKE pin output can be augmented with an external PNP circuit Q1, R1 and R2, as shown in Figure 40. In this case, when the WAKE pin pulls low, Q1 turns on, and draws more current through the secondary winding. A current limiting resistor R1 is recommended in series with either collector or emitter. Effectively R1 swamps the UCC24650 internal WAKE pin resistance, R_{WAKE}. A pull-up resistor R2 from base to emitter is also required, to ensure that the WAKE pin is adequately pulled up/down during normal switching activity to properly trigger the internal sample and hold on the VDD pin. The external PNP device Q1 must have at least the same voltage rating as the main rectifier diode.

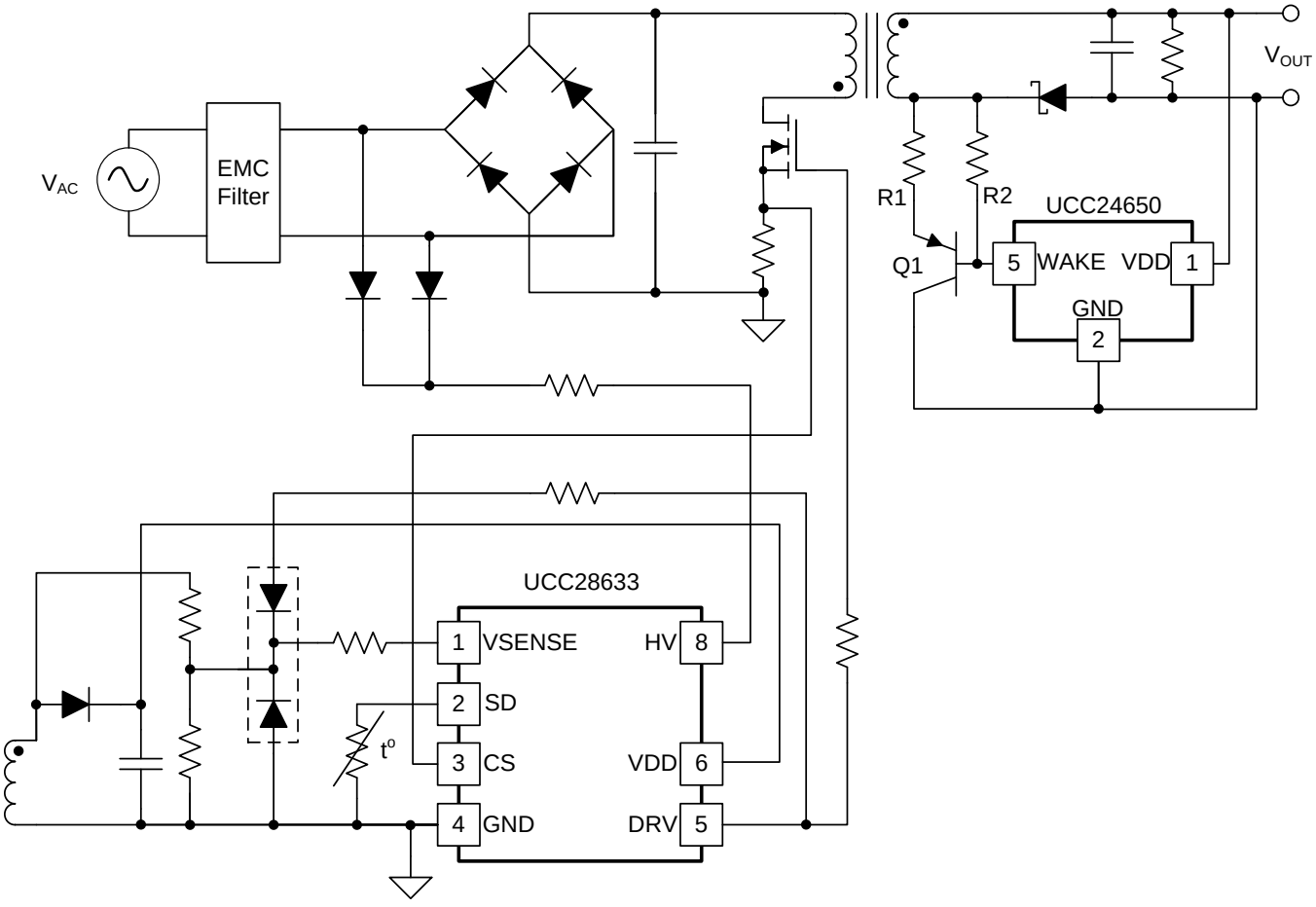

Figure 40. Augmented UCC24650 Secondary-Side Voltage Monitor and Wake-Up Circuit

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8.3.21 Mode Control and Switching Frequency Modulation

The flyback controller supports applications that require a wide range of operating power levels. This range can include effectively zero output power in standby conditions, up to a maximum rated continuous power, and then beyond this, to a mode of peak operating power for a limited time. The modulator operates in multiple modes to support these power requirements in an efficient way. In some regions, the modulator operates in AM mode at fixed frequency, where the device adjusts the amplitude of the peak current to regulate the output. In other regions, the modulator operates in FM mode at fixed peak current, where the device adjusts the switching frequency to regulate the output. By adjusting only peak current or frequency, (depending on operating region) the control loop smoothly regulates the power flow of the power stage. The shape of the modulator gain curve helps counteract the increasing power stage gain as load is decreased.

In the high-power region of the modulator, the device adjusts both peak current and frequency together, to allow higher power delivery with a modest increase in peak current. In this high-power region, the power stage typically transitions into continuous-conduction mode (CCM), particularly at low line. The combination of up to 2× frequency increase and 1.25× peak current increase in CCM allows up to 2× peak power delivery capability for a given transformer size. Figure 41 provides details regarding the modulator peak current (in mV at the CS pin) and switching frequency variation vs power demand level. The frequency adjusts from a minimum of 200 Hz up to a maximum of 120 kHz. The peak-current sense voltage at the CS pin varies from 172 mV to 800 mV. Table 5 summarizes the modulator breakpoints and corresponding percentage power levels.

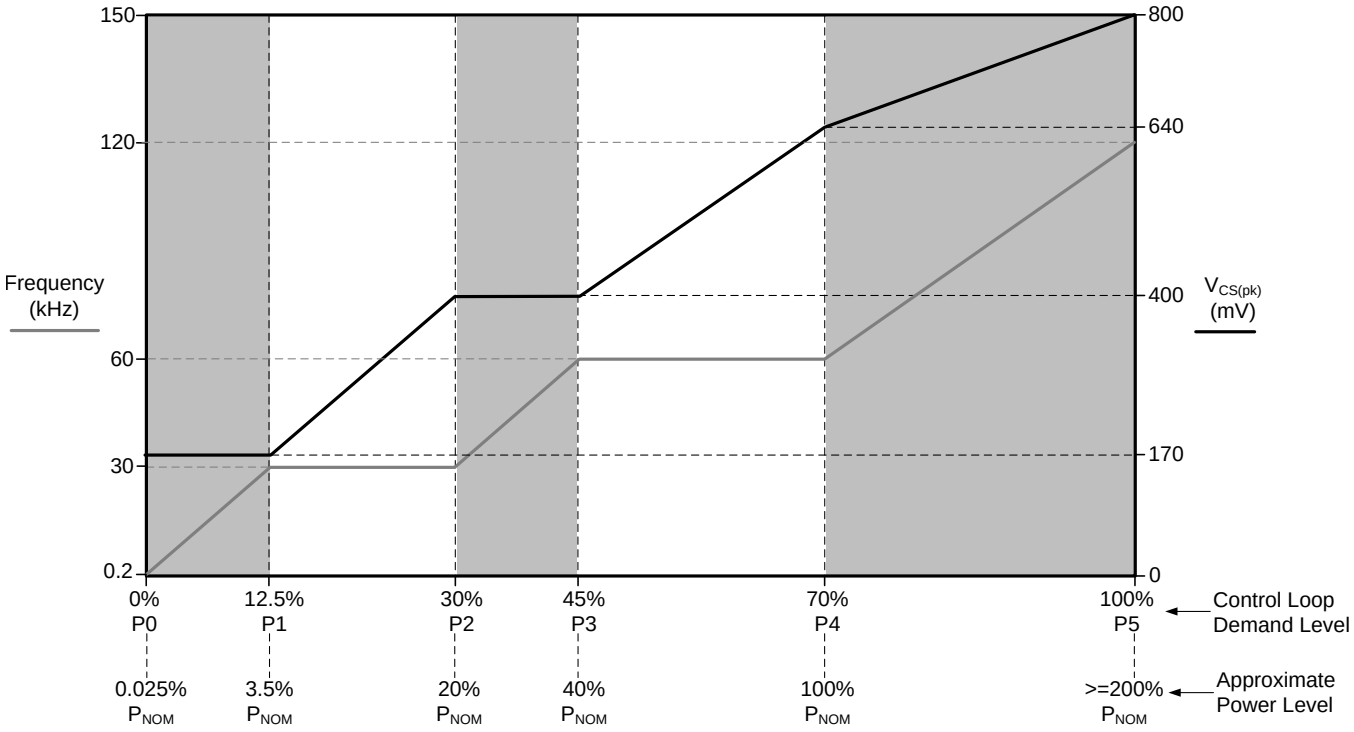

Figure 41. Modulator Modes and Frequency Variations with Power Level

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For no load and very light loads (P_0 to P_1 region) the modulator operates in a pulse frequency modulation (PFM) mode. In PFM mode, the device maintains a constant peak current in the transformer magnetizing inductance, so that the energy transferred in each switching cycle is fixed. The magnetic sensing, fixed-point sampling scheme requires that the device always imposes a minimum peak current. This minimum peak-current demand naturally results in a minimum transformer magnetizing volt-second product that the device maintains across the input line voltage range. Ensuring a minimum on-time magnetizing volt-seconds also ensures a balancing volt-second flyback interval, during which the device guarantees the availability of the output voltage sample. Magnetic Sensing: Power Stage Design Constraints outlines the transformer design constraints necessary to comply with the minimum on-time and minimum required volt-seconds.

In the P_0 to P_1 region, the energy transfer per switching cycle is maximized, which in turn minimizes the switching frequency and associated switching and drive losses, to improve efficiency. However, due to concerns about audible noise in this region, the peak current $V_{CS(min)}$ in this region is limited to 22% of the peak $V_{CS(max)}$ at the maximum demand level. This peak-current derating maintains the transformer peak flux density to 22% of the peak, to minimize transformer-induced audible noise. Assuming a maximum peak flux density of typically 300 mT at highest peak current, this derating sets the peak flux level at approximately 65 mT in the light-load region. Empirically, this flux level greatly reduces magnetic audible noise for a variety of power levels and transformer designs. In this region, the use of sleep modes (where most of the device internal blocks are powered down in between switching cycles) minimizes the controller power consumption. Minimizing controller power consumption helps reduce total standby power consumption, and also greatly eases the bias design constraints.

For higher loads above P_1 (P_1 to P_2 region), the device fixes the modulator frequency at a low value above the audible range, while the peak switch current ramps up from the minimum level, to deliver the increased output power. Maintaining a fixed low-switching frequency while ramping peak current, minimizes switching losses to provide good light-load efficiency.

For higher loads above P_2 (P_2 to P_3 region), the device maintains a constant peak-switch current, while the modulator frequency ramps to its nominal operating value. The normal heavy load (between 40% and 100% of rated) operating power range lies between P_3 and P_4. In this region the device maintains a constant switching frequency at the nominal value $f_{SW(nom)}$, and the peak switch current ramps to achieve increased output power. Fixed-frequency operation at nominal operating power results in consistent EMI and transient load step performance.

Table 5. Frequency and Peak-Current Modulator Operating Ranges and Breakpoints

MODULATOR BREAKPOINT	DEMAND LEVEL (%)	APPROXIMATE POWER LEVEL % of P_{NOM}	V_{CS} PEAK		FREQUENCY f_{SW}	
			(mV)		(kHz)	
P_{O0}	0	0.025	172	$V_{CS(min)}$	0.200	$f_{SW(min)}$
P_{O1}	12.5	3.5	172	$V_{CS(min)}$	30	$f_{SW(LL)}$
P_{O2}	30	20	400	$V_{CS(nom)}$	30	$f_{SW(LL)}$
P_{O3}	45	40	400	$V_{CS(nom)}$	60	$f_{SW(nom)}$
P_{O4}	70	100	640	$V_{CS(bcm)}$	60	$f_{SW(nom)}$
P_{O5}	100	> 200	800	$V_{CS(max)}$	120	$f_{SW(max)}$

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The peak-power range lies between P_4 and P_5. In this region the transformer can operate in CCM depending on loading and line voltage. By increasing the frequency appropriately, higher average input current can be processed for the same peak current, so the transformer size does not need to increase substantially for a high-rated transient peak power. The modulator does, however, also increase the peak current in this region of operation, requiring a modest increase in transformer size, but this allows a larger transient peak power to be delivered. The modulator control loop adjusts both the frequency and peak current according to the power demand so that the increased frequency and peak current meets the load demand.

Figure 42 shows the modulator gain curve, specifically the non-linear modulator gain vs load. At very light loads, the modulator gain remains low, to help counteract the effect of the higher power stage gain as the load resistance increases. This low gain helps stabilize the magnetic regulation loop in the light load territory, where the output voltage sample rate drops with decreasing switching frequency. At heavier loads, the modulator gain progressively and smoothly increases to help improve transient response. When the switching frequency increases above the maximum magnetic sense sample rate ($f_{SMP(max)}$), the magnetic sense voltage control sample rate is clamped.

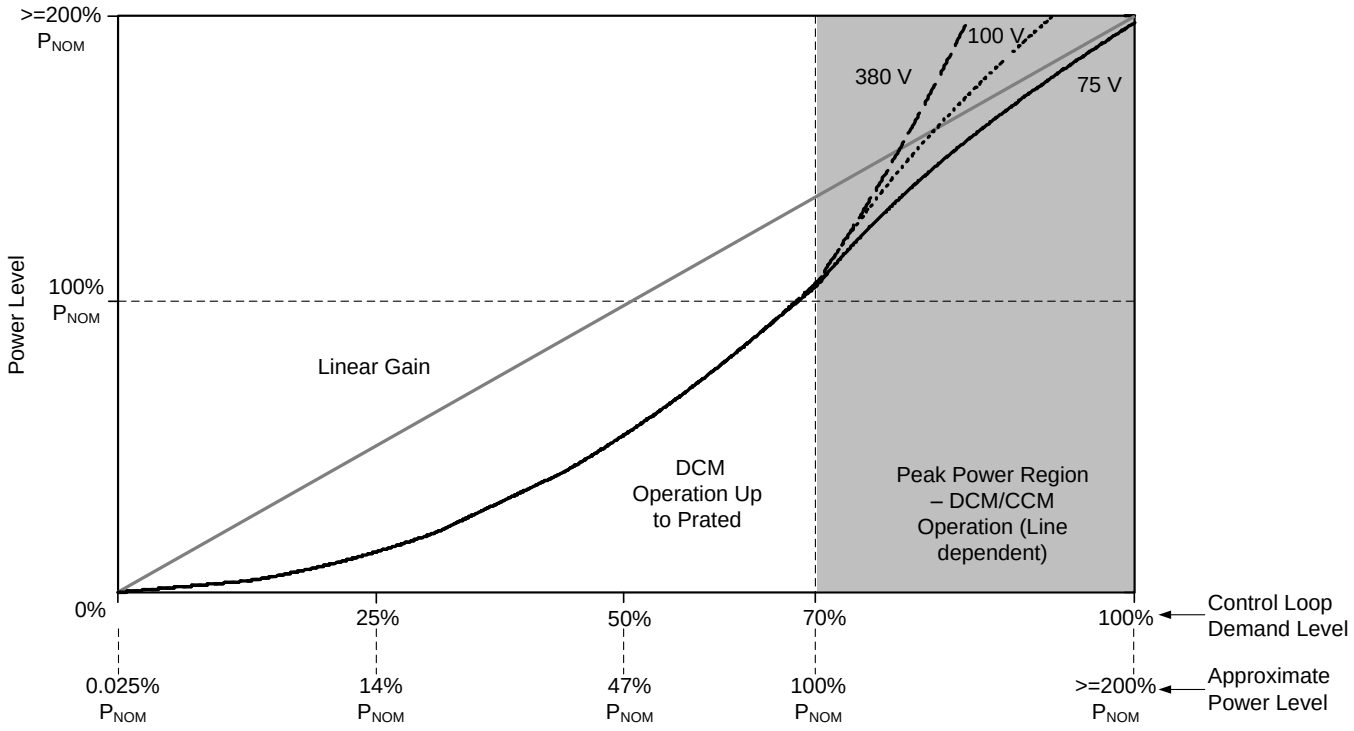

Figure 42. Modulator Gain Curves vs Bulk Capacitor Voltage

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8.3.22 Frequency Dither For EMI (except UCC28632)

To help ease EMI compliance of the system, the device dithers the switching frequency over time. This dithering of frequency is active only above the light-load region threshold ($P_{LL(\%)}$) point on the modulator curve. In the light load regions, frequency dither is disabled. The frequency dither follows a repeating pattern, in the sequence:

{(f_{NOM}), (f_{NOM} + 6.7%), (f_{NOM} + 6.7%), f_{NOM}), (f_{NOM} – 6.7%), (f_{NOM} – 6.7%), (f_{NOM}), ...}

The controller dwells at each frequency for 1 ms. The pattern repeats every 6 ms, as shown graphically in Figure 43.

NOTE

The device always dithers frequency between 6.7% and –6.7% at every operating point in the modulator. The dither frequency delta is not an absolute delta, it scales with actual operating frequency, depending on the exact operating point value.

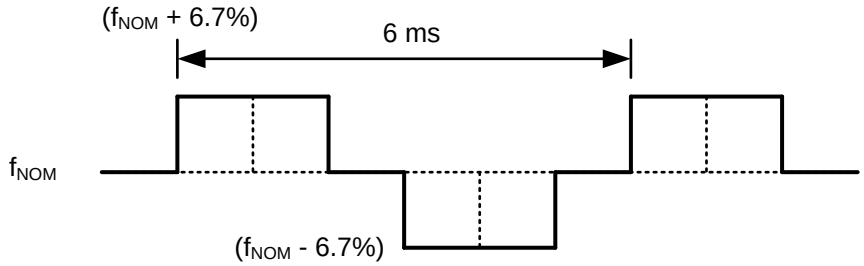

Figure 43. Frequency Dither Pattern Details

In order to balance the power flow and reduce and output ripple as a consequence of frequency dithering, the device automatically adjusts peak-current demand in inverse-proportion to the square-root of the frequency dither deviation. Thus, since the power flow (in DCM) is given by (½ × L × I^2 × f_{SW}), this balances the power flow, and cancels the output ripple as a consequence of frequency dithering.

8.4 Device Functional Modes

8.4.1 Device Internal Key Parameters

The application designer requires some key device internal parameters in order to calculate the required power stage components and values for a given design specification . Table 6 summarizes the key parameters.

Table 6. Key Internal Device Parameters

PARAMETER	DESCRIPTION	VALUE	UNIT
AC_{ON}	Minimum AC mains input RMS voltage to allow initial start-up, or restart, UCC28630, UCC28631, UCC28632, UCC28633	80	V_{AC}
	Minimum AC mains input RMS voltage to allow initial start-up, or restart, UCC28634	68	V_{AC}
AC_{OFF}	Minimum AC mains input RMS voltage below which PWM stops, UCC28630, UCC28631, UCC28632, UCC28633	65	V_{AC}
	Minimum AC mains input RMS voltage below which PWM stops, UCC28634	58	V_{AC}
$t_{UV(delay)}$	Delay time for which AC mains must remain below AC_{OFF} level to disable PWM, i.e. brownout delay time	40	ms
$t_{RESET(short)}$	Delay time in sleep mode before restart is initiated – applies to AC_{UV}, X-capacitor discharge responses	500	ms
$t_{RESET(long)}$	Delay time in sleep mode before restart is initiated – applies to all other auto-restart faults	1,000	ms
$f_{SW(uv)}$	Switching frequency used during initial 3-cycle exploratory pulses for AC_{ON} detection at start-up	15	kHz
$t_{ON(max_uv)}$	Maximum on-time used during initial 3-cycle exploratory pulses for AC_{ON} detection at start-up	2.3	µs
K_{LINE}	Device internal line sense gain factor	49.25	
K_{CC1}	Device internal CC mode gain factor	44.5	
K_{CC2}	Device internal CC mode offset factor	69.5	
$f_{SMP(max)}$	Maximum magnetic sense sample rate; in effect when $f_{SW} > f_{SMP(max)}$	16	kHz
$V_{DD(latch_hi)}$	Upper VDD regulation level during latched fault mode	10	V
$V_{DD(latch_lo)}$	Lower VDD regulation level during latched fault mode	8	V
$t_{ON(hv)}$	HV current source on-time during X-capacitor sampling	20	µs
$t_{SMP(hv)}$	HV current source sample repetition rate during X-capacitor sample burst	1	ms
$t_{WAIT(hv)}$	HV current source wait-time between X-capacitor sampling bursts	200	ms
$P_{LL(\%)}$	Light-load region threshold as % of P_{NOM}	12.5%	
$V_{DD(sc)}$	VDD short-circuit threshold below which charging current is limited	1.0	V
$t_{PROP(gate)}$	Internal PWM comparator + latch + gate driver aggregate delay	100	ns
$t_{START(del)}$	Internal start-up initialization delay	3	ms
$V_{SENSE(wake)}$	VSENSE pin wake threshold for fast transient response (UCC28633 only)	0.8	V

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC2863x device is a highly integrated primary-side-regulated (PSR) flyback controller, supporting magnetically-sensed output voltage regulation via the transformer bias winding. This sensing eliminates the need for a secondary-side reference, error amplifier and opto-isolator for output voltage regulation. The device delivers accurate output voltage static load and line regulation, and accurate control of the output constant-current limit.

The fixed-point magnetic sampling scheme allows operation in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The combination of the sampling scheme and high current gate driver source and sink capability, makes this device ideal for high power flyback converters up to 100 W and beyond.

The modulator adjusts both frequency and peak current in different load regions to maximize efficiency throughout the operating range. The control approach improves performance (efficiency, size and cost) and can reduce transformer size and cost by allowing operation in CCM with FM during peak overload conditions. The modulator supports peak-to-average transient overload power up to 200% of the nominal average rating.

9.2 Typical Application

9.2.1 Notebook Adapter, 19.5 V, 65 W

This design example describes the PWR572 EVM design and outlines the design steps required to design a constant-voltage, constant-current flyback converter for a 19.5-V/65-W notebook adapter. For all equations and design steps, refer to Table 6 for definitions and values of key internal device parameters that are relevant for calculations of external component values.

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Typical Application (continued)

9.2.2 UCC28630 Application Schematic

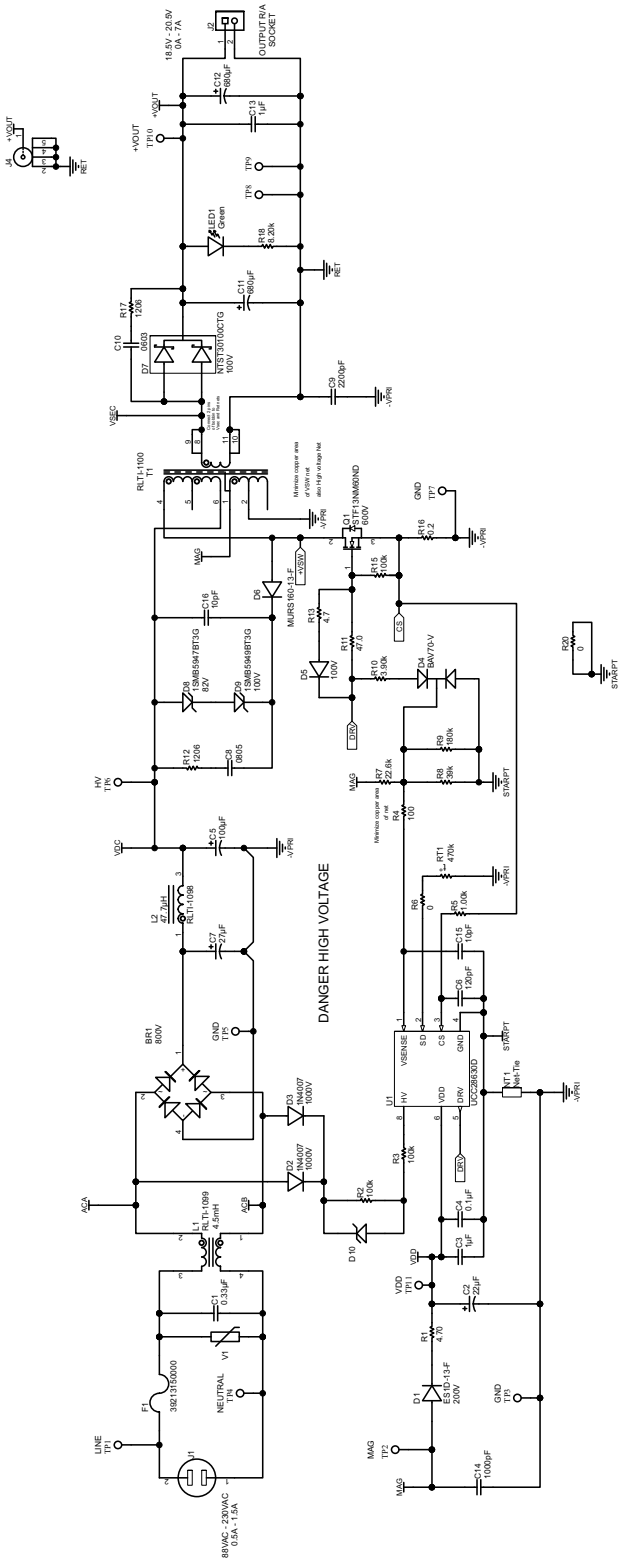

Figure 44. Typical Application Circuit for 19.5-V / 65-W Adapter

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Typical Application (continued)

9.2.3 Design Requirements

Table 7. Design Requirements

DESIGN PARAMETER	TARGET VALUE
Output voltage	19.5 V
Rated (continuous) output power	65 W
Peak (transient) output power	130 W
Peak (transient) output power duration	2 ms
Input AC voltage range	88 V_{RMS} to 264 V_{RMS}
Typical efficiency	88%
Minimum bulk voltage at 88 V_{AC}/47 Hz and rated (continuous) output power	82 V

9.2.4 Detailed Design Procedure

9.2.4.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC2863x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.4.2 Input Bulk Capacitance and Minimum Bulk Voltage

The required bulk capacitance value depends on the target minimum bulk capacitor ripple voltage at minimum AC input line, minimum line frequency and on the power level of interest. As a way of estimating, use 1.5-µF to 2-µF per Watt of rated, continuous power to achieve approximately 70 V to 80 V minimum at 88 V_{RMS} input. This case indicates a required bulk capacitance of between approximately 100 µF and 130 µF. Alternatively, the required capacitance may be explicitly calculated for a specific set of requirements using Equation 21.

$$C_{BULK} = \frac{\frac{P_{OUT}}{\eta} \times \left(0.5 + \frac{1}{\pi} \times \sin^{-1}\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{AC(min)}}\right)\right)}{\left(2 \times V_{AC(min)}^2 - V_{BULK(min)}^2\right) \times f_{LINE(min)}} \quad (21)$$

Using the parameters in Table 7, this calculates a required C_{BULK} of 130 µF.

To help reduce differential mode (DM) emissions for conducted EMC compliance, the bulk capacitance has been split into two separate capacitors C5 and C7 in Figure 44, with a small DM choke L2 inserted between the capacitors. The total resulting capacitance of 127 µF is close to the required minimum requirement per Equation 21, and the design results in a small decrease in the actual bulk capacitor minimum ripple voltage.

Next, verify that the choice of bulk capacitance satisfies the X-capacitor discharge constraints for rate of discharge by the load when X-capacitor sampling is inactive, per Equation 5. The bulk capacitance should be less than the value calculated by Equation 22.

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$$C_{BULK} \leq \frac{2\left(\frac{P_{NOM}}{\eta}\right) \times P_{LL\,(\%)} \times t_{DIS}}{\left(V_{AC(pk)}{}^2 - V_{SELV}{}^2\right)} = \frac{2(65 \times 0.125) \times 1}{(373^2 - 60^2)} = 136\ \mu F \quad (22)$$

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9.2.4.3 Transformer Turn Ratio

Choose the transformer primary-to-secondary-side turns ratio based on the allowed voltage stress for the output rectifier, or the primary MOSFET. For 19.5-V charger designs, it is valid to choose a turns ratio that allows the use of a more efficient 100-V Schottky rectifier.

$$\frac{N_P}{N_S} = \frac{V_{AC(pk_max)}}{\left(V_{REV(rated)} \times \%Derating\right) - \left(V_{OUT} + V_{RECT}\right)} \tag{23}$$

For a good Schottky diode with 100-V reverse rating, $V_{REV(rated)}$, the rectifier forward voltage drop, V_{RECT}, can be expected to be in the range of 0.4 V to 0.5 V at 3 A to 5 A, at practical operating temperatures in the region of 100°C. Allowing an 85% derating on the rectifier reverse voltage stress, Equation 23 indicates a required turns ratio of 5.734 for a maximum AC peak voltage of 373 V (264 V_{RMS}).

Choose the bias winding turns ratio to set the nominal bias voltage for the device VDD pin. Use an initial $V_{BIAS(target)}$ of 12 V.

$$\frac{N_B}{N_S} = \frac{V_{BIAS(target)} + V_F}{\left(V_{OUT} + V_{RECT}\right)}$$

where

- V_F is the forward voltage drop of the rectifier on the bias winding. (24)

For a typical 0.7-V bias-diode drop, this equation calculates to 0.6366.

When the transformer size and type are chosen, the actual turns values can be calculated. Because the turns need to be rounded to integer values, the actual turns ratios achieved deviates from these targets. Check the final ratios to ensure that the secondary-side Schottky rectifier stress and the bias winding nominal level are acceptable. Adjust the specific turns counts to meet the target ratios.

9.2.4.4 Transformer Magnetizing Inductance

Match the power stage design to the modulator curves by ensuring that the boundary conduction mode (BCM – boundary of operation between DCM and CCM) point coincides with the minimum bulk-capacitor voltage at minimum line, at rated output power. This choice results in DCM operation at all line voltages for all loads up to continuous rated load, and minimizes power loss and EMC impacts due to output rectifier reverse recovery during CCM operation. This design choice allows operation to extend into the CCM region of operation as required to deliver the transient peak load.

To achieve this design target, the required primary magnetizing inductance, L_{PRI} is calculated from Equation 25. In this equation, the value of $F_{SW(nom)}$ is 60 kHz, taken from the modulator curve region P_3 to P_4, in Table 5. The value of $V_{BULK(min)}$ is the value that occurs with the actual used bulk capacitance of 127 µF.

$$L_{PRI} = \frac{1}{2 \times \left(\frac{P_{RATED}}{\eta}\right) \times \left(\frac{1}{V_{BULK(min)}} + \frac{1}{\frac{N_P}{N_S} \times \left(V_{OUT} + V_{RECT}\right)}\right)^2 \times f_{SW(nom)}} \tag{25}$$

This calculates a value of 257 µH. Round the value to 260 µH.

9.2.4.5 Current Sense Resistor R_{CS}

In addition to choosing L_{PRI} value to map the rated power to the target BCM point at minimum bulk voltage, choose the R_{CS} value according to Equation 26. This calculation ensures that the resulting peak current, in conjunction with the chosen value of magnetizing inductance, and the 60-kHz modulator frequency, delivers the required input power to meet the rated output load power, at minimum bulk voltage ripple.

$$R_{CS} = \frac{V_{CS(bcm)}}{2 \times \left(\frac{P_{RATED}}{\eta}\right) \times \left(\frac{1}{V_{BULK(min)}} + \frac{1}{\frac{N_P}{N_S} \times (V_{OUT} + V_{RECT})}\right)} \quad (26)$$

where

- $V_{CS(bcm)}$ is the modulator peak-current sense level at point P_4 (640 mV)

This equation calculates a value of 207 mΩ. Use the nearest standard E24 value of 200 mΩ.

9.2.4.6 Transformer Constraint Verification

As outlined in Magnetic Sensing: Power Stage Design Constraints, there are constraints on the ratio of R_{CS}/L_{PRI} to ensure the design is consistent with the required volt-seconds for output sampling at minimum load, and with the controller $t_{ON(min)}$ at high line. Per Equation 15 and Equation 16, limit the ratio of R_{CS}/L_{PRI}.

$$\frac{R_{CS}}{L_{PRI}} \leq \frac{V_{CS(min)}}{t_{OUT(smp)}} \times \frac{N_S}{N_P} \times \frac{1}{(V_{OUT} + V_{RECT})} = \frac{172\ mV}{1.7\ \mu s} \times \frac{6}{34} \times \frac{1}{(19.5\ V + 0.4\ V)} \cong 900 \quad (27)$$

and,

$$\frac{R_{CS}}{L_{PRI}} \leq \frac{1}{V_{IN(pk_max)}} \times \frac{V_{CS(min)}}{t_{ON(min)}} = \frac{172\ mV}{373\ V\ \times 0.6\ \mu s} \cong 770 \quad (28)$$

In this case, the ratio equates to 769, so both constraints are met.

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9.2.4.7 Transformer Selection and Design

After determining the value of current sense resistor R_{CS}, determine the maximum peak current at maximum demand point on the modulator. Accommodate for the I_{PEAK} adjustment for frequency dithering. Use this value when calculating the margin for core saturation. In this case, $I_{PK(sat)}$ calculates to 4.13 A.

$$I_{PK(sat)} = \frac{V_{CS(max)} \times \sqrt{106.7\%}}{R_{CS}} \tag{29}$$

In subsequent calculations of required primary turns etc, the average maximum peak current, $I_{PK(max)}$, during the frequency dither period should be used, which calculates to 4.0 A.

$$I_{PK(max)} = \frac{V_{CS(max)}}{R_{CS}} \tag{30}$$

Knowing $I_{PK(max)}$, L_{PRI} and the turns ratio, the choice of transformer size and core shape and type dictates the required number of primary, secondary and bias turns, and the size of the air-gap. Various trade-offs, design preferences, and transformer design targets (size, cost, target losses, etc.) influence the specific choice of transformer core in any given design.

In the case of the UCC28630EVM-572 (PWR572 EVM), core area-product geometry was used to choose the minimum core size available to meet the power level. The core geometry factor K_g is a figure-of-merit that reflects the core power capability, in terms of its physical size, shape and design. It combines the core effective cross-sectional area, A_e, winding window area, A_w, and the mean length per turn (MLT) of wire around the core.

$$K_G = \frac{A_e^2 \times A_W}{MLT} \tag{31}$$

Estimate the required design core geometry, $K_{G(des)}$, using the required transformer inductance L_{PRI}, maximum peak current $I_{PK(max)}$, allowed maximum core flux density B_{max} and a target copper loss budget, P_{CU}.

$$K_{G(des)} = \frac{L_{PRI}^2 \times I_{PK(sat)}^2 \times I_{TOT}^2 \times \rho_{CU}}{B_{max}^2 \times K_U \times P_{CU}}$$

where

- ρ_{cu} is the resistivity of Copper (approximately 1.7×10^{-8} Ωm at room temperature, 2.2×10^{-8} Ωm at 100°C),
- K_u is a winding window utilization factor that accounts for the percentage of the window that is occupied by Copper

(32)

K_u can often be as low as 25%, due to the fill factor (gaps between wires), wire insulation (especially for triple-insulated wire), and the need for insulating tapes and EMC shielding layers. The estimate of the required core geometry needs an estimate of the aggregate total winding current I_{TOT}. The analysis models the flyback transformer primary and secondary windings as a single lumped non-isolated inductor (such as a single winding buck inductor), only for the purpose of sizing the required core winding window to achieve the target copper loss. In this case, the secondary-side current amplitude reflects to the primary side so that aggregate total primary current. I_{TOT} can be estimated in Equation 33.

$$I_{TOT} = I_{PK} \times \sqrt{d/3} + I_{PK} \times \sqrt{d_{SEC}/3}$$

where

- d is the primary on-time duty cycle
- d_{SEC} is the secondary-side flyback period duty cycle

(33)

At rated power and minimum bulk capacitor voltage, the inductance L_{PRI} has been chosen to achieve boundary-mode conduction, therefore the duty cycle is given in Equation 34.

$$d = \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_{RECT})}{\left(V_{BULK(min)} + \frac{N_P}{N_S} \times (V_{OUT} + V_{RECT})\right)} \tag{34}$$

and

$$d_{SEC} = 1 - d \tag{35}$$

At the boundary conduction point, the primary peak current I_{PK} is at the level set by the modulator, $V_{CS(bcm)}$. So from Equation 33, I_{TOT} becomes Equation 36.

$$I_{TOT} = \frac{V_{CS(bcm)}}{\sqrt{3}R_{CS}} \times \left[\sqrt{\frac{\frac{N_P}{N_S} \times (V_{OUT}+V_{RECT})}{\left(V_{BULK(min)}+\frac{N_P}{N_S} \times (V_{OUT}+V_{RECT})\right)}} + \sqrt{\frac{V_{BULK(min)}}{\left(V_{BULK(min)}+\frac{N_P}{N_S} \times (V_{OUT}+V_{RECT})\right)}} \right] \quad (36)$$

Equation 36 calculates I_{TOT} as 2.6 A. Thus the required design $K_{G(des)}$, assuming K_U of 25%, B_{max} of 315 mT and a target of 1-W copper loss, is shown in Equation 37.

$$K_{G(des)} = \frac{260\ \mu H^2 \times 4.13^2 \times 2.6^2 \times 2.2 \times 10^{-8}}{0.315^2 \times 0.25 \times 1.0} \quad (37)$$

Equation 37 indicates that this design requires a core size and shape with a K_G of more than 6.9×10^{-12}. A review of commonly used cores indicated that the RM10/I core set meets this requirement. With A_e of 96.6 mm^2, A_w of 44.2 mm^2 and mean length per turn (MLT) of 52 mm, $K_{G(RM10)}$ is 7.9×10^{-12}, giving some margin over the design target.

$$K_{G(RM10)} = \frac{(96.6 \times 10^{-6})^2 \times (44.2 \times 10^{-6})}{(52 \times 10^{-3})} = 7.932 \times 10^{-12} \quad (38)$$

With the chosen core, the actual primary, secondary-side and bias turns can be calculated. The required primary turns depend on the allowed B_{max}. For most power ferrites, a value in the region of 315 mT is commonly used.

$$N_P = \frac{L_{PRI} \times I_{PK(max)}}{B_{max} \times A_e} = \frac{260\ \mu \times 4.0}{0.315 \times 96.6\ \mu} = 34.18 \quad (39)$$

Round N_P to 34. Now the required secondary-side turns can be calculated, using the previously calculated turns ratio per Equation 23.

$$N_S = \frac{N_P}{5.734} = 5.93 \quad (40)$$

Again, N_S is rounded to 6. Due to the integer rounding of the turns count, ensure that the actual turns ratio is within 5% of original target (if outside this range, secondary-side rectifier or primary MOSFET stress may be too high).

$$\frac{\frac{N_P}{N_S}}{5.734} = 98.8\% \quad (41)$$

From Equation 24, the required bias turns can be calculated using Equation 42.

$$N_B = \frac{V_{BIAS(target)} + V_F}{(V_{OUT} + V_{RECT})} \times N_S = \frac{12 + 0.7}{19.5 + 0.45} \times 6 = 3.82 \quad (42)$$

Again, N_B is rounded to 4. The effect of integer scaling in the turns is verified by calculating the expected bias voltage versus target.

$$V_{BIAS} = (V_{OUT} + V_{RECT}) \times \frac{N_B}{N_S} - V_F = (19.5 + 0.45) \times \frac{4}{6} - 0.7 = 12.6\ V \quad (43)$$

The V_{BIAS} target was 12 V, so this is acceptable.

The required core inductance factor, A_L, to achieve the target inductance can be calculated as in Equation 44. The transformer manufacturer uses this factor to gap the core center leg.

$$A_L = \frac{L_{PRI}}{{N_P}^2} = \frac{260\mu}{34^2} = 225\ nH \quad (44)$$

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Finally, calculate the required air-gap length l_g, based on the required inductance and the core geometry.

$$l_g = \frac{N_P^2 \times \mu_0 \times A_{CENTRE}}{L_{PRI}} - \frac{l_m}{\mu_r}$$

where

- μ_0 is the permittivity of free-air
- μ_r is the relative permeability of the chosen core ferrite material
- A_{CENTRE} is the cross-sectional area of the core center leg
- l_m is the core average magnetic path length (45)

For the RM10/I core in 3C95 material (chosen for low core loss over a wide temperature range), the required air-gap length is calaulated using Equation 46.

$$l_g = \frac{34^2 \times 4\pi \times 10^{-7} \times 93.3\,\mu}{260\,\mu} - \frac{44.6\,m}{5500} = 514\,\mu m \quad (46)$$

Typically, the air-gap calculation in Equation 45 underestimates l_g, due to flux fringing in the air-gap. The fringing causes the affective area of the air-gap A_g to be somewhat larger than the ferrite core center leg A_{CENTRE}, depending on the gap length. This difference requires an increase in the required air-gap length to get the required inductance, which results in a further increase in fringing. However use Equation 45 to determine an initial value for l_g, which can then be used to estimate A_g. For round centre legs, the increase in effective area within the gap can be estimated empirically from Equation 47

$$A_g = A_{CENTRE} \times \left(1 + \frac{l_g}{D_{CENTRE}}\right)^2 = 93.3\,\mu \times \left(1 + \frac{0.514}{10.9}\right)^2 = 102.31\,mm^2$$

where

- D_{CENTRE} is the center leg diameter (47)

(For more information about this subject, download the paper *Inductor and Flyback Transformer Design*, Lloyd Dixon, TI Power Supply Design Seminar SLUP127).

Because Equation 45 assumes that A_g equals A_{CENTRE}, it must be modified using Equation 48.

$$l_g = \left(\frac{N_P^2 \times \mu_0 \times A_g}{L_{PRI}}\right) - \left(\frac{l_m}{\mu_r} \times \frac{A_g}{A_e}\right) \quad (48)$$

Re-iterating the air-gap calculation in Equation 49 .

$$l_g = \left(\frac{34^2 \times 4\pi \times 10^{-7} \times 102.31\,\mu}{260\,\mu}\right) - \left(\frac{44.6\,m}{5500} \times \frac{102.31\,\mu}{96.6\,\mu}\right) = 563.0\,\mu m \quad (49)$$

Typically, after the second iteration above in Equation 48, the estimated air-gap is very close to the required value. Further iterations can be made, but should not be necessary.

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9.2.4.8 Slope Compensation Verification

After choosing the current sense resistor, transformer inductance and transformer turns ratio, verify the required slope compensation against the fixed internal slope compensation. The worst case slope compensation requirement always occurs at the highest duty cycle operating point (at minimum bulk voltage level).

For stability, the slope compensation should be at least 50% of the difference between the inductor up-slope and down-slope. [reference Bob Mammano TI Power Supply Design Seminar paper, 2001, SLUP173]. For a flyback converter, the difference in slopes in CCM is equal the operating duty cycle multiplied by the inductor current down-slope value. For example, for 50% $d_{BULK(min)}$ at minimum bulk capacitor voltage, the required slope compensation ramp is 25% of the inductor current down-slope.

As listed in Table 7, the specified peak-load transient is 130 W for 2 ms. In a worst case, peak transient timing with respect to the AC phase, the V_{BULK} minimum level dips to 65 V. This corresponds to a duty cycle of approximately 63.5% according to Equation 50.

$$d_{BULK(min)} = \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_{RECT})}{\left(V_{BULK(min)} + \frac{N_P}{N_S} \times (V_{OUT} + V_{RECT})\right)} = \frac{34/6 \times (19.95)}{(65 + 34/6 \times (19.95))} = 63.5\% \quad (50)$$

The required slope compensation ramp is calculated at 63.5% duty cycle.

$$V_{CS(slope)} = 50\% \times d_{BULK(min)} \times R_{CS} \times \left(\frac{\frac{N_S}{N_P} \times (V_{OUT} + V_{RECT})}{L_{PRI}}\right) = 0.5 \times 0.635 \times 0.2 \times \left(\frac{34/6 \times 19.95}{260\ \mu}\right) = 27.6\ mV/\mu s \quad (51)$$

This value is within the 30 mV/µs of internal slope compensation provided by the controller.

9.2.4.9 Power MOSFET and Output Rectifier Selection

The initial design target proposed the use of a 100-V Schottky rectifier. The secondary-side reverse voltage stress can be verified using the final transformer design sh own in Equation 52.

$$V_{RECT(rev)} = \left(\frac{N_S}{N_P} \times V_{AC(pk_max)}\right) + (V_{OUT} + V_{RECT}) = \frac{6}{34} \times 373 + 19.95 = 85.8\ V \quad (52)$$

The value derived from Equation 52 is close to the original design target of 85 V.

For 65-W load, the average DC output current is 3.35 A for 19.5-V output. However, to reduce losses, a much higher current rated diode is typically used, to yield a much lower forward voltage drop V_{RECT}. As shown in Figure 44, a 30-A rated diode D7 is used in this case, with a forward drop of approximately 0.45 V at 3.5 A, 100°C.

For the primary-side MOSFET, the peak voltage stress can be estimated using Equation 53.

$$V_{DS(max)} = V_{AC(pk_max)} + \frac{N_P}{N_S} \times (V_{OUT} + V_{RECT}) = 373 + \frac{34}{6} \times 19.95 = 486\ V \quad (53)$$

An allowance of at least 100 V must be added to this figure to account for the leakage inductance spike at turn-off. This voltage spike depends on the transformer implementation and the amount of leakage inductance, as well as the specific design of the snubber. A more aggressive snubber may reduce the voltage spike, but at the expense of higher losses in the snubber. A voltage rating of at least 600 V is recommended for the power MOSFET to allow for leakage.

The MOSFET rms current at low line, rated load, can be estimated using Equation 54.

$$I_{PRI(rms)} = \frac{V_{CS(bcm)}}{\sqrt{3}R_{CS}} \times \sqrt{\frac{\frac{N_P}{N_S} \times (V_{OUT} + V_{RECT})}{\left(V_{BULK(min)} + \frac{N_P}{N_S} \times (V_{OUT} + V_{RECT})\right)}} = \frac{0.64}{\sqrt{3} \cdot 0.2} \times \sqrt{0.58} = 1.41\ A \quad (54)$$

As can be seen in Figure 44, the chosen MOSFET Q1 is a 13-A, 600-V device.

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9.2.4.10 Output Capacitor Selection

Select the output capacitor value on the basis of one of the following, depending on which one is the limiting factor:

- Required ripple current rating to absorb the high secondary-side peak current
- Required esr to achieve a target peak-peak ripple voltage
- Required holdup capacitance to achieve target minimum output voltage for a specified load transient from no load when the device is switching at $f_{SW(min)}$

For flyback converters, ripple current rating often dictates the output capacitance value. The required ripple current rating can be calculated from Equation 55.

$$I_{CAP(rms)} = \sqrt{\left(\frac{V_{CS(bcm)}}{R_{CS}} \times \frac{N_P}{N_S} \times \sqrt{\frac{V_{BULK(min)}}{3 \times \left(V_{BULK(min)} + \left(\frac{N_P}{N_S} \times (V_{OUT} + V_{RECT}) \right) \right)}} \right)^2 - {I_{OUT}}^2} \quad (55)$$

At rated 65-W load, $I_{CAP(rms)}$ = 5.9 A_{RMS}. Capacitors C11 and C13 in Figure 43 are chosen to meet this ripple requirement, (each capacitor has a 2.5-A minimum rating at 105°C). Total output capacitance is 1360 µF.

9.2.4.11 Calculation of CC Mode Limit Point

Calculate the expected output constant-current (CC) limit point from Equation 20. As previously noted, K_{CC1} is 44.5 and K_{CC1} is 69.5. Thus, $I_{OUT(lim)}$ in this case is approximately calculated in Equation 56.

$$I_{OUT(lim)} = \frac{1}{R_{CS}} \times \frac{N_P}{N_S} \times \frac{K_{CC1}}{K_{CC2} + V_{OUT} \times \frac{N_P}{N_S}} = \frac{1}{0.2} \times \frac{34}{6} \times \frac{44.5}{69.5 + \left(19.5 \times \frac{34}{6}\right)} = 7.0 \text{ A} \quad (56)$$

9.2.4.12 VDD Capacitor Selection

Size the VDD capacitor to supply sufficient $I_{DD(run)}$ current to the device during initial start-up, and also during the charging phase of the main output capacitors. During the charging phase the bias winding on the transformer must supply the bias power. When VDD reaches the $V_{DD(start)}$ threshold, the device consumes $I_{DD(run)}$ for $t_{START(del)}$ before the PWM switching commences. Thereafter, the bias current is the device current plus the MOSFET gate current. The VDD capacitor must support this higher level of current until the output is sufficiently charged that the bias winding rail has increased above the $V_{DD(stop)}$ level.

Calculate the required bias capacitance from the total bias charge associated with the device run current during the $t_{START(del)}$ phase, plus the device run current during the output charge phase, plus the primary MOSFET gate charge current during the output charge phase. The time taken for the output charge phase to reach a sufficient level to supply the bias can be calculated from the size of the output capacitor, target output regulation voltage, and the difference between the available CC mode current limit and the maximum load current (assuming that the output capacitor has to be charged whilst also supplying full rated load current). Assume that the MOSFET is switched at 60 kHz throughout the charging phase.

Combining these into one equation, the required VDD capacitor can be calculated as shown in Equation 57.

$$C_{VDD} = \frac{\left(I_{DD(run)} \times t_{START(del)}\right) + \left(I_{DD(run)} + F_{SW(nom)} \times Q_{g(tot)}\right) \times \left(\frac{V_{OUT} \times C_{OUT}}{I_{OUT(lim)} - I_{O(max)}}\right) \times \left(\frac{V_{DD(stop_max)}}{V_{BIAS(nom)}}\right)}{\left[V_{DD(start_min)} - V_{DD(stop_max)}\right]} \quad (57)$$

This can be re-written with the explicit device values substituted:

$$C_{VDD} = \frac{(8m \times 3m) + \left(8m + 60\,k \times Q_{g(tot)}\right) \times \left(\frac{V_{OUT} \times C_{OUT}}{I_{OUT(lim)} - I_{O(max)}}\right) \times \left(\frac{8.5}{V_{BIAS(nom)}}\right)}{(13.0 - 8.5)} \quad (58)$$

For this EVM design, the MOSFET $Q_{g(tot)}$ is 30 nC, $V_{BIAS(nom)}$ is 12.6 V. $I_{O(max)}$ is 3.35 A, so this equates to:

$$C_{VDD} = \frac{(8m \times 3m) + (8m + 60\,k \times 30n) \times \left(\frac{19.5 \times 1360\mu}{7.0 - 3.35}\right) \times \left(\frac{8.5}{12.6}\right)}{(13.0 - 8.5)} = 16.0\ \mu F \quad (59)$$

Choose the next higher standard value, 22 µF.

Verify that the bias capacitance is sufficient to absorb all the X-capacitor energy when it has to be discharged, per Equation 3. From Figure 44, the value of X-capacitor is 330 nF.

$$C_{VDD} \geq C_X \times \left(\frac{V_{AC(pk)} - V_{SELV}}{V_{DD(start_min)} - V_{DD(reset_max)}}\right) = 330\ nF \times \left(\frac{373 - 60}{13 - 6.5}\right) = 15.9\ \mu F \quad (60)$$

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9.2.4.13 Magnetic Sense Resistor Network Selection

The required values for the magnetic sense divider network are calculated from Equation 11 and Equation 12. For the RM10/I transformer used in the PWR572 EVM, the secondary-side to bias leakage inductance was measured and found to be approximately 4%. This figure can be reasonably estimated as the ratio of the inductance value measured across the secondary-side pins with the bias pins shorted together (primary winding should remain open-circuit), to the inductance value measured across the secondary-side pins with all other windings open:

$$\%L_{LK(sec_bias)} = \frac{L_{SEC(bias_short)}}{L_{SEC(bias_open)}} \tag{61}$$

R_A is calculated as shown in Equation 62.

$$R_A = R_P \times \left(\frac{N_B}{N_P}\right) \times K_{LINE} = 3.9\ k\Omega \times \left(\frac{4}{34}\right) \times 49.25 = 22.597\ \ k\Omega \tag{62}$$

The nearest standard E96 value 22.6 kΩ is selected. R_B may then be calculated to set V_{OUT} at 19.5 V.

$$R_B = \frac{R_A}{\left(\frac{\left(V_{OUT} \times \left(1 - \%L_{LK(sec_bias)}\right) + V_{RECT}\right) \times \left(N_B/N_S\right)}{V_{OUT(ref)}} - 1\right)} = \frac{22.6\ k\Omega}{\left(\frac{(19.5 \times (1 - 0.04) + 0.45) \times (4/6)}{7.50} - 1\right)} = 32.10\ k\Omega \tag{63}$$

The nearest E96 value is 32.4 kΩ, which could be used, but results in some set-point regulation error. As shown in Figure 44, the setpoint may be fine-tuned by using two parallel resistors for R_B. In this case use values of 39 kΩ and 180 kΩ, to give a net equivalent of 32.05 kΩ, very close to the target value in Equation 63.

Note that the pull-up diode to DRV pin should be a standard switching signal diode such as BAS21 or similar. The reverse recovery of the diode should be 100 ns or less. A slow-recovery diode clamps the VSENSE pin low for an initial portion of the flyback interval, and may impair or prevent the ability to take a valid output voltage sample.

9.2.4.14 Output LED Pre-Load Resistor Calculation

As shown in Figure 44, the output power good LED1 and series resistor R18 form an output pre-load or minimum load. This pre-load is necessary in order to maintain regulation at no load, or when the power converter output is disconnected from the load system. Magnetic regulation relies on sensing the output voltage during switching cycles, so it is necessary to maintain a certain minimum switching frequency $f_{SW(min)}$ in order to continue sensing the output voltage. However, generating switching cycles at $f_{SW(min)}$ transfers energy to the output, which requires some load on the secondary-side to absorb this energy and prevent the output capacitors from being charged out of regulation. The minimum energy transferred at $f_{SW(min)}$ depends on the choice of magnetizing inductance L_{PRI} and current sense resistor R_{CS}.

$$P_{PRELOAD(min)} = 0.5 \times L_{PRI} \times \left(\frac{V_{CS(min)}}{R_{CS}}\right)^2 \times f_{SW(min)} = 0.5 \times 260\ \mu H \times \left(\frac{0.172}{0.2}\right)^2 \times 200 = 19.23\ \ mW \tag{64}$$

In order to ensure that the control loop operates at a frequency above the minimum switching frequency, $f_{SW(min)}$ (to ensure that the loop has adjustment range up/down as required to maintain regulation), the recommended minimum pre-load is at least twice the value calculated in Equation 64.

The required value of R18 can then be calculated, assuming a forward voltage drop of 1.8 V for the LED:

$$R_{LED} = \frac{V_{OUT}^2 - V_{OUT} \times V_{LED}}{2 \times P_{(preload_min)}} = \frac{19.5^2 - 19.5 \times 1.8}{2 \times 19.23m} = 8.97\ k\Omega \tag{65}$$

Use the next lower E24 value of 8.2 kΩ. For a design without an LED, a pre-load resistor of similar value is still required across the output voltage.

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9.2.5 External Wake Pulse Calculation at VSENSE Pin (UCC28633 Only)

The typical application circuit of Figure 39 may be redrawn as a simplified equivalent circuit as shown in Figure 45. In this equivalent circuit, the capacitor C_P is the total parasitic capacitance (MOSFET C_{oss}, transformer capacitance, etc), and resistance R_{WAKE} is the effective internal resistance of the UCC24650 WAKE pin to GND pin when the internal WAKE pull-down is active (see UCC24650 detailed datasheet specifications).

If all the elements on the primary and secondary of the transformer are referred to the bias winding, this can be further simplified as in Figure 46.

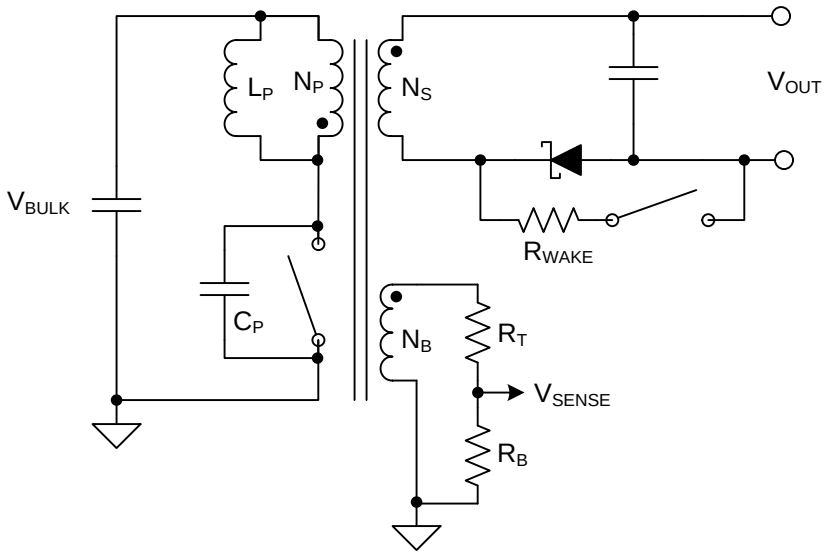

Figure 45. Simplified Equivalent Circuit of Wake Event with UCC24650

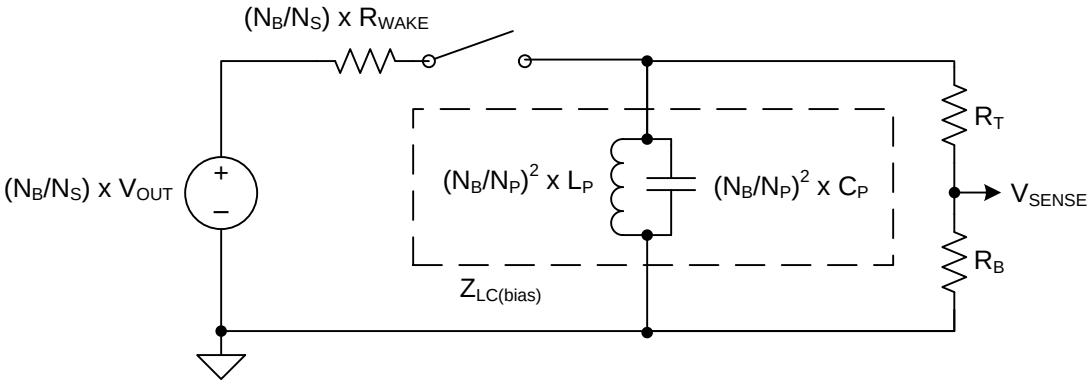

Figure 46. Bias-Referred Simplified Equivalent Circuit of Wake Event with UCC24650

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Thus, knowing L_P and C_P, the power stage impedance $Z_{LC(bias)}$ (reflected to the bias winding) may be calculated from Equation 66, and the effective wake resistance can be referred to the bias winding using Equation 67. The wake pulse amplitude can be calculated from Equation 68. If C_P is not known, it can be measured by observing the resonant ring period at the primary drain node, T_{RES}, and calculating C_P from Equation 69. Worst case values should be used to estimate the worst case minimum wake pulse amplitude at the VSENSE pin. It should also be noted that any filter cap on the VSENSE pin (including internal parasitic pin capacitance) adds an RC filter in conjunction with the Thevenin resistance of the VSENSE divider, R_T, R_B; this delays and further attenuate the wake pulse amplitude. Additionally, the internal wake comparator requires some over-drive to trip, and exhibits propagation delay that depends on the amount of overdrive. So some margin should be allowed in the wake pulse amplitude to ensure that the minimum wake pulse can adequately overdrive the internal wake comparator. A margin of at least 20% over the threshold $V_{SENSE(wake)}$ is recommended.

$$Z_{LC(bias)} = \sqrt{\frac{L_P}{C_P}} \times \left(\frac{N_B}{N_P}\right)^2 \tag{66}$$

$$R_{WAKE(bias)} = R_{WAKE} \times \left(\frac{N_B}{N_S}\right)^2 \tag{67}$$

$$V_{SENSE_WAKE(pk)} = \left(\frac{R_B}{R_A + R_B}\right) \times \left(V_{OUT} \times (1 - \Delta_{WAKE\%}) \times \frac{N_B}{N_S}\right) \times \left(\frac{Z_{LC(bias)}}{Z_{LC(bias)} + R_{WAKE(bias)}}\right) \tag{68}$$

$$C_P = \left(\frac{T_{res}}{2\pi}\right)^2 \times \frac{1}{L_P} \tag{69}$$

If the worst case wake pulse amplitude is too low, then the UCC24650 WAKE output can be augmented with an external PNP circuit Q1, R1 and R2, as shown in Figure 40. This circuit reduces the effective wake resistance to ground, so that a larger proportion of the output voltage appears across the transformer secondary pins when the UCC24650 WAKE activates.

Using the UCC28630EVM-572, (TI Literature Number SLUUAX9) circuit parameters from Figure 44, the nominal wake pulse amplitude at the VSENSE pin can be estimated. Of course, the rectifying diode D7 in Figure 44 would need to be relocated to return end of the secondary winding (pins 10, 11) to allow UCC24650 to be deployed.

From observation of the DCM ringing period, the period T_{RES} was found to be 1.138 µs. From Equation 69, C_P is estimated:

$$C_P = \left(\frac{T_{res}}{2\pi}\right)^2 \times \frac{1}{L_P} = \left(\frac{1.138\mu}{2\pi}\right)^2 \times \frac{1}{260\mu} = 126\,pF \tag{70}$$

From Equation 66, the power circuit impedance is:

$$Z_{LC(bias)} = \sqrt{\frac{L_P}{C_P}} \times \left(\frac{N_B}{N_P}\right)^2 = \sqrt{\frac{260\mu}{126p}} \times \left(\frac{4}{34}\right)^2 = 19.9\,\Omega \tag{71}$$

The WAKE pin resistance R_{WAKE} can be determined form the UCC24650 datasheet; for now a nominal value of 400 Ω is assumed. Referred to the bias winding (scaled by $(N_B/N_S)^2$), this becomes 178 Ω. Similarly $\Delta_{WAKE\%}$ can be determined from the UCC24650 datasheet; for now, a value of 97% is assumed. From Equation 68, the wake pulse amplitude can be calculated:

$$\begin{aligned} V_{SENSE_{WAKE(pk)}} &= \left(\frac{R_B}{R_A + R_B}\right) \times \left(V_{OUT} \times (1 - \Delta_{WAKE\%}) \times \frac{N_B}{N_S}\right) \times \left(\frac{Z_{LC(bias)}}{Z_{LC(bias)} + R_{WAKE(bias)}}\right) \\ &= \left(\frac{32.05}{22.6 + 32.05}\right) \times \left(19.5 \times 97\% \times \frac{4}{6}\right) \times \left(\frac{19.9}{19.9 + 178}\right) = 0.743V \end{aligned} \tag{72}$$

In this case, the VSENSE wake pulse amplitude would be insufficient to trip the internal wake comparator. If the power stage had higher L_P, or lower C_P, a larger wake pulse would be produced.

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Alternatively, the effective wake resistance R_{WAKE} may be reduced by adding the PNP circuit per Figure 40. This has been verified using Q1 = FMMTA92 PNP transistor, R1= 100 Ω and R2 = 2.2 kΩ. A wake pulse amplitude of almost 2 V_{PK} was produced at the VSENSE pin, giving generous margin to the internal threshold $V_{SENSE(wake)}$. The observed waveforms are shown in Figure 47 for a worst case 0% to 100% (65 W) load transient (where the PWM is at F_{MIN}). The PWM is re-activated when V_{OUT} has dropped by ~3%, rather waiting for the next timed wake-up (~5 ms later).

Figure 48 shows a zoomed waveform of the wake pulsing ringing as measured on the bias winding. It can be seen that the peak level is approximately 3 V_{PK}, which would produce a pulse of approximately 1.8 V at the VSENSE pin (scaled by VSENSE divider resistors R_T and R_B). As noted in Test and Debug Recommendations, the VSENSE pin should never be directly probed, doing so affects the regulation setpoint.

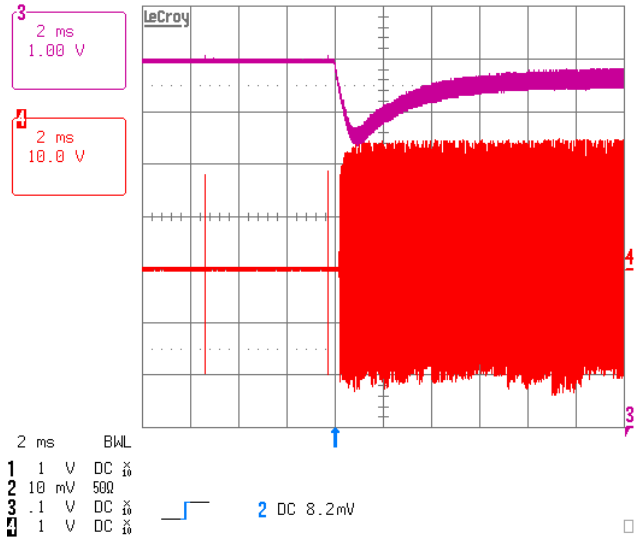

Figure 47. Observed Output Voltage (Ch3) and Bias Winding (Ch4) (showing wake event generated by UCC24650)

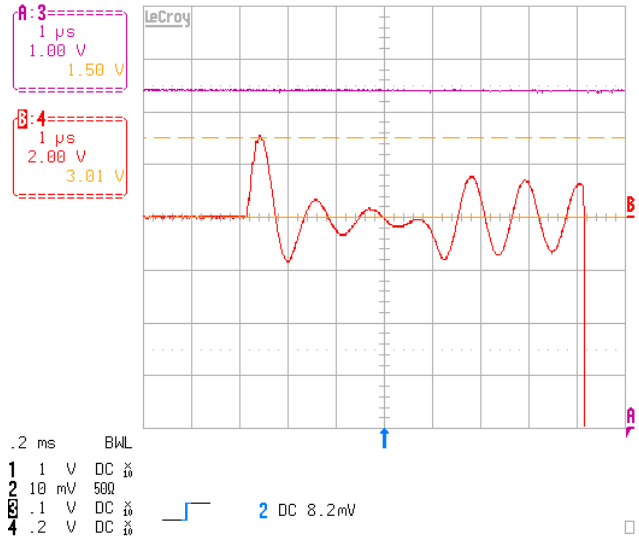

Figure 48. Zoom In of Wake-Pulse Ringing (observed across bias winding (ChB) generated by UCC24650)

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9.2.6 Energy Star Average Efficiency and Standby Power

Table 8 summarize the standby power, and Table 9 summarizes the average efficiency performance of the UCC28630EVM-572, (TI Literature Number SLUUAX9).

Table 8. Standby Power Performance

STANDBY POWER	
115 V_{AC} (mW)	**230 V_{AC} (mW)**
57	60

Table 9. Average Efficiency Performance

AVERAGE EFFICIENCY (INCLUDING OUTPUT 76-mΩ CABLE DROP)		
LOAD LEVEL (%)	**115 V_{AC} (%)**	**230 V_{AC} (%)**
25 (16.25 W)	89.44	89.26
50 (32.5 W)	88.98	89.38
75 (48.75 W)	88.24	89.10
100 (65 W)	87.59	88.73
Average	**88.6**	**89.1**

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9.2.7 Application Performance Plots

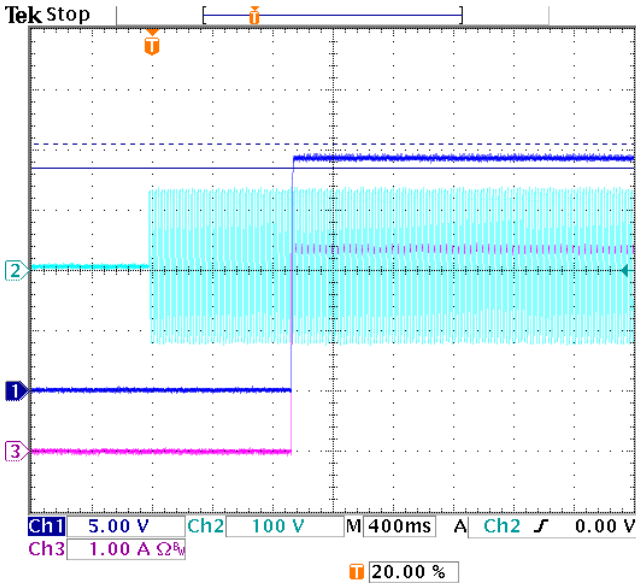

Figure 49. Start-Up from 90-V_{AC}, 3.35-A CC Load

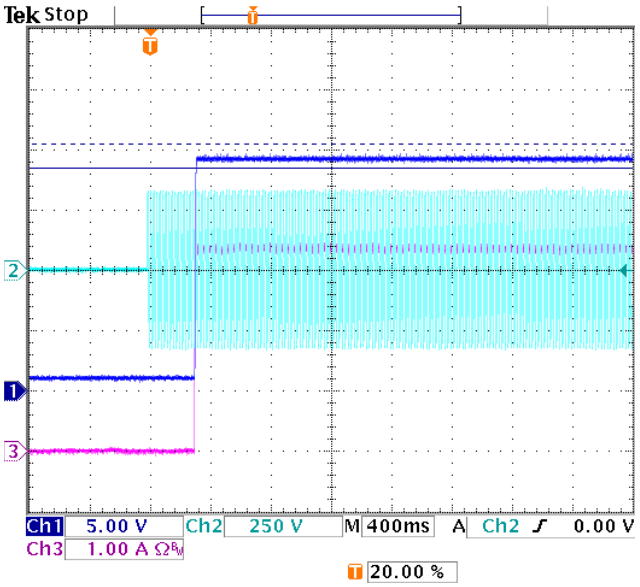

Figure 50. Start-Up from 230-V_{AC}, 3.35-A CC Load

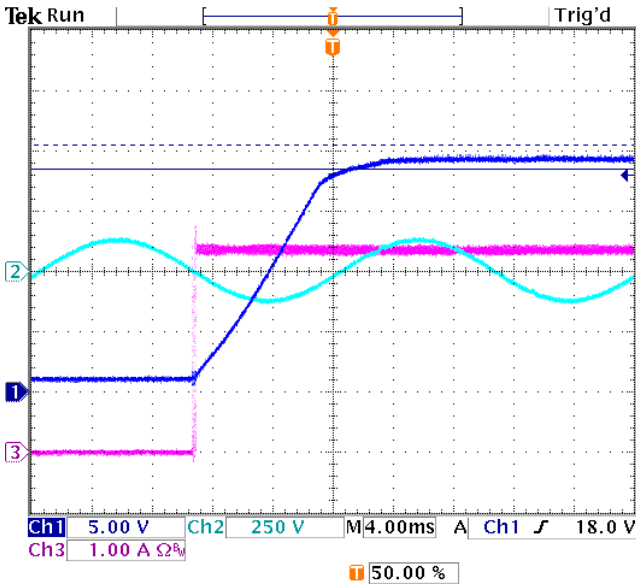

Figure 51. Output Rise-Time, 90-V_{AC}, 3.35-A CC Load

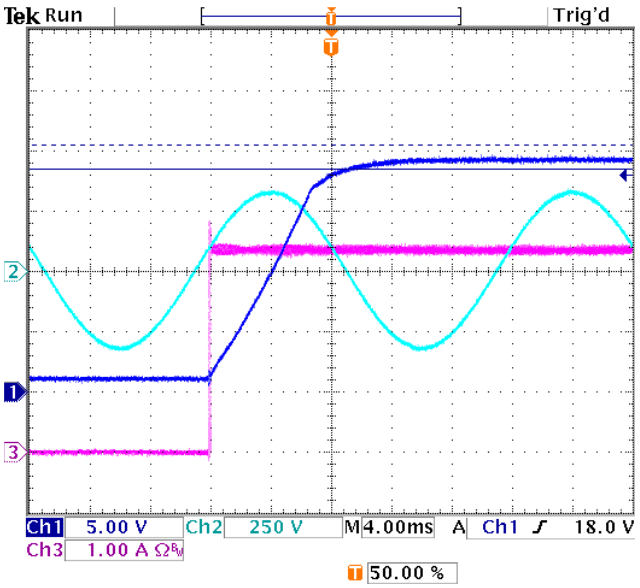

Figure 52. Output Rise-Time, 230-V_{AC}, 3.35 A CC Load

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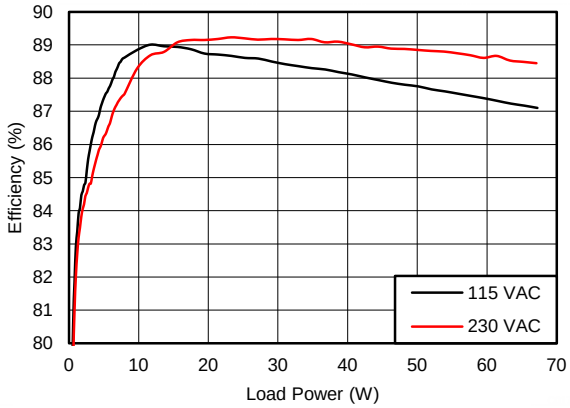

Figure 53. Efficiency vs. Load/Line (cable drop included)

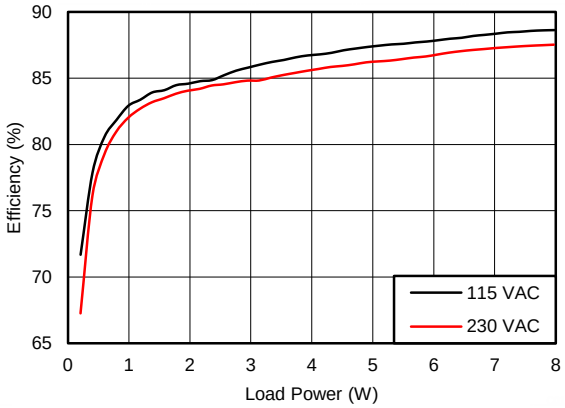

Figure 54. Zoom Light-Load Efficiency vs. Load/Line (cable drop included)

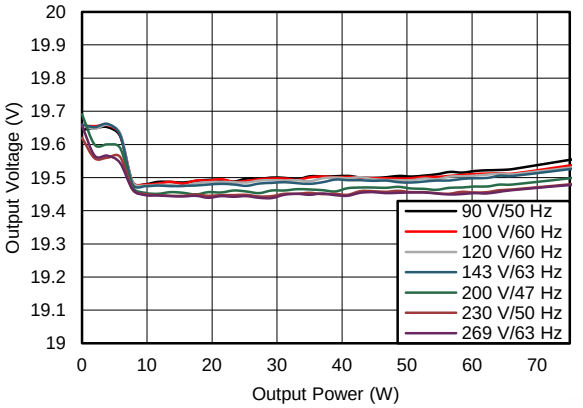

Figure 55. Output Voltage Regulation vs. Line/Load (without cable drop)

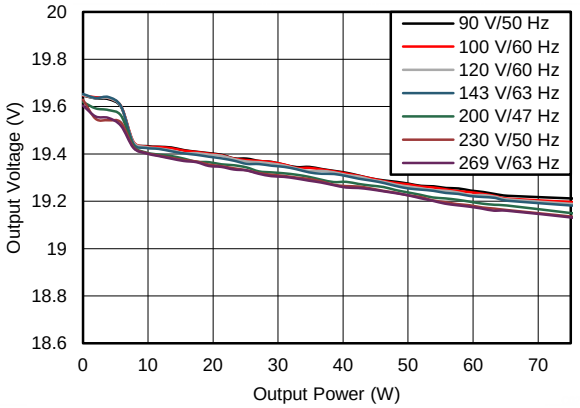

Figure 56. Output Voltage Regulation vs. Line/Load (with cable drop included)

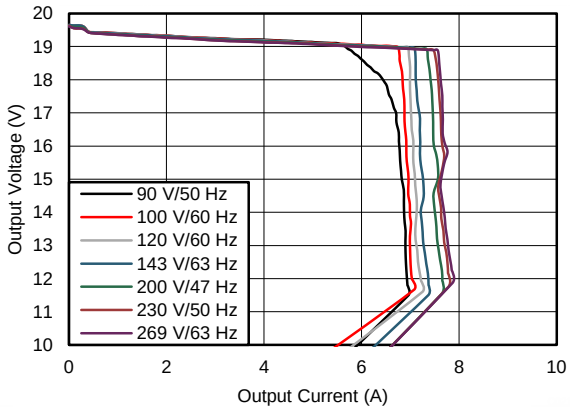

Figure 57. CC Mode Regulation vs. Line

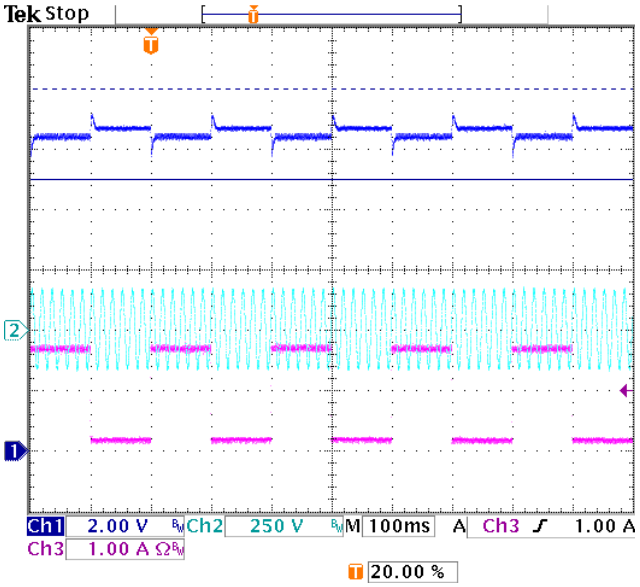

Figure 58. Transient Step 5% to 50% Load, 115 V_{AC}

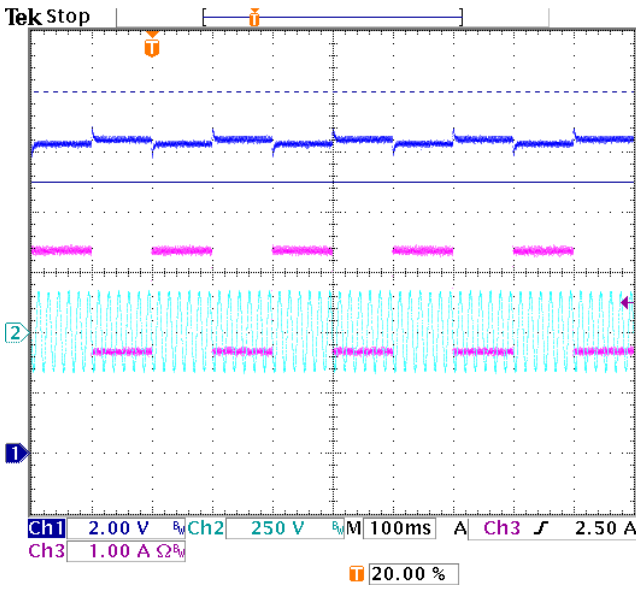

Figure 59. Transient Step 50% to 100% Load, 115 V_{AC}

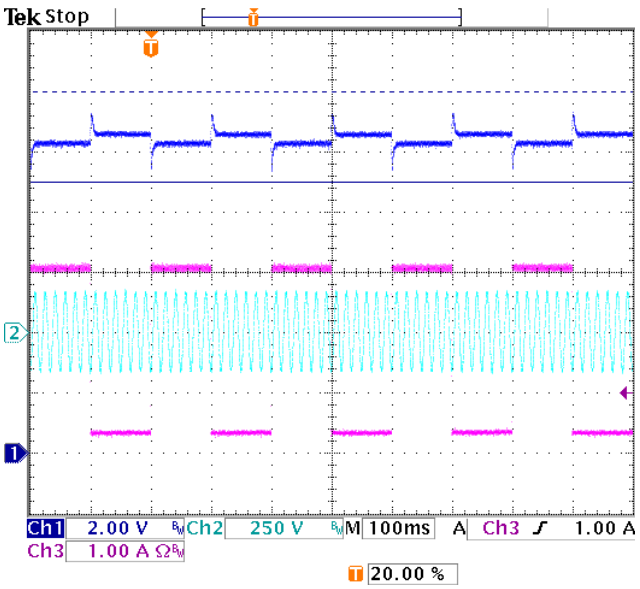

Figure 60. Transient Step 10% to 90% Load, 115 V_{AC}

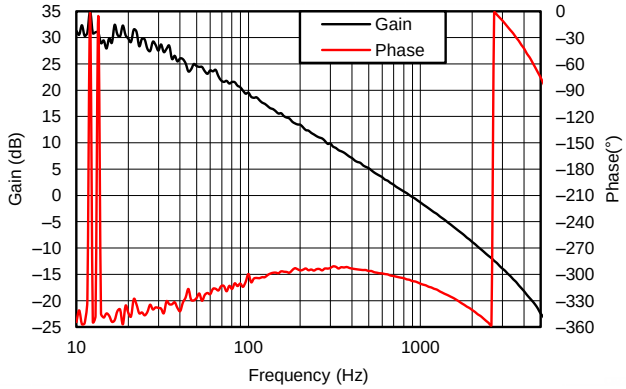

Figure 61. Measured Control Loop Gain/Phase at 300 V_{DC}, Full Load 3.35 A

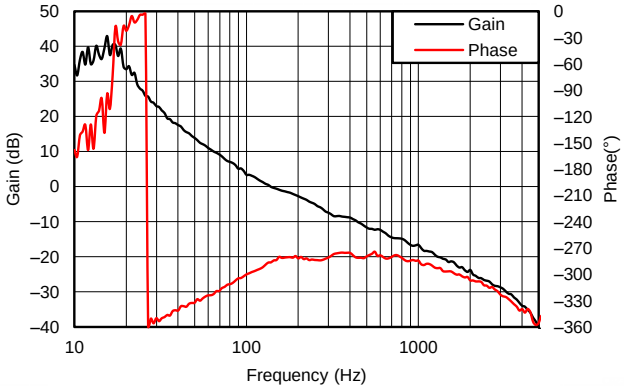

Figure 62. Measured Control Loop Gain/Phase at 300 V_{DC}, Light Load 0.2 A

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9.3 Dos and Don'ts

9.3.1 Test and Debug Recommendations

One important precaution must be noted during test and debug. Do not probe the VSENSE pin with an oscilloscope probe, meter or differential probe. Doing so adds excessive capacitance to the pin, delaying the pin rise-time, and causing the regulated system output voltage to increase.

10 Power Supply Recommendations

The VDD power pin for the device requires the placement of low-esr noise-decoupling capacitance as directly as possible from the VDD pin to the GND pin. Ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better. Depending on the operating temperature range of the application, X5R may be acceptable, but the drop in capacitance value at high temperature and with applied DC-bias may not be tolerable. Avoid dielectrics with poor temperature-stability. (such Y5V, Z5U)

The recommended decoupling capacitors are a 1-μF 1206-sized 50-V X7R capacitor, ideally with (but not essential) a second smaller parallel 100-nF 0603-sized 50-V X7R capacitor. Higher voltage rating parts can also be used. The use of 25-V rated parts is not recommended, due to the reduction in effective capacitance value with applied DC bias.

In parallel with the ceramic noise-decoupling capacitor(s), a larger-capacitance energy storage capacitor is also required, per Equation 58. This energy-storage capacitor does not require low esr, and does not necessarily need to be located close to the device.

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11 Layout

11.1 Layout Guidelines

11.1.1 HV Pin

- This pin is connected to the rectified AC input, and as such requires appropriate separation to other PCB traces to meet the application requirements for functional isolation;
- This pin must have 200 kΩ of external resistance to allow the line voltage to be sensed for the X-capacitor discharge block. At least two series resistors should be used to reduce the voltage across the pins of each resistor, with each resistor rated for at least 200 V;
- The connection to the resistors that feed the HV pin should have separate dedicated rectifying diodes from the AC input lines, to avoid the DC filtering that the bulk capacitor provides after the main diode bridge; the lower section of the main diode bridge can be shared by the device and the power stage;
- A filtering or noise-decoupling capacitor is not recommended, such a capacitor will degrade the X-capacitor sampling ability to distinguish AC from DC input.

11.1.2 VDD Pin

- A 1-µF ceramic decoupling capacitor is recommended, placed as close as possible between the VDD pin and GND, tracked directly to both pins.

11.1.3 VSENSE Pin

- The tracking and layout of the VSENSE pin and connecting components is critical to minimizing noise pick-up and interference in the magnetic sensing block. (See Figure 63 for suggested component placement and tracking). Reduce the total surface area of traces on the VSENSE net to a minimum.
- Because the resistance values of R_A and R_B are relatively high to minimize power dissipation, the high impedance makes the VSENSE pin potentially noise-sensitive. To minimize noise pick-up, locate resistors R_A and R_B as close as possible to the VSENSE pin, with R_B in particular placed as directly as possible between VSENSE and GND pins;
- Depending on layout, a small noise filter capacitor may be useful on the VSENSE pin, such as C15 shown in Figure 44. Connect this capacitor as directly as possible between the VSENSE and GND pins. Choose the value of this capacitor as small as possible, and no greater than 10 pF. A larger value significantly delays the voltage rise-time at the pin, and affects the regulation set-point;
- In case of possible board faults that can pull the VSENSE pin below GND (such as R7 shorted), in order to protect the pin and limit possible negative current out of the pin, a series resistor R4 (as shown in Figure 44) and clamping diode from GND are recommended. Maintain the value of R4 between 100 Ω and 500 Ω. A larger value may affect regulation and line sense accuracy.
- For correct line sense operation, the switched pull-up R10 and D4 must be added. The value of R10 must be 3.9 kΩ to match the internal device gain. The switched pull-up diode and the GND clamping diode can be combined into a dual-diode common-cathode package, such as D4 as shown in Figure 44.

11.1.4 CS Pin

- A small, external filter capacitor is recommended on the CS pin. Track the filter capacitor as directly as possible from the CS to GND pin.
- Referring to Figure 44, a series resistor such as R5 is typically connected between the current sensing resistor R16 and the CS pin to form an R-C filter. A filter time constant between 100 ns and 200 ns is recommended. If the filter time constant is made too large, the filtering causes the transformer peak current to exceed the control loop demand level, which affects regulation and standby power. Place resistor R5 as close as possible to the CS pin.
- Reduce the total surface area of traces on the CS net to a minimum.

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Layout Guidelines (continued)

11.1.5 SD Pin

- Referring to Figure 44, the SD pin is connected to a temperature-sensing NTC RT1 in series with an adjust resistor R6. The NTC can be tracked to the required hot-spot location, or it can be wired with flying leads to the required hotspot.
- Track the RT1 return to GND as directly as possible back to the GND pin of the device. RT1 should not be connected to a power GND track or plane, in order to minimize error in the trip level.
- The device internally filters the SD pin, so an external filter capacitor is not usually required. If the application design requires an external capacitor, limit the value to 1 nF maximum.

11.1.6 DRV Pin

- The DRV pin has high internal sink/source current capability. An external gate resistor is recommended. The value depends on the choice of power MOSFET, efficiency and EMI considerations.
- As shown in Figure 44 an anti-parallel path formed by D5 and R13 are placed across the gate resistor R11 to allow turn-on and turn-off of the MOSFET to be independently adjusted.
- A pull-down resistor (such as R15 in this example) on the gate of the external MOSFET is recommended to prevent the MOSFET gate from floating on if there is an open circuit error in the gate drive path. The value of R15 also affects the overload timer settings, so carefully choose the value of R15 according to Table 1.
- Ensure that the noisy gate drive traces are routed away from the sensitive VSENSE pin and CS pin traces.

11.1.7 GND Pin

- Connect decoupling and noise filter capacitors, as well as sensing resistors directly to the GND pin in a star-point fashion, ensuring that the current-carrying power tracks (such as the gate drive return) are track separately to avoid noise and ground-drops that could affect the analogue signal integrity.

11.2 Layout Example

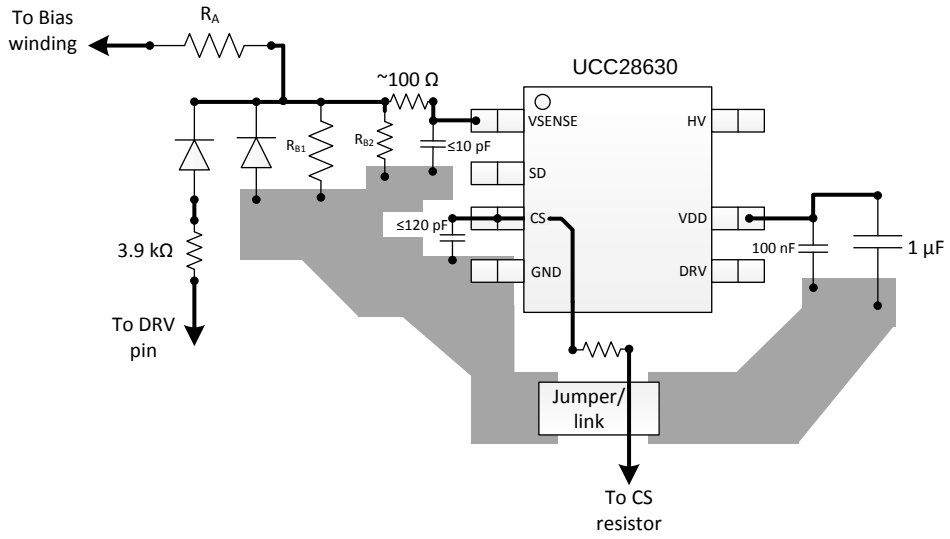

Figure 63. Recommended PCB Layout for Single-Sided Assembly

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC2863x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

UCC28630EVM-572, 65-W Nominal, 130-W Peak, Primary-Side Regulated Adapter Module (Texas Instruments Literature Number SLUSAX9)

12.2.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC28630	Click here	Click here	Click here	Click here	Click here
UCC28631	Click here	Click here	Click here	Click here	Click here
UCC28632	Click here	Click here	Click here	Click here	Click here
UCC28633	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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Community Resources (continued)

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28630D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28630	Samples
UCC28630DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28630	Samples
UCC28631D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28631	Samples
UCC28631DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28631	Samples
UCC28632D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28632	Samples
UCC28632DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28632	Samples
UCC28633D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28633	Samples
UCC28633DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28633	Samples
UCC28634D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28634	Samples
UCC28634DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28634	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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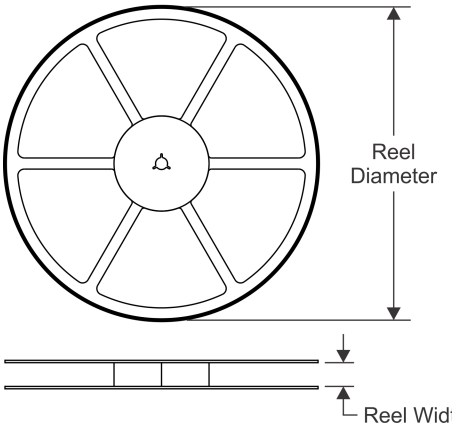
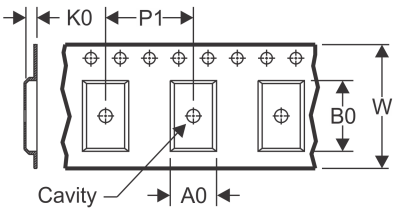
TAPE AND REEL INFORMATION

REEL DIMENSIONS

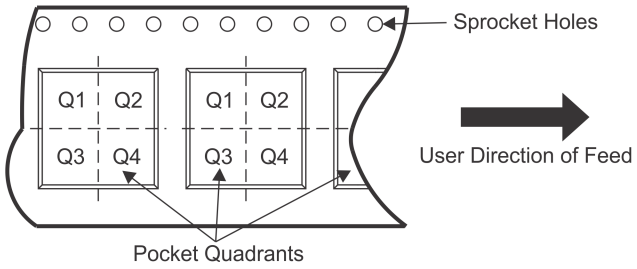


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

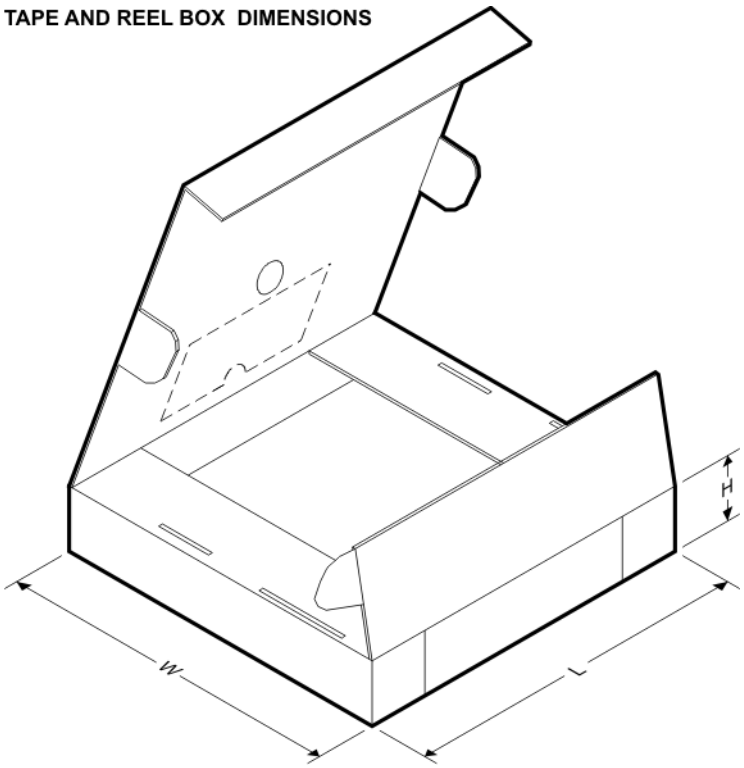
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

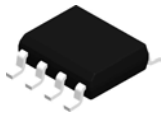
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28630DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28631DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28632DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28633DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28634DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28630DR	SOIC	D	7	2500	367.0	367.0	35.0
UCC28631DR	SOIC	D	7	2500	367.0	367.0	35.0
UCC28632DR	SOIC	D	7	2500	367.0	367.0	35.0
UCC28633DR	SOIC	D	7	2500	367.0	367.0	35.0
UCC28634DR	SOIC	D	7	2500	367.0	367.0	35.0

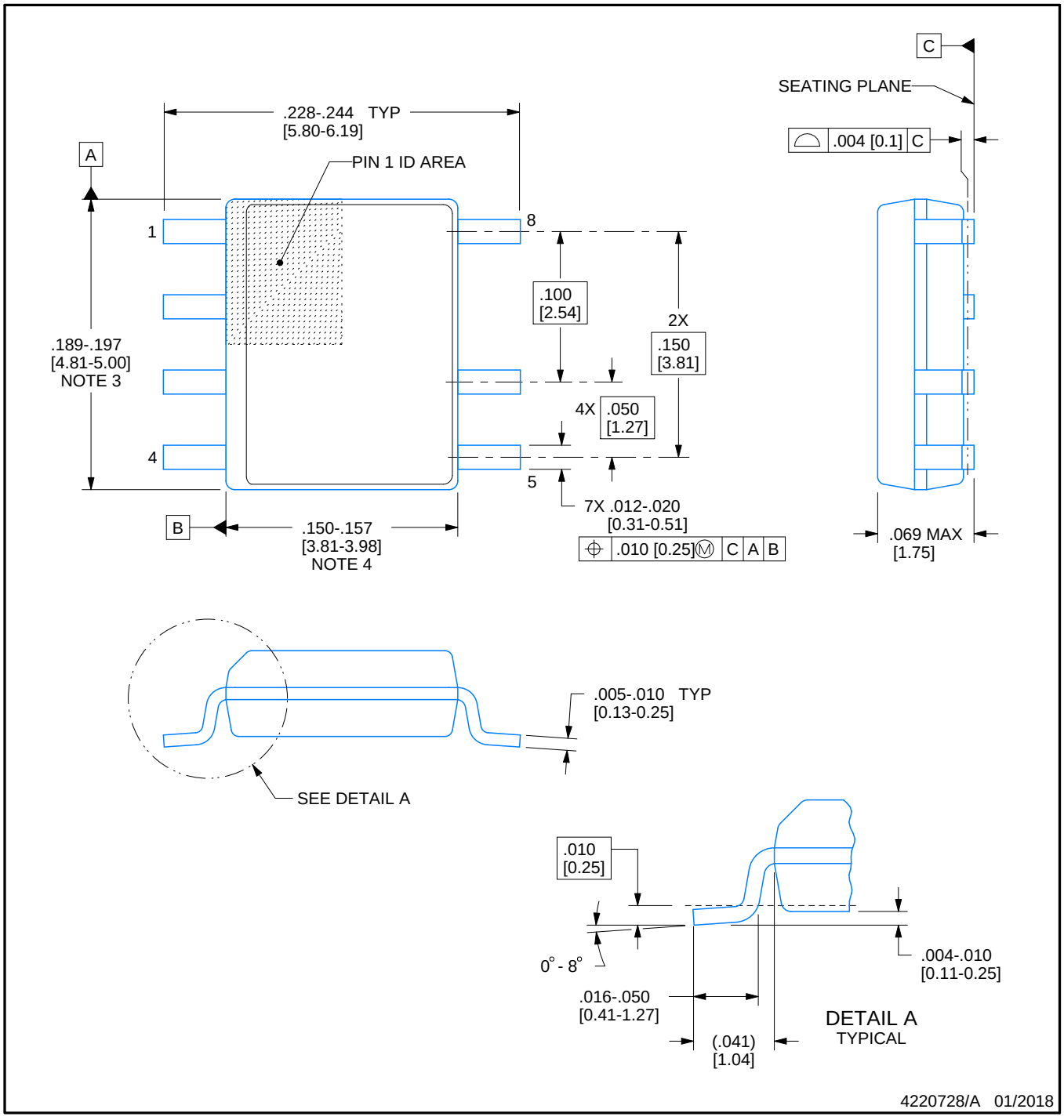


PACKAGE OUTLINE

D0007A

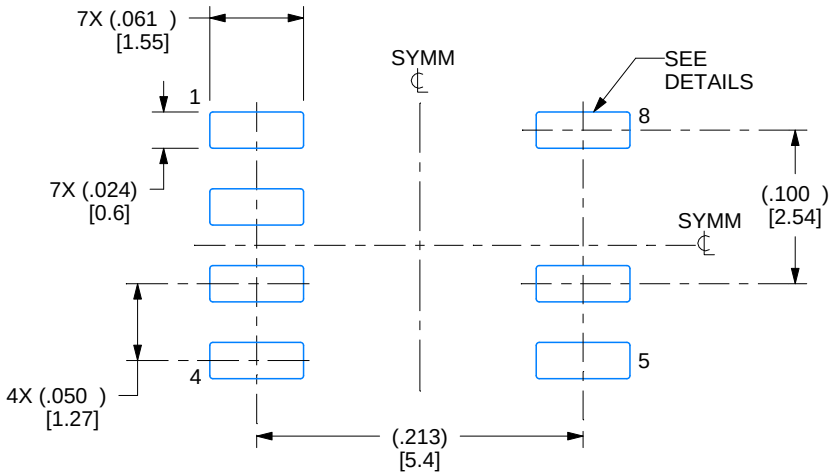
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

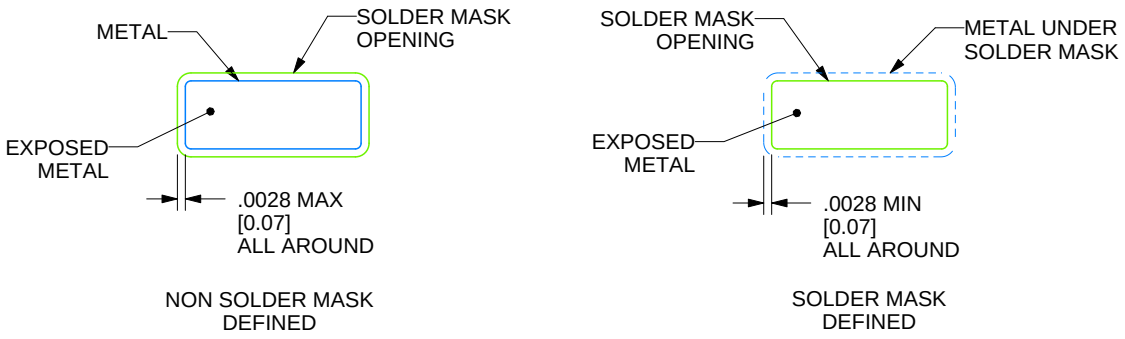


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

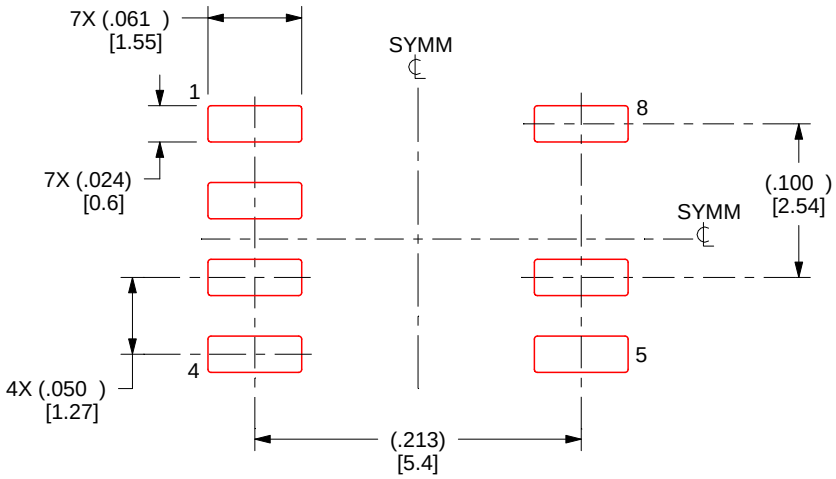
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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