ON Semiconductor®

FSA2259 Low-Voltage, Dual-SPDT (0.8Ω) Analog Switch with 16kV ESD

Features

- 0.8Ω Typical On Resistance (R_{ON}) for +3.0V Supply
- 0.40Ω Maximum R_{ON} Flatness for +3.0V Supply
- -3db Bandwidth: > 50MHz
- Low I_{CCT} Current Over an Expanded Control Input Range
- Packaged in 10-Lead UMLP (1.4 x 1.8mm)
- Power-Off Protection on Common Ports
- Broad V_{CC} Operating Range: 1.65 to 4.4V
- ESD HBM JEDEC: JESD22-A114
  - I/O to GND: 8.5kV
  - Power to GND: 16.0kV

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

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October-2017, Rev. 2

Publication Order Number:
FSA2259UMX/D

Description

The FSA2259 is a high-performance, dual, Single Pole Double Throw (SPDT) analog switch that features low R_{ON} of 0.8Ω (typical) at 3.0V V_{CC}. The FSA2259 operates over a wide V_{CC} range of 1.65V to 4.4V and is designed for break-before-make operation. The select input is TTL-level compatible.

The FSA2259 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature suits mobile handset applications by allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

rdering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA2259UMX	JT	-40 to +85°C	10-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm

Analog Symbol

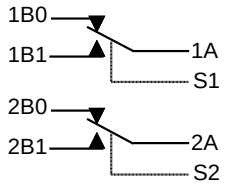


Figure 1. FSA2259

Pin Configuration

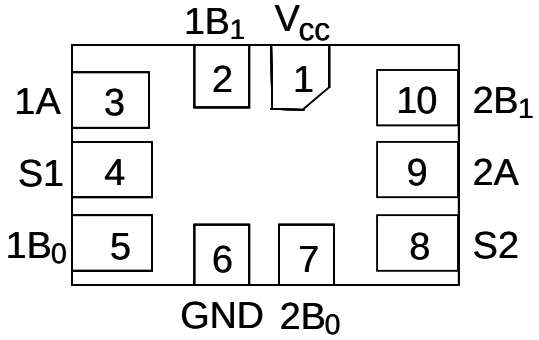


Figure 2. 10-Pin UMLP (Top Through View)

Pin Description

Pin#	Name	Description
1	V_{CC}	Supply Voltage
2	$1B_1$	Data Ports
3	1A	Data Ports
4	S1	Switch Select Pins
5	$1B_0$	Data Ports
6	GND	Ground
7	$2B_0$	Data Ports
8	S2	Switch Select Pins
9	2A	Data Ports
10	$2B_1$	Data Ports

Truth Table

Control Input, Sn	Function
LOW Logic Level	nB0 Connected to nA
HIGH Logic Level	nB1 Connected to nA

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	5.5	V
V_{SW}	Switch I/O Voltage[1]	1B0, 1B1, 2B0, 2B1, 1A, 2A Pins	-0.5	V_{CC} + 0.3	V
V_{IN}	Control Input Voltage[1]	S1, S2	-0.5	5.5	V
I_{IK}	Input Clamp Diode Current			-50	mA
I_{SW}	Switch I/O Current (Continuous)			350	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			500	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)			+260	°C
ESD	Human Body Model, JEDEC: JESD22-A114	I/O to GND		8.5	kV
		Power to GND		16.0	
		All Other Pins		8.0	
	Charged Device Model, JEDEC: JESD22-C101			2.0	kV

Note:

1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	1.65	4.40	V
V_{IN}	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			T_A=-40 to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Control Input Voltage High		3.60 to 4.30				1.7		V
			2.70 to 3.60				1.5		
			2.30 to 2.70				1.4		
			1.65 to 1.95				0.9		
V_{IL}	Control Input Voltage Low		3.60 to 4.30					0.7	V
			2.70 to 3.60					0.5	
			2.30 to 2.70					0.4	
			1.65 to 1.95					0.4	
I_{IN}	Control Input Leakage (S1,S2)	V_{IN}=0 to V_{CC}	1.65 to 4.30				-0.5	0.5	µA
$I_{NO(0FF)}$, $I_{NC(OFF)}$	Off Leakage Current of Port nB0 and nB1	nA=0.3V, V_{CC}–0.3V nB0 or nB1=V_{CC}-0.3V, 0.3V, or Floating Figure 4	1.95 to 4.30	-10		10	-50	50	nA
$I_{A(ON)}$	On Leakage Current of Port nA	nA=0.3V, V_{CC}–0.3V nB0 or nB1=V_{CC}-0.3V, 0.3V, or Floating Figure 5	1.95 to 4.30	-20		20	-100	100	nA
I_{OFF}	Power-Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A), V_{IN}=0V to 4.3V, V_{CC}=0V nB0, nB1=Floating	0V					±1	µA
R_{ON}	Switch On Resistance[2,5]	I_{ON}=100mA, nB0 or nB1=0.7V, 3.6V Figure 3	4.30		0.50			1.00	Ω
		I_{ON}=100mA, nB0 or nB1=0.7V, 2.3V Figure 3	3.00		0.80			1.20	
		I_{ON}=100mA, nB0 or nB1=0V, 0.7V, 1.6V, 2.3V Figure 3	2.30		1.10				
		I_{ON}=100mA, nB0 or nB1=0V, 0.7V, 1.65V Figure 3	1.65		1.50				
ΔR_{ON}	On Resistance Matching Between Channels[3,5]	I_{ON}=100mA, nB0 or nB1=0.7V	4.30		0.08			0.25	Ω
			3.00		0.20			0.25	
			2.30		0.40				
			1.65		0.50				
$R_{FLAT(ON)}$	On Resistance Flatness[4,5]	I_{OUT}=100mA, nB0 or nB1=0V to V_{CC}	4.30					0.4	Ω
			3.00					0.4	
			2.30		0.9				
			1.65		1.2				
I_{CC}	Quiescent Supply Current	V_{IN}=0 or V_{CC}, I_{OUT}=0	4.30	-100		100	-500	500	nA
I_{CCT}	Increase in I_{CC} per Input	Input at 2.6V	4.30		3			7	µA
		Input at 1.8V			7			15	

Notes:

2. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
3. $\Delta R_{ON}=R_{ON\ max} – R_{ON\ min}$ measured at identical V_{CC}, temperature, and voltage.
4. Flatness is defined as the difference between the maximum and minimum value of on resistance (R_{ON}) over the specified range of conditions.
5. Guaranteed by characterization, not production tested for V_{CC}=1.65 – 3.0V.

AC Electrical Characteristics

All typical value are for V_{CC}=3.3V at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			T_A=-40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time	nB0 or nB1=1.5V, R_L=50Ω, C_L=35pF	3.60 to 4.30			55		60	ns	Figure 6 Figure 7
			2.70 to 3.60			60		65		
			2.30 to 2.70			65		70		
			1.65 to 1.95		70					
t_{OFF}	Turn-Off Time	nB0 or nB1=1.5V, R_L=50Ω, C_L=35pF	3.60 to 4.30			30	5	35	ns	
			2.70 to 3.60			35	5	40		
			2.30 to 2.70			40	5	45		
			1.65 to 1.95		40					
t_{BBM}	Break-Before-Make Time[6]	nB0 or nB1=1.5V, R_L=50Ω, C_L=35pF	3.60 to 4.30		15		2		ns	Figure 8
			2.70 to 3.60		15		2			
			2.30 to 2.70		15		2			
			1.65 to 1.95		16		2			
Q	Charge Injection[6]	C_L=1.0nF, V_S=0V, R_S=0Ω	1.65 to 4.30		25				pC	Figure 12
OIRR	Off Isolation[6]	f=100kHz, R_L=50Ω, C_L=0pF	1.65 to 4.30		-80				dB	Figure 10
Xtalk	Crosstalk[6]	f=100kHz, R_L=50Ω, C_L=0pF	1.65 to 4.30		-100				dB	Figure 11
BW	-3db Bandwidth[6]	R_L=50Ω, C_L=0pF	1.65 to 4.30		>50				MHz	Figure 9
THD+N	Total Harmonic Distortion + Noise[6]	f=20Hz to 20kHz, R_L=32Ω, V_{IN}=2V_{pp}	1.65 to 4.30		.06				%	Figure 15

Notes:

6. Guaranteed by characterization, not production tested

Capacitance

All capacitance specifications are guaranteed by characterization and are not production tested.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			Unit	Figure
				Min.	Typ.	Max.		
C_{IN}	Control Pin Input Capacitance	f=1MHz	0		1.5		pF	Figure 13
C_{OFF}	B Port Off Capacitance	f=1MHz	3.3		30		pF	Figure 13
C_{ON}	A Port On Capacitance	f=1MHz	3.3		50		pF	Figure 14

Test Diagrams

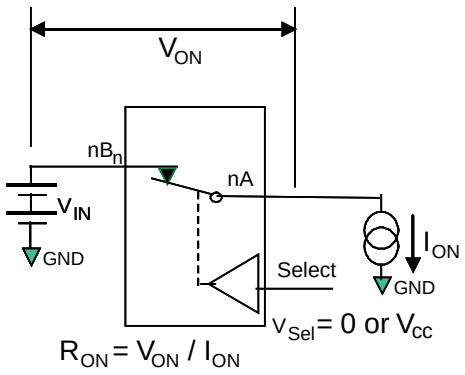
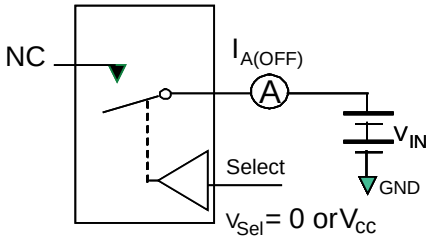


Figure 3. On Resistance



**Each switch port is tested separately.

Figure 4. Off Leakage (Ports Tested Separately)

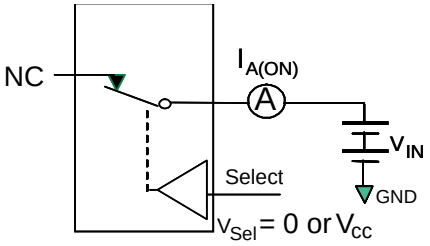


Figure 5. On Leakage

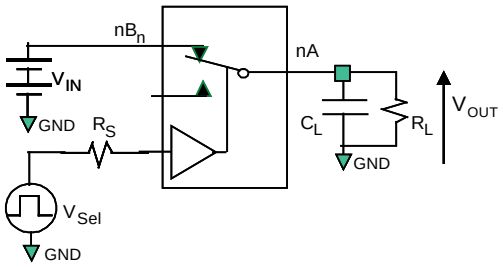


Figure 6. Test Circuit Load

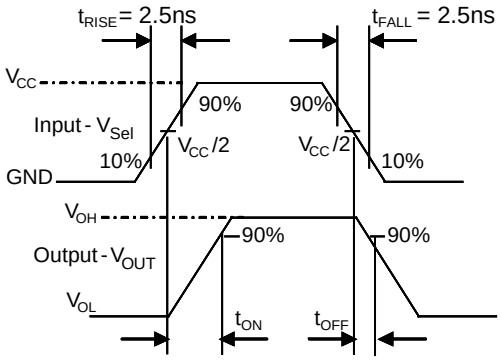
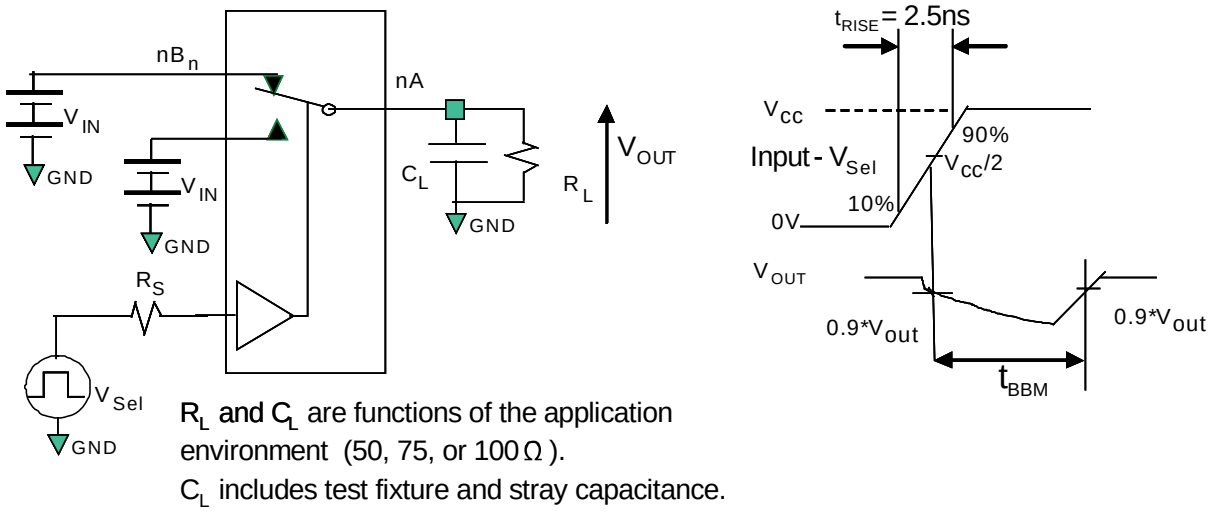


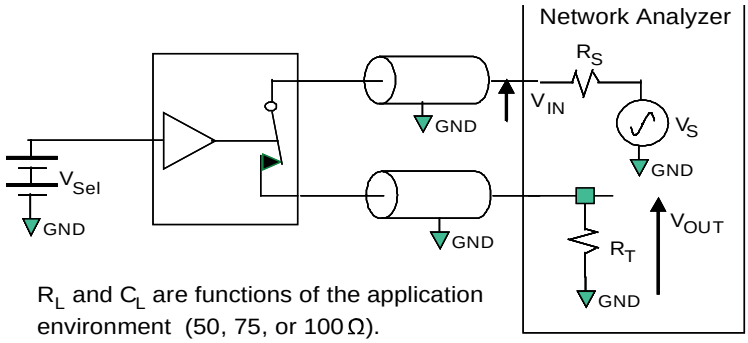
Figure 7. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)



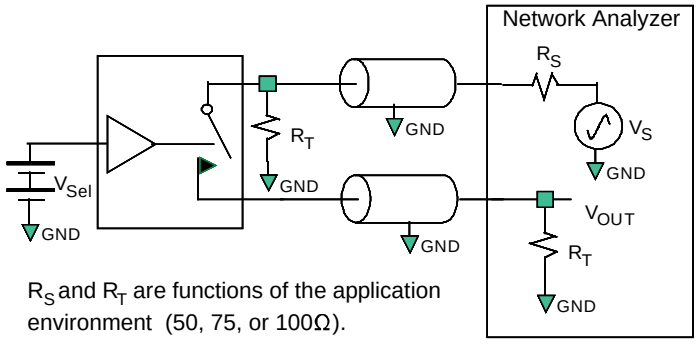
R_L and C_L are functions of the application environment (50, 75, or 100 Ω).
C_L includes test fixture and stray capacitance.

Figure 8. Break-Before-Make Interval Timing



R_L and C_L are functions of the application environment (50, 75, or 100 Ω).
C_L includes test fixture and stray capacitance.

Figure 9. Bandwidth

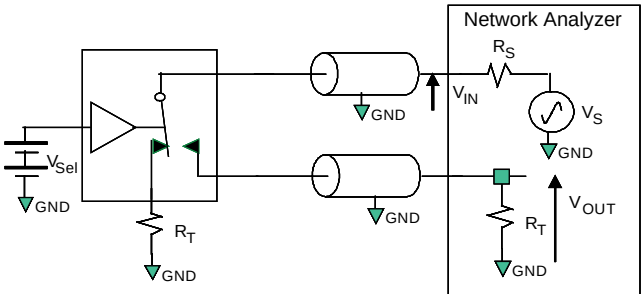


R_S and R_T are functions of the application environment (50, 75, or 100Ω).

Off-Isolation = 20 Log (V_{OUT} / V_{IN})

Figure 10. Channel Off Isolation

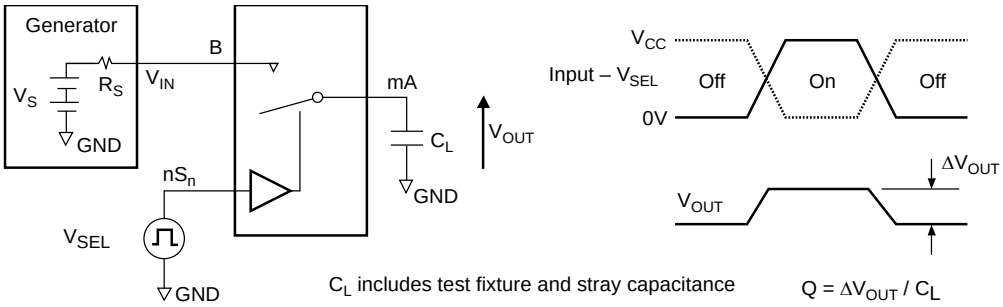
Test Diagrams (Continued)



R_S and R_T are functions of the application environment (50, 75, or 100Ω).

CROSSTALK = 20 Log (V_{OUT}/ V_{IN})

Figure 11. Adjacent Channel Crosstalk



C_L includes test fixture and stray capacitance

$Q = \Delta V_{OUT} / C_L$

Figure 12. Charge Injection Test

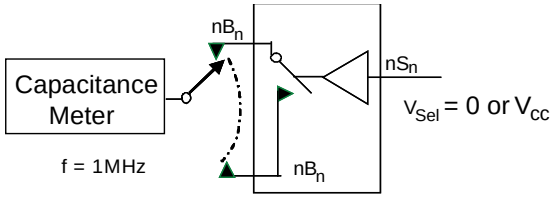


Figure 13. Channel Off Capacitance

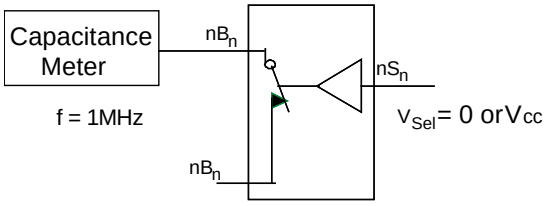
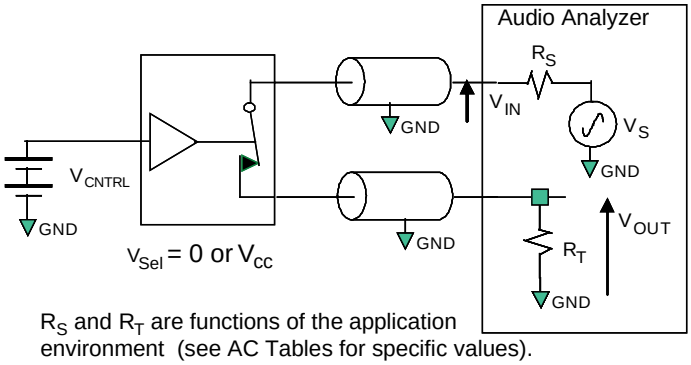


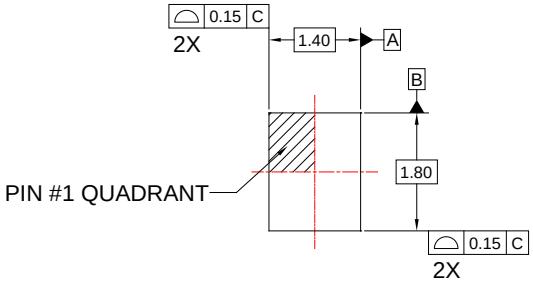
Figure 14. Channel On Capacitance



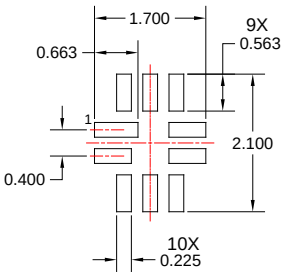
R_S and R_T are functions of the application environment (see AC Tables for specific values).

Figure 15. Total Harmonic Distortion

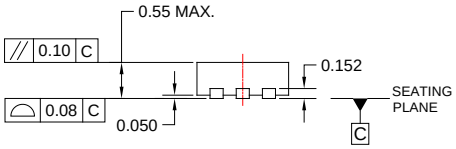
Physical Dimensions



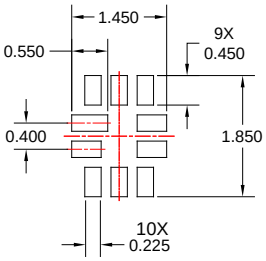
TOP VIEW



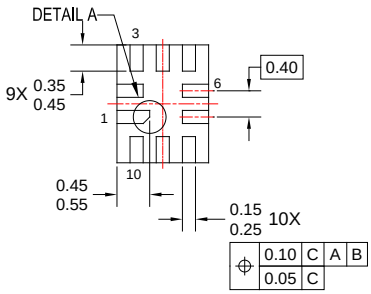
RECOMMENDED LAND PATTERN



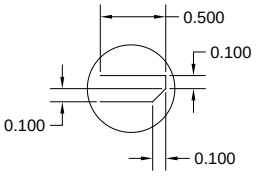
SIDE VIEW



OPTIONAL MINIMIAL TOE LAND PATTERN



BOTTOM VIEW



DETAIL A
PIN #1 TERMINAL
SCALE: 2X

NOTES:

A. DIMENSIONS ARE IN MILLIMETERS.

B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

C. DRAWING FILENAME: UMLP10Arev2

Figure 16. 10-Lead Quad Ultrathin Molded Leadless Package (UMLP)

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