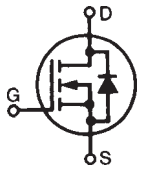
HiPerFET™ MOSFET ISOPLUS220™

IXFC13N50

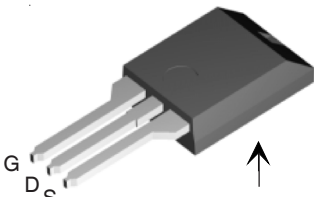
Electrically Isolated Back Surface

N-Channel Enhancement Mode
High dv/dt, Low t_{rr}, HDMOS™ Family

V_{DSS} = 500 V
I_{D25} = 12 A
$R_{DS(on)}$ = 0.4 Ω
t_{rr} ≤ 250 ns



ISOPLUS 220™



Isolated back surface*

G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	500	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	12	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	48	A
I_{AR}	T_C = 25°C	13	A
E_{AR}	T_C = 25°C	18	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 2 Ω	5	V/ns
P_D	T_C = 25°C	140	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
Weight		3	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA		500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 2.5 mA		2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = 0.8 \bullet V_{DSS}$	T_J = 25°C			200	μA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$ Notes 1, 2				0.4	Ω

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<35pF)
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages

- Easy assembly: no screws or isolation foils required
- Space savings
- High power density
- Low collector capacitance to ground (low EMI)

See IXFH13N50 data sheet for characteristic curves

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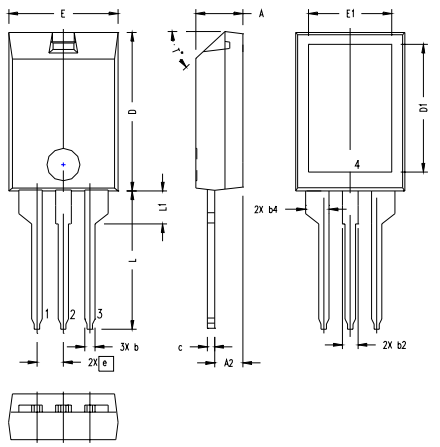
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0; I_T Notes 1, 2	7.5	9.0		S
C_{iss}			2800		pF
C_{oss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		300		pF
C_{rss}			70		pF
$t_{d(on)}$			18	30	ns
t_r	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS},		27	40	ns
$t_{d(off)}$	I_D = 0.5 • I_{D25}, R_G = 4.7 Ω (External)		76	100	ns
t_f			32	60	ns
$Q_{g(on)}$			110	120	nC
Q_{gs}	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = I_T		15	25	nC
Q_{gd}			40	50	nC
R_{thJC}				0.90	K/W
R_{thCK}			0.30		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V			13	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			52	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = I_S, -di/dt = 100 A/µs, V_R = 100 V; T_J = 25°C			250	ns
	T_J = 125°C			350	ns
Q_{RM}	T_J = 25°C		0.6		µC
	T_J = 125°C		1.25		µC
I_{RM}	T_J = 25°C		9		A
	T_J = 125°C		15		A

Note: 1. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %
2. I_T test current: I_T = 6.5A
3. See IXFH13N50 data sheet for characteristic curves.

ISOPLUS220 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T°			42.5°	47.5°

NOTE:
1. Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
2. This drawing will meet dimensional requirement of JEDEC SS Product Outline TO-273 except D and D1 dimension.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343