NCP3136

Integrated Synchronous Buck Converter

6 A

NCP3136 is a fully integrated synchronous buck converter for 3.3 V and 5 V step−down applications. It can provide up to 6.5 A instantaneous current. NCP3136 supports high efficiency, fast transient response and provides power good indicator. The control scheme includes two operation modes: FCCM and automatic CCM/DCM. In automatic CCM/DCM mode, the controller can smoothly switch between CCM and DCM, where converter runs at reduced switching frequency with much higher efficiency. NCP3136 is available in 3 mm x 3 mm QFN16 pin package.

Features

- High Efficiency in Both CCM and DCM
- Operation Frequency: 1.1 MHz
- Support MLCC Output Capacitor
- Small Footprint, 3 mm x 3 mm, 16−pin QFN Package
- 2.9 V to 5.5 V Wide Conversion Voltage Range
- Output Voltage Range from 0.6 V to 0.84 X V_{IN}
- Automatic Power−Saving Mode
- Voltage Mode Control
- Support Pre−bias Start−up Functionality
- Output Discharge Operation
- Over−Temperature Protection
- Built−in Over−Voltage, Under−Voltage and Over−Current Protection
- Power Good Indicator
- This Device is Pb−Free and is RoHS Compliant

Applications

- 5 V Step Down Rail
- 3.3 V Step Down Rail

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QFN16
CASE 485DA

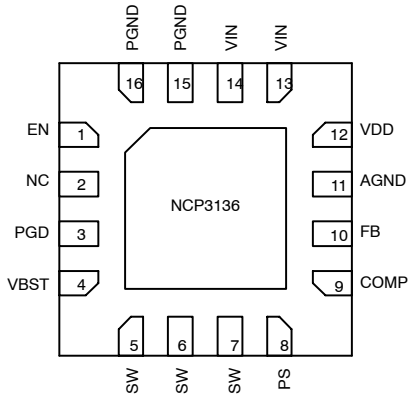
MARKING DIAGRAM



3136	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCP3136MNTXG	QFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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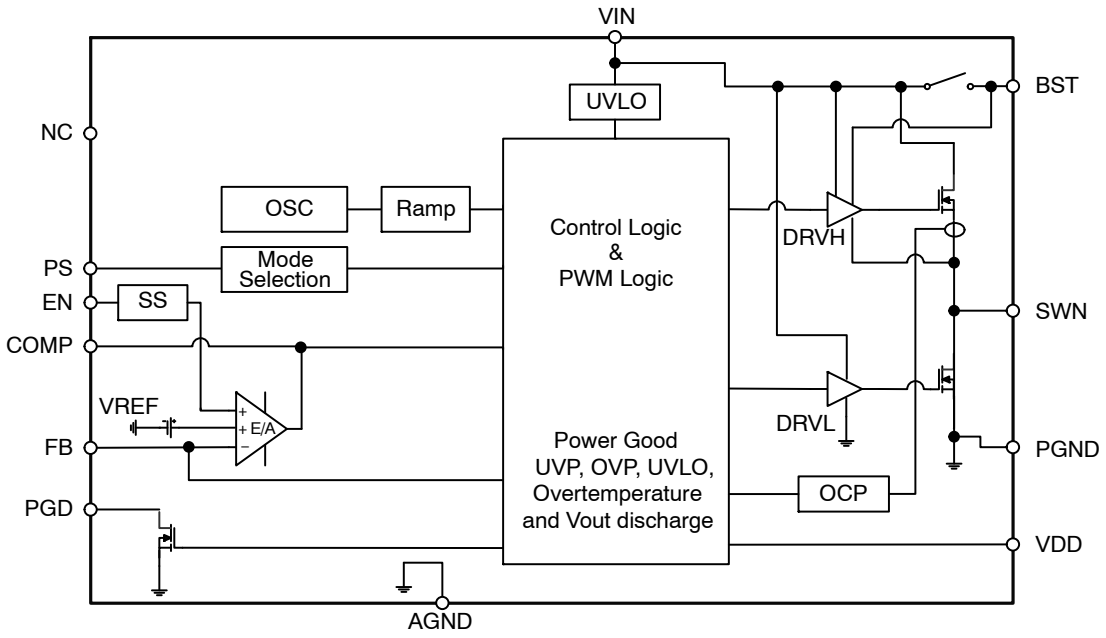


Figure 1. Block Diagram

PIN DESCRIPTION

Pin No.	Symbol	Description
1	EN	Logic control to enabling the switcher. Internally pulled up to VDD with a 1.35 MΩ resistor.
2	NC	Not connected.
3	PGD	Open drain power good output.
4	BST	Gate drive voltage for high side FET. Connect capacitor from this pin to SWN.
5,6,7	SWN	Switch node between high−side MOSFET and low−side MOSFET.
8	PS	Mode configuration pin: Connecting to ground: Forced CCM Pulled high or floating (internal pulled high): Forced CCM Connect with 24.3 kΩ to GND: Automatic CCM/DCM Connect with 57.6 kΩ to GND: Automatic CCM/DCM Connect with 105 kΩ to GND: Automatic CCM/DCM Connect with 174 kΩ to GND: Automatic CCM/DCM
9	COMP	Output of the error amplifier.
10	FB	Feedback pin. Connect to resistor divider to set up the desired output voltage.
11	AGND	Analog ground
12	VDD	Power supply input for control circuitry.
13,14	VIN	Power input for power conversion and gate driver supply.
15,16	PGND	Power ground

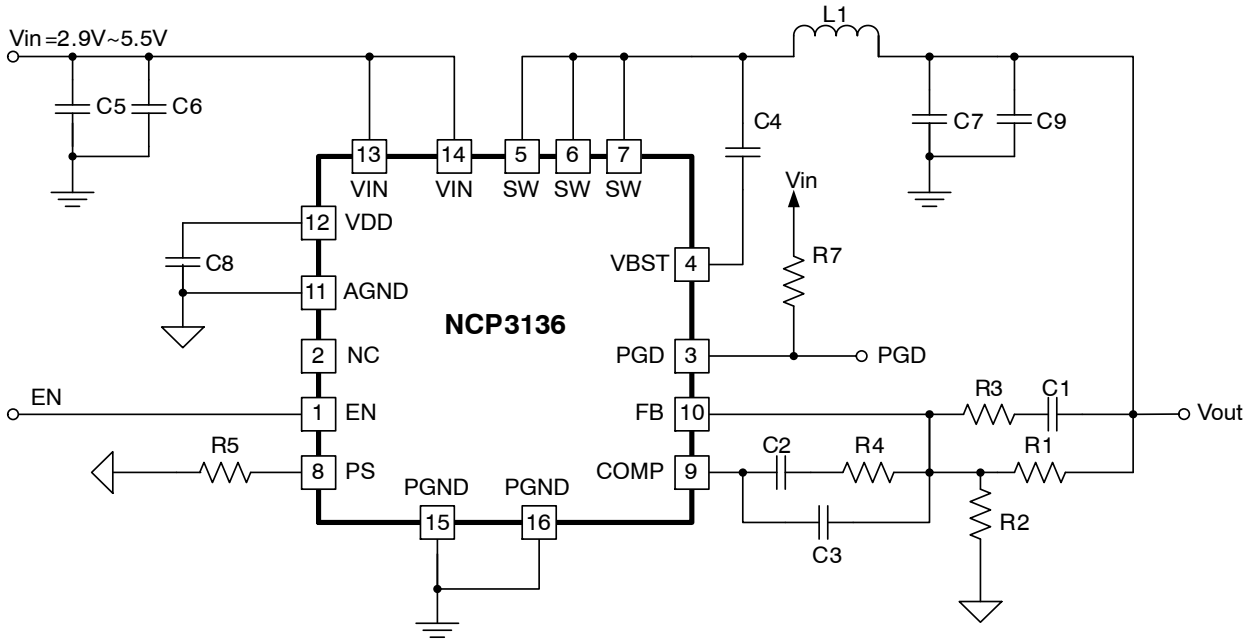


Figure 2. Application Circuit

ABSOLUTE MAXIMUM RATINGS

Parameter	Condition		Value Min	Value Max	Unit
Input Voltage Range	VIN, PS		−0.3	6.5	V
	VBST		−0.3	17	
	VBST (with respect to SW)		−0.3	6.5	
	EN, FB		−0.3	VDD + 0.3	
Output Voltage Range	SW	DC	−1	6.5	V
		Pulse < 20 ns, E = 5 μJ	−3	10	
	PGD		−0.3	6.5	
	COMP		−0.3	VDD + 0.3	
	PGND		−0.3	0.3	
Operation ambient temperature	T_A		−40	125	°C
Storage temperature	T_S		−55	150	
Junction temperature	T_J		−40	150	
Thermal Characteristics	$R_{\theta JA}$		45.4		°C/W
Electrostatic Discharge	Human Body Model (HBM)		2000		V
	Charged Device Model (CDM)		2000		
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATION RATINGS

Parameter	Condition	Value Min	Value Typ	Value Max	Unit
Input Voltage Range	VIN	2.9		5.5	V
	VBST	−0.1		13.5	
	VBST (with respect to SW)	−0.1		6.0	
	EN, PS, FB	−0.1		VDD	
Output Voltage Range	VDD	2.9		5.5	V
	SW	−1		6.5	
	PGD	−0.1		6.0	
	COMP	−0.1		VDD	
	PGND	−0.1		0.1	
Junction temperature range, T_J		−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{IN} = 3.3 V, T_A = T_J = −40°C to +125°C. Typical values are at T_A = 25°C, PGND = GND unless otherwise noted)

Parameter	SYMBOL	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VIN operation voltage	V_{IN}	Nominal input voltage range	2.9		5.5	V
VIN UVLO threshold		Ramp up; EN = 'HI'		2.8		V
VIN UVLO hysteresis				110		mV
VOLTAGE MONITOR						
Power good low voltage		Pull−down voltage with 4 mA sink current		60	200	mV
Power good high leakage current			−2.0	0	2.0	μA
Power good threshold		Feedback lower voltage limit	80	83	86	%Vref
Power good threshold		Feedback higher voltage limit	114	117	120	%Vref
Power good high delay	$t_{PGDELAY}$			400		μs
Output over-voltage protection threshold at FB			114	117	120	%Vref
Over-voltage blanking time	T_{OVPDLY}	Time from FB higher than 20% of Vref to OVP fault	1.0	1.5	2.5	μs
Output under−voltage protection threshold at FB			80	83	86	%Vref
Under-voltage blanking time	T_{UVPDLY}	Time from FB lower than 20% of Vref to UVP fault		11		μs
SUPPLY CURRENT (T_J = +25°C)						
VIN quiescent current	I_{VIN}	EN = 'HI', no switching		1.5	3.5	mA
VIN shutdown supply current	I_{VIN_SD}	EN = 'LO'			15	μA
FEEDBACK VOLTAGE & ERROR AMPLIFIER						
Reference voltage at FB	V_{REF}		594	600	606	mV
Unity gain bandwidth (Note 1)			14			MHz
Open loop gain (Note 1)			80			dB
FB pin leakage current					100	nA
Output sourcing and sinking current (Note 1)		C_{comp} = 20 pF		5		mA
Slew rate (Note 1)				5		V/μs
OVER CURRENT PROTECTION & ZERO CROSSING						
Over−current limit on high−side FET		When I_{out} exceeds this threshold for 4 consecutive cycles, V_{IN} = 3.3 V, V_{OUT} = 1.5 V with 1 μH inductor, F_{sw} = 1.1 MHz, T_A = 25°C	7.6	8.2	8.8	A
Hiccup time duration	t_{hiccup}	F_{sw} = 1.1 MHz		14.5		ms
Zero crossing comparator internal offset (Note 1)		PGND−SWN, Automatic CCM/DCM mode	−4.5	−3.0	−1.5	mV
LOGIC PINS:I/O VOLTAGE AND CURRENT						
EN high threshold voltage			1.1	1.18	1.30	V
EN hysteresis				0.18	0.24	V
EN input pull up resistor				1.2		MΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{IN} = 3.3 V, T_A = T_J = −40°C to +125°C. Typical values are at T_A = 25°C, PGND = GND unless otherwise noted)

Parameter	SYMBOL	Test Conditions	Min	Typ	Max	Unit
LOGIC PINS:I/O VOLTAGE AND CURRENT						
PS mode threshold voltage	PS_{THS}	Level 1 to Level 2		0.05		V
		Level 2 to Level 3		1.3		
PS source current	I_{PS}	7 μA pull-up current when enabled		7		μA
INTERNAL BST DIODE						
Reverse−bias leakage current		V_{BST} = 6.6 V, V_{IN} = 3.3 V, T_A = 25°C			1	μA
SOFT STOP						
Output discharge on−resistance		EN = 0, V_{IN} = 3.3 V, V_{OUT} = 0.5 V		36		Ω
TIMERS: SOFT−START						
Soft−Start ramp−up time	T_{SS}	Rising from V_{SS} = 0 V to V_{SS} = 0.6 V		1.5		ms
Delay after EN asserting		EN = 'HI'		0.5		ms
Switching Frequency Control		FCCM mode Frequency setting = 1.1 MHz	0.99	1.10	1.21	MHz
PWM						
Minimum OFF time		FCCM mode or Automatic CCM/DCM mode		100	140	ns
PWM ramp amplitude (Note 1)		2.9 V< V_{IN} < 6.0 V		V_{IN}/4		V
Maximum duty cycle, FCCM mode or Automatic CCM/DCM mode		F_{SW} = 1.1 MHz	84%	89%		
THERMAL SHUTDOWN						
Thermal shutdown threshold (Note 1)			130	140	150	°C
Thermal shutdown hysteresis (Note 1)				40		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by design, not production tested.

TYPICAL CHARACTERISTICS

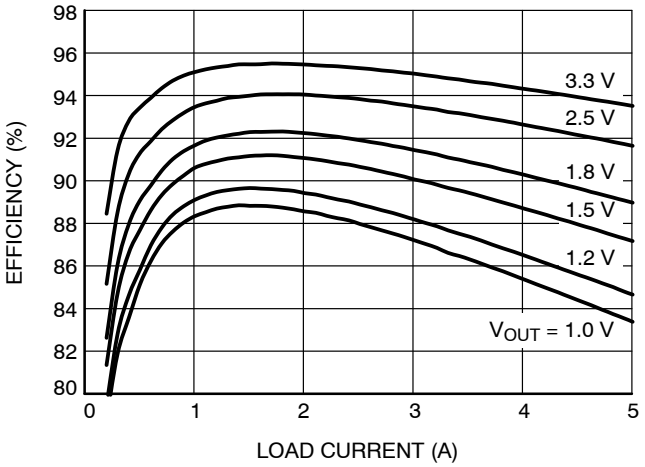


Figure 3. Efficiency at Vin = 5.0 V FCCM Operation Mode

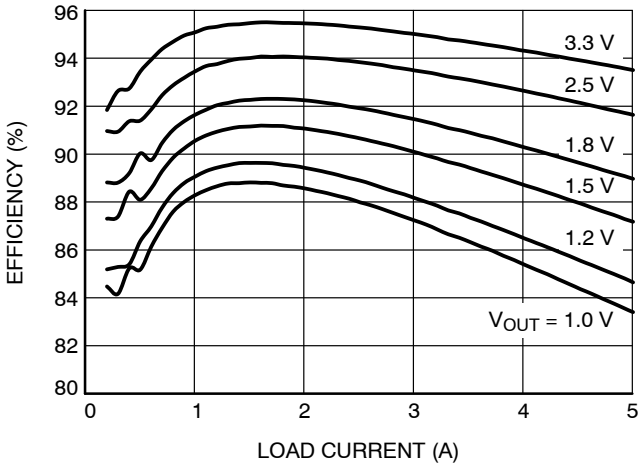


Figure 4. Efficiency at Vin = 5.0 V Auto CCM/DCM Operation Mode

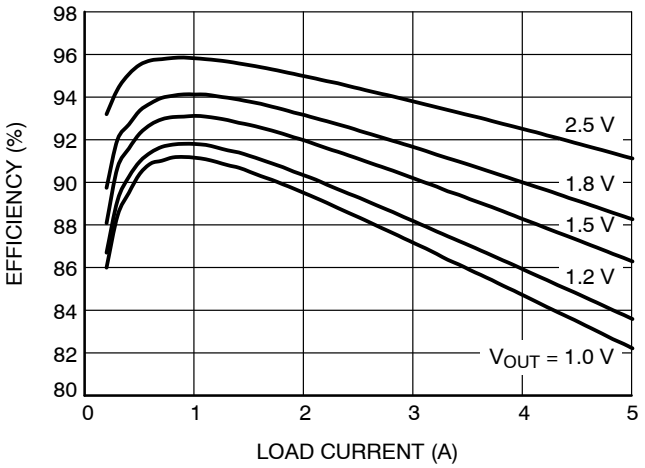


Figure 5. Efficiency at Vin = 3.3 V FCCM Operation Mode

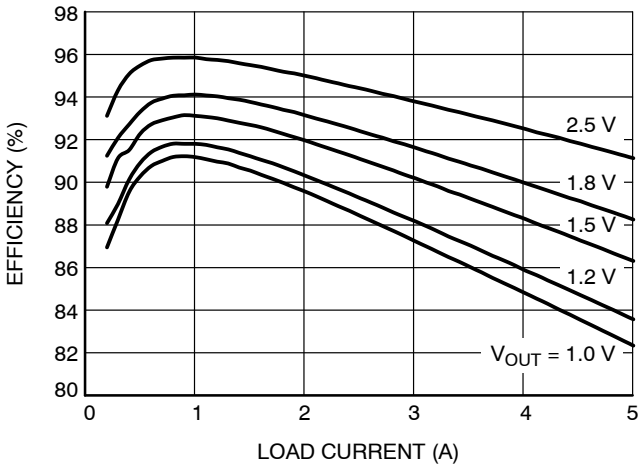


Figure 6. Efficiency at Vin = 3.3 V Auto CCM/DCM Operation Mode

DETAILED DESCRIPTION

Overview

NCP3136 is a low input voltage high performance synchronous buck converter with two integrated N−MOSFETs. NCP3136's output voltage range is from 0.6 V to 0.84 x Vin and it has wide input voltage range from 2.9 V to 5.5 V. The features of NCP3136 include supporting pre−bias start−up to protect sensitive loads, cycle−by−cycle over−current limiting and short circuit protection, power good monitor, over voltage and under voltage protection, built in output discharge and thermal shutdown.

NCP3136 provides two operation modes to fit various application requirements. The automatic CCM/DCM mode operation provides reduced power loss and increases the efficiency at light load. The adaptive power control architecture enables smooth transition between light load and heavy load while maintaining fast response to load transients.

Operation Mode

In forced continuous conduction mode (FCCM), the high−side FET is ON during the on−time and the low−side FET is ON during the off−time. The switching is synchronized to an internal clock thus the switching frequency is fixed.

In Automatic CCM/DCM mode, the high−side FET is ON during the on−time and low−side FET is ON during the off−time until the inductor current reaches zero. An internal zero−crossing comparator detects the zero crossing of the inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic circuitry and turns off the low−side FET.

When the load is increased, the inductor current is always positive and the zero−crossing comparator does not send any zero−crossing signal. The converter enters into continuous conduction mode (CCM) when no zero−crossing is detected for two consecutive PWM pulses. In CCM mode, the switching synchronizes to the internal clock and the switching frequency is fixed.

VDD Voltage

The VDD voltage is supplied from VIN via an intrenal resistor. Meanwhile, it is also ok to short the VDD pin and VIN pins externally.

Reference Voltage

The NCP3136 incorporates 600 mV reference voltage with 1.0% tolerance.

Internal Soft−Start

To limit the start−up inrush current, an internal soft start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The internal soft start time is 2.0 ms typically.

Soft Stop

Soft−Stop or discharge mode is always on during faults or disable. In this mode, disable (EN) causes the output to be discharged through an internal 40 Ω transistor inside of SW terminal. The time constant of soft−stop is a function of output capacitance and the resistance of the discharge transistor.

Automatic Power Saving Mode

In Automatic CCM/DCM mode when the load current decreases, the converter will enter power saving mode operation. During power saving mode, the low−side MOSFET will turn off when the inductor current reaches zero. So the converter skips switching and operates with reduced frequency, which minimizes the quiescent current and maintains high efficiency.

Forced Continuous Conduction Mode

When PS pin is floating or pulled high, NCP3136 is operating in forced continuous conduction mode in both light load and heavy load conditions. In this mode, the switching frequency remains constant over the entire load range, making it suitable for applications that need tight regulation of switching frequency at a cost of lower efficiency at light load.

PROTECTIONS

Under Voltage Lockout (UVLO)

There is under-voltage lock out protection (UVLO) for VIN in NCP3136, which has a typical trip threshold voltage 2.8 V and trip hysteresis 130 mV for VIN. If UVLO is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. Please note this protection function DOES NOT trigger the fault counter to latch off the part.

Over Voltage Protection (OVP)

When feedback voltage is above 17% (typical) of nominal voltage for over 1.7 μs blanking time, an OV fault is set. In this case, the converter de−asserts the PGD signal and performs the over−voltage protection function. The top gate drive is turned off and the bottom gate drive is turned on to discharge the output. The bottom gate drive will be turned off until VFB drops below the UVP threshold. The device enters a high−impedance state. This protection is latched.

Under Voltage Protection (UVP)

Output under−voltage protection works in conjunction with the current protection described in the Over−current Protection sections. An UVP circuit monitors the feedback voltage to detect under−voltage event. The under−voltage limit is 17% (typical) below of nominal voltage at FB pin. If the feedback voltage is below this threshold over 11 μs, an UV fault is set and both the high−side and the low−side FETs turn off. After a hiccup delay, the part tries to restart. This protection behavior is hiccup.

Power Good Monitor (PGD)

NCP3136 provides window comparator to monitor the output voltage at FB pin. When the output voltage is within ±17% of regulation voltage, the power good pin outputs a high signal. Otherwise, PGD stays low. The PGD pin is open drain 5 mA pull down output. During startup, PGD stays low until the feedback voltage is within the specified range for about 0.4 ms. If feedback voltage falls outside the tolerance band, the PG pin goes low after 10 μs delay.

The PGD pin de−asserts as soon as the EN pin is pulled low or an under−voltage event on VDD is detected.

Over Current Protection (OCP)

NCP3136 provides high−side MOSFET current limiting. When the current through the high−side FET exceeds 7.5 A, the high−side FET turns off and the low−side FET turns on until next PWM cycle. An over−current counter is triggered and starts to increment each occurrence of an over−current event. Both the high−side and the low−side FETs turn off when the OC counter reaches four. The OC counter resets if the detected current is less than 7.5 A after an OC event.

Pre−Bias Startup

In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP3136 supports pre−bias start up by holding low−side FETs off until soft start ramp reaches the FB pin voltage.

Thermal Shutdown

The NCP3136 protects itself from over heating with an internal thermal monitoring circuit. When the die temperature goes beyond a threshold value 135°C, both the high−side and the low−side FETs turn off until the temperature falls 40°C below of the threshold value. Then the converter restarts.

Application Note

For higher output voltage application cases (Vout = 3.3 V), choose the inductor value not to be lower than 1 μH to avoid over-current protection being triggered by inductor current ripple; For Vin = 5 V and Vout = 3.3 V case, add a voltage divider between Vin and EN to ensure that the part can start up without triggering UVP. Use Figure 7 as design reference for schematics. For other lower output voltage cases, it is not necessary to add this divider.

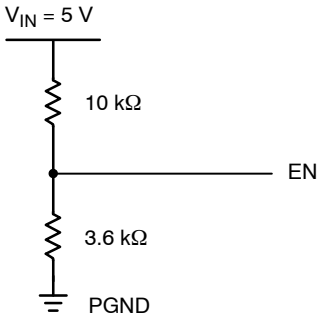


Figure 7. Voltage divider between VIN and EN for start−up in VIN = 5 V and VOUT = 3.3 V case

Layout Guidelines

When laying out a power PCB for the NCP3136 there are several key points to consider.

Use four vias to connect the thermal pad to power ground. Separate the power ground and analog ground planes; connect them together at a single point.

Increase the thickness of PCB copper, it can help to lower the die temperature and improve the overall efficiency but meanwhile increase the cost of the board fabrication.

Use wide traces for the nodes conducting high current such as VIN, VOUT, PGND and SW.

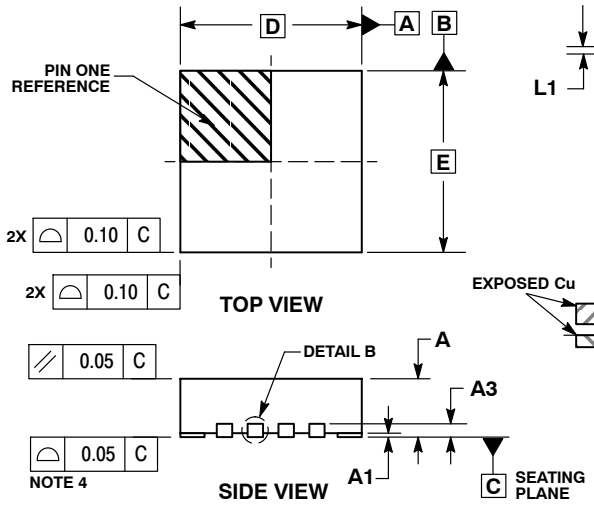
Place feedback and compensation network components close to the IC.

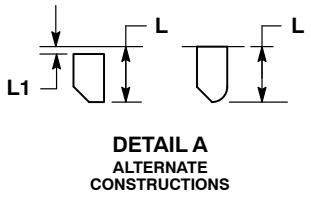
Keep FB, COMP away from noisy signals such as SW, BST.

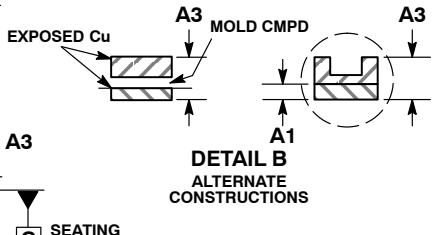
Place VIN and VDD decoupling capacitors as close to the IC as possible.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485DA
ISSUE A

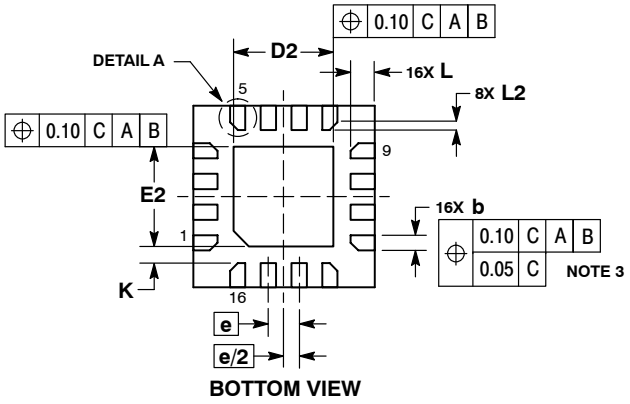


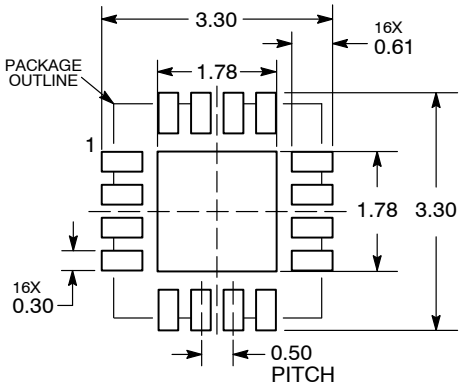




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.55	1.75
E	3.00 BSC	
E2	1.55	1.75
e	0.50 BSC	
K	0.275 REF	
L	0.30	0.50
L1	0.00	0.15
L2	0.09 REF	





DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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