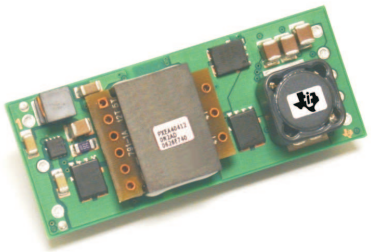
20-A, 48-V INPUT, ISOLATED, 1/8th BRICK DC-DC CONVERTER

Check for Samples: PTEA420025, PTEA420033

FEATURES

- **20–A Output Current Rating**
- **Input Voltage Range: 36 V to 75 V**
- **92% Efficiency**
- **1500 Vdc Isolation**
- **Fast Transient Response**
- **On/Off Control**
- **Overcurrent Protection**
- **Differential Remote Sense**
- **Adjustable Output Voltage**
- **Output Overvoltage Protection**
- **Over-Temperature Shutdown**
- **Undervoltage Lockout**
- **Standard 1/8-Brick Footprint**
- **UL Safety Agency Approval**



DESCRIPTION

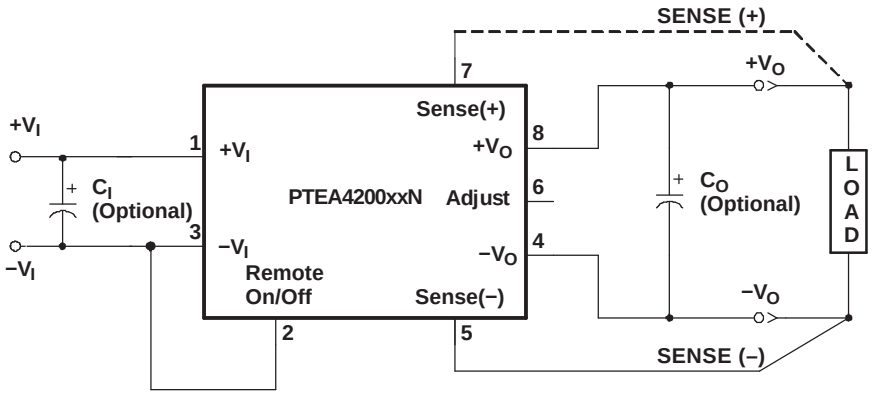
The PTEA series of power modules are single-output isolated DC/DC converters, housed in an industry standard 1/8thbrick package. These modules are rated up to 66 W with a maximum load current of 20 A.

The PTEA series operates from a standard 48-V telecom central office (CO) supply and occupies only 2.0 in^2 of PCB area. The modules offer OEMs a compact and flexible high-output power source in an industry standard footprint. They are suitable for distributed power applications in both telecom and computing environments, and may be used for powering high-end microprocessors, DSPs, general purpose logic and analog.

Features include a remote On/Off control with optional logic polarity, an undervoltage lockout (UVLO), a differential remote sense, and an industry standard output voltage adjustment using an external resistor. Protection features include output overcurrent protection (OCP), overvoltage protection (OVP), and thermal shutdown (OTP).

The modules are fully integrated for stand-alone operation, and require no additional components.

STANDARD APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

Table 1. PART NUMBERING SCHEME

	Input Voltage	Output Current	Output Voltage	Enable	Electrical Options		Pin Style
PTEA	**4**	**20**	**033**	**N**	**2**	**A**	**D**
	4 = 48 V	20 = 20 A	025 = 2.5 V 033 = 3.3 V	N = Negative P = Positive	2 = V_O Adjust		D = Through-hole, Pb-free

ABSOLUTE MAXIMUM RATING

				UNIT
T_A	Operating Temperature Range	Over V_I Range		–40°C to 85°C(1)
$V_{I,MAX}$	Maximum Input Voltage	Continuous voltage		80 V
		Peak voltage for 100 ms duration		100 V
$P_{O,MAX}$	Maximum Output Power		PTEA420033x2	66 W
			PTEA420025x2	50 W
T_S	Storage Temperature			–55°C to 125°C
	Mechanical Shock	Per Mil-STD-883, Method 2002.3 1 ms, 1/2 Sine, mounted	AD Suffix	250 G
	Mechanical Vibrarion	Per Mil-STD-883, Method 2007.2 20-2000 Hz, PCB mounted	AD Suffix	15 G
	Weight			18 grams
	Flammability	Meets UL 94V-O		

(1) See SOA curves or consult factory for appropriate derating.

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ELECTRICAL CHARACTERISTICS PTEA420025

(Unless otherwise stated, T_A =25°C, V_I = 48 V, V_O = 2.5 V, C_O = 0 µF, and I_O = $I_{O(max)}$)

PARAMETER		TEST CONDITIONS		PTEA420025			
				MIN	TYP	MAX	UNIT
I_O	Output Current	Over V_I range		0		20	A
V_I	Input Voltage Range	Over I_O Range		36	48	75	V
V_O tol	Set Point Voltage Tolerance				±1(1)		$\%V_O$
Reg_{temp}	Temperature Variation	–40°C >T_A > 85°C			±1.15		$\%V_O$
Reg_{line}	Line Regulation	Over V_I range			±5		mV
Reg_{load}	Load Regulation	Over I_O range			±5		mV
ΔV_otot	Total Output Voltage Variation	Includes set-point, line, load, –40°C >T_A > 85°C			±1.5	±3	$\%V_O$
ΔV_{ADJ}	Output Adjust Range	P_O ≤ 75 W		–20		10	$\%V_O$
η	Efficiency	I_O = 50% I_O(max)			89%		
V_R	V_O Ripple (pk-pk)	20 MHz bandwidth			50		mV_{pp}
t_{tr}	Transient Response	0.1 A/µs slew rate, 50% to 75% $I_{O(max)}$			150		µs
ΔV_{tr}		V_O over/undershoot			90		mV
I_{TRIP}	Overcurrent Threshold	Shutdown, followed by auto-recovery			28		A
OVP	Output Overvoltage Protection	Output shutdown and latch off			120		$\%V_O$
OTP	Over Temperature Protection	Temperature Measurement at thermal sensor. Hysteresis = 10°C nominal.			105		° C
f_s	Switching Frequency	Over V_I range			290		kHz
UVLO	Undervoltage Lockout	V_{OFF}	V_I decreasing, I_O = 6 A		29.4		V
		V_{HYS}	Hysteresis		3.3		
On/Off Input: **Negative Enable**							
V_{IH}	Input High Voltage	Referenced to –V_I		2.4		Open(2)	V
V_{IL}	Input Low Voltage			–0.2		0.8	
I_{IL}	Input Low Current				–0.2		mA
On/Off Input: **Positive Enable**							
V_{IH}	Input High Voltage	Referenced to –V_I		2.4		Open(2)	V
V_{IL}	Input Low Voltage			–0.2		0.8	
I_{IL}	Input Low Current				–0.2		mA
I_{ISB}	Standby Input Current	Output disabled (pin 2 status set to Off)			37		mA
C_I	External Input Capacitance	Between +V_I and –V_I			100		µF
C_O	External Output Capacitance	Between +V_O and –V_O		0		20000	µF
	Isolation Voltage	Input-to-output and input-to-case			1500		Vdc
	Isolation Capacitance	Input-to-output			1200		pF
	Isolation Resistance	Input-to-output		10			MΩ

(1) If Sense(–) is not used, pin 5 must be connected to pin 4 for optimum output voltage accuracy.
(2) The Remote On/Off input has an internal pull-up and may be controlled with an open collector (drain) interface. An open circuit correlates to a logic high. Consult the application notes for interface considerations.

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ELECTRICAL CHARACTERISTICS PTEA420033

(Unless otherwise stated, T_A =25°C, V_I = 48 V, V_O = 3.3 V, C_O = 0 µF, and I_O = $I_{O(max)}$)

PARAMETER		TEST CONDITIONS		PTEA420033			
				MIN	TYP	MAX	UNIT
I_O	Output Current	Over V_I range		0		20	A
V_I	Input Voltage Range	Over I_O Range		36	48	75	V
V_O tol	Set Point Voltage Tolerance				±1(1)		$\%V_O$
Reg_{temp}	Temperature Variation	–40°C >T_A > 85°C			±1.15		$\%V_O$
Reg_{line}	Line Regulation	Over V_I range			±5		mV
Reg_{load}	Load Regulation	Over I_O range			±5		mV
ΔV_otot	Total Output Voltage Variation	Includes set-point, line, load, –40°C >T_A > 85°C			±1.5	±3	$\%V_O$
ΔV_{ADJ}	Output Adjust Range	P_O ≤ 100 W		–20		10	$\%V_O$
η	Efficiency	I_O = 50% $I_{O(max)}$			91%		
V_R	V_O Ripple (pk-pk)	20 MHz bandwidth			50		mV_{pp}
t_{tr}	Transient Response	0.1 A/µs slew rate, 50% to 75% $I_{O(max)}$			150		µs
ΔV_{tr}		V_O over/undershoot			90		mV
I_{TRIP}	Overcurrent Threshold	Shutdown, followed by auto-recovery			28		A
OVP	Output Overvoltage Protection	Output shutdown and latch off			120		$\%V_O$
OTP	Over Temperature Protection	Temperature Measurement at thermal sensor. Hysteresis = 10°C nominal.			105		° C
f_s	Switching Frequency	Over V_I range			290		kHz
UVLO	Undervoltage Lockout	V_{OFF}	V_I decreasing, I_O = 6 A		29.4		V
		V_{HYS}	Hysteresis		3.3		
On/Off Input: **Negative Enable**							
V_{IH}	Input High Voltage	Referenced to –V_I		2.4		Open(2)	V
V_{IL}	Input Low Voltage			–0.2		0.8	
I_{IL}	Input Low Current				–0.2		mA
On/Off Input: **Positive Enable**							
V_{IH}	Input High Voltage	Referenced to –V_I		2.4		Open(2)	V
V_{IL}	Input Low Voltage			–0.2		0.8	
I_{IL}	Input Low Current				–0.2		mA
I_{lsb}	Standby Input Current	Output disabled (pin 2 status set to Off)			42		mA
C_I	External Input Capacitance	Between +V_I and –V_I			100		µF
C_O	External Output Capacitance	Between +V_O and –V_O		0		20000	µF
	Isolation Voltage	Input-to-output and input-to-case			1500		Vdc
	Isolation Capacitance	Input-to-output			1200		pF
	Isolation Resistance	Input-to-output		10			MΩ

(1) If Sense(–) is not used, pin 5 must be connected to pin 4 for optimum output voltage accuracy.
(2) The Remote On/Off input has an internal pull-up and may be controlled with an open collector (drain) interface. An open circuit correlates to a logic high. Consult the application notes for interface considerations.

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PIN DESCRIPTIONS

$+V_I$: The positive input for the module with respect to $–V_I$. When powering the module from a –48-V telecom central office supply, this input is connected to the primary system ground.

$–V_I$: The negative input supply for the module, and the 0 VDC reference for the Remote On/Off input. When powering the module from a +48-V supply, this input is connected to the 48-V return.

Remote On/Off: This input controls the On/Off status of the output voltage. It is either driven low ($–V_I$ potential), or left open-circuit. For units identified with the NEN option, applying a logic low to this pin will enable the output. And for units identified with the PEN option, the output will be disabled.

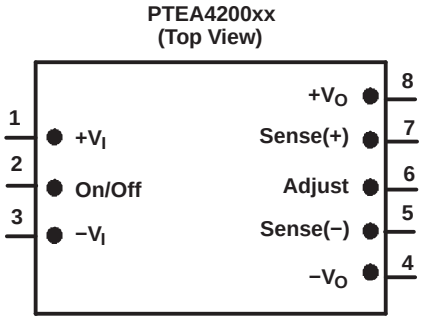
V_O Adjust: Allows the output voltage to be trimmed by up or down between +10% and –20% of its nominal value. The adjustment method uses a single external resistor. Connecting the resistor between V_O Adjust and $–V_O$ adjusts the output voltage lower, and placing it between V_O Adjust and $+V_O$ adjusts the output higher. The calculations for the resistance value follows industry standard formulas. For further information consult the application note on output voltage adustment.

$+V_O$: The positive power output with respect to $–V_O$, which is DC isolated from the input supply pins. If a negative output voltage is desired, $+V_O$ should be connected to the secondary circuit common and the output taken from $–V_O$.

$–V_O$: The negative power output with respect to $+V_O$, which is DC isolated from the input supply pins. This output is normally connected to the secondary circuit common when a positive output voltage is desired.

Sense(+): Provides the converter with an output sense capability to regulate the set-point voltage directly at the load. When used with Sense(-), the regulation circuitry will compensate for voltage drop between the converter and the load. The pin may be left open circuit, but connecting it to $+V_O$ will improve load regulation.

Sense(–): Provides the converter with an output sense capability when used in conjunction with Sense(+) input. For optimum output voltage accuracy this pin should always be connected to $–V_O$.



TYPICAL CHARACTERISTICS

PTEA420025, V_O = 2.5 V (1) (2)

EFFICIENCY VS LOAD CURRENT

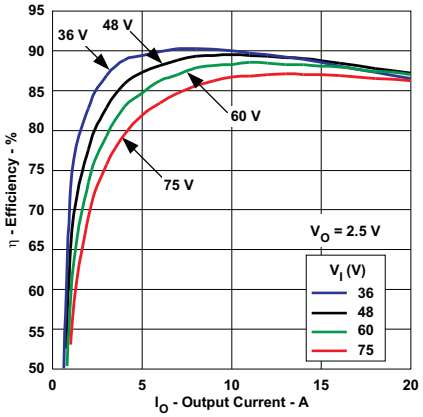


Figure 1.

OUTPUT RIPPLE VS LOAD CURRENT

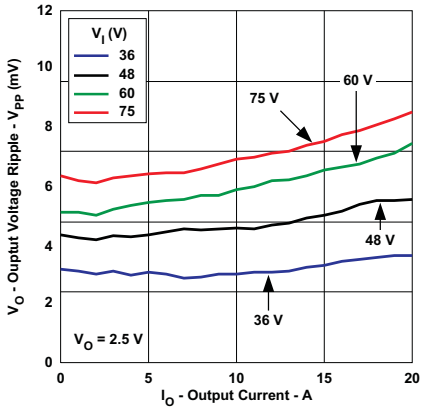


Figure 2.

POWER DISSIPATION VS LOAD CURRENT

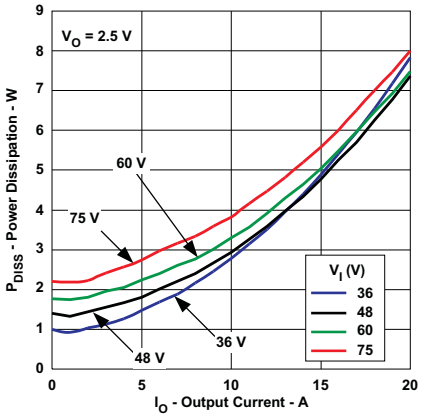


Figure 3.

AMBIENT TEMPERATURE VS LOAD CURRENT

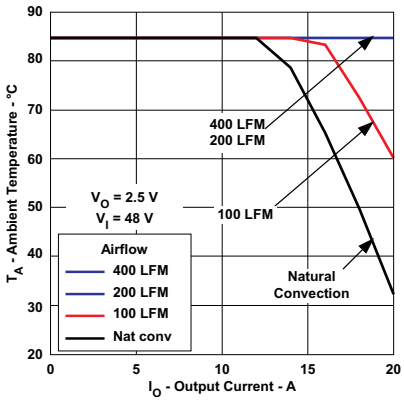


Figure 4.

(1) All data listed in Figure 1, Figure 2, and Figure 3 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(2) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 4.

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TYPICAL CHARACTERISTICS

PTEA420033, V_O = 3.3 V (1) (2)

EFFICIENCY VS LOAD CURRENT

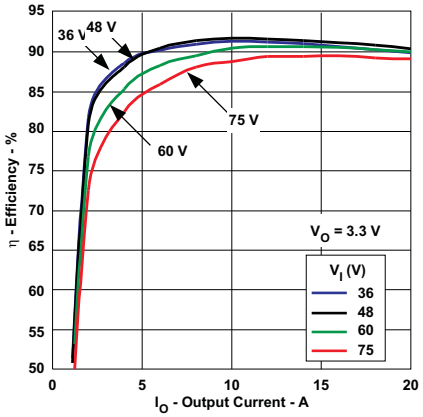


Figure 5.

OUTPUT RIPPLE VS LOAD CURRENT

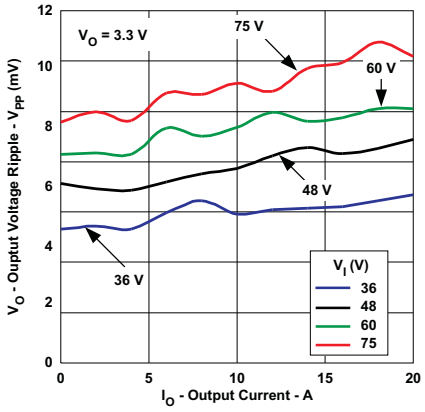


Figure 6.

POWER DISSIPATION VS LOAD CURRENT

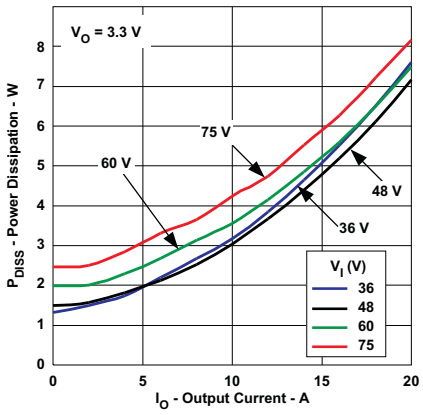


Figure 7.

AMBIENT TEMPERATURE VS LOAD CURRENT

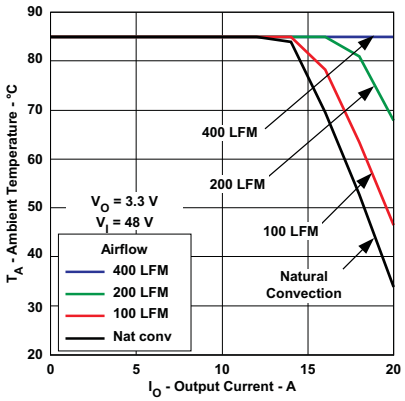


Figure 8.

(1) All data listed in Figure 5, Figure 6, and Figure 7 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(2) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 8.

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APPLICATION INFORMATION

Operating Features and System Considerations for the PTEA Series of DC/DC Converters

Overcurrent Protection

To protect against load faults, these converters incorporate output overcurrent protection. Applying a load to the output that exceeds the converter's overcurrent threshold (see applicable specification) will cause the output voltage to momentarily fold back, and then shut down. Following shutdown the module will periodically attempt to automatically recover by initiating a soft-start power-up. This is often described as a *hiccup* mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. Once the fault is removed, the converter automatically recovers and returns to normal operation.

Output Overvoltage Protection

Each converter incorporates protection circuitry that continually senses for an output overvoltage (OV) condition. The OV threshold is set approximately 20% higher than the nominal output voltage. If the converter output voltage exceeds this threshold, the converter is immediately shut down and remains in a latched-off state. To resume normal operation the converter must be actively reset. This can only be done by momentarily removing the input power to the converter. For fail-safe operation and redundancy, the OV protection uses circuitry that is independent of the converter's internal feedback loop.

Overtemperature Protection

Overtemperature protection is provided by an internal temperature sensor, which closely monitors the temperature of the converter's printed circuit board (PCB). If the sensor exceeds a temperature of approximately 105°C, the converter will shut down. The converter will then automatically restart when the sensed temperature drops back to approximately 95°C. When operated outside its recommended thermal derating envelope (see data sheet SOA curves), the converter will typcially cycle on and off at intervals from a few seconds to one or two minutes. This is to ensure that the internal components are not permanently damaged from excessive thermal stress.

Undervoltage Lockout

The Undervoltage lockout (UVLO) is designed to prevent the operation of the converter until the input voltage is at the minimum input voltage. This prevents high start-up current during normal power-up of the converter, and minimizes the current drain from the input source during low input voltage conditions. The UVLO circuitry also overrides the operation of the *Remote On/Off* control.

Primary-Secondary Isolation

These converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are production tested to a withstand voltage of 1500 VDC. This specification complies with UL60950 and EN60950 requirements. This allows the converter to be configured for either a positive or negative input voltage source. The data sheet *Pin Descriptions* section provides guidance as to the correct reference that must be used for the external control signals.

Input Current Limiting

The converter is not internally fused. For safety and overall system protection, the maximum input current to the converter must be limited. Active or passive current limiting can be used. Passive current limiting can be a fast acting fuse. A 125-V fuse, rated no more than 10 A, is recommended. Active current limiting can be implemented with a current limited *Hot-Swap* controller.

Thermal Considerations

Airflow may be necessary to ensure that the module can supply the desired load current in environments with elevated ambient temperatures. The required airflow rate may be determined from the Safe Operating Area (SOA) thermal derating chart (see typical characteristics).

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Differential Remote Sense

The remote sense pins allows the converter to precisely regulate the DC output voltage at a remote location. This might be a power plane on an inner layer of the host PCB. *Connecting Sense(+)* directly to $+V_O$, and *Sense(–)* to $–V_O$ will improve output voltage accuracy. In the event that the sense pins are left open-circuit, an internal 100-Ω (S+) or 10-Ω (S–) resistor between each sense pin and its corresponding output prevents an excessive rise in the output voltage. For practical reasons, the amount of IR voltage compensation should be limited to 0.5 V maximum.

The remote sense feature is designed to compensate for limited amounts of *IR* voltage drop. It is **not** intended to compensate for the forward drop of a non-linear or frequency dependent components that may be placed in series with the converter output. Examples of such components include OR-ing diodes, filter inductors, ferrite beads, and fuses. Enclosing these components with the remote sense connections effectively places them inside the regulation control loop, which can affect the stability of the regulator.

Using the Remote On/Off Function on the PTEA Series of DC/DC Converters

For applications requiring output voltage On/Off control, the PTEA series of DC/DC converters incorporate a *Remote On/Off* control (pin 2). This feature can be used to switch the module off without removing the applied input source voltage. When placed in the *Off* state, the standby current drawn from the input source is typically reduced to 3 mA.

Negative Output Enable (NEN)

Models using the negative enable option, the *Remote On/Off* (pin 2) control must be driven to a logic low voltage for the converter to produce an output. This is accomplished by either permanently connecting pin 2 to $–V_I$ (pin 3), or driving it low with an external control signal. Table 2 shows the input requirements of pin 2 for those modules with the *NEN* option.

Table 2. On/Off Control Requirements for Negative Enable

	PARAMETER	MIN	TYP	MAX
V_{IH}	Disable	2.4 V		20 V
V_{IL}	Enable	–0.2 V		0.8 V
$V_{o/c}$	Open-Circuit		3.3 V	4V
I_I	Pin 2 at $–V_I$			–0.2 mA

Positive Output Enable (PEN)

For those models with the positive enable (PEN) option, leaving pin 2 open circuit, (or driving it to an equivalent logic high voltage), will enable the converter output. This allows the module to produce an output voltage whenever a valid input source voltage is applied to $+V_I$ with respect to $–V_I$. If a logic-low signal is then applied to pin 2 the converter output is disabled. Table 3 gives the input requirements of pin 2 for modules with the *PEN* option.

Table 3. On/Off Control Requirements for Positive Enable

	PARAMETER	MIN	TYP	MAX
V_{IH}	Enable	4.5 V		20 V
V_{IL}	Disable	–0.2 V		0.8 V
$V_{o/c}$	Open-Circuit		3.3 V	4 V
I_I	Pin 2 at $–V_I$			–0.2 mA

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Notes:

1. The *Remote On/Off* control uses $-V_I$ (pin 3) as its ground reference. All voltages are with respect to $-V_I$.
2. An open-collector device (preferably a discrete transistor) is recommended. A pull-up resistor is not required. If one is added the pull-up voltage should not exceed 20 V.

   Caution: *Do not use a pull-resistor to $+V_I$ (pin 1). The remote On/Off control has a maximum input voltage of 20 V. Exceeding this voltage will overstress, and possibly damage, the converter*.
3. The *Remote On/Off* pin may be controlled with devices that have a totem-pole output. This is provided the output high level voltage (V_{OH}) meets the module's minimum V_{IH} specified in Table 2. If a TTL gate is used, a pull-up resistor may be required to the logic supply voltage.
4. The converter incorporates an *undervoltage lockout* (UVLO). The UVLO keeps the converter off until the input voltage is close to the minimum specified operating voltage. This is regardless of the state of the *Remote On/Off* control. Consult the product specification for the UVLO input voltage thresholds.

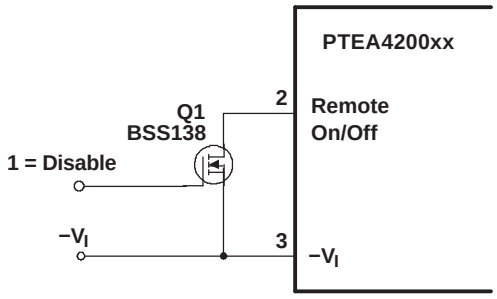


Figure 9. Recommended Control or Remote On/Off Input

Turn-On: With a valid input source voltage applied, the converter produces a regulated output voltage within 75 ms of the output being enabled. Figure 10 shows the output response of the PTEA420033P following the removal of the logic-low signal from the *Remote On/Off* (pin 2); see Figure 9. This corresponds to the drop in Q1 V_{GS} in Figure 10. Although the rise-time of the output voltage is short (<10 ms), the indicated delay time will vary depending upon the input voltage and the module's internal timing. The waveforms were measured with 48 VDC input voltage, and a 10-A resistive load.

Turn-Off Time: When a valid input source is removed or if the *Remote On/Off* (pin 2) is used to disable the output, with no external output capacitance, the module powers down within 200 µs. Figure 11 shows that, during power down, there is no output voltage undershoot. If used to supply processor I/O voltages, the lack of undershoot ensures the parasitic diodes do not conduct current and potentially cause damage to external circuitry.

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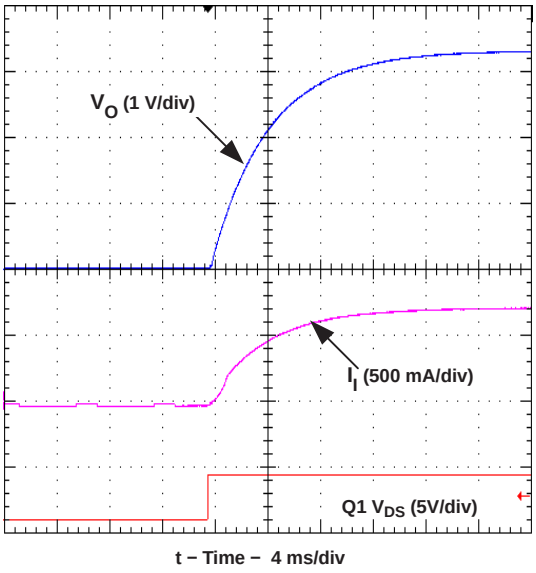


Figure 10. Power Up

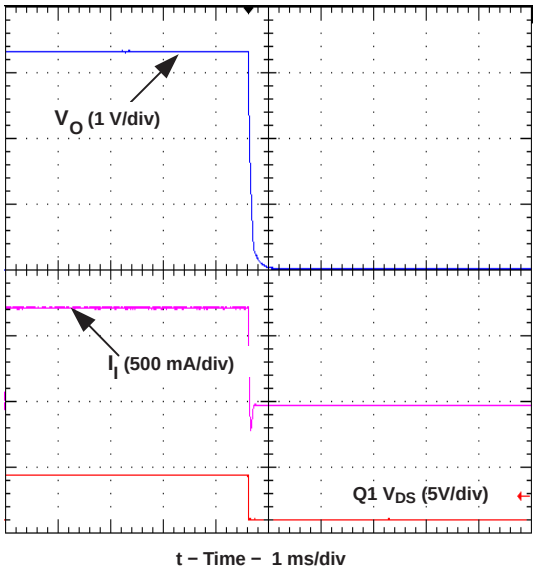


Figure 11. Power Down

Adjusting the Output Voltage of the 20–A Rated PTEA Series of Isolated DC/DC Converters

The output voltage adjustment of the PTEA series of isolated DC/DC converters follows the standard adopted by popular 1/8-brick DC/DC converters. Adjustment is accomplished with a single external resistor that can adjust the output voltage from –20% to +10% of the nominal set-point voltage. The placement of the resistor determines the direction of adjustment, up or down, and the value of the magnitude of adjustment.

Adjust Up: To increase the output voltage add a resistor, R1, between *V_O Adjust* (pin 6) and *Sense(+)* (pin 7).

Adjust Down: Add a resistor, (R2), between *V_O Adjust* (pin 6) and *Sense(–)* (pin 5).

Refer to Figure 12 for the placement of the required resistor, R1 or (R2).

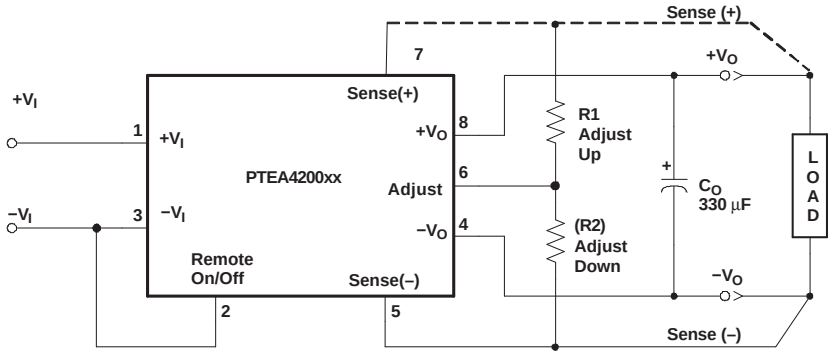


Figure 12.

The values of R1 [adjust up], and (R2) [adjust down], can be calculated using the following formulas.

$$R1 = \frac{5.11\,V_O\,(100+\Delta\%)}{1.224\,\Delta\%} - \frac{511}{\Delta\%} - 10.22\ (k\Omega) \quad (1)$$

$$(R2) = 5.11\left(\frac{100}{\Delta\%}\right) - 10.22\ (k\Omega) \quad (2)$$

Where:

Δ% = Amount of adjustment in %

V_O = Original set-point voltage

Notes:

1. Use only a single 1% resistor in either the R1 or (R2) location. Place the resistor as close to the converter as possible.
2. If the output voltage is increased, the maximum load current must be derated according to the following equation.

$$I_{O(max)} = \frac{V_O \times I_{O(rated)}}{V_A} \quad (3)$$

Where:

V_O = Original set-point voltage

V_A = Adjusted output voltage (measured between pins 8 and 4)

In any instance, the load current must not exceed the converter's maximum rated output current of 20 A.

3. The overvoltage threshold is fixed, and is set approximately 20% above the nominal output voltage. Adjusting the output voltage higher reduces the voltage margin between the adjusted output voltage and the overvoltage (OV) protection threshold. This could make the module sensitive to OV fault detection, as a result of random noise and load transients.

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Table 4. Adjustment Resistor Values

	Adjusted Output Voltage (V)		Trim-Up R_{ADJ}		Trim-Down R_{ADJ}	
V_O (nom) % Adjust (V)	3.3 V	2.5 V	3.3 V R1 (kΩ)	2.5 V R1 (kΩ)	3.3 V R2 (kΩ)	2.5 V R2 (kΩ)
+10	3.630	2.750	90.9	53.6	-	-
+ 9	3.597	2.725	100	59.0	-	-
+ 8	3.564	2.700	113	66.5	-	-
+ 7	3.531	2.675	127	76.8	-	-
+ 6	3.498	2.650	147	88.7	-	-
+ 5	3.465	2.625	178	107	-	-
+ 4	3.432	2.600	221	133	-	-
+ 3	3.399	2.575	294	178	-	-
+ 2	3.366	2.550	432	267	-	-
+ 1	3.333	2.525	866	536	-	-
0	3.300	2.500	Open	Open	-	-
–1	3.267	2.475	-	-	499	499
–2	3.234	2.450	-	-	243	243
–3	3.201	2.425	-	-	158	158
–4	3.168	2.400	-	-	118	118
–5	3.135	2.375	-	-	90.9	90.9
–6	3.102	2.350	-	-	75	75
–7	3.069	2.325	-	-	63.4	63.4
–8	3.036	2.300	-	-	53.6	53.6
–9	3.003	2.275	-	-	46.4	46.4
–10	2.970	2.250	-	-	41.2	41.2
–11	2.937	2.225	-	-	36.5	36.5
–12	2.904	2.200	-	-	32.4	32.4
–13	2.871	2.175	-	-	28.7	28.7
–14	2.838	2.150	-	-	26.1	26.1
–15	2.805	2.125	-	-	23.7	23.7
–16	2.772	2.100	-	-	21.5	21.5
–17	2.739	2.075	-	-	19.6	19.6
–18	2.706	2.050	-	-	18.2	18.2
–19	2.673	2.025	-	-	16.5	16.5
–20	2.640	2.000	-	-	15.4	15.4

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTEA420025P2AD	NRND	Through-Hole Module	EAW	8	15	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTEA420033N2AD	NRND	Through-Hole Module	EAW	8	15	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTEA420033P2AD	NRND	Through-Hole Module	EAW	8	15	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

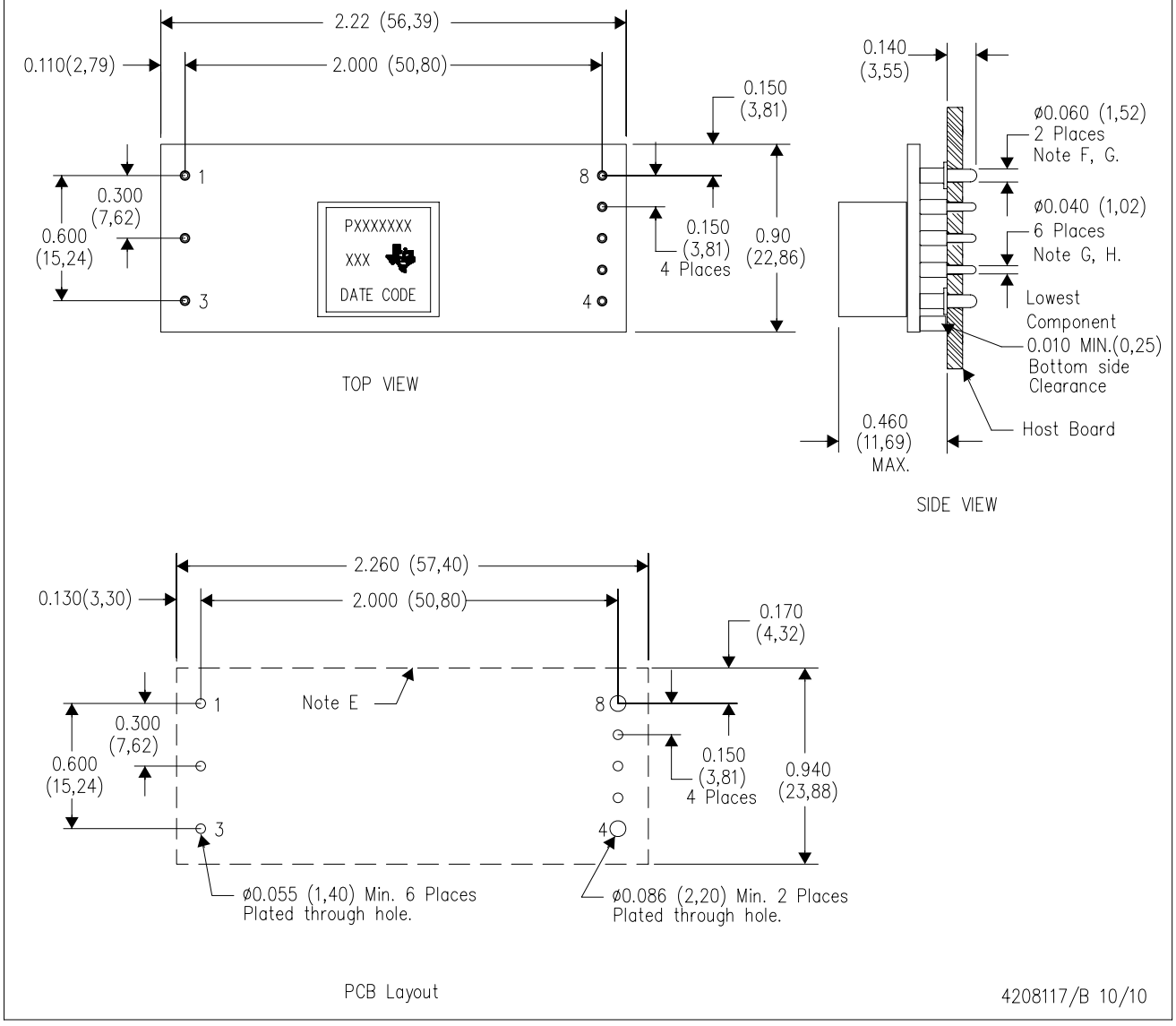
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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EAW (R–PDSS–T8) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.020 (±0,51mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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