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July 2014

FDMS86202

N-Channel Shielded Gate PowerTrench® MOSFET

120 V, 64 A, 7.2 mΩ

Features

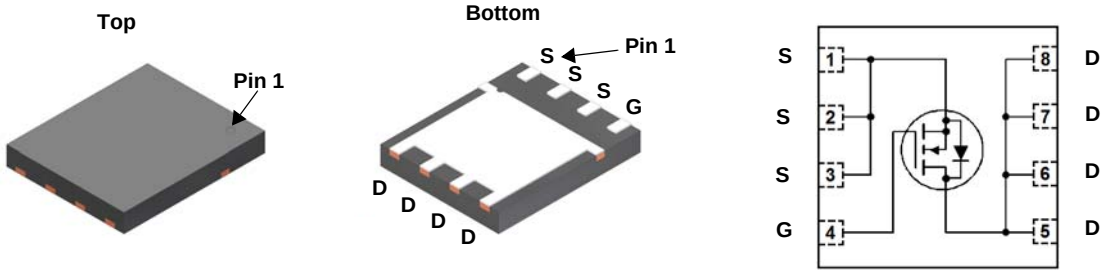
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 7.2 mΩ at V_{GS} = 10 V, I_D = 13.5 A
- Max $r_{DS(on)}$ = 10.3 mΩ at V_{GS} = 6 V, I_D = 11.5 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

- DC-DC Conversion



Power 56

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			120	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		64	A
	-Continuous	T_A = 25 °C	(Note 1a)	13.5	
	-Pulsed		(Note 4)	240	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	600	mJ
P_D	Power Dissipation	T_C = 25 °C		156	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86202	FDMS86202	Power 56	13 ”	12 mm	3000 units

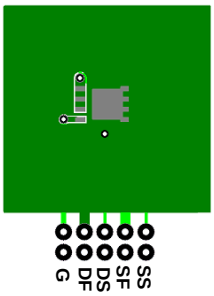
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Electrical Characteristics T_J = 25 °C unless otherwise noted

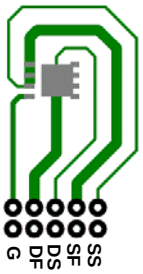
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	120			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		103		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 96 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-10		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 13.5 A		6.0	7.2	mΩ
		V_{GS} = 6 V, I_D = 11.5 A		8.1	10.3	
		V_{GS} = 10 V, I_D = 13.5 A,T_J = 125 °C		10.9	13.2	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13.5 A		44		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 60 V, V_{GS} = 0 V, f = 1 MHz		3195	4250	pF
C_{oss}	Output Capacitance			449	600	pF
C_{rss}	Reverse Transfer Capacitance			17	30	pF
R_g	Gate Resistance		0.1	0.9	2.7	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 60 V, I_D = 13.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		21	33	ns
t_r	Rise Time			6	13	ns
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns
t_f	Fall Time			5	11	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 60 V, I_D = 13.5 A		45	64	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 6 V; V_{DD} = 60 V, I_D = 13.5 A		29	41	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 60 V, I_D = 13.5 A		14.3		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 60 V, I_D = 13.5 A		8.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.69	1.2	V
		V_{GS} = 0 V, I_S = 13.5 A (Note 2)		0.76	1.3	
t_{rr}	Reverse Recovery Time	I_F = 13.5 A, di/dt = 100 A/μs		73	118	ns
Q_{rr}	Reverse Recovery Charge			117	187	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 45 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 115 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. E_{AS} of 600 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 20 A, V_{DD} = 120 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 65 A.

4. Pulse Id limited by junction temperature, td ≤ 100 μs, please refer to SOA curve for more details.

Typical Characteristics T_J = 25 °C unless otherwise noted

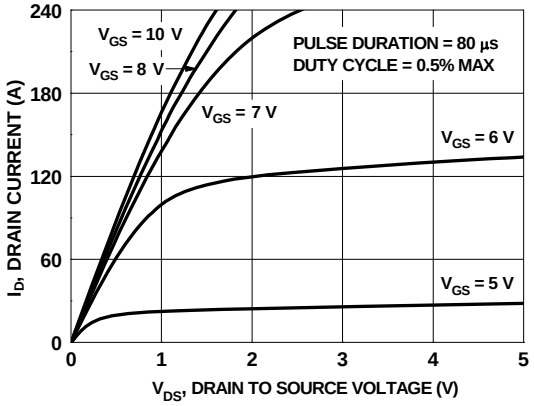


Figure 1. On Region Characteristics

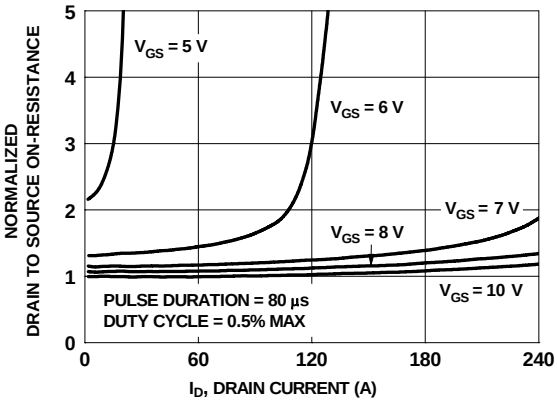


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

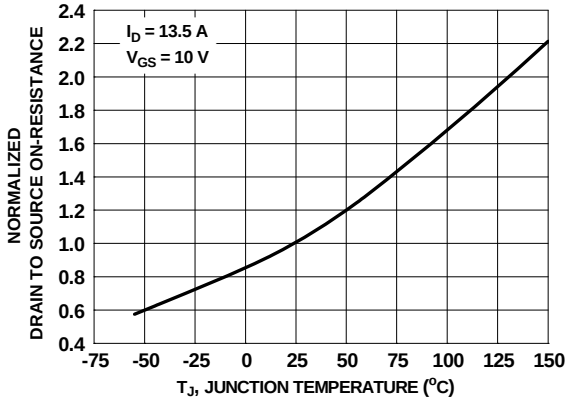


Figure 3. Normalized On Resistance vs Junction Temperature

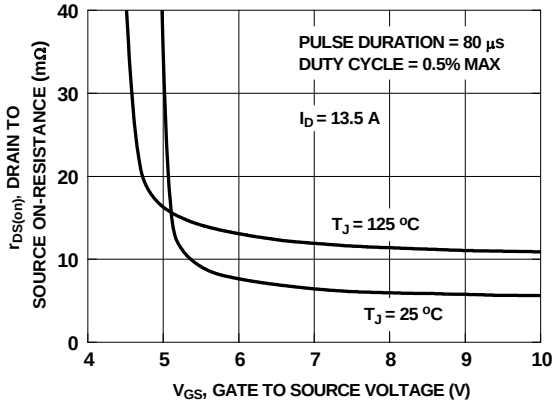


Figure 4. On-Resistance vs Gate to Source Voltage

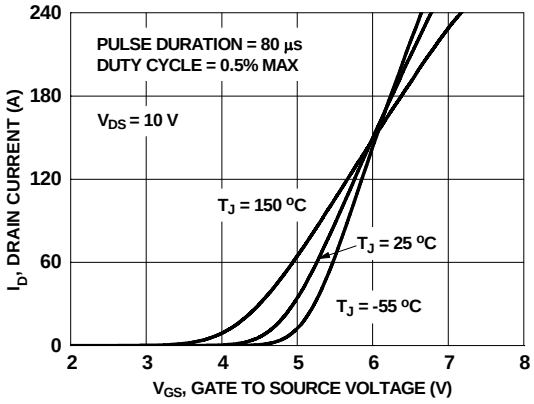


Figure 5. Transfer Characteristics

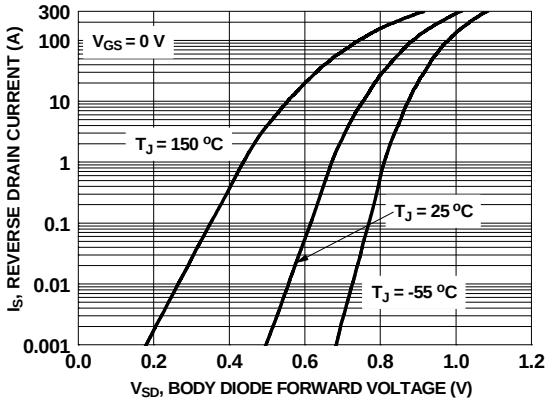


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

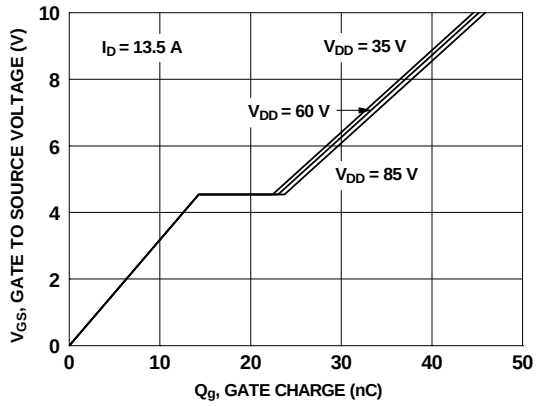


Figure 7. Gate Charge Characteristics

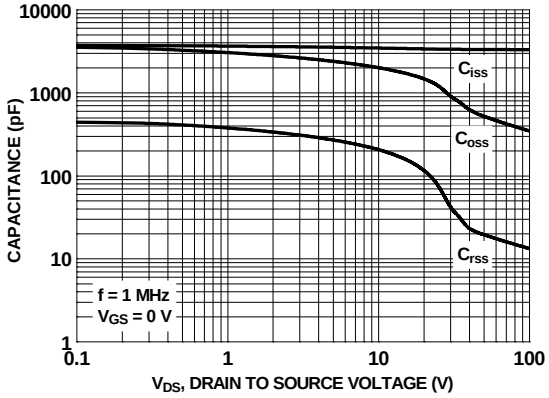


Figure 8. Capacitance vs Drain to Source Voltage

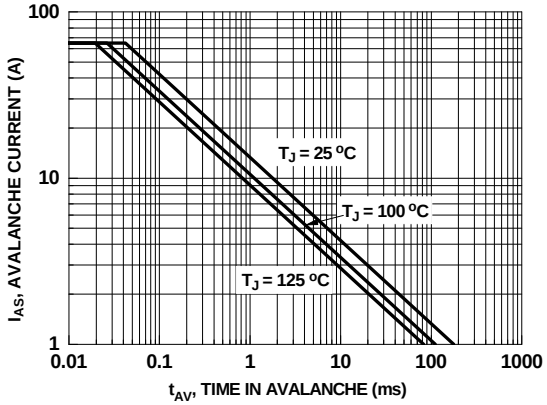


Figure 9. Unclamped Inductive Switching Capability

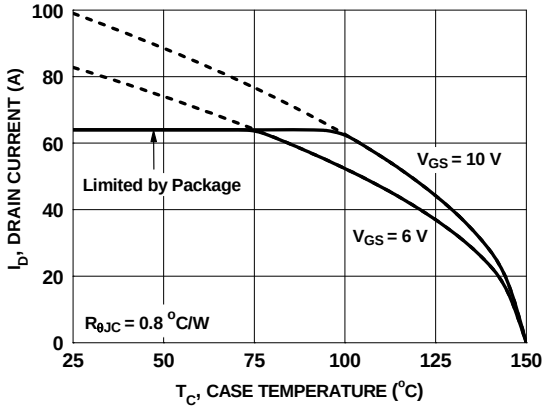


Figure 10. Maximum Continuous Drain Current vs Case Temperature

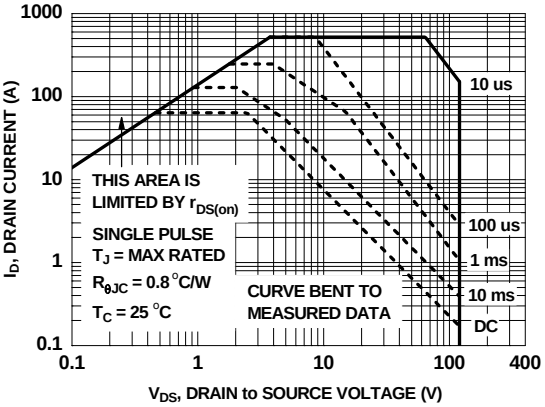


Figure 11. Forward Bias Safe Operating Area

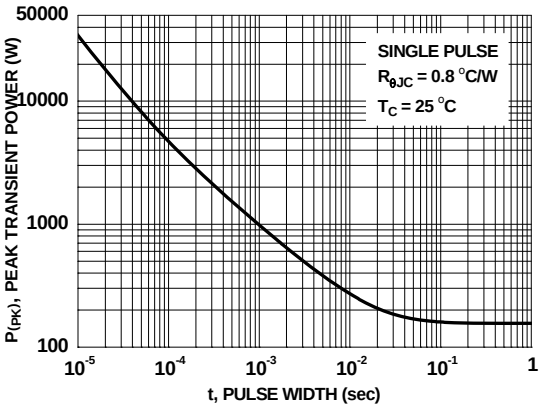


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

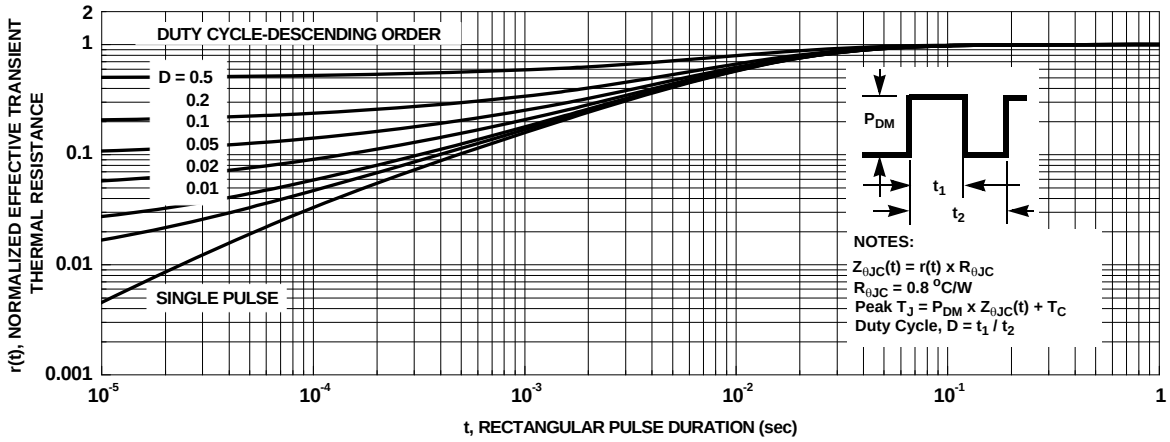
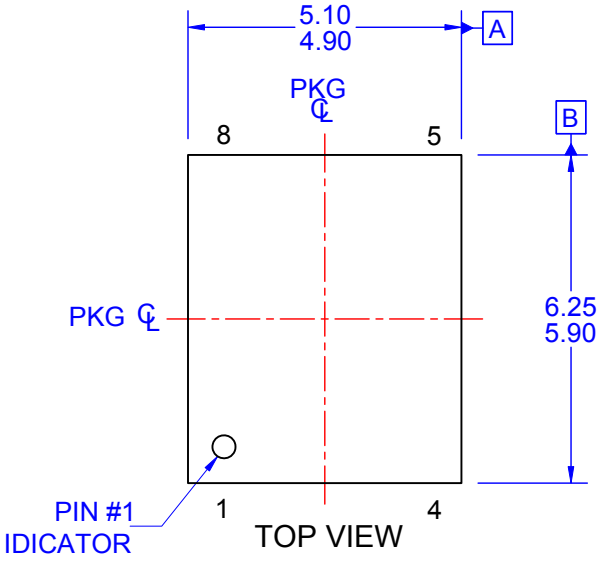
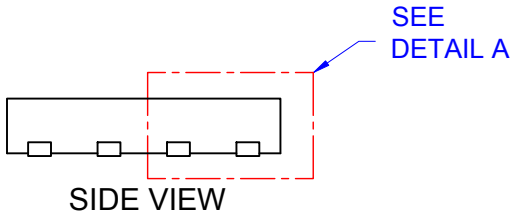
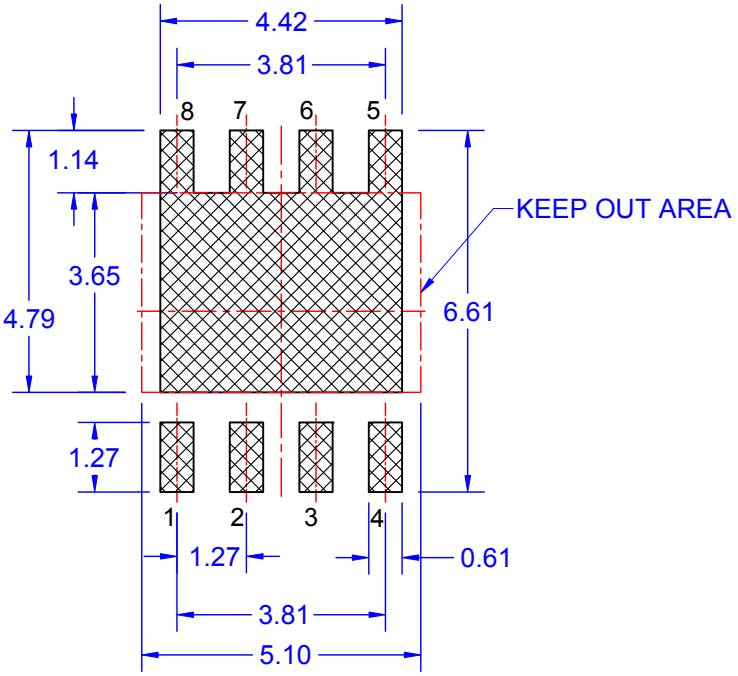
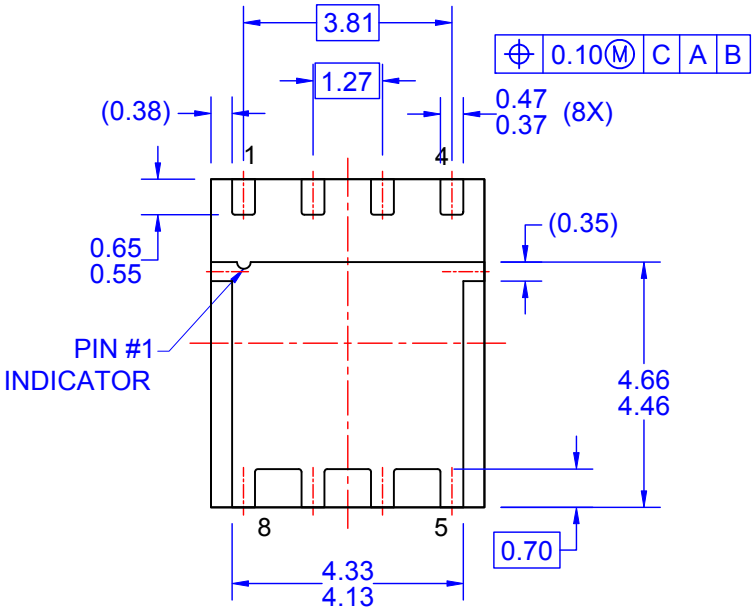


Figure 13. Junction-to-Case Transient Thermal Response Curve









NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,

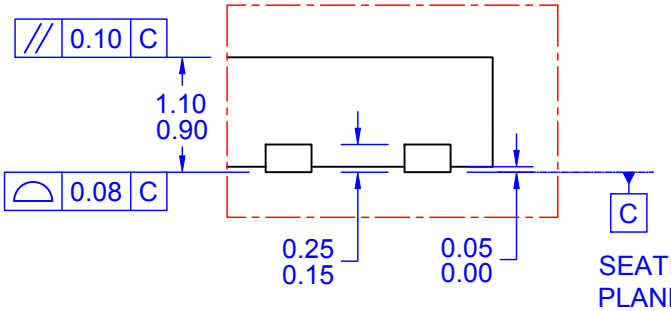
B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: PQFN08JREV3.



DETAIL A

SCALE: 2:1

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