ARM® Cortex®-M0
32-bit Microcontroller

NuMicro® Family
Mini58DE Series
Datasheet

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MINI58DE SERIES DATASHEET

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1   GENERAL DESCRIPTION

The NuMicro® Mini58 series is pin-to-pin and function compatible with the NuMicro® Mini51 series, the 32-bit microcontroller (MCU) embedded with the ARM® Cortex®-M0 core. The Mini58 series can bridge the gap and replace the cost equivalent to traditional 8- and 16-bit microcontroller by 32-bit performance and rich functions. The Mini58 series supports a wide range of applications from low-end, price sensitive designs to computing-intensive ones and provides advanced high-end features in economical products.

The Mini58 series can run up to 50 MHz which is faster than 24 MHz in Mini51 series, and operate at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40℃ ~ +105℃. For the Mini58 series, the embedded program flash size upgrades from 16 Kbytes to 32 Kbytes and SRAM upgrades from 2 Kbytes to 4 Kbytes. The Mini58 series also offers size configurable Data Flash (shared with program flash), and 2.5 Kbytes flash for the ISP.

The Mini58 series has many high-performance peripheral functions, such as 22.1184 MHz internal RC oscillator (±1% accuracy), I/O port with up to 30 pins, four 32-bit timers, two UARTs with the RS485 function and IrDA function interface, one SPI interface, two I^{2}C interfaces, up to three 16-bit PWM generators providing six channels, an 8-channel 10-bit ADC, Watchdog Timer, Window Watchdog Timer, two Analog Comparators and a Brown-out Detector. All these peripherals have been incorporated into the Mini58 series to reduce component count, board space and system cost. Compared to the Mini51 series, the Mini58 series supports additional one UART and one I^{2}C interface for better and more flexible connectivity applications.

Additionally, the Mini58 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product. The Mini58 series also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

2 FEATURES

- Core
    - ARM® Cortex®-M0 core running up to 50 MHz
    - One 24-bit system timer
    - Supports low power Idle mode
    - A single-cycle 32-bit hardware multiplier
    - NVIC for the 32 interrupt inputs, each with 4-level of priority
    - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- Built-in LDO for wide operating voltage: 2.5V to 5.5V
- Memory
    - 32 KB Flash memory for program memory (APROM)
    - Configurable Flash memory for data memory (Data Flash)
    - 2.5 KB Flash for loader (LDROM)
    - 4 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
    - Programmable system clock source
        - Switch clock sources on-the-fly
    - Support 4 ~ 24 MHz external high speed crystal oscillator (HXT) for precise timing operation
    - Support 32.768 kHz external low speed crystal oscillator (LXT) for idle wake-up and system operation clock
    - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (1% accuracy at 25^0C, 5V)
        - Dynamically calibrating the HIRC OSC to 22.1184 MHz ±1% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)
    - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
    - PLL allowing CPU operation up to the maximum 50 MHz
- I/O Port
    - Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
    - Four I/O modes:
        - Quasi-bidirectional input/output
        - Push-Pull output
        - Open-Drain output
        - Input only with high impendence
    - Optional Schmitt trigger input
- Timer
    - Provides two channel 32-bit Timers; one 8-bit pre-scaler counter with 24-bit up-timer for each timer

◆ Supports Event Counter mode

◆ Supports Toggle Output mode

◆ Supports external trigger in Pulse Width Measurement mode

◆ Supports external trigger in Pulse Width Capture mode

● WDT (Watchdog Timer)

■ Programmable clock source and time-out period

■ Supports wake-up function in Power-down mode and Idle mode

■ Interrupt or reset selectable on watchdog time-out

● WWDT (Window Watchdog Timer)

■ 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible

■ Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter

● PWM

■ Up to three built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs

■ Individual clock source, clock divider, 8-bit pre-scalar and dead-time generator for each PWM generator

■ PWM interrupt synchronized to PWM period

■ Supports edge-alignment or center-alignment

■ Supports fault detection

● UART (Universal Asynchronous Receiver/Transmitters)

■ Two UART devices

■ Buffered receiver and transmitter, each with 16-byte FIFO

■ Optional flow control function (CTSn and RTSn)

■ Supports IrDA (SIR) function

■ Programmable baud-rate generator up to 1/16 system clock

■ Supports RS-485 function

● SPI (Serial Peripheral Interface)

■ One SPI device

■ Master up to 25 MHz, and Slave up to 10 MHz

■ Supports Master/Slave mode

■ Full-duplex synchronous serial data transfer

■ Variable length of transfer data from 1 to 32 bits

■ MSB or LSB first data transfer

■ RX latching data can be either at rising edge or at falling edge of serial clock

■ TX sending data can be either at rising edge or at falling edge of serial clock

■ Supports Byte Suspend mode in 32-bit transmission

● I^{2}C

- Two I^{2}C devices
    - Supports Master/Slave mode
    - Bidirectional data transfer between masters and slaves
    - Multi-master bus (no central master)
    - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
    - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
    - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
    - Programmable clocks allow for versatile rate control
    - Supports multiple address recognition (four slave addresses with mask option)
- ADC (Analog-to-Digital Converter)
    - 10-bit SAR ADC with 250 kSPS
    - Up to 8-ch single-end input and one internal input from band-gap
    - Conversion started either by software trigger or external pin trigger
- Analog Comparator
    - Two analog comparators with programmable 16-level internal voltage reference
    - Built-in CRV (comparator reference voltage)
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD (Brown-out Detector)
    - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V
    - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
    - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
    - Green package (RoHS)
    - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

3   ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4   PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1   NuMicro® Mini58 Series Naming Rule

**ARM‑Based
32-bit Microcontroller**   **Mini58-X X X**

CPU Core
Corte®-M0

Flash ROM
58   : 32 KB Flash ROM

Package Type
L: LQFP 48 7x7mm
Z: QFN 33 5x5mm
T: QFN 33 4x4mm
F: TSSOP 20

Temperature
E: -40°C ~ +105°C

Reserved
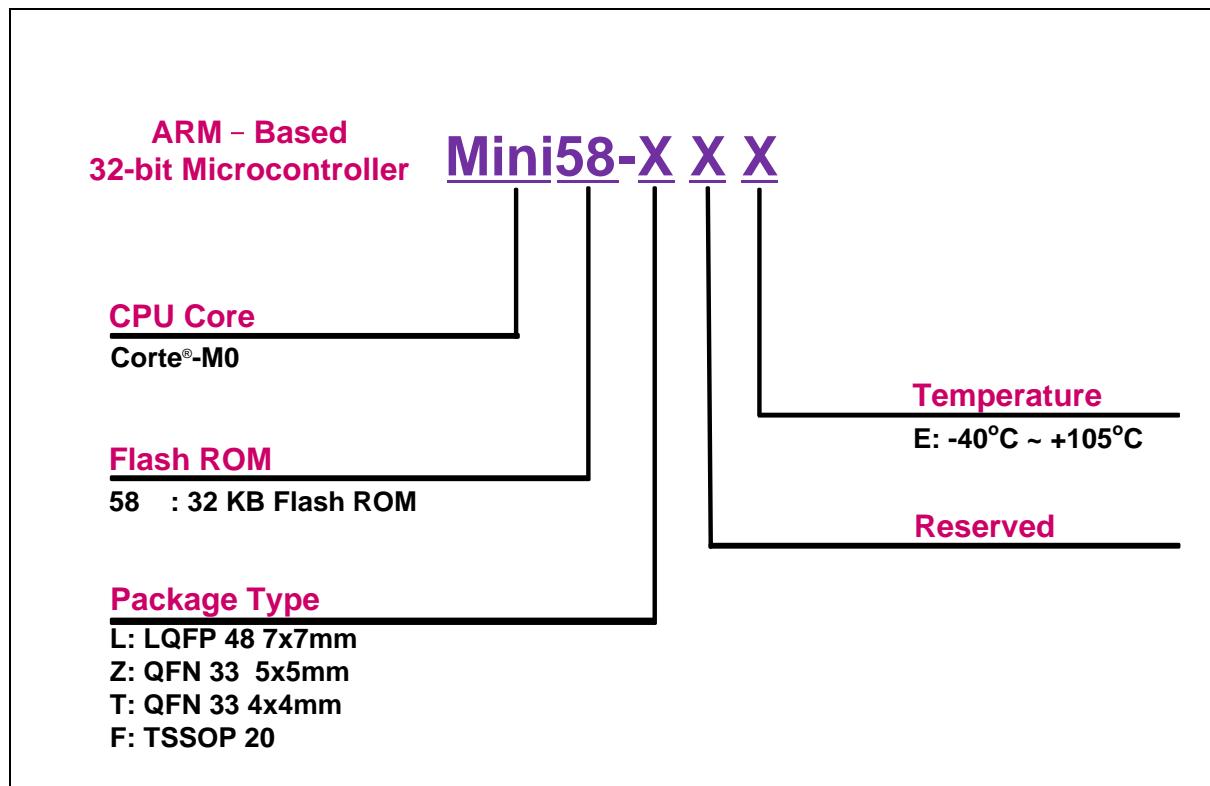
Figure 4.1-1 NuMicro® Mini58 Series Naming Rule

4.2 NuMicro® Mini58 Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I²C						
MINI58LDE	32 KB	4 KB	Configurable	2.5 KB	up to 30	2x32-bit	2	1	2	2	6	8x10-bit	v	v	LQFP48
MINI58ZDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(5x5)
MINI58TDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(4x4)
MINI58FDE	32 KB	4 KB	Configurable	2.5 KB	up to 17	2x32-bit	2	1	2	-	6	4x10-bit	v	v	TSSOP20

Table 4.2-1 NuMicro® Mini58 Series Product Selection Guide

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin
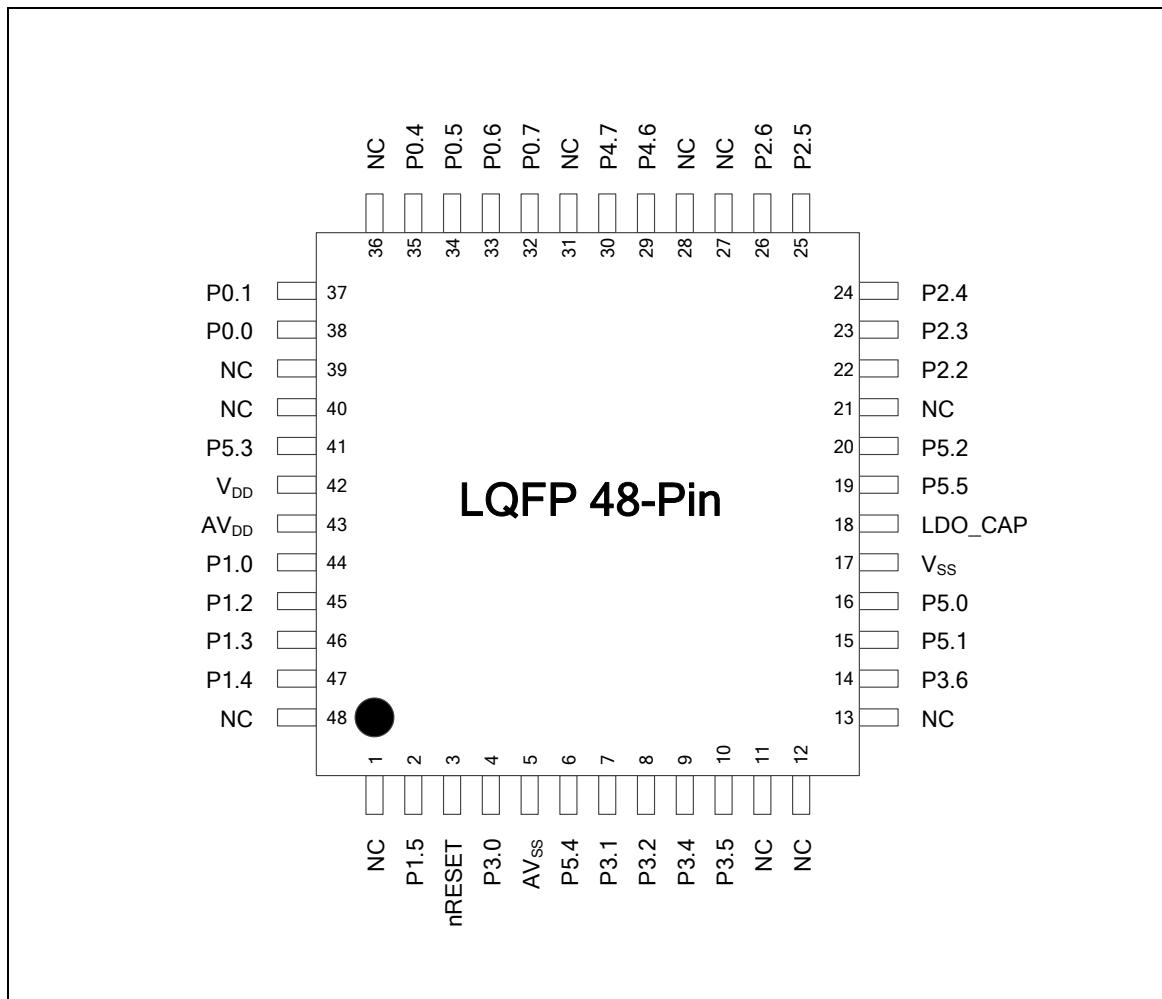
Figure 4.3-1 NuMicro® Mini58 Series LQFP 48-pin Diagram
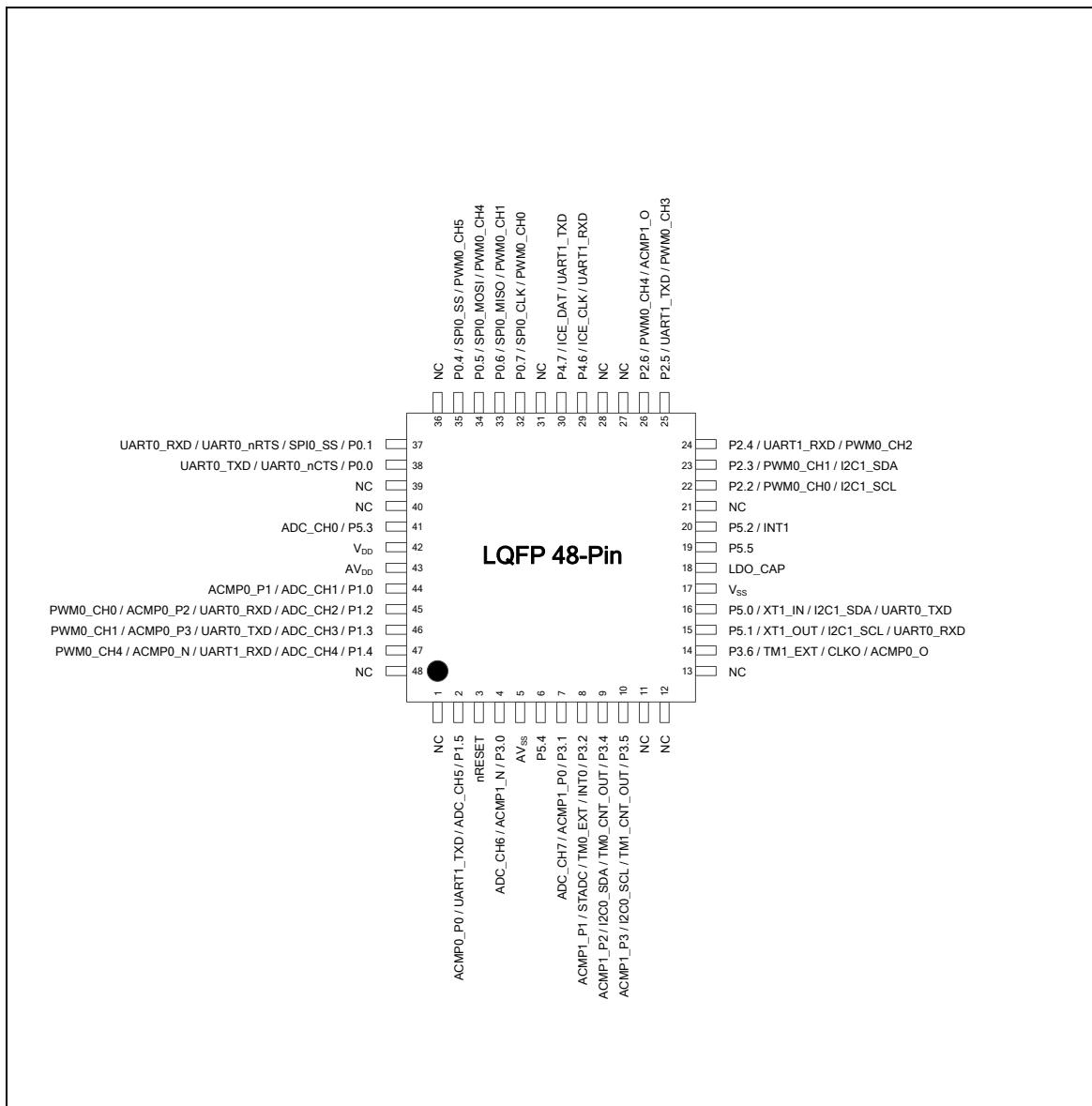
Figure 4.3-2 NuMicro® Mini58 Series LQFP 48-pin Multi-Function Diagram

4.3.2 QFN 33-pin
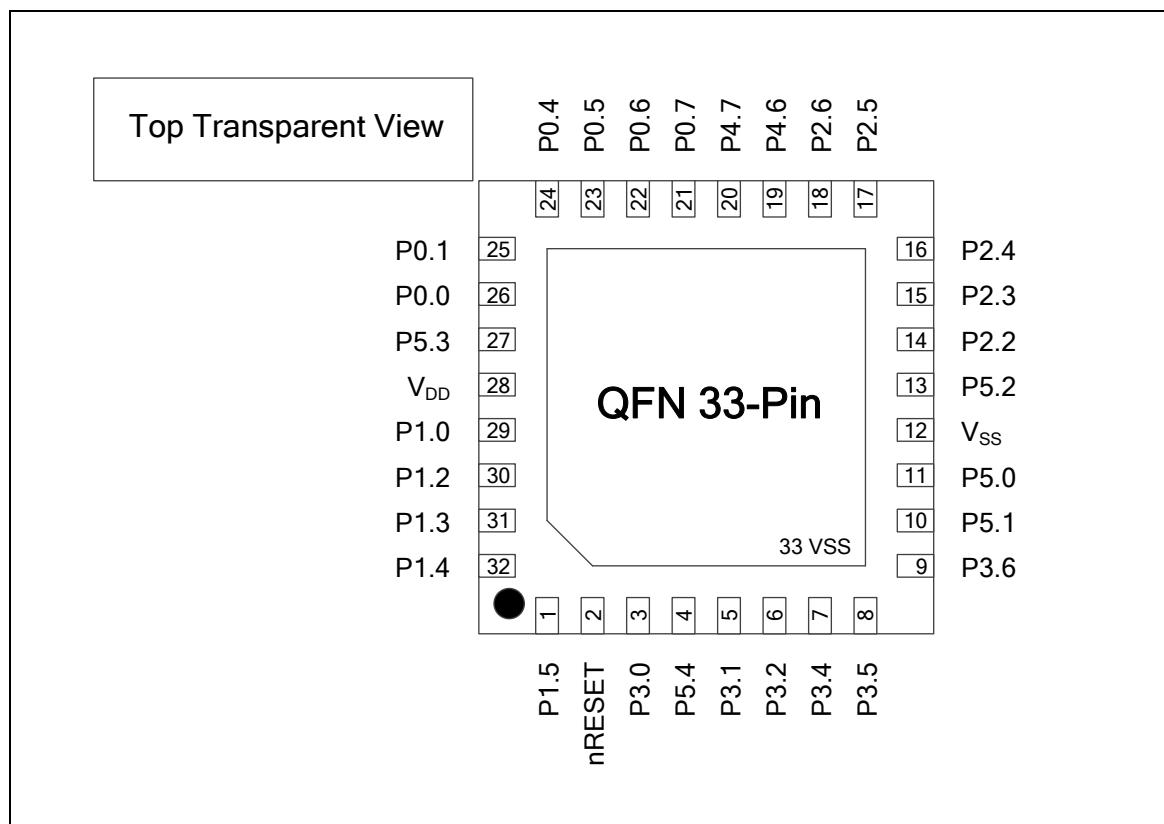
Figure 4.3-3 NuMicro® Mini58 Series QFN 33-pin Diagram
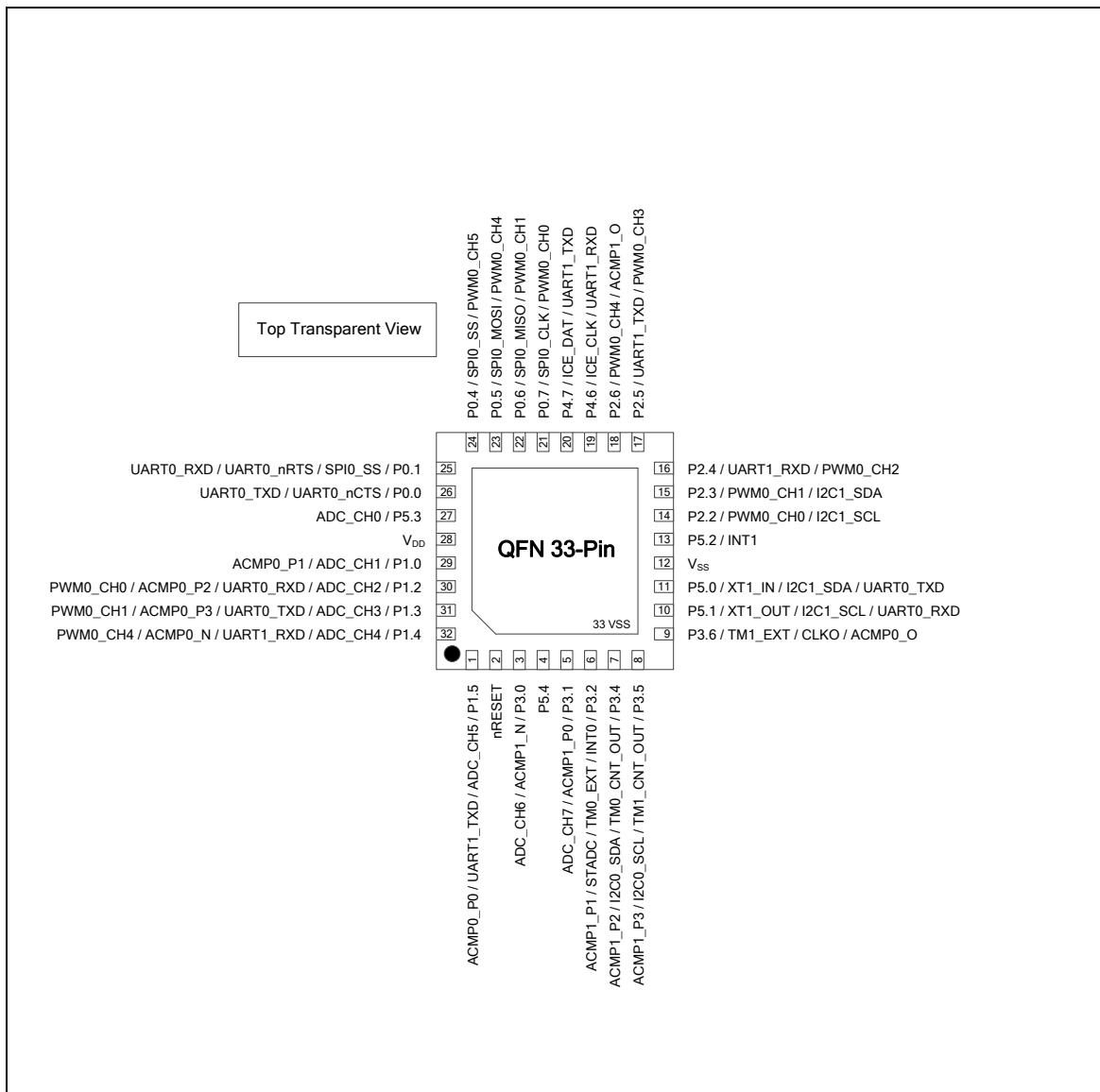
Figure 4.3-4 NuMicro® Mini58 Series QFN 33-pin Multi-funciton Diagram

4.3.3   TSSOP 20-pin
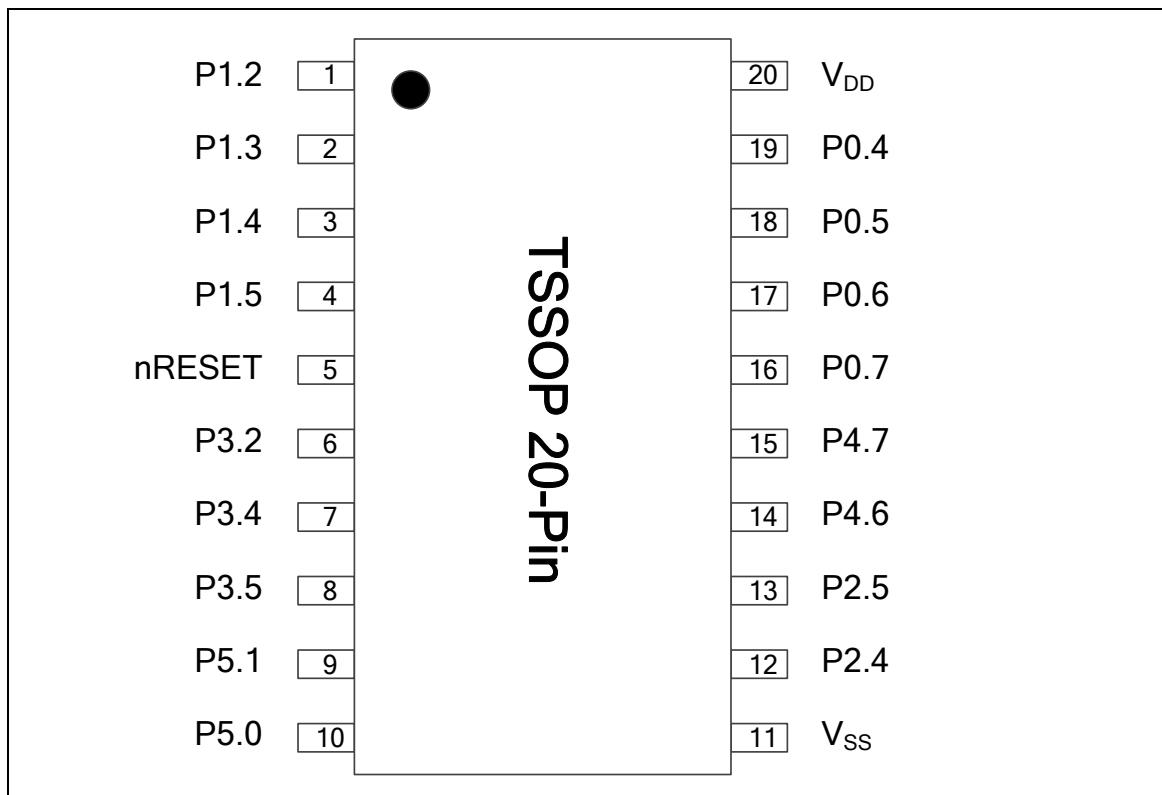
Figure 4.3-5 NuMicro® Mini58 Series TSSOP 20-pin Diagram
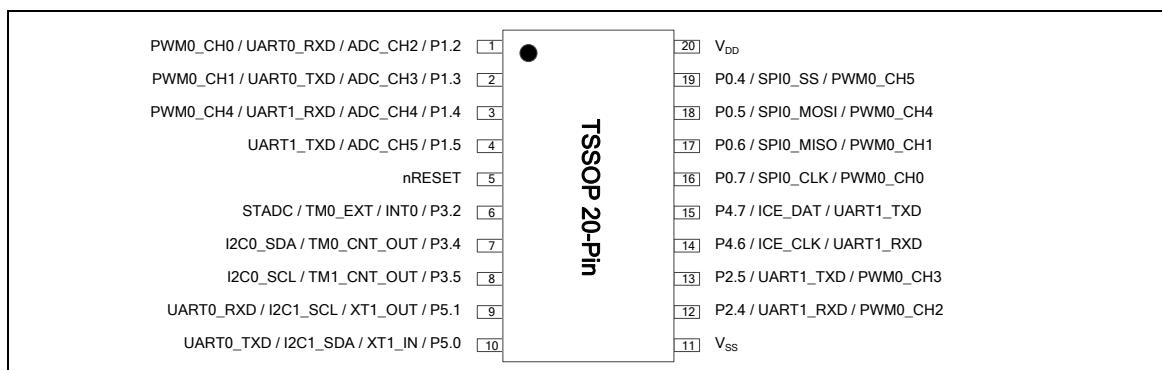
Figure 4.3-6 NuMicro® Mini58 Series TSSOP 20-pin Multi-function Diagram

4.4 Pin Description

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
1	---	---	NC	---	Not connected
2	1	4	P1.5	I/O	General purpose digital I/O pin
			ADC_CH5	AI	ADC analog input pin
			UART1_TXD	O	UART1 transmitter output pin
			ACMP0_P0	AI	Analog comparator positive input pin
3	2	5	nRESET	I(ST)	The Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
4	3	---	P3.0	I/O	General purpose digital I/O pin
			ADC_CH6	AI	ADC analog input pin
			ACMP1_N	AI	Analog comparator negative input pin
5	---	---	AV$_{SS}$	AP	Ground pin for analog circuit
6	4	---	P5.4	I/O	General purpose digital I/O pin
7	5	---	P3.1	I/O	General purpose digital I/O pin
			ADC_CH7	AI	ADC analog input pin
			ACMP1_P0	AI	Analog comparator positive input pin
8	6	6	P3.2	I/O	General purpose digital I/O pin
			INT0	I	External interrupt 0 input pin
			STADC	I	ADC external trigger input pin
			TM0_EXT	I/O	Timer 0 external capture / reset trigger input pin / toggle output pin
			ACMP1_P1	AI	Analog comparator positive input pin (not support in TSSOP20 package)
9	7	7	P3.4	I/O	General purpose digital I/O pin
			TM0_CNT_OUT	I/O	Timer 0 external event counter input pin / toggle output pin
			I2C0_SDA	I/O	I^{2}C0 data I/O pin
			ACMP1_P2	AI	Analog comparator positive input pin
10	8	8	P3.5	I/O	General purpose digital I/O pin
			TM1_CNT_OUT	I/O	Timer 1 external event counter input pin / toggle output pin
			I2C0_SCL	I/O	I^{2}C0 clock I/O pin
			ACMP1_P3	AI	Analog comparator positive input pin

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
11	---	---	NC	---	Not connected
12	---	---	NC	---	Not connected
13	---	--	NC	---	Not connected
14	9	---	P3.6	I/O	General purpose digital I/O pin
			ACMP0_O	O	Analog comparator output pin
			CLKO	O	Frequency divider output pin
			TM1_EXT	I/O	Timer 1 external capture / reset trigger input pin / toggle output pin
15	10	9	P5.1	I/O	General purpose digital I/O pin
			XT1_OUT	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XT1_IN.
			I2C1_SCL	I/O	I^{2}C1 clock I/O pin
			UART0_RXD	I	UART0 data receiver input pin
16	11	10	P5.0	I/O	General purpose digital I/O pin
			XT1_IN	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
			I2C1_SDA	I/O	I^{2}C1 data I/O pin
			UART0_TXD	O	UART0 transmitter output pin
17	12	11	V$_{SS}$	P	Ground pin for digital circuit
	33				
18	---	---	LDO_CAP	P	LDO output pin
19	---	---	P5.5	I/O	General purpose digital I/O pin User program must enable pull-up resistor in the QFN-33 package.
20	13	---	P5.2	I/O	General purpose digital I/O pin
			INT1	I	External interrupt 1 input pin
21	---	---	NC	---	Not connected
22	14	---	P2.2	I/O	General purpose digital I/O pin
			PWM0_CH0	O	PWM0 output of PWM unit
			I2C1_SCL	I/O	I^{2}C1 clock I/O pin
23	15	---	P2.3	I/O	General purpose digital I/O pin
			PWM0_CH1	O	PWM1 output of PWM unit
			I2C1_SDA	I/O	I^{2}C1 data I/O pin
24	16	12	P2.4	I/O	General purpose input/output digital pin
			UART1_RXD	I	UART1 data receiver input pin

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
			PWM0_CH2	O	PWM2 output of PWM unit
25	17	13	P2.5	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 transmitter output pin
			PWM0_CH3	O	PWM3 output of PWM unit
26	18	---	P2.6	I/O	General purpose digital I/O pin
			PWM0_CH4	O	PWM4 output of PWM unit
			ACMP1_O	O	Analog comparator output pin
27	---	---	NC	---	Not connected
28	---	---	NC	---	Not connected
29	19	14	P4.6	I/O	General purpose digital I/O pin
			ICE_CLK	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
			UART1_RXD	I	UART1 data receiver input pin
30	20	15	P4.7	I/O	General purpose digital I/O pin
			ICE_DAT	I/O	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
			UART1_TXD	O	UART1 transmitter output pin
31	---	---	NC	---	Not connected
32	21	16	P0.7	I/O	General purpose digital I/O pin
			SPI0_CLK	I/O	SPI serial clock pin
			PWM0_CH0	O	PWM0 output of PWM unit
33	22	17	P0.6	I/O	General purpose digital I/O pin
			SPI0_MISO	I/O	SPI MISO (master in/slave out) pin
			PWM0_CH1	O	PWM1 output of PWM unit
34	23	18	P0.5	I/O	General purpose digital I/O pin
			SPI0_MOSI	O	SPI MOSI (master out/slave in) pin
			PWM0_CH4	O	PWM4 output of PWM unit
35	24	19	P0.4	I/O	General purpose digital I/O pin
			SPI0_SS	I/O	SPI slave select pin
			PWM0_CH5	O	PWM5 output of PWM unit
36	---	---	NC	---	Not connected
37	25	---	P0.1	I/O	General purpose digital I/O pin

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
			UART0_nRTS	O	UART0 RTS pin
			UART0_RXD	I	UART0 data receiver input pin
			SPI0_SS	I/O	SPI slave select pin
38	26	---	P0.0	I/O	General purpose digital I/O pin
			UART0_nCTS	I	UART0 CTS pin
			UAR0_TXD	O	UART0 transmitter output pin
39	---	---	NC	---	Not connected
40	---	---	NC	---	Not connected
41	27	---	P5.3	I/O	General purpose digital I/O pin
			ADC_CH0	AI	ADC analog input pin
42	28	20	V_{DD}	P	Power supply for digital circuit
43			AV_{DD}	P	Power supply for analog circuit
44	29	---	P1.0	I/O	General purpose digital I/O pin
			ADC_CH1	AI	ADC analog input pin
			ACMP0_P1	AI	Analog comparator positive input pin
45	30	1	P1.2	I/O	General purpose digital I/O pin
			ADC_CH2	AI	ADC analog input pin
			UART0_RXD	I	UART0 data receiver input pin
			ACMP0_P2	AI	Analog comparator positive input pin (not support in TSSOP20 package)
			PWM0_CH0	O	PWM0 output of PWM unit
46	31	2	P1.3	I/O	General purpose digital I/O pin
			ADC_CH3	AI	ADC analog input pin
			UART0_TXD	O	UART0 transmitter output pin
			ACMP0_P3	AI	Analog comparator positive input pin (not support in TSSOP20 package)
			PWM0_CH1	O	PWM1 output of PWM unit
47	32	3	P1.4	I/O	General purpose digital I/O pin
			ADC_CH4	I/O	ADC analog input pin
			UART1_RXD	I	UART1 data receiver input pin
			ACMP0_N	AI	Analog comparator negative input pin (not support in TSSOP20 package)
			PWM0_CH4	O	PWM4 output of PWM unit

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
48	---	--	NC	---	Not connected

Table 4.4-1 NuMicro® Mini58 Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

5 BLOCK DIAGRAM

5.1 NuMicro® Mini58 Block Diagram
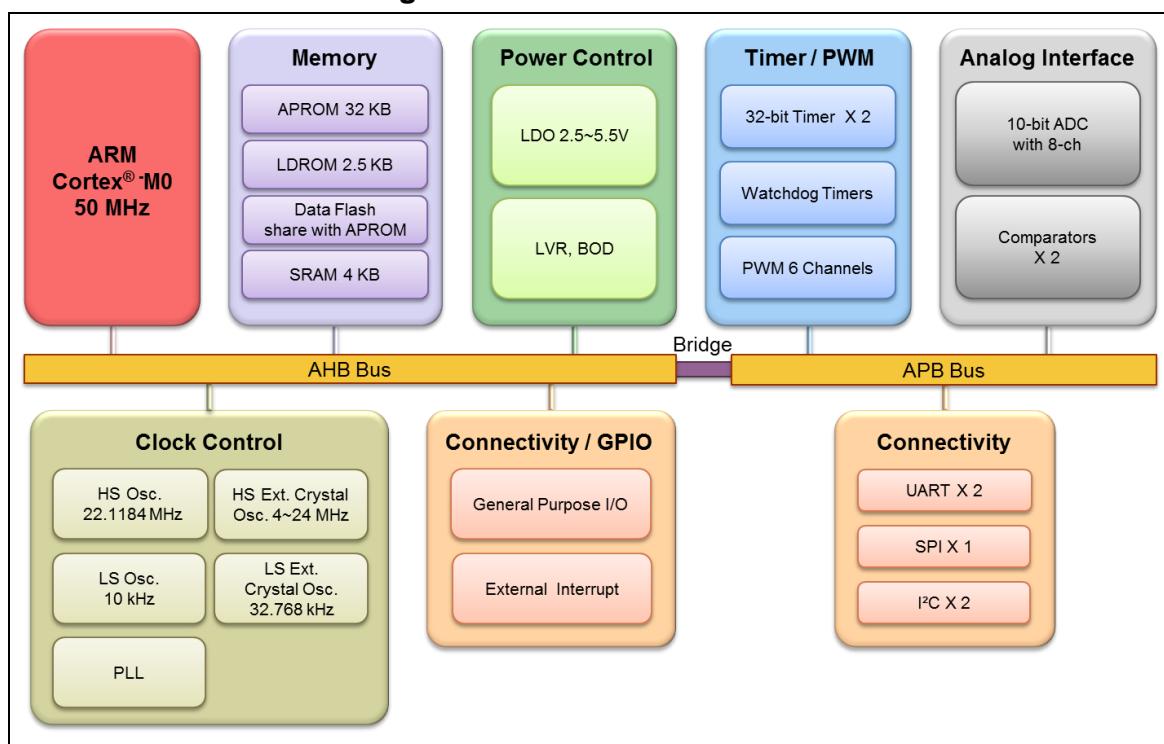
Figure 5.1-1 NuMicro® Mini58 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

6.1.1 Overview

The Cortex®-M0 processor, a configurable, multistage, 32-bit RISC processor, has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of the processor.
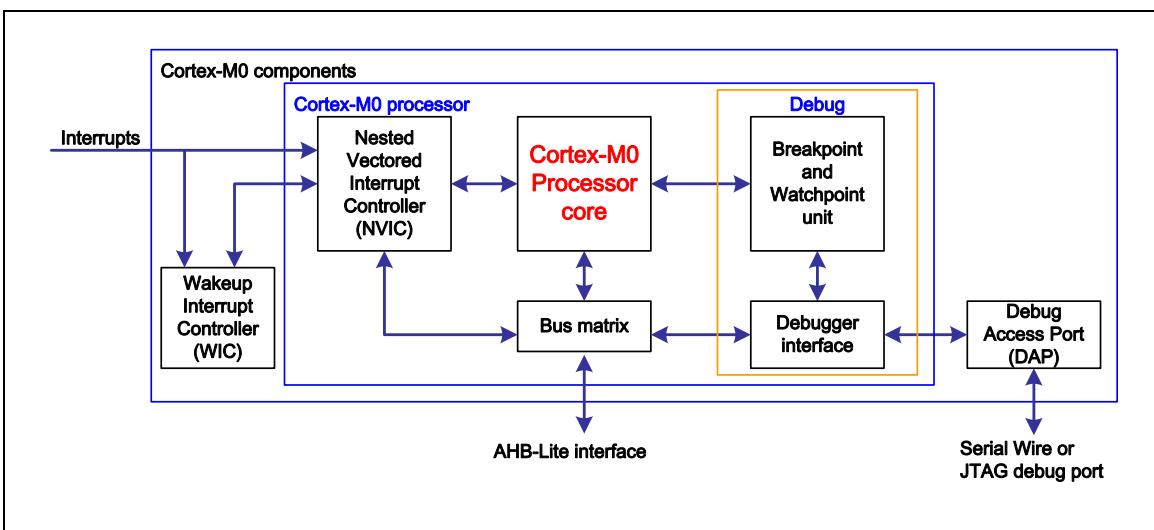
Figure 6.1-1 Functional Block Diagram

6.1.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode
- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - ◆ Power-on Reset (POR)
  - ◆ Low level on the nRESET pin
  - ◆ Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - ◆ Low Voltage Reset (LVR)
  - ◆ Brown-out Detector Reset (BOD Reset)
  - ◆ CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (SCS_AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])
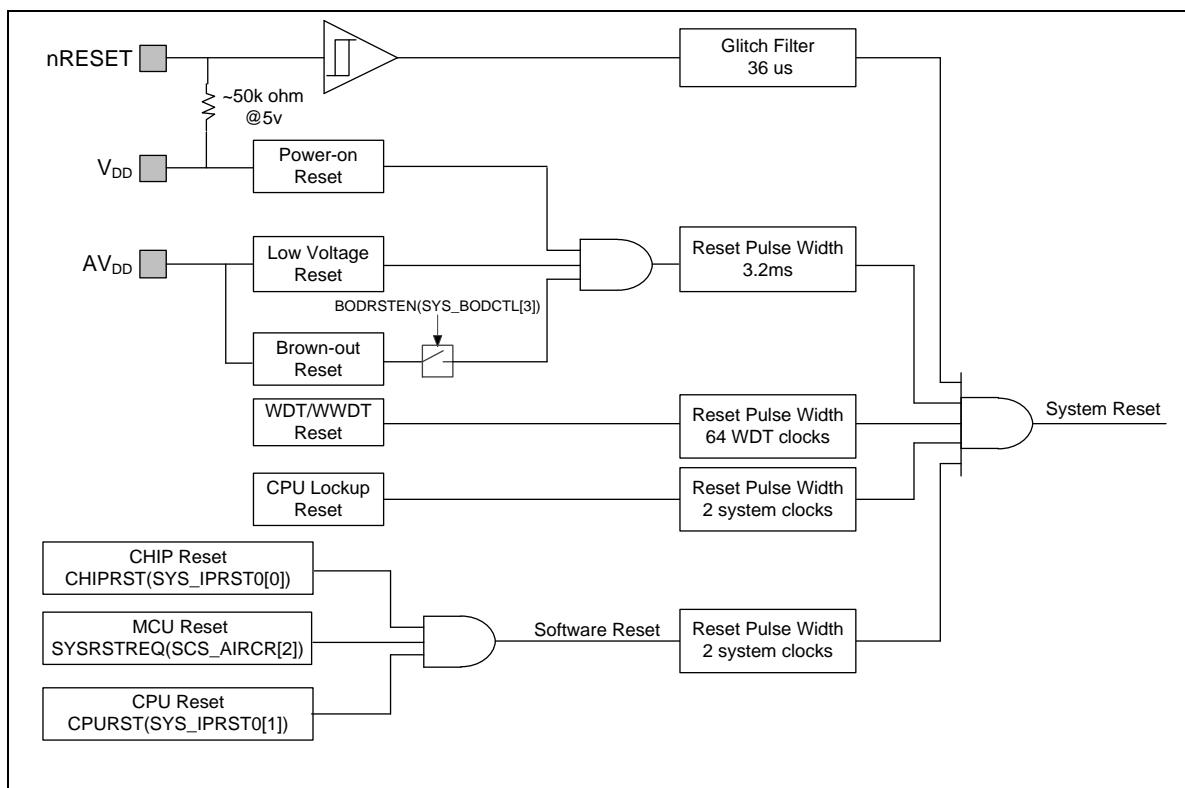
Figure 6.2-1 System Rese Resources

There are a total of 9 reset sources in the NuMicro[®] family. In general, CPU reset is used to reset Cortex[®]-M0 only; the other reset sources will reset Cortex[®]-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-5.

Reset Sources / Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	0x001	Bit 1 = 1	Bit 2 = 1	0x001	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0]) **BODVL** (SYS_BODCTL[2:1]) **BODRSTEN** (SYS_BODCTL[3])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
XTLEN (CLK_PWRCTL[1:0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x8	0x8	0x8	0x8	0x8	0x8	0x8	0x8	-

WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
XLTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
LIRCSTB (CLK_STATUS[3])	0x0								
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
WDT_CTL	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1]) ISPEN (FMC_ISPCTL[16])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[20:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 36 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 36 us (glitch filter). The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.
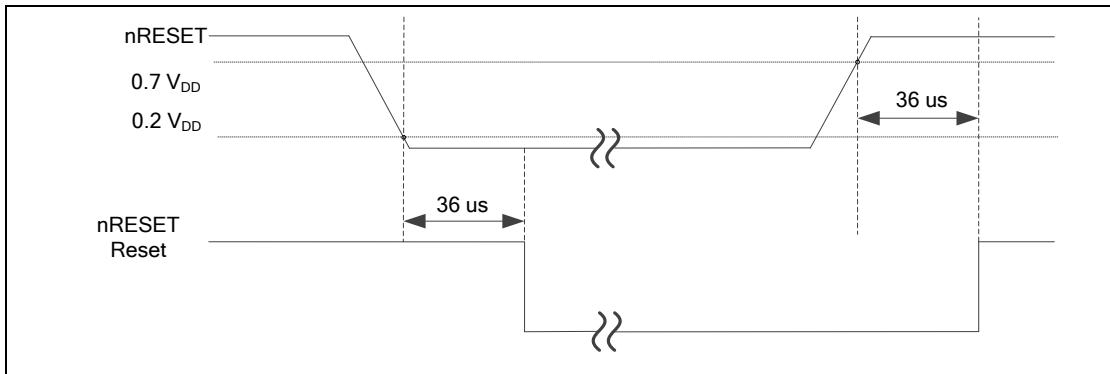
Figure 6.2-2 nRESET Reset Waveform

6.2.2.2   Power-On Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF (SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF (SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the waveform of Power-On reset.
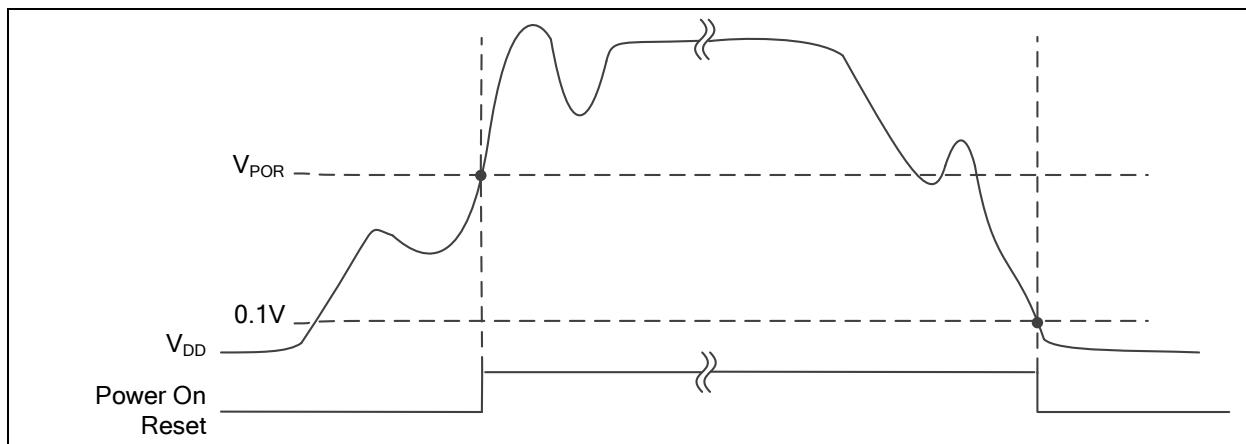
Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3   Low Voltage Reset (LVR)

Low Voltage Reset detects AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time (16*HCLK cycles), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time. The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-4 shows the Low Voltage Reset waveform.
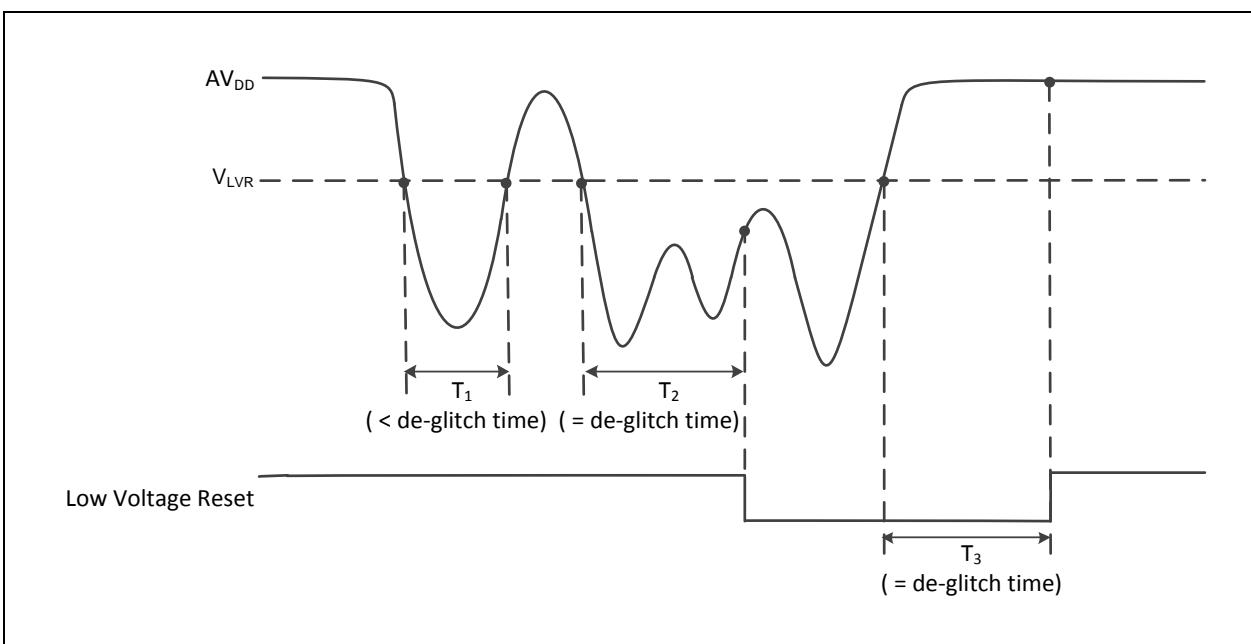
Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-Out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN (SYS_BODCTL[0]) and BODVL (SYS_BODCTL[2:1]) and the state keeps longer than De-glitch time (Max(20*HCLK cycles, 1*LIRC cycle)), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time. The default value of BODEN, BODVL and BODRSTEN is set by flash controller user configuration register CBOVEXT (CONFIG0[23]), CBOV (CONFIG0[22:21]) and CBORST (CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-Out Detector waveform.
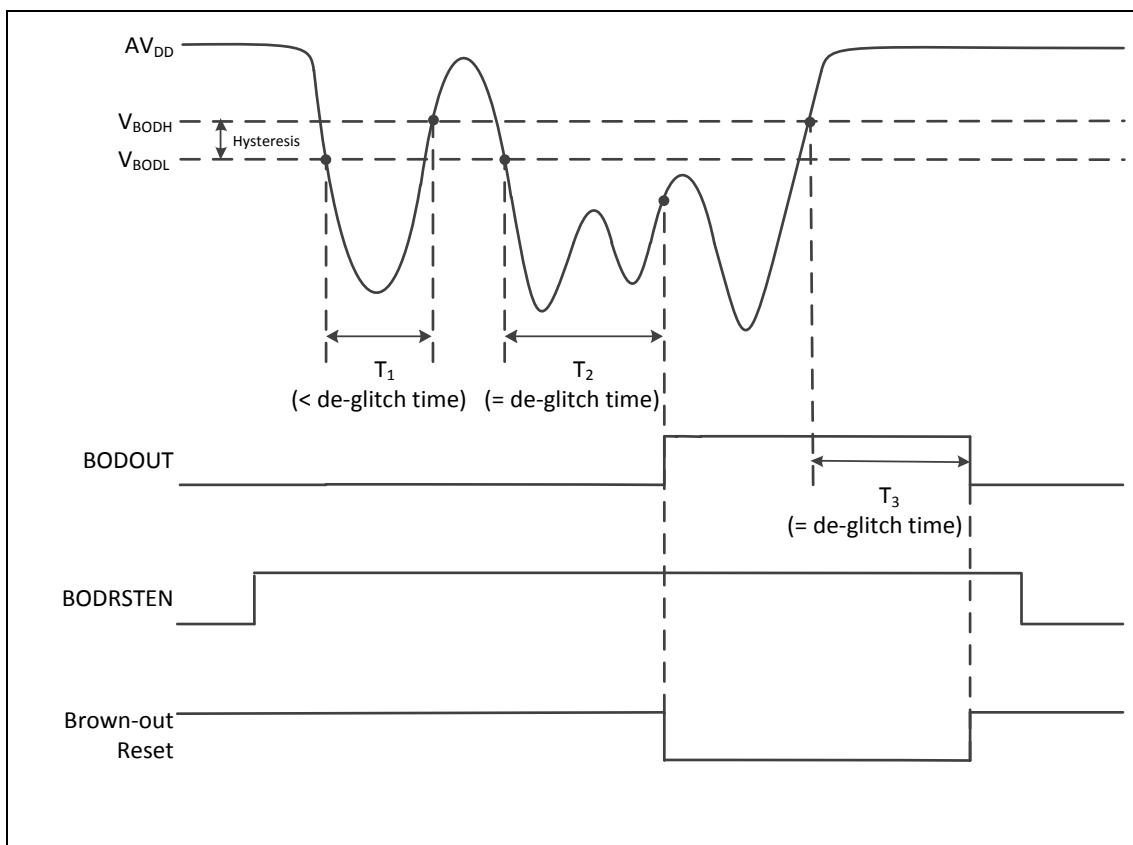
Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watch Dog Timer Reset

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watch dog timer (WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watch dog time-out. User may decide to enable system reset during watch dog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watch dog time-out to indicate the previous reset is a watch dog reset and handle the failure of MCU after watch dog time-out reset by checking WDTRF (SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and SYSTEM Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST (SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-On Reset. The CPU and all peripherals are reset and BS

(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG setting. User can set the CHIPRST (SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS (FMC_ISPCTL[1]) will not be reloaded from CONFIG setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ (SCS_AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD and GPIO
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table
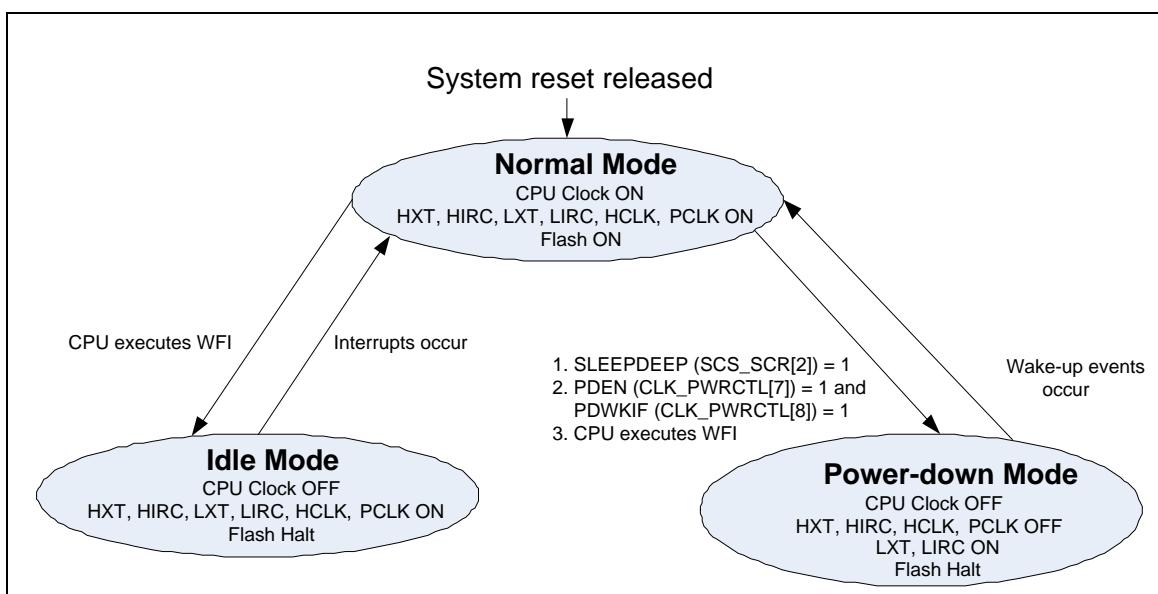
Figure 6.2-6 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in run mode.

2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in run mode.

3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.

4. If WDT clock source is selected as LIRC and LIRC is on.

	Normal Mode	Idle Mode	Power-down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (12/16 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
WWDT	ON	ON	Halt
UART	ON	ON	Halt
I^{2}C	ON	ON	Halt
SPI	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, BOD and GPIO

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN (CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-up Source	Wake-up condition	System can enter Power-down mode again condition*

BOD	Brown-Out Detector Interrupt	After software writes 1 to clear SYS_BODCTL[BODIF].
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
UART	nCTS wake-up	After software writes 1 to clear CTSWKIF (UARTx_INTSTS[16]).
I^{2}C	Falling edge in the I2C_SDA or I2C_CLK	After software writes 1 to clear WKIF (I2C_STATUS1[0]).

Table 6.2-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Architecture

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.

- Digital power from V_{DD} and V_{SS} supplies power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.

- Built-in a capacitor for internal voltage regulator

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). Figure 6.2-7 shows the power distribution of the Mini58 series.
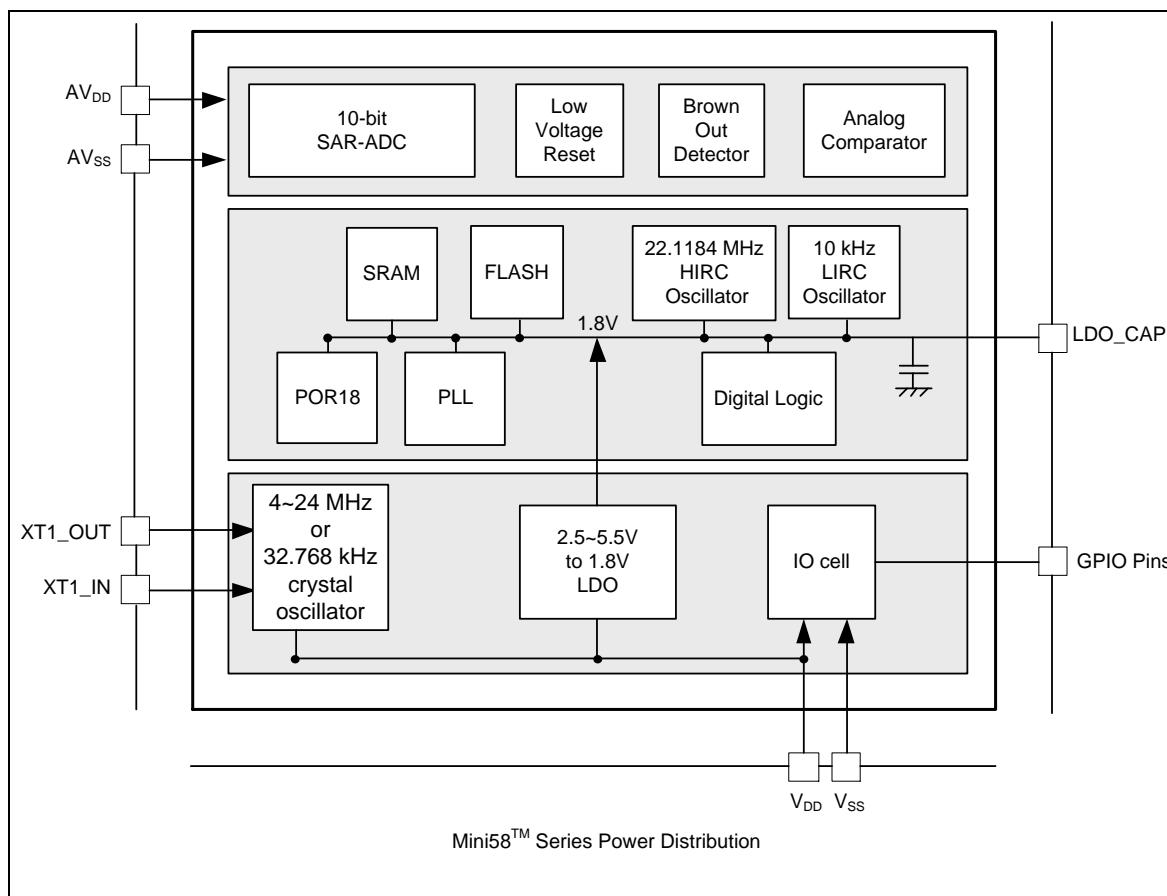
Figure 6.2-7 NuMicro® Mini58 Series Power Architecture Diagram

6.2.5 System Memory Mapping

Mini58				System Control		
4 GB	Reserved	0xFFFF_FFFF | 0xE000_F000		System Control	0xE000_ED00	SCS_BA
				External Interrupt Control	0xE000_E100	SCS_BA
	System Control	0xE000_EFFF 0xE000_E000		System Timer Control	0xE000_E010	SCS_BA
	Reserved	0xE000_E00F | 0x6002_0000				
	Reserved	0x6001_FFFF 0x6000_0000				
	Reserved	0x5FFF_FFFF | 0x5020_0000		AHB peripherals		
	AHB	0x501F_FFFF 0x5000_0000		FMC	0x5000_C000	FMC_BA
				GPIO Control	0x5000_4000	GP_BA
	Reserved	0x4FFF_FFFF | 0x4020_0000		Interrupt Multiplexer Control	0x5000_0300	INT_BA
				Clock Control	0x5000_0200	CLK_BA
	APB	0x401F_FFFF | 0x4000_0000		System Global Control	0x5000_0000	SYS_BA
1 GB	Reserved	0x3FFF_FFFF | 0x2000_1000		APB peripherals		
				UART1 Control	0x4015_0000	UART1_BA
				I^{2}C1 Control	0x4012_0000	I2C1_BA
				ADC Control	0x400E_0000	ADC_BA
				ACMP Control	0x400D_0000	CMP_BA
				UART0 Control	0x4005_0000	UART0_BA
	4 KB SRAM	0x2000_0FFF 0x2000_0000		PWM Control	0x4004_0000	PWM_BA
0.5 GB				SPI Control	0x4003_0000	SPI_BA
	Reserved	0x1FFF_FFFF | 0x0000_8000		I^{2}C0 Control	0x4002_0000	I2C0_BA
				Timer0/Timer1 Control	0x4001_0000	TMR_BA
				WWDT Control	0x4000_4100	WWDT_BA
	32 KB on-chip Flash (Mini58)	0x0000_7FFF | 0x0000_0000		WDT Control	0x4000_4000	WDT_BA
0 GB						

Table 6.2-5 Memory Mapping Table

6.2.6 Memory Organization

6.2.6.1 Overview

The NuMicro® Mini58 series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers is shown the following table. The detailed register definition, addressing space, and programming details will be described in the following sections for each

on-chip peripheral. The Mini58 series only supports little-endian data format.

6.2.6.2   System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Addressing Space	Token	Modules
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_7FFF	FLASH_BA	Flash Memory Space (32 KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4 KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO (P0~P5) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB Modules Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_00FF	WDT_BA	Watchdog Timer Control Registers
0x4000_4100 – 0x4000_47FF	WWDT_BA	Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI with Master/slave Function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
System Control Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Block Registers

Table 6.2-6 Address Space Assignments for On-Chip Modules

6.2.7 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer to count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.8 Nested Vectored Interrupt Controller (NVIC)

6.2.8.1 Overview

The Cortex®-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features.

6.2.8.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority change
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the Interrupt Service Routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.8.3 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro® Mini58 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as 0 and the lowest priority is denoted as 3. The default priority of all the user-configurable interrupts is 0. Note that the priority 0 is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-7 Exception Model

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
1 ~ 15	-	**-**	-	System exceptions	-
16	0	**BODOUT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM Brake interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	**-**	-	-	
28	12	**UART0_INT**	UART0	UART0 interrupt	Yes
29	13	**UART1_INT**	UART1	UART1 interrupt	Yes
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	**-**	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt	Yes

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
35	19	**I2C1_INT**	I^{2}C1	I^{2}C1 interrupt	No
36 ~ 40	20 ~ 24	**-**	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or Comparator 1 interrupt	Yes
42 ~ 43	26 ~ 27	**-**	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	**-**	-	-	

Table 6.2-8 System Interrupt Map Vector Table

6.2.8.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-9 Vector Table Format

6.2.8.5 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.9 System Control Registers (SCB)

The Cortex®-M0 status and operating mode control are managed System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PDEN (CLK_PWRCTL[7]) bit is set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 3 sources as listed below:

● 4~24 MHz external high speed crystal oscillator (HXT) or 32.768 kHz (LXT) external low speed crystal oscillator

● Programmable PLL output clock frequency (PLL source can be selected from external 4 ~ 24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)) (PLL FOUT)

● 22.1184 MHz internal high speed RC oscillator (HIRC)

● 10 kHz internal low speed RC oscillator (LIRC)
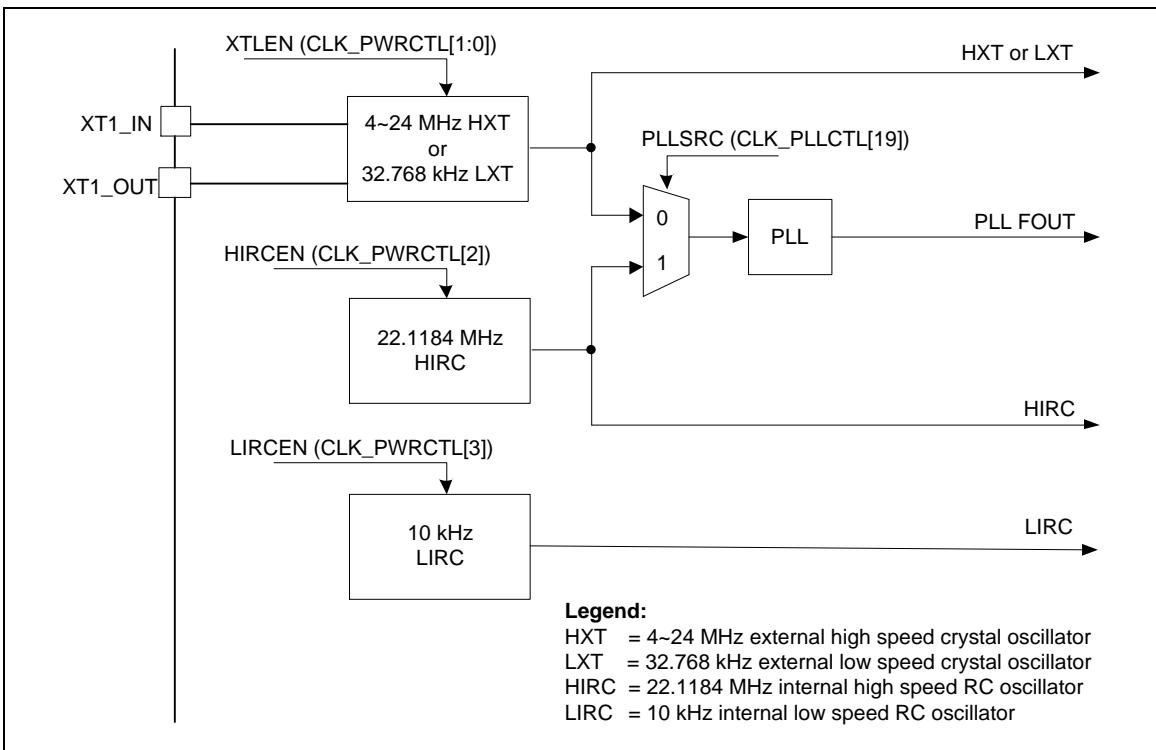
Figure 6.3-1 Clock Generator Block Diagram
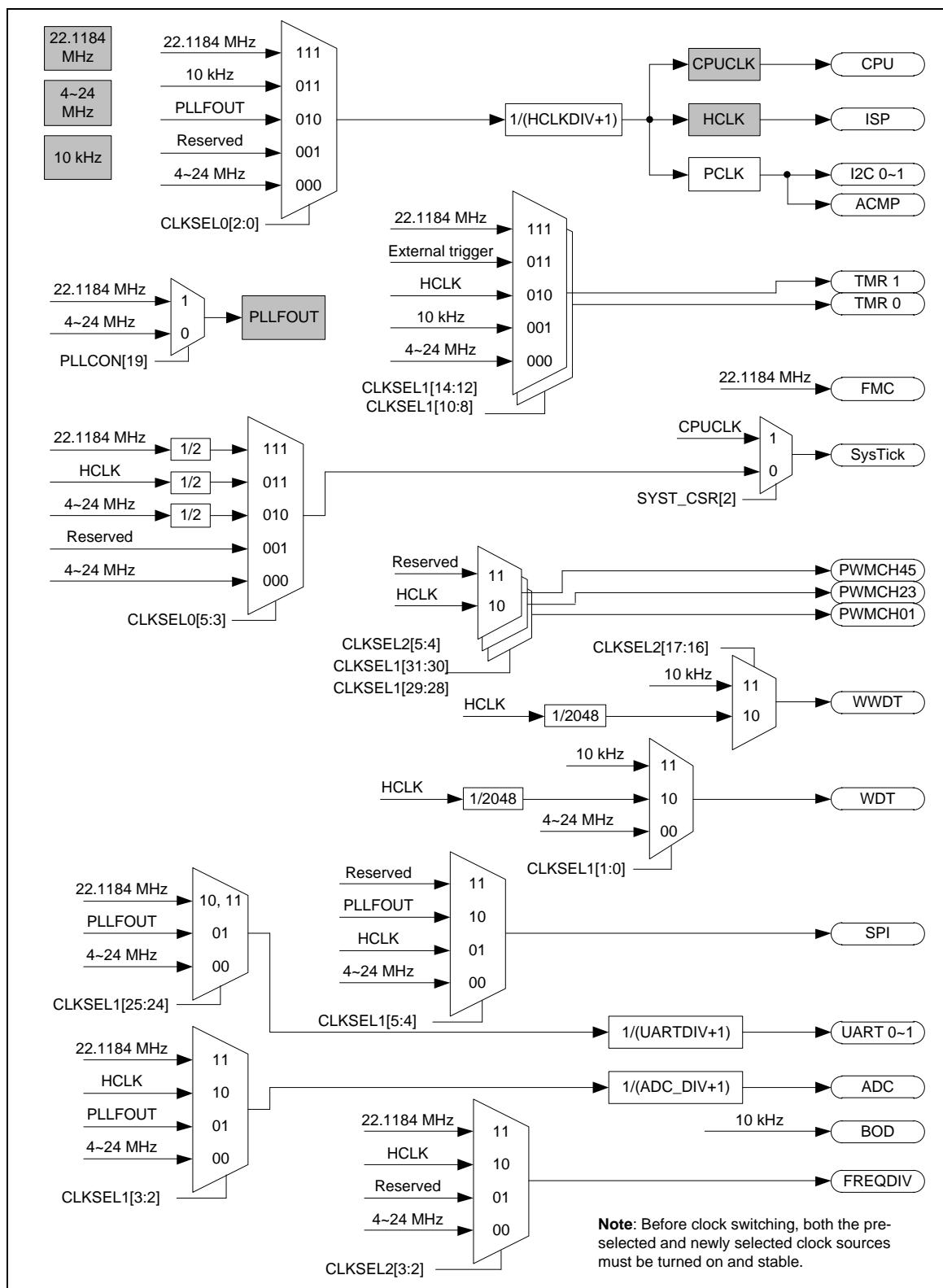
Figure 6.3-2 Clock Generator Global View Diagram

6.3.2   Auto-trim

This chip supports auto-trim function: the HIRC trim (22.1184 MHz internal RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 1 % deviation within all temperature ranges. For instance, the system needs an accurate 22.1184 MHz clock. In such case, if users do not want to use 22.1184 MHz HXT as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL[0] trim frequency selection) to "1", and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) high indicates the HIRC output frequency is accurate within 1% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to "11".

6.3.3   System Clock and SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.
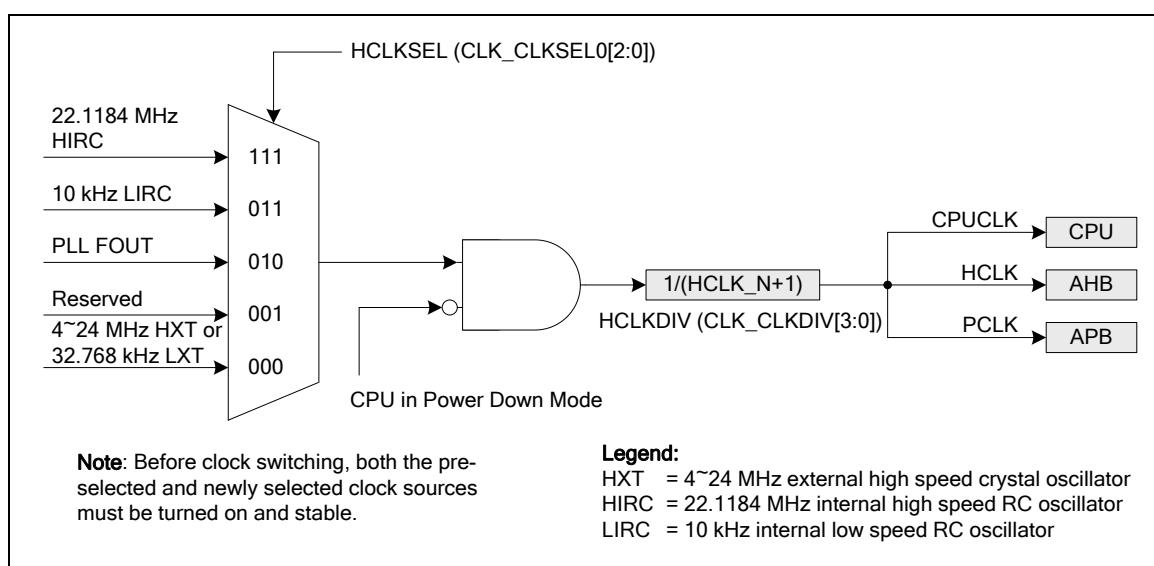
Figure 6.3-3 System Clock Block Diagram

The source of PCLK is equal to HCLK in system clock architecture.

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock CLKSRC(SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-4.

STCLKSEL (CLK_CLKSEL0[5:3])

22.1184 MHz
HIRC
1/2 → 111

HCLK
1/2 → 011
4~24 MHz HXT or
32.768 kHz LXT
1/2 → 010

Reserved → 001
4~24 MHz HXT or
32.768 kHz LXT → 000

STCLK

Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Legend:
HXT = 4~24 MHz external high speed crystal oscillator
HIRC = 22.1184 MHz internal high speed RC oscillator
LIRC = 10 kHz internal low speed RC oscillator

Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.4   Peripherals Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please note that, while switching clock source from one to another, user must wait until both clock sources are running stabled.

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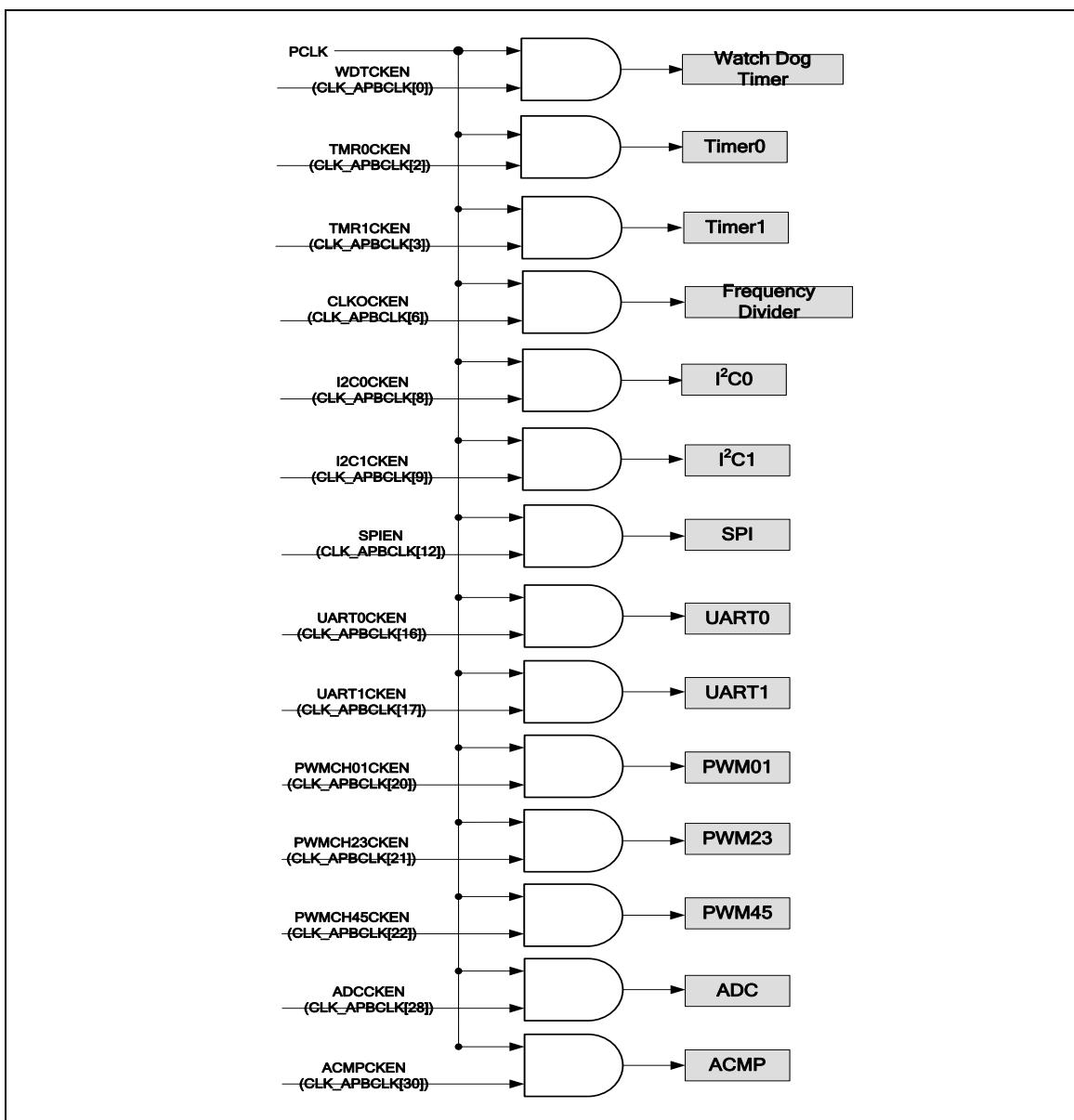
Figure 6.3-5 Peripherals Bus Clock Source Selection for PCLK

	Peripheral Clok Selectable	Ext. CLK (HXT Or LXT)	HIRC	LIRC	HCLK	PLL
WDT	Yes	Yes	No	Yes	Yes	No
WWDT	Yes	Yes	No	Yes	Yes	No
Timer0	Yes	Yes	Yes	Yes	Yes	No
Timer1	Yes	Yes	Yes	Yes	Yes	No
I^{2}C0	No	-	-	-	-	-
I^{2}C1	No	-	-	-	-	-
SPI	Yes	Yes	No	No	Yes	Yes
UART0	Yes	Yes	Yes	No	No	Yes
UART1	Yes	Yes	Yes	No	No	Yes
PWM	No	-	-	-	-	-
ADC	Yes	Yes	Yes	No	Yes	Yes
ACMP	No	-	-	-	-	-

Table 6.3-1 Peripheral Clock Source Selection Table

Note: For the peripherals those peripheral clock are not selectable, its clock source is fixed to PCLK.

6.3.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PDLXT = 1 and XTLEN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CLKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIV1EN (CLK_CLKOCTL[5]) set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.
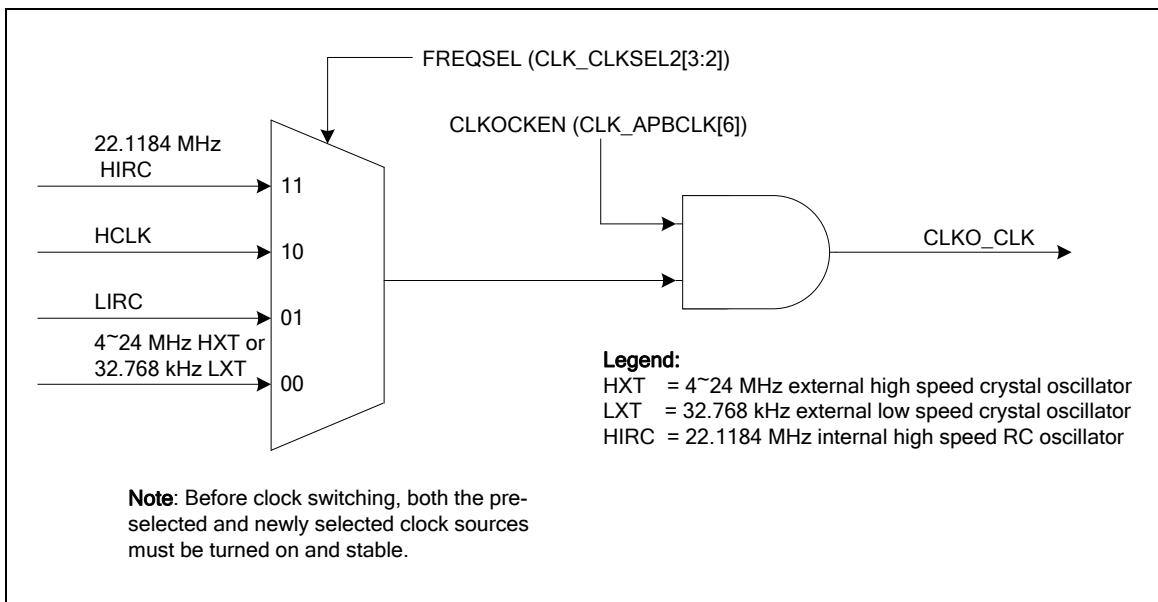
Figure 6.3-6 Clock Source of Frequency Divider
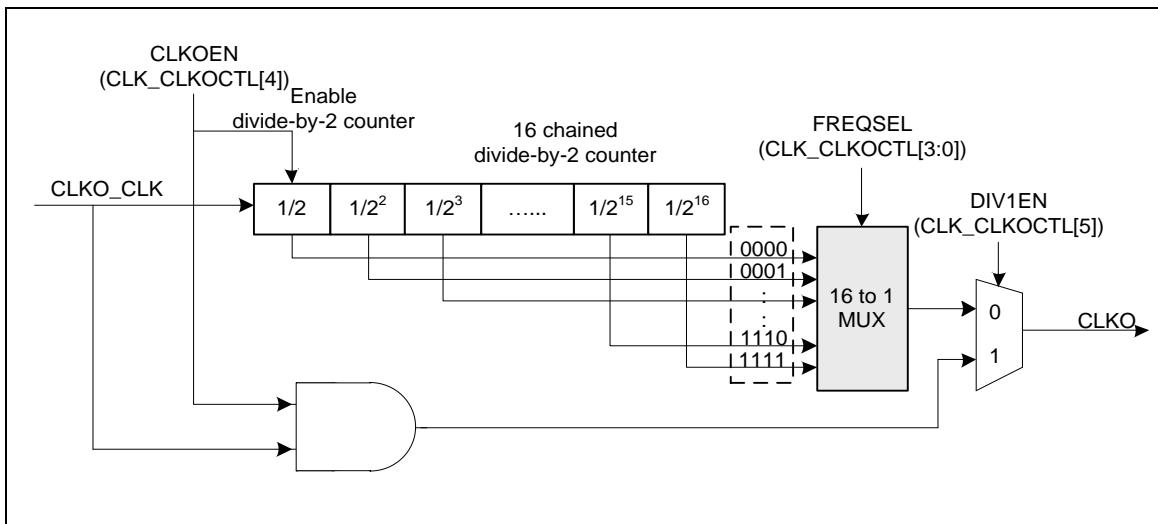
Figure 6.3-7 Block Diagram of Frequency Divider

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® Mini58 series is equipped with 32 Kbytes on-chip embedded flash for application and Data Flash to store some application dependent data. A User Configuration block provides for system initialization. A 2.5 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 512 bytes security protection ROM (SPROM) can conceal user program. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

6.4.2 Features

- Supports 32 Kbytes application ROM (APROM).
- Supports 2.5 Kbytes loader ROM (LDROM).
- Supports configurable Data Flash size to share with APROM.
- Supports 512 bytes security protection ROM (SPROM) to conceal user program.
- Supports 12 bytes User Configuration block to control system initialization.
- Supports 512 bytes page erase for all embedded flash.
- Supports CRC-32 checksum calculation function.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® Mini58 series has up to 30 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 30 pins are arranged in 6 ports named as P0, P1, P2, P3, P4 and P5. Each of the 30 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each pin can be configured by software individually as Input, Push-pull output, Open-drain output, or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins is stay in input mode and each port data register Px_DOUT[n] resets to 1. For Quasi-bidirectional mode, each I/O pin is equipped with a very weak individual pull-up resistor about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - ◆ Quasi-bidirectional mode
  - ◆ Push-pull output
  - ◆ Open-drain output
  - ◆ Input-only with high impendence
- Quasi-bidirectional TTL/Schmitt trigger input mode selected by SYS_Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- High driver and high sink I/O mode support
- Configurable default I/O mode of all pins after reset by CIOINI (Config0[10]) setting
  - ◆ CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - ◆ CIOINI = 1, all GPIO pins in Input tri-state mode after chip reset

6.6 Timer Controller (TMR)

6.6.1 Overview

The Timer Controller includes two 32-bit timers, TMR0 and TMR1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Two sets of 32-bit timer with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMRTx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports internal capture triggered while internal ACMP output signal transition

6.7 Enhanced PWM Generator

6.7.1 Overview

The NuMicro® Mini58 series has built in one PWM unit (PWM0) which is specially designed for motor driving control applications. The PWM0 supports six PWM generators which can be configured as six independent PWM outputs, PWM0_CH0~PWM0_CH5, or as three complementary PWM pairs, (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3) and (PWM0_CH4, PWM0_CH5) with three programmable dead-time generators.

Every complementary PWM pairs share one 8-bit prescaler. There are six clock dividers providing five divided frequencies (1, 1/2, 1/4, 1/8, 1/16) for each channel. Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide twelve independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer, ACMP and ADC to work together. In order to control motor more precisely, we provide some registers that not only configure PWM but also Timer, ADC and ACMP, by doing so, it can save more CPU time and control motor with ease especially in BLDC.

6.7.2 Features

The PWM0 supports the following features:

- Six independent 16-bit PWM duty control units with maximum six port pins:
  - Six independent PWM outputs – PWM0_CH0, PWM0_CH1, PWM0_CH2, PWM0_CH3, PWM0_CH4, and PWM0_CH5
  - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion – (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3) and (PWM0_CH4, PWM0_CH5)
  - Three synchronous PWM pairs, with each pin in a pair in-phase – (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3) and (PWM0_CH4, PWM0_CH5)
- Group control bit – PWM0_CH2 and PWM0_CH4 are synchronized with PWM0_CH0, PWM0_CH3 and PWM0_CH5 are synchronized with PWM0_CH1
- One-shot (only support edge-aligned type) or Auto-reload mode PWM
- Up to 16-bit resolution
- Supports edge-aligned, center-aligned and precise center-aligned mode
- Supports asymmetric PWM generating in center-aligned and precise center-aligned mode
- Supports center loading in center-aligned and precise center-aligned mode
- Programmable dead-time insertion between complementary paired PWMs

- Each pin of PWM0_CH0 to PWM0_CH5 has independent polarity setting control
- Hardware fault brake protections
    - Supports software trigger
    - Two Interrupt source types:
        - Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned type) or underflow (edge-aligned type)
        - Requested when external fault brake asserted
            - BKP0: EINT0 or CPO1
            - BKP1: EINT1 or CPO0
- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register
- Supports mask aligned function
- Supports independently rising CMP matching, PERIOD matching, falling CMP matching (in Center-aligned type), period matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Provides interrupt accumulation function
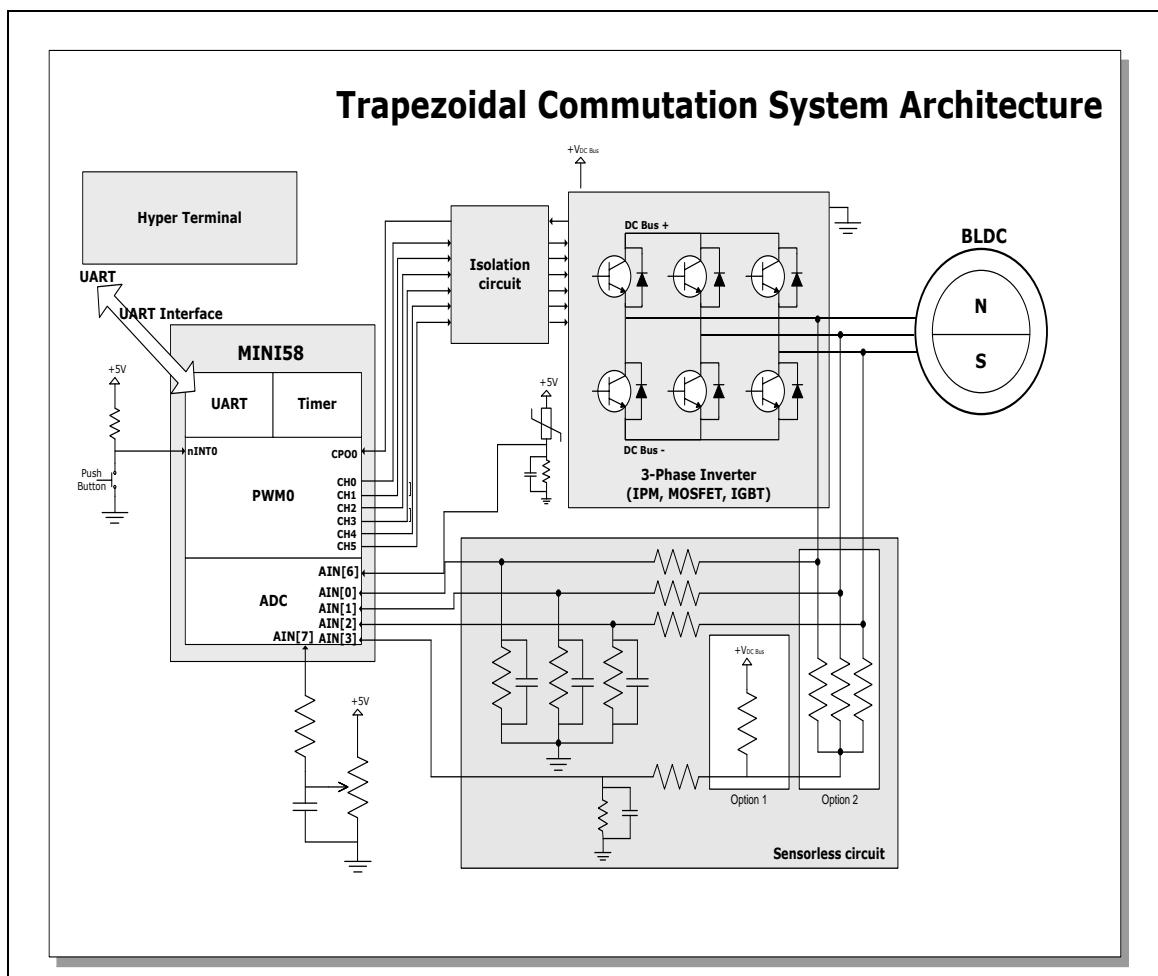
Figure 6.7-1 Application Circuit Diagram

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.8.2 Features

- 18-bit free running up counter for WDT time-out interval

- Selectable time-out interval ($2^4 \sim 2^{18}$) WDT_CLK cycles and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK = 10 kHz

- System kept in reset state for a period of (1 / WDT_CLK) * 63

- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period

- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register

- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.9.2 Features

● 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible

● Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter

6.10 UART Controller (UART)

6.10.1 Overview

The NuMicro® Mini58 series provides two channels of Universal Asynchronous Receiver/Transmitters (UART). The UART0 performs supports flow control function. The UART0 performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART0 controller also supports IrDA SIR Function, and RS-485 function mode. The UART0 channel supports six types of interrupts. The UART1 channel supports five types of interrupts. The UART1 only performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART0 has 16 bytes Receiver/Transmitter FIFO. The UART1 only has one Receiver/Transmitter buffer.

6.10.2 Features

- Full duplex, asynchronous communications

- Separates receive/transmit 16/16 bytes entry FIFO for data payloads (Only Available in UART0)

- Separates receive/transmit 1/1 byte buffer for data payloads (Only Available in UART1)

- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (Only Available in UART0)

- Programmable receiver buffer trigger level (Only Available in UART0)

- Supports programmable baud-rate generator for each channel individually

- Supports CTS wake-up function (Only Available in UART0)

- Supports 8-bit receiver buffer time-out detection function

- Programmable transmitting data delay time between the last stop and the next start bit by setting UART_TOUT[15:8] register

- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function

- Fully programmable serial-interface characteristics

  - Programmable number of data bit, 5, 6, 7, 8 character

  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection

  - Programmable stop bit, 1, 1.5, or 2 stop bit generation

- Supports IrDA SIR function mode (Only Available in UART0)

  - Supports 3/16-bit duration for normal mode

- Supports RS-485 function mode (Only Available in UART0)

  - Supports RS-485 9-bit mode

  - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

6.11 I^{2}C Serial Interface Controller (I^{2}C)

6.11.1 Overview

I^{2}C is a two-wire, bi-directional serial bus that provides a simple and efficient method for data exchange between devices. The I^{2}C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. There are two sets of I^{2}C controller and only I^{2}C0 supports Power-down wake-up function.

6.11.2 Features

The I^{2}C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Supports up to two I^{2}C ports
- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter that requests the I^{2}C interrupt if the I^{2}C bus hangs up and timer-out counter overflows
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address registers with mask option)
- Supports Power-down wake-up function (Only I^{2}C0 channel support this function)
- Supports two-level buffer function

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be configured as a master or a slave device.

6.12.2 Features

- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides four 32-bit FIFO buffers
- Supports MSB first or LSB first transfer
- Supports byte reorder function
- Supports byte or word suspend mode
- Supports Slave 3-wire mode

6.13 Analog-to-Digital Converter (ADC)

6.13.1 Overview

The Mini58 series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with eight input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.13.2 Features

- Analog input voltage range: 0 ~ Analog Supply Voltage from AV_{DD}

- 10-bit resolution and 8-bit accuracy is guaranteed

- Up to eight single-end analog input channels

- Maximum ADC clock frequency is 6 MHz, and 14 ADC clocks per sample

- Two operating modes

  - Single mode: A/D conversion is performed one time on a specified channel

  - PWM sequence mode: When PWM trigger, two of three ADC channels from 0 to 2 will automatically convert analog data in the sequence of channel [0,1] or channel[1,2] or channel[0,2] defined by MODESEL (ADC_SEQCTL[3:2])

- An A/D conversion can be started by:

  - Software write 1 to SWTRG bit

  - External pin STADC

  - PWM trigger with optional start delay period

- Each Conversion result is held in data register with valid and overrun indicators

- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting

- Channel 7 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

6.14 Analog Comparator (ACMP)

6.14.1 Overview

The NuMicro® Mini58 series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input is greater than negative input, otherwise the output is 0. Each comparator can be configured to generate interrupt when the comparator output value changes.

6.14.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports Hysteresis function
- Optional internal reference voltage source for each comparator negative input
- ACMP0 supports:
  - Four positive sources
    - P1.5, P1.0, P1.2, or P1.3
  - Three negative sources
    - P1.4
    - Internal Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})
- ACMP1 supports:
  - Four positive sources
    - P3.1, P3.2, P3.4, or P3.5
  - Three negative sources
    - P3.0
    - Internal Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})

7 APPLICATION CIRCUIT
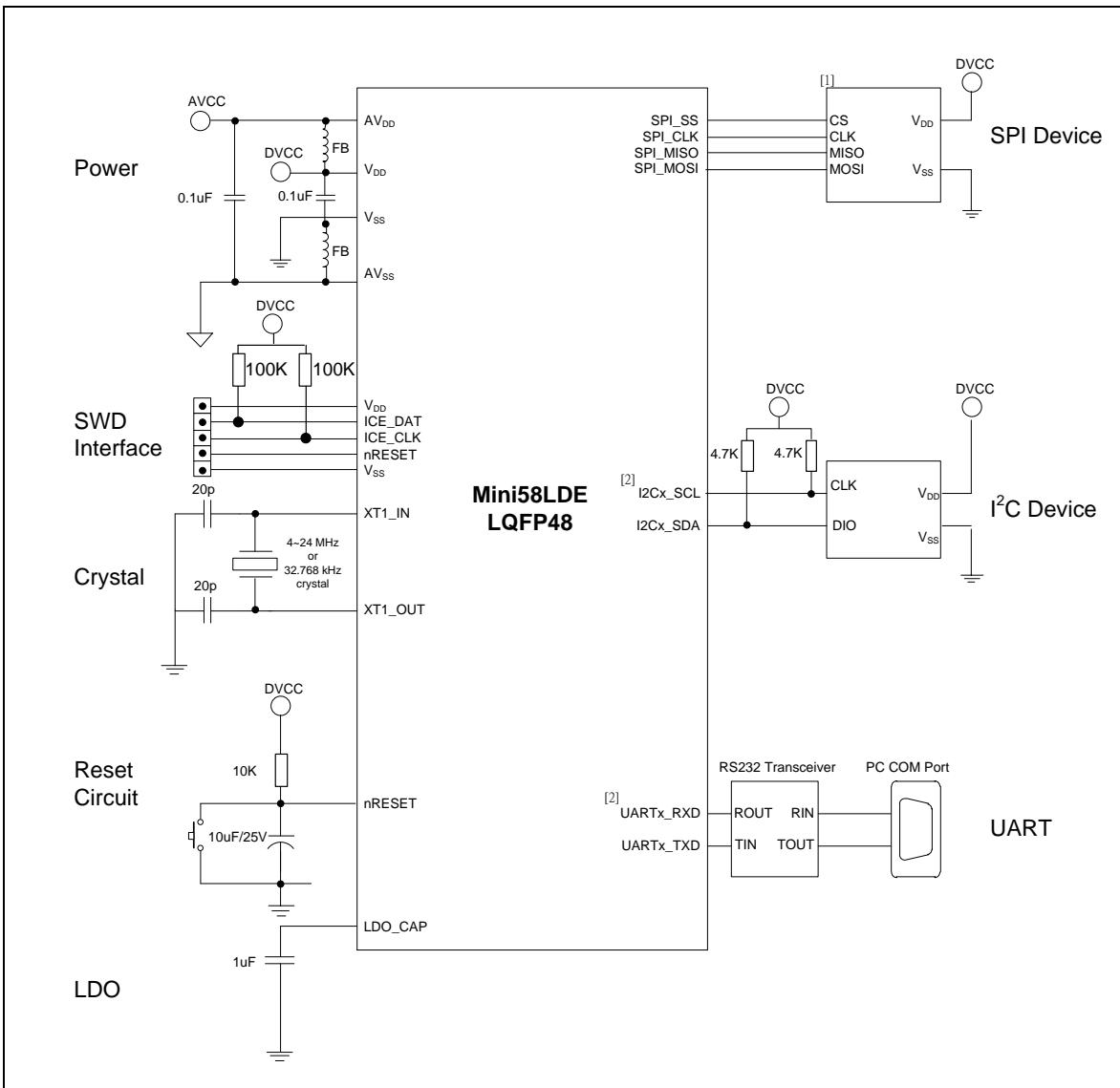
Note 1: For the SPI device, the Mini58 chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the Mini58 chip supply voltage must also be 3.3V.

Note 2: x denotes 0 or 1.

Note 3: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 4: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

8.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.5 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions				
V_{DD}	Operation voltage	2.5	-	5.5	V	V_{DD} = 2.5V ~ 5.5V up to 50 MHz				
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V					
V_{LDO}	LDO Output Voltage	1.62	1.8	1.98	V	V_{DD} ≥ 2.5 V				
V_{BG}	Band-gap Voltage	1.20	1.24	1.28	V	V_{DD} = 2.5V ~ 5.5V, T_A = 25°C				
		1.18	1.24	1.32	V	V_{DD} = 2.5V ~ 5.5V, T_A = -40°C~105°C				
V_{DD}-AV_{DD}	Allowed Voltage Difference for V_{DD} and AV_{DD}	-0.3	0	0.3	V	-				
I_{DD1}	Operating Current Normal Run Mode HCLK = 50 MHz while(1){} Executed from Flash	-	16.277	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	24 MHz	X	V	V
I_{DD2}		-	11.272	-	mA	5.5V	24 MHz	X	V	X
I_{DD3}		-	14.651	-	mA	3.3V	24 MHz	X	V	V
I_{DD4}		-	9.739	-	mA	3.3V	24 MHz	X	V	X
I_{DD5}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	7.098	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	X	V	X	V
I_{DD6}		-	4.050	-	mA	5.5V	X	V	X	X
I_{DD7}		-	6.997	-	mA	3.3V	X	V	X	V
I_{DD8}		-	4.001	-	mA	3.3V	X	V	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 12MHz while(1){} Executed from Flash	-	5.514	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	12 MHz	X	X	V
I_{DD10}		-	4.038	-	mA	5.5V	12 MHz	X	X	X
I_{DD11}		-	3.992	-	mA	3.3V	12 MHz	X	X	V
I_{DD12}		-	2.809	-	mA	3.3V	12 MHz	X	X	X

Symbol	Description	Min	Typ	Max	Unit	VDD	HXT	HIRC	PLL	All Digital Modules
I_{DD13}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	3.151	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	4 MHz	X	X	V
I_{DD14}		-	2.747	-	mA	5.5V	4 MHz	X	X	X
I_{DD15}		-	1.757	-	mA	3.3V	4 MHz	X	X	V
I_{DD16}		-	1.360	-	mA	3.3V	4 MHz	X	X	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 32.768 kHz while(1){} Executed from Flash	-	176	-	µA	V_{DD}	LXT	HIRC	PLL	All Digital Modules
						5.5V	32.768 kHz	X	X	V
I_{DD18}		-	173	-	µA	5.5V	32.768 kHz	X	X	X
I_{DD19}		-	158	-	µA	3.3V	32.768 kHz	X	X	V
I_{DD20}		-	155	-	µA	3.3V	32.768 kHz	X	X	X
I_{DD21}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	168	-	µA	V_{DD}	HXT	LIRC	PLL	All Digital Modules
						5.5V	X	V	X	V[4]
I_{DD22}		-	167	-	µA	5.5V	X	V	X	X
I_{DD23}		-	150	-	µA	3.3V	X	V	X	V[4]
I_{DD24}		-	150	-	µA	3.3V	X	V	X	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 50MHz	-	12.386	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	24 MHz	X	V	V
I_{IDLE2}		-	7.346	-	mA	5.5V	24 MHz	X	V	X
I_{IDLE3}		-	10.784	-	mA	3.3V	24 MHz	X	V	V
I_{IDLE4}		-	5.838	-	mA	3.3V	24 MHz	X	V	X
I_{IDLE5}	Operating Current Idle Mode HCLK=22.1184 MHz	-	5.378	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	X	V	X	V
I_{IDLE6}		-	2.300	-	mA	5.5V	X	V	X	X
I_{IDLE7}		-	5.291	-	mA	3.3V	X	V	X	V

I_{IDLE8}		-	2.265	-	mA	3.3V	X	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	4.577	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE10}		-	3.364	-	mA	5.5V	V	X	X	X
I_{IDLE11}		-	3.062	-	mA	3.3V	V	X	X	V
I_{IDLE12}		-	1.871	-	mA	3.3V	V	X	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	2.838	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE14}		-	2.433	-	mA	5.5V	V	X	X	X
I_{IDLE15}		-	1.446	-	mA	3.3V	V	X	X	V
I_{IDLE16}		-	1.048	-	mA	3.3V	V	X	X	X
I_{IDLE17}	Operating Current Idle Mode HCLK = 32.768 kHz	-	167	-	µA	V_{DD}	LXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE18}		-	166	-	µA	5.5V	V	X	X	X
I_{IDLE19}		-	150	-	µA	3.3V	V	X	X	V
I_{IDLE20}		-	149	-	µA	3.3V	V	X	X	X
$I_{IDLE\ 21}$	Operating Current Idle Mode HCLK = 10 kHz	-	167	-	µA	V_{DD}	HXT	LIRC	PLL	All Digital Modules
						5.5V	X	V	X	V[4]
$I_{IDLE\ 22}$		-	166	-	µA	5.5V	X	V	X	X
$I_{IDLE\ 23}$		-	150	-	µA	3.3V	X	V	X	V[4]
$I_{IDLE\ 24}$		-	149	-	µA	3.3V	X	V	X	X
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	6.2	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.				
I_{PWD2}		-	5.8	-	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.				
I_{IL}	Logic 0 Input Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-	-70	-75	µA	V_{DD} = 5.5 V, V_{IN} = 0V				

|						
I_{TL}	Logic 1 to 0 Transition Current P0/1/2/3/4/5 (Quasi-bidirectional Mode) [*3]	-	-595	-750	μA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current P0/1/2/3/4/5	-1	-	+1	μA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P0/1/2/3/4/5 (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P0/1/2/3/4/5 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XTAL1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XTAL1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-0.3	-	0.2V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal nRESETPin Pull-up Resistor	40		150	kΩ	V_{DD} = 2.5 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), P0/1/2/3/4/5	-0.3	-	0.3V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), P0/1/2/3/4/5	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-300	-400	-	μA	V_{DD} = 4.5 V, V_{SS} = 2.4 V
I_{SR12}		-50	-80	-	μA	V_{DD} = 2.7 V, V_{SS} = 2.2 V
I_{SR13}		-40	-73	-	μA	V_{DD} = 2.5 V, V_{SS} = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4/5 (Push-pull Mode)	-20	-26	-	mA	V_{DD} = 4.5 V, V_{SS} = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_{SS} = 2.2 V
I_{SR23}		-2.5	-5	-	mA	V_{DD} = 2.5 V, V_{SS} = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4/5 (Quasi-bidirectional, Open-Drain and Push-pull Mode)	10	15	-	mA	V_{DD} = 4.5 V, V_{SS} = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_{SS} = 0.45 V
I_{SK13}		5	8	-	mA	V_{DD} = 2.5 V, V_{SS} = 0.45 V

Notes:

1. nRESET pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{IN} approximates to 2V.

4. Only enable modules which support 10 kHz LIRC clock source

8.3 AC Electrical Characteristics

8.3.1 External Input Clock
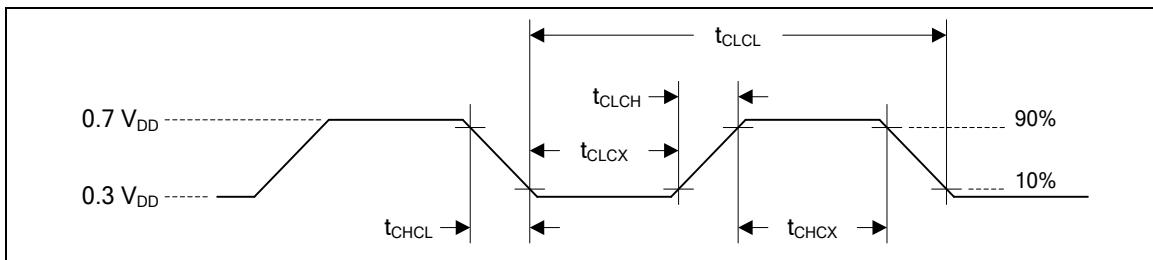
Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

8.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.5	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.0	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

8.3.3 External 32.768 kHz XTAL Oscillator (LXT)

Sym.	Parameter	Specifications				Test Conditions
		Min.	Typ.	Max.	Unit	
f_{LXTAL}	Oscillator frequency		32.768		kHz	V_{DD} = 2.5V ~ 5.5V
T_{LXTAL}	Temperature	-40		+105	ºC	
I_{LXTAL}	Operating current		5		µA	V_{DD} = 2.5V

8.3.4 Typical Crystal Application Circuits

Crystal	C1	C2

4 MHz ~ 24 MHz	20 pF	20 pF
32.768 kHz	20 pF	20 pF
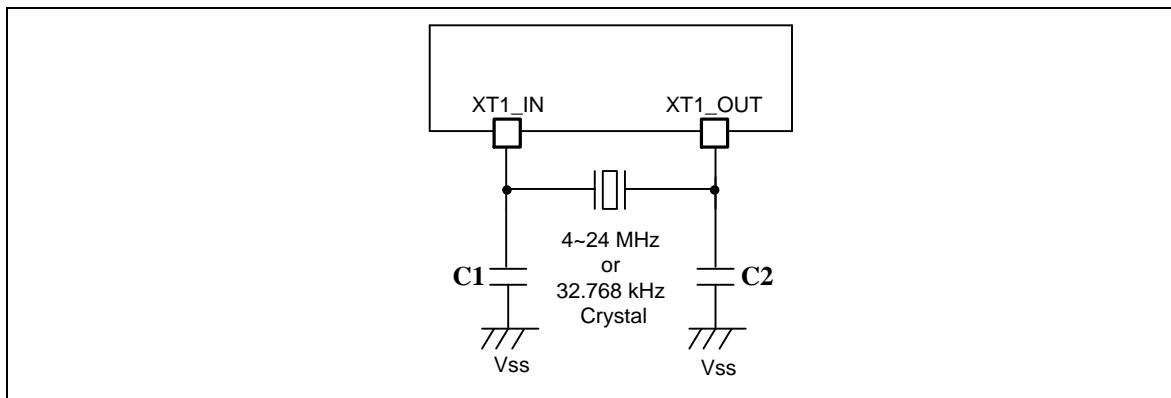
Figure 8.3-1 Mini58 Typical Crystal Application Circuit

8.3.5 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	$T_A = 25\ ℃$ $V_{DD} = 5$ V
		-2	-	+2	%	$T_A = -40℃\sim105℃$ $V_{DD}=2.5$ V~ 5.5 V
I_{HRC}	Operating Current	-	700	-	µA	$T_A = 25\ ℃, V_{DD} = 5$ V

HIRC oscillator accuracy vs. temperature
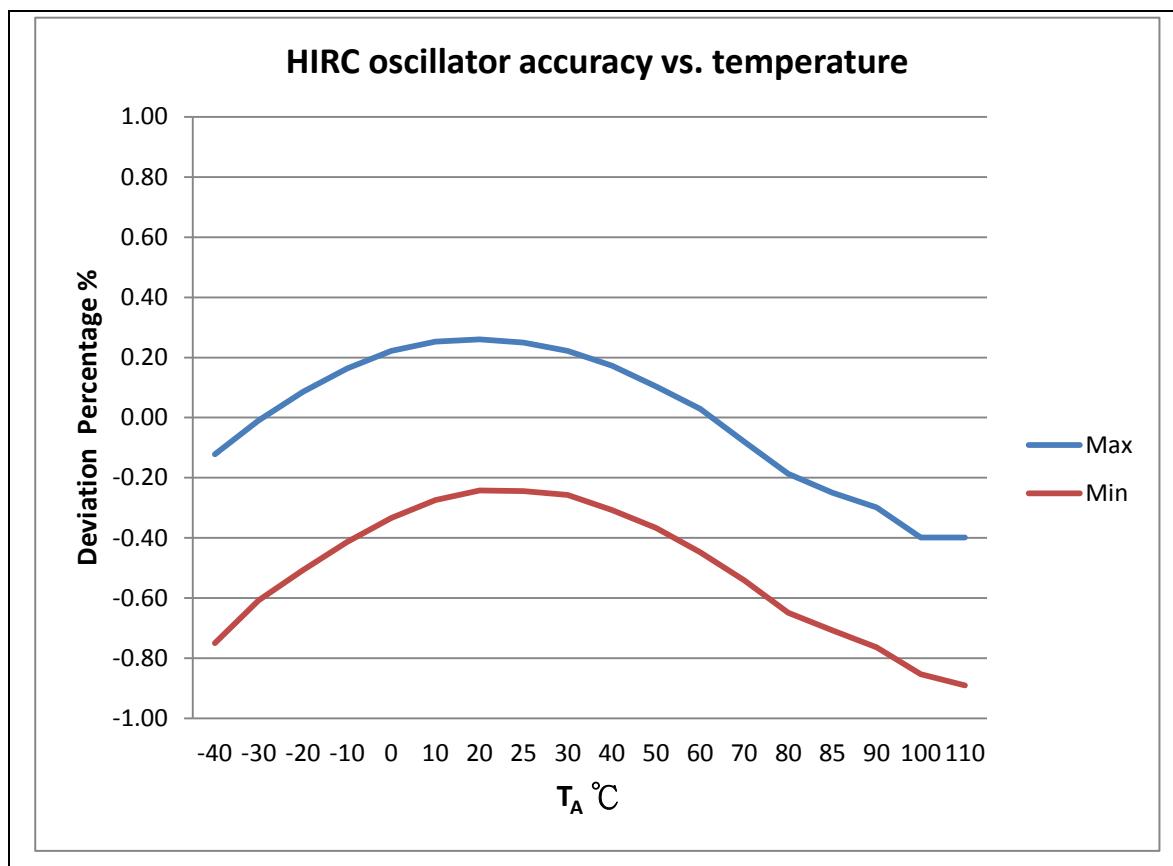
8.3.6   10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
	Center Frequency	-	10	-	kHz	-
f_{LRC}	Oscillator Frequency	-10	-	+10	%	V_{DD}=2.5V~ 5.5V T_A = 25℃
		-40	-	+40	%	V_{DD}=2.5V~ 5.5V T_A = -40℃~+105℃

8.4 Analog Characteristics

8.4.1 10-bit SARADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	10	Bit	-
DNL	Differential Nonlinearity Error	-	-1~1.5	-1~+2.5	LSB	-
INL	Integral Nonlinearity Error	-	±1	±2	LSB	-
E_O	Offset Error	-	1	2	LSB	-
E_G	Gain Error (Transfer Gain)	-	-1	-3	LSB	-
E_A	Absolute Error	-	3	4	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	4.2	MHz	AV_{DD} = 4.5~5.5 V
		-	-	2.8		AV_{DD} =2.5~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	300	kSPS	AV_{DD} = 4.5~5.5 V
		-	-	200	kSPS	AV_{DD} = 2.5~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	N is sampling counter, N=0,1,2, 4,8, 16,32, 4, 128, 256,1024
T_{CONV}	Total Conversion Time	N+14			$1/F_{ADC}$	
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	600	-	µA	AV_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	3.2	-	pF	-
R_{IN}	Input Load	-	6	-	kΩ	-

Note: ADC voltage reference is same with AV_{DD}
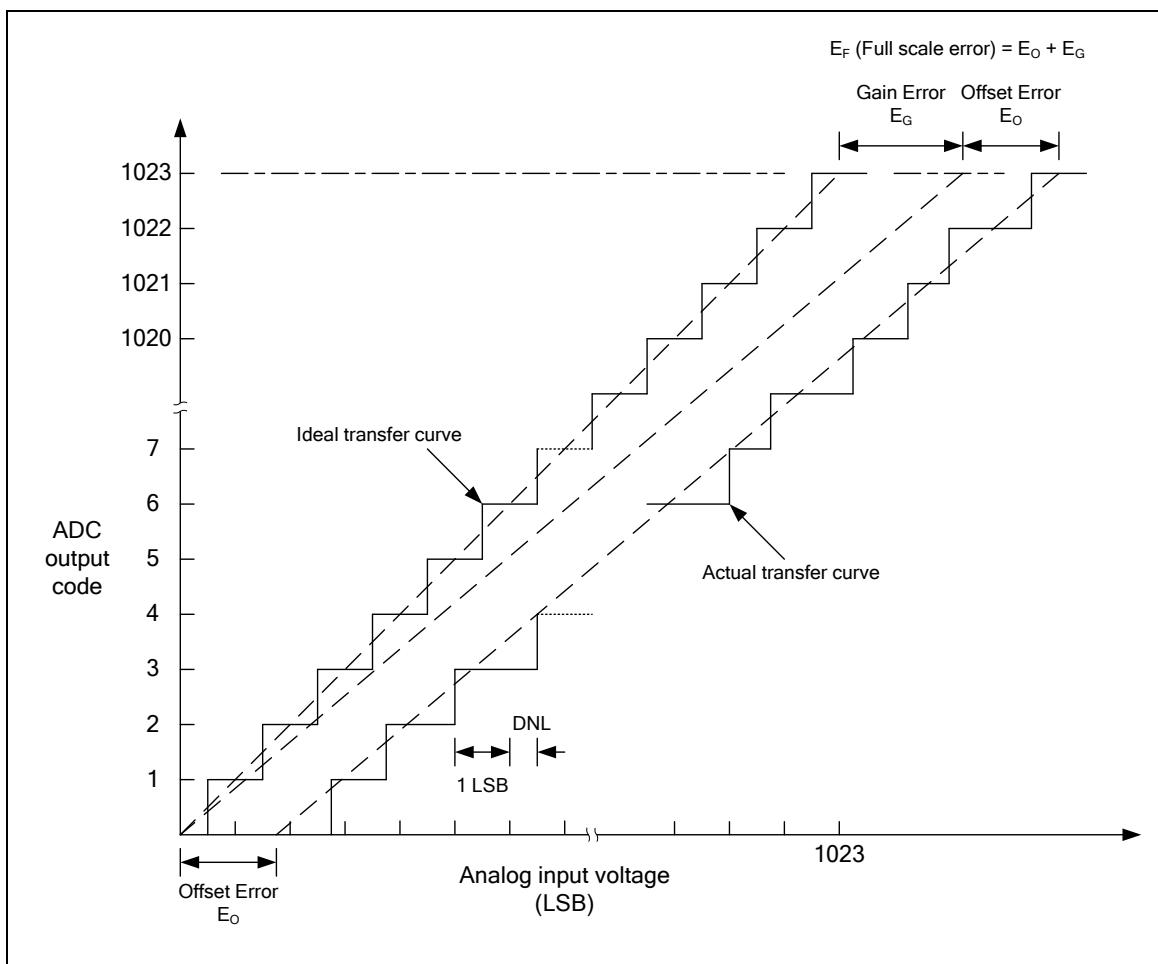
8.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	

Notes:

1. It is recommended a 0.1µF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

8.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-

I_{LVR}	Quiescent Current	-	1	5	µA	AV$_{DD}$ =5.5V
V$_{LVR}$	Threshold Voltage	1.90	2.00	2.10	V	T$_A$=25°C
		1.70	1.90	2.05	V	T$_A$=-40°C
		2.00	2.20	2.45	V	T$_A$ =105°C

8.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV$_{DD}$	Supply Voltage	0	-	5.5	V	-
T$_A$	Temperature	-40	25	105	$^{\circ}$C	-
I$_{BOD}$	Quiescent Current	-	-	140	µA	AV$_{DD}$ =5.5V
V$_{BOD}$	Brown-out Detector (Falling edge)	4.2	4.38	4.55	V	BODEN = 1, BOD_VL [1:0]=11
		3.5	3.68	3.85	V	BODEN = 1, BOD_VL [1:0]=10
		2.5	2.68	2.85	V	BODEN = 1, BOD_VL [1:0]=01
		2.0	2.18	2.35	V	BODEN = 1, BOD_VL [1:0]=00
V$_{BOD}$	Brown-out Detector (Rising edge)	4.3	4.52	4.75	V	BODEN = 1, BOD_VL [1:0]=11
		3.5	3.8	4.05	V	BODEN = 1, BOD_VL [1:0]=10
		2.5	2.77	3.05	V	BODEN = 1, BOD_VL [1:0]=01
		2.0	2.25	2.55	V	BODEN = 1, BOD_VL [1:0]=00

8.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T$_A$	Temperature	-40	25	105	$^{\circ}$C	-
V$_{POR}$	Reset Voltage	1.6	2	2.4	V	-
V$_{POR}$	V$_{DD}$ Start Voltage to Ensure Power-on Reset	-	-	100	mV	
RR$_{VDD}$	V$_{DD}$ Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	
t$_{POR}$	Minimum Time for V$_{DD}$ Stays at V$_{POR}$ to Ensure Power-on Reset	0.5	-	-	ms	
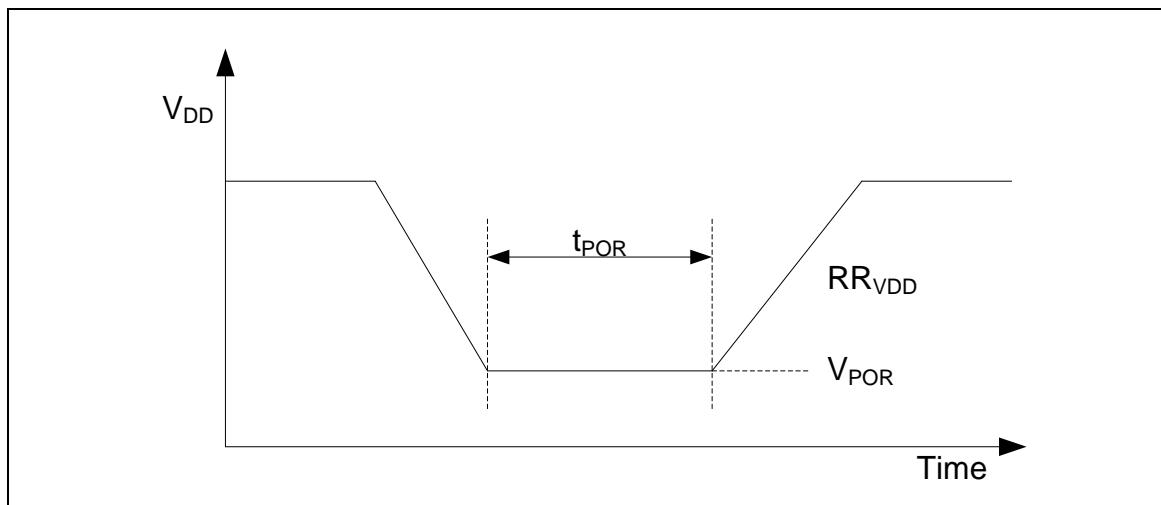
Figure 8.4-1 Power-up Ramp Condition

8.4.6 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	40	80	µA	AV_{DD}=5V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	$AV_{DD} - 0.1$	V	-
V_{COM}	Input Common Mode Range	0.1	-	$AV_{DD} - 0.1$	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{COM}=1.2 V, V_{DIFF}=0.1 V
V_{HYS}	Hysteresis	-	±30	±60	mV	V_{COM}=1.2 V
T_{STB}	Stable time	-	-	1	µs	

8.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Page Erase Time	-	20	-	ms	
T_{PROG}	Program Time	-	40	-	us	
I_{DD1}	Read Current	-	7	-	mA	
I_{DD2}	Program Current	-	8	-	mA	
I_{DD3}	Erase Current	-	12	-	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

9 PACKAGE DIMENSIONS

9.1 48-pin LQFP

COTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

9.2   33-pin QFN (4 mm x 4 mm)

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
L	0.25	0.30	0.35
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
K	0.20	—	—

9.3 33-pin QFN (5 mm x 5 mm)

TOP VIEW

32

1

PIN 1 CORNER

SEATING PLANE

A1
(A3)
A2
A

BOTTOM VIEW
VIEW M—M

25 32
24 PIN 1 I.D.
1
e/2
K
17
8
16 9
32X L
32X b
EXPOSED DIE
ATTACH PAD

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

9.4   20-pin TSSOP

SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~	~	1.20	~	~	0.047
A1	0.05	~	0.15	0.002	~	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	~	0.30	0.007	~	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	~	0.20	0.004	~	0.008
θ	0°	~	8°	0°	~	8°
Y	0.10 BASIC			0.004 BASIC		

10 REVISION HISTORY

Date	Revision	Description
2015.06.11	1.00	Initial version.
2015.10.12	1.01	Updated LDROM size from 2 Kbytes to 2.5 Kbytes.
2015.12.09	1.02	Fixed cross reference error.
2018.05.09	1.03	1. Rearranged pins of SWD interface in chapter 7 APPLICATION CIRCUIT. 2. Modified Flash data retention time to 10 years in sectoin 8.5.
2020.04.15	1.04	1. Updated 33-pin QFN (4 mm x 4 mm) Package Dimension in section 9.2 2. Added notes about the hardware reference design for ICE_DAT, ICE_CLK and nRESET pins in section 4.4 and chapter 7.

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