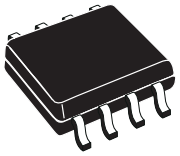
STSJ50NH3LL

N-channel 30 V - 0.008 Ω - 12 A - PowerSO-8™ ultra low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ (max)	I_D
STSJ50NH3LL	30V	< 0.0105Ω	12A(1)

- Optimal $R_{DS(on)}$ x Qg trade-off @ 4.5V
- Reduced switching losses
- Reduced conduction losses
- Improved junction-case thermal resistance



PowerSO-8™

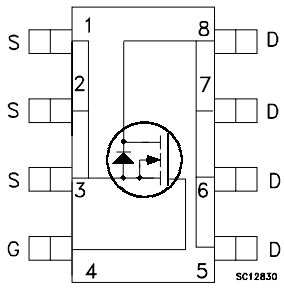
Applications

- Switching application

Description

This series utilizes the latest advanced design rules of ST's proprietary STripFET™ technology, and a propriertary process for integrating a monolithic Scottky diode. The new Power MOSFET is optimized for the most demanding synchronous switch function in DC-DC converter for computer and telecom.

Figure 1. Internal schematic diagram



Drain contact also on the backside

Table 1. Device summary

Order code	Marking	Package	Packaging
STSJ50NH3LL	50H3LL-	PowerSO-8	Tape & reel

Obsolete Product(s) - Obsolete Product(s)

Contents

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuit 9

4 Package mechanical data 10

5 Revision history 12

Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}(1)	Gate-source voltage	±16	V
V_{GS}(2)	Gate-source voltage	±18	V
I_D(4)	Drain current (continuous) at T_C = 25°C	50	A
I_D(3)	Drain current (continuous) at T_C=25°C	12	A
I_D(4)	Drain current (continuous) at T_C=100°C	31.3	A
I_D(3)	Drain current (continuous) at T_C=100°C	7.5	A
I_{DM}(5)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25°C (3) Total dissipation at T_C = 25°C (4)	3 50	W W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Continuous mode
2. Guaranteed for test time ≤ 15ms
3. This value is rated accordingly to Rthj-pcb
4. This value is rated accordingly to Rthj-c
5. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}c}$	Thermal resistance junction-case Max	2.5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb Max	42	°C/W

1. When mounted on 1 inch² FR-4 board, 2oz Cu (t<10sec.)

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not repetitive avalanche current	7.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, I_D=7.5 A)	150	mJ

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating T_C=125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D =250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 6 A V_{GS}= 4.5 V, I_D= 6 A		0.008 0.010	0.0105 0.013	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 6 A @125°C V_{GS}= 4.5 V, I_D= 6 A @125°C		0.012 0.016		Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =10 V, I_D = 12 A		38		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0		965 285 38		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D =12 A V_{GS} =4.5V,(see Figure 16)		9 3.7 3	12	nC nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level =20 mv open drain	0.5	1.5	2.5	Ω

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=15 V, I_D=6 A, R_G=4.7 Ω, V_{GS}=4.5 V (see Figure 15)		15 32		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=15 V, I_D=6 A, R_G=4.7 Ω, V_{GS}=4.5 V (see Figure 15)		18 8.5		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				12 48	A A
V_{SD}(2)	Forward on voltage	I_{SD}=12 A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=12 A, di/dt = 100 A/µs, V_{DD}=20 V, Tj=150 °C (see Figure 20)		24 17.4 1.45		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

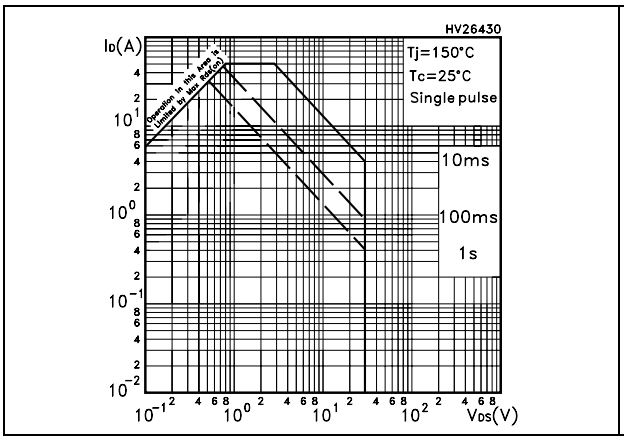


Figure 3. Thermal impedance

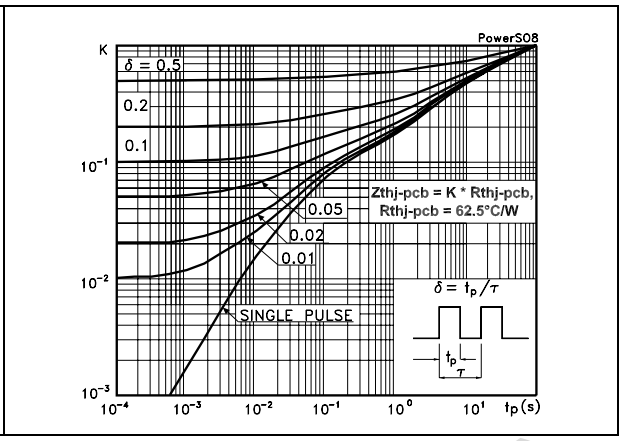


Figure 4. Output characteristics

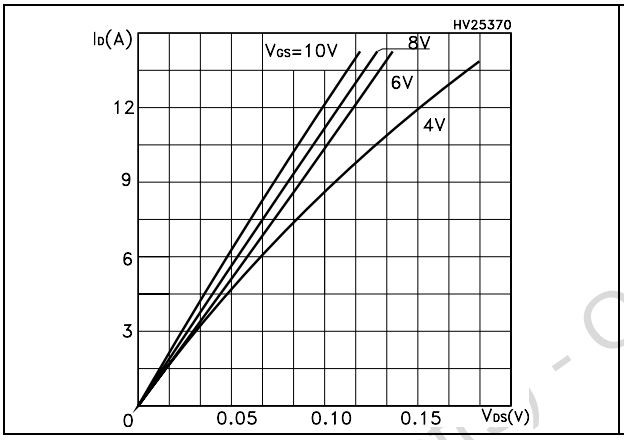


Figure 5. Transfer characteristics

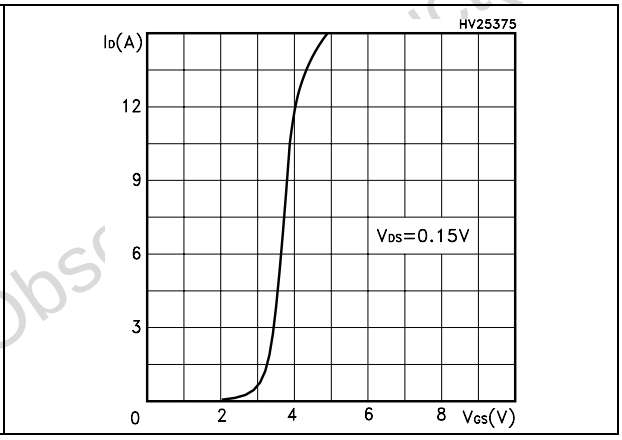


Figure 6. Transconductance

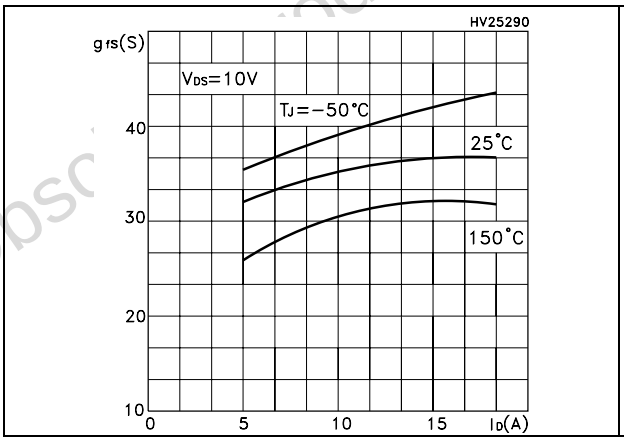
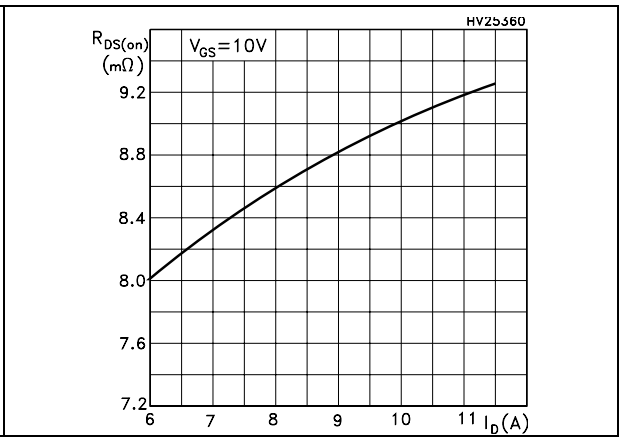


Figure 7. Static drain-source on resistance



Obsolete Product(s) - Obsolete Product(s)

Figure 8. Gate charge vs gate-source voltage

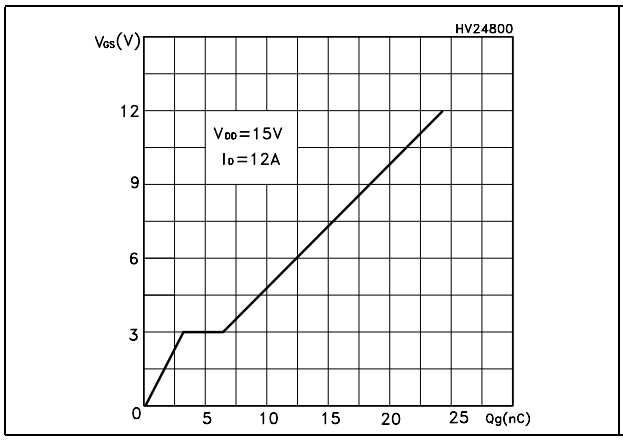


Figure 9. Capacitance variations

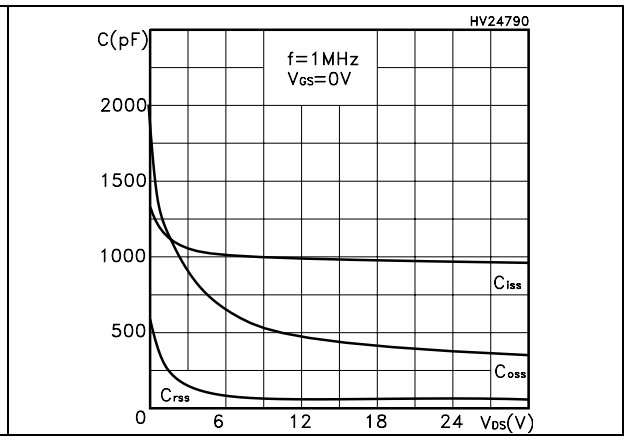


Figure 10. Normalized gate threshold voltage vs temperature

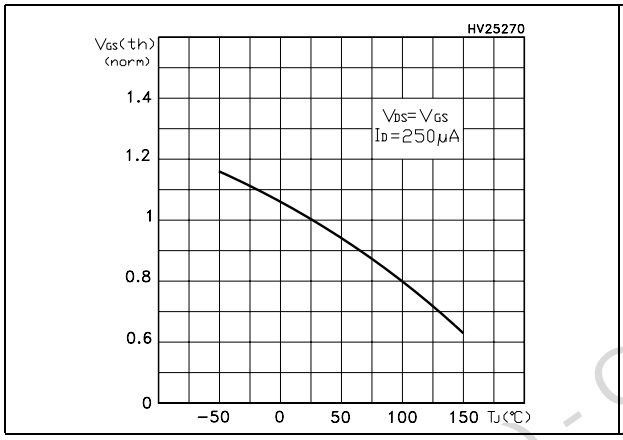


Figure 11. Normalized on resistance vs temperature

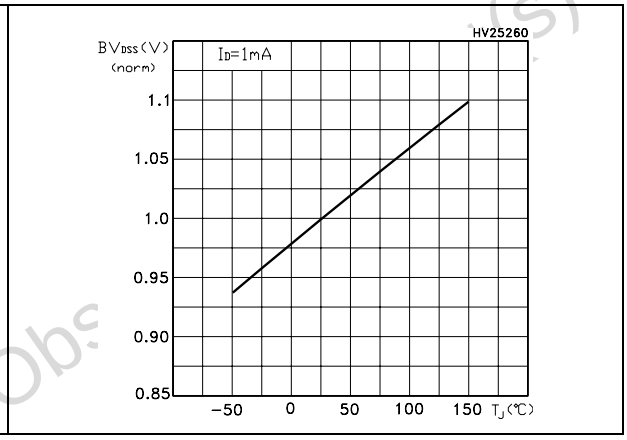


Figure 12. Source-drain diode forward characteristics

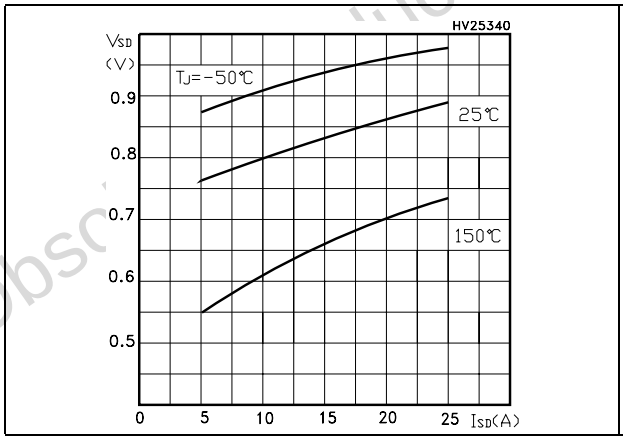


Figure 13. Normalized B_{VDSS} vs temperature

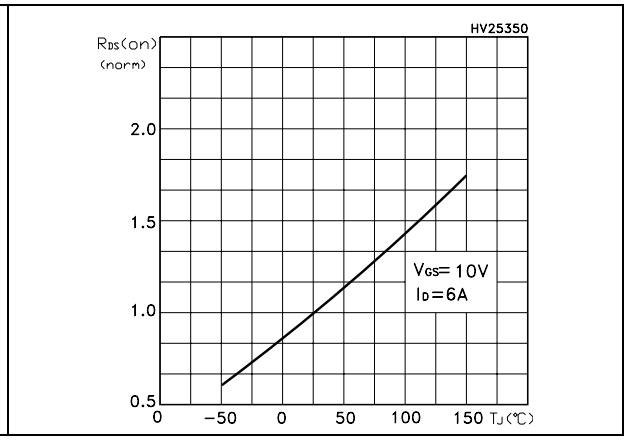
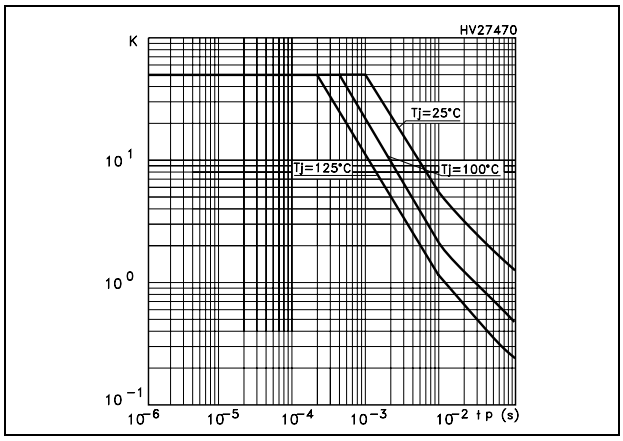


Figure 14. Allowable Iav vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads under the following conditions:

$P_{D(AVE)} = 0.5*(1.3*BV_{DSS} *I_{AV})$

$EAS_{(AR)} = P_{D(AVE)} *t_{AV}$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{av} is the time in avalanche

Obsolete Product(s) - Obsolete Product(s)

3 Test circuit

Figure 15. Switching times test circuit for resistive load

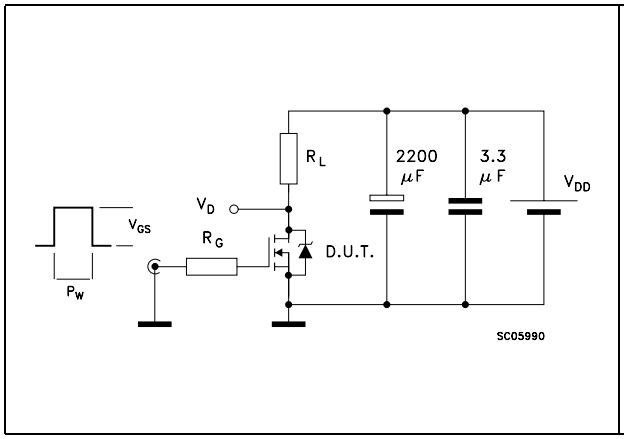


Figure 16. Gate charge test circuit

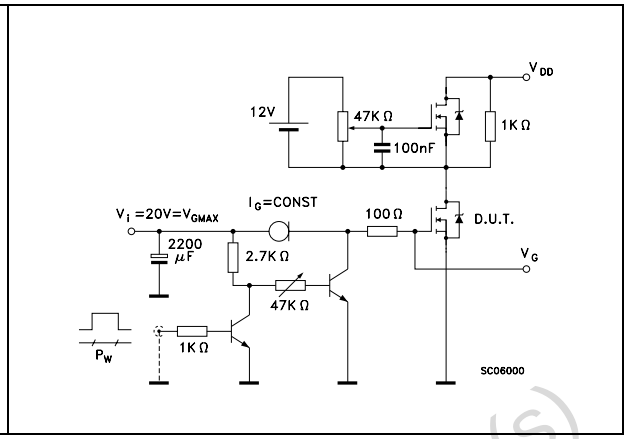


Figure 17. Test circuit for inductive load switching and diode recovery times

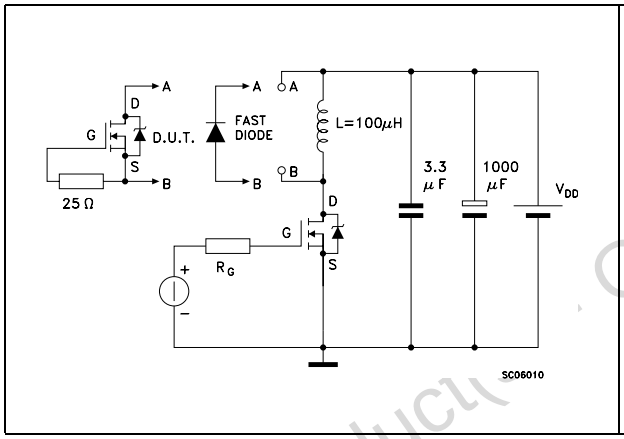


Figure 18. Unclamped inductive load test circuit

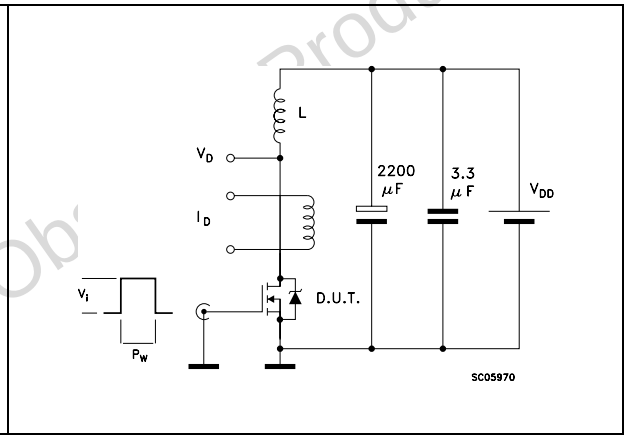


Figure 19. Unclamped inductive waveform

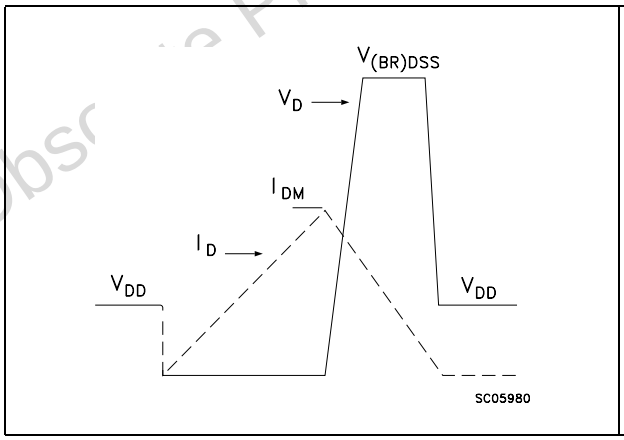
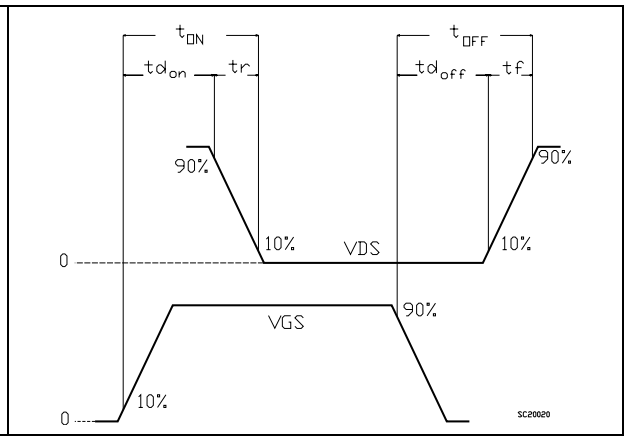


Figure 20. Switching time waveform



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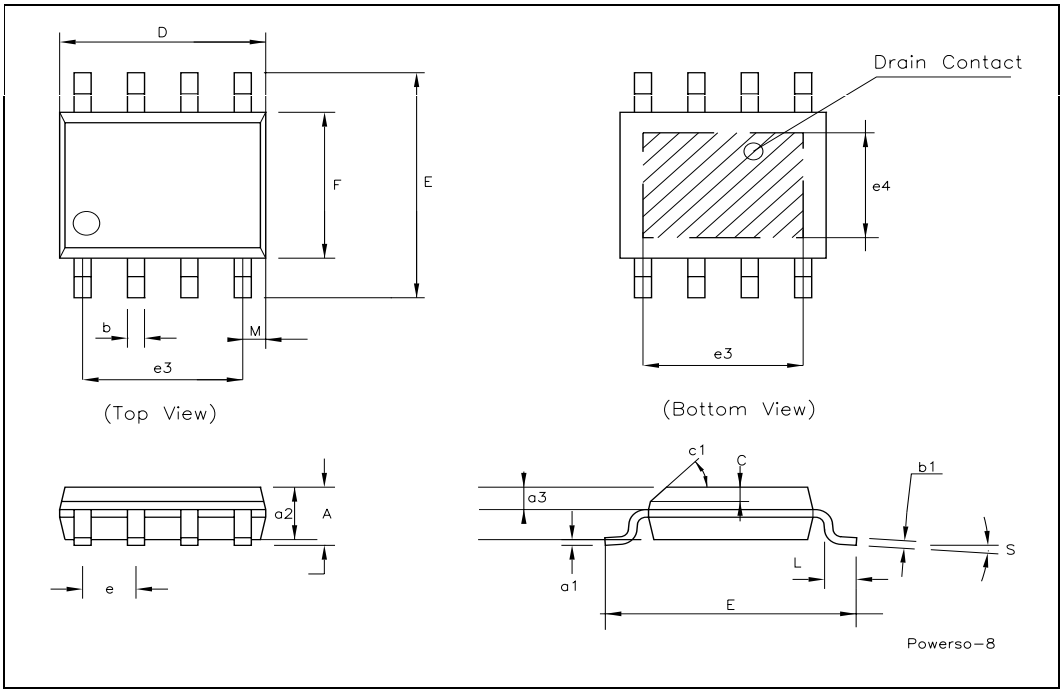
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

PowerSO-8™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



Obsole

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Jul-2004	1	Initial release.
24-May-2005	2	New value on *Table 7*
23-Jun-2005	3	New Rg value on *Table 7*
16-Nov-2005	4	Complete version
30-Mar-2006	5	New template
10-Dec-2007	6	Updated data on *Table 4: Avalanche data*

Obsolete Product(s) - Obsolete Product(s)

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