High Speed, 200 dB Range, Logarithmic Converter

Data Sheet

ADL5304

FEATURES

Optimized for very fast response at all input currents
- **Overall bandwidth of >4 MHz for inputs >1 µA**
- **Bandwidth: 25 kHz at input of 1 nA and 350 kHz at 10 nA**

10 decades of input range: 1 pA to 10 mA
Law conformance: ±0.25 dB from 100 pA to 100 µA
Log ratio or fixed-intercept operation
Precision voltage references and reference current
Adaptive photodiode (PD) bias for low dark current
Programmable log slope and intercept
Default log slope of 10 mV/dB at VLOG pin
Single- or dual-supply operation

APPLICATIONS

High accuracy optical power measurement
Wide range baseband log compression
Versatile detector for high speed APC loops

GENERAL DESCRIPTION

The ADL5304 is a high speed logarithmic converter with fast response and low noise over a 200 dB (1 pA to 10 mA) measurement range. The ADL5304 provides a nominal logarithmic slope of 10 mV/dB (200 mV/decade); other values are easily configured. Logarithmic intercept can be programmed over a wide range with the internal 100 nA current source or externally for log ratio applications. The default intercept value of 3.162 fA places the midpoint of the measurement range of 100 nA at V_{LOG} = 1.5 V.

A single positive supply of 5 V is all that is required for operation over a specified 1 pA to 3 mA input range. Dual-supply operation extends the specified input current range to 10 mA.

The ADL5304 accepts two current inputs to the logarithmic argument. The numerator input, I_{NUM}, flows in the collector of an NPN transistor, connected in a feedback path around a low offset JFET amplifier. The denominator current, I_{DEN}, is treated in the same way, which allows for log ratio operation. The input summing nodes (INUM and IDEN) operate at a constant default voltage of 1.5 V. The VSM1 to VSM4 pins flank the INUM and IDEN inputs to provide a guard voltage to minimize leakage currents.

Adaptive photodiode biasing is provided for optical measurements. A monitor current 1.1 times I_{NUM} is output at the IMON pin, and an external resistor, R_{MNTR}, at 10 times the photodiode series resistance (R_S) applies a voltage across the photodiode that 1st order keeps the internal PD junction at 0 V to minimize dark current.

The VLOG output is buffered and can be rescaled through internal gain setting resistors. The internal I_{LOG} varies from −400 µA to +400 µA as I_{NUM} changes over 10 decades from 1 pA to 10 mA. This corresponds to 0.5 V to 2.5 V at the VLOG pin in the default configuration shown in Figure 1.

Accurate 1.5 V (Pin 1P5V) and 2.0 V (Pin 2VLT) reference outputs allow precise repositioning of the intercept using external resistors.

The ADL5304 is available in a 32-lead, 5 mm × 5 mm LFCSP and specified for operation from −40°C to +85°C.

SIMPLIFIED BLOCK DIAGRAM

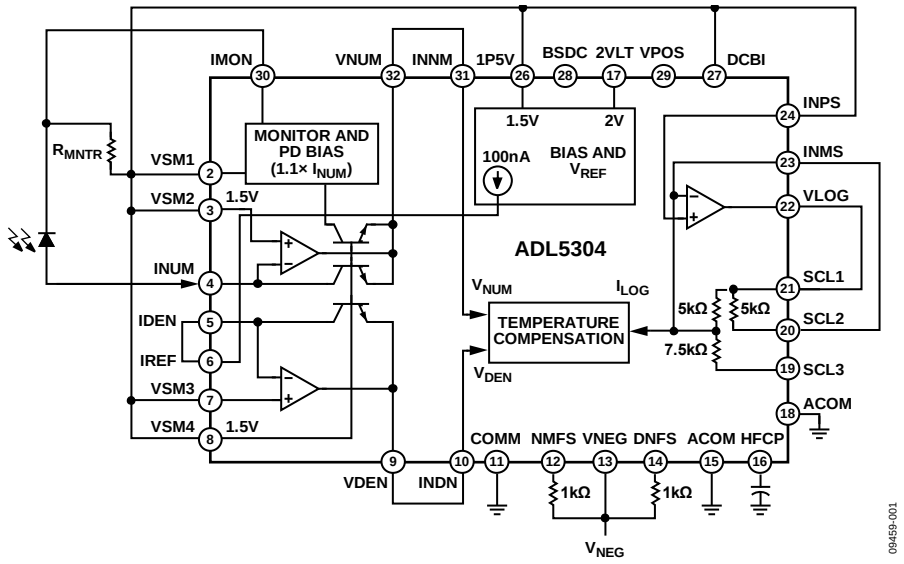


Figure 1.

Rev. A Document Feedback

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Simplified Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Test Circuits ... 13
Terminology ... 16
Theory of Operation ... 17
Basic Concepts ... 17
Optical Measurements ... 17
Circuit Description ... 18
Applications Information ... 25
Using the ADL5304 ... 25
Using a Negative Supply ... 26
Evaluation Board Schematic and Silkscreens ... 27
Outline Dimensions ... 29
Ordering Guide ... 29

REVISION HISTORY

3/16—Rev. 0 to Rev. A

Changes to Specified Current Range Parameter, Table 1 ... 3
Changes to Figure 2 and Table 3 ... 6
Changes to Figure 58 ... 27
Updated Outline Dimensions ... 29
Changes to Ordering Guide ... 29

9/11—Revision 0: Initial Version

SPECIFICATIONS

V_{POS} = 5 V, V_{NEG} = 0 V, T_A = 25°C; IDEN = IREF; VSM1 to VSM4, 1P5V, DCBI, and INPS tied together; SCL1 = VLOG; SCL2 = INMS; SCL3 = open; scale = 200 mV/dec; VLOG output load R_L > 2 kΩ, unless otherwise noted. Upper case indicates a pin name (for example, VLOG) and subscripted indicates signal name (for example, V_{LOG}).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT INTERFACES	INUM, IDEN, VSMx pins				
Specified Current Range	Flows toward each input pin (INUM and IDEN), $-5\ V \le V_{NEG} \le -2\ V$	1×10^{-12}		1×10^{-3}	A
	V_{NEG} = 0 V	1×10^{-12}		3×10^{-3}	A
Temperature Drift (INUM and IDEN)	−40°C < T_A < +85°C		0.01		mV/°C
Input Guard Offset Voltage	$V_{INUM} - V_{VSUM}$	−2	±0.6	+2	mV
LOGARITHMIC OUTPUT	VLOG pin, referenced to ACOM; input applied to INUM[1]				
Logarithmic Slope, V_Y	25°C	195	200	205	mV/dec
	−40°C < T_A < +85°C	−2		+3	mV/dec
Logarithmic Intercept, I_Z[2]	Extrapolated input current at VLOG = 0 V		3.162		fA
Logarithmic Offset	Difference between V_{LOG} and V_{SUM} with $I_{NUM} = I_{DEN}$	−8		+5	mV
	−40°C < T_A < +85°C		25		µV/°C
Logarithmic Law Conformance Error	Maximum deviation from best fit over 1 nA to 100 µA range	−0.7	±0.2	+0.7	dB
VLOG OUTPUT	INPS, INMS, VLOG, SCL1, SCL2, SCL3 pins				
Output Buffer Offset Voltage		−3	+0.1	+3	mV
Output Buffer Bias Current	Flowing out of the INPS pin		−1.3		µA
Incremental Input Resistance	Pin INPS		12		MΩ
Output Range	R_L open	VNEG + 0.2		VPOS − 0.2	V
Output Noise Spectral Density[3]	I_{NUM} > 1 nA		<6		µV/√Hz
Small Signal Bandwidth	I_{NUM} = 1 nA		25		kHz
	I_{NUM} = 10 nA		350		kHz
	I_{NUM} = 100 nA		1.2		MHz
	I_{NUM} > 1 µA		4		MHz
Falling Edge Settling Times[4]	I_{NUM} = 100 nA to 10 nA		10		µs
	I_{NUM} = 1 µA to 100 nA		2.2		µs
	I_{NUM} = 10 µA to 1 µA		0.5		µs
	I_{NUM} > 10 µA		<0.5		µs
Nominal Voltage Swing	For input current range of 1 pA to 10 mA	0.5		2.5	V
Output Impedance	Frequency < 1 MHz		<2		Ω
REFERENCE OUTPUTS	1P5V, 2VLT, IREF pins				
1P5V (Referenced to ACOM)	25°C	1.495	1.500	1.505	V
	−40°C < T_A < +85°C		30		µV/°C
Output Current		−10		+5	mA
2VLT (Referenced to ACOM)	25°C	1.995	2.000	2.005	V
	−40°C < T_A < +85°C		31		µV/°C
Output Current	Sourcing only	0		20	mA
IREF[5]	25°C		100		nA
	−40°C < T_A < +85°C		−70		pA/°C
PHOTODIODE BIAS	IMON pin; $I_{MON} = 1.1 \times I_{NUM}$				
Midrange Value	At a photodiode current = I_{NUM} = 100 nA		110		nA
Maximum Value	At I_{NUM} = 1 mA ($R_S \le 100\ \Omega$), $R_{MNTR} = 10 \times R_S$ (R_S = photodiode series resistance)	10.5	11	11.5	mA
IMON Compliance		0	3.0		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY	VPOS, VNEG				
VPOS		4.5	5.0	5.5	V
Quiescent Current	INUM = IDEN = 10 µA; VPOS = 5 V, VNEG = 0 V		13.5	16	mA
	4.5 V ≤ VPOS ≤ 5.5 V	10		17	mA
VNEG[6]	Nominal 0 V for single supply	0		−5	V
Quiescent Current	INUM = IDEN = 10 µA; VPOS = 5 V, VNEG = 0 V	−8.5	−7.3		mA
	VNEG = −5 V	−10.5		−6	mA

[1] Slope is of the same magnitude but opposite sign for input applied to IDEN.

[2] $I_Z = I_{REF}/10^{(V_{OFS}/V_Y)}$. Note that the error of I_Z is dependent on three parameters, I_{REF}, V_{OFS}, and V_Y. All three of those are trimmed.

[3] Output noise and small signal bandwidth are functions of input current; measured from the INUM input to the VLOG output. See the Typical Performance Characteristics section.

[4] High-to-low currents (falling edge) represent the worst-case settling condition. Low-to-high currents (rising edge) settling times are approximately 2× faster than the falling edge settling. Settling time is measured to 1 dB error (10 mV/dB; V_{LOG} settles to within 10 mV of the final value).

[5] IREF applied to IDEN together with 1P5V determines the logarithmic intercept current, I_Z, and thereby the accuracy of the intercept.

[6] Using dual-supply operation with the VSMx, DCBI, and INPS pins at ground, VNEG needs to be in the −2 V to −5 V range for proper device function.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{POS}	+6 V
V_{NEG}	−6 V
Input Current to INUM, IDEN	20 mA
Thermal Data, 2-Layer JEDEC Board No Air Flow (Exposed Pad Soldered to PCB)	
θ_{JA}	61.6°C/W
θ_{JC}	1.2°C/W
Maximum Power Dissipation (Exposed Pad Soldered to PC Board)	0.6 W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

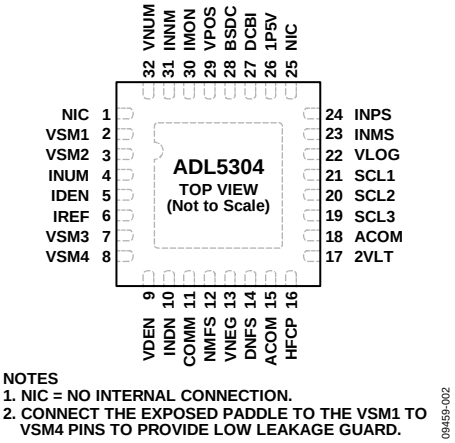


Figure 2. 32-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 25	NIC	No Internal Connection.
2, 3, 7, 8	VSM1 to VSM4	Guard Pins for the INUM and IDEN Inputs. Connect these pins to the 1P5V, DCBI, and INPS pins for default single-supply setup; connect to ground if INUM (photodiode bias) is desired to be at ground (must have −5 V < VNEG < −2 V).
4	INUM	Numerator Current Input.
5	IDEN	Denominator Current Input. Connect to the IREF pin for most applications.
6	IREF	100 nA Trimmed Reference Current Output. Connect to the IDEN pin for most applications.
9	VDEN	Voltage Output of Denominator Log Amplifier. Connect this pin to the INDN pin and decouple with an external 0.1 µF capacitor to ground.
10	INDN	Denominator Voltage Input to Temperature Compensation Circuit.
11	COMM	Main Ground.
12	NMFS	Numerator Speed Bias (Nominal 1 kΩ Resistor to VNEG Pin).
13	VNEG	Negative Supply.
14	DNFS	Denominator Speed Bias (Nominal 1 kΩ Resistor to VNEG Pin).
15, 18	ACOM	Analog Common, Low Noise Reference Ground. Important that both pins are always grounded.
16	HFCP	High Frequency Compensation.
17	2VLT	2.0 V Reference Output.
19	SCL3	7.5 kΩ Scaling Resistor (See Figure 1). Default is NIC.
20	SCL2	5 kΩ Scaling Resistor (See Figure 1). Default is to connect to the INMS pin.
21	SCL1	5 kΩ Scaling Resistor (See Figure 1). Default is to connect to the VLOG pin.
22	VLOG	Primary Logarithmic Output. For $I_{NUM} = I_{DEN}$, the VLOG pin is at the voltage applied to the INPS pin.
23	INMS	Output Buffer Amplifier Inverting Input.
24	INPS	Output Buffer Amplifier Noninverting Input. The INPS, DCBI, and VSM1 to VSM4 pins must be tied together.
26	1P5V	1.5 V Reference Output. Connect to the INPS, DCBI, and VSM1 to VSM4 pins for single-supply operation.
27	DCBI	Approximately 1.3 mA Bias Current. Connect this pin to the VSM1 to VSM4 pins. See Pin 2, Pin 3, Pin 7, and Pin 8 description.
28	BSDC	Internal Bias Node. Decouple with a series connection of 4 Ω and 1 µF to ground.
29	VPOS	Positive Supply.
30	IMON	Photodiode Monitor Output. $I_{MON} = 1.1 \times I_{NUM}$.
31	INNM	Numerator Voltage Input to Temperature Compensation Circuit.
32	VNUM	Voltage Output of Numerator Log Amplifier. Connect this pin to the INNM pin. For the fastest response, do not add an external capacitor.
0	EPAD	Exposed paddle. Connect the exposed paddle to the VSM1 to VSM4 pins to provide low leakage guard.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 5 V, V_{NEG} = 0 V, T_A = 25°C; IDEN = IREF; VSM1 to VSM4, 1P5V, DCBI, and INPS tied together; SCL1 = VLOG; SCL2 = INMS; SCL3 = open; scale = 200 mV/dec; VLOG output load R_L > 2 kΩ, unless otherwise noted.

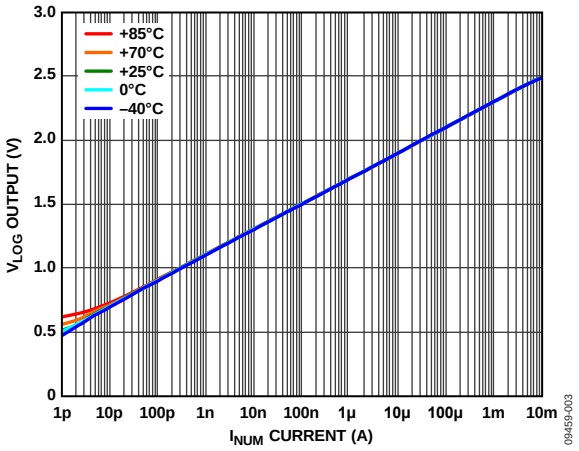


Figure 3. V_{LOG} vs. I_{NUM} for Multiple Temperatures

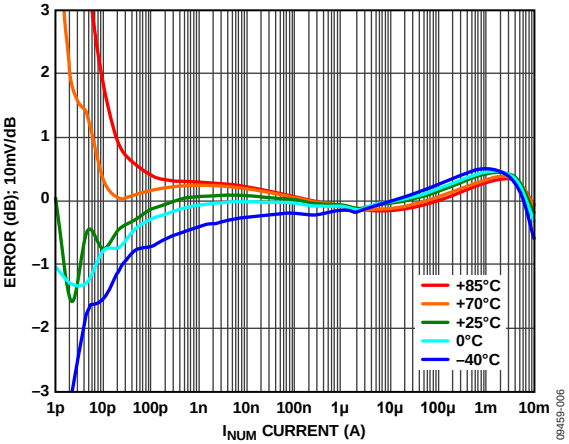


Figure 6. Law Conformance Error vs. I_{NUM} for Multiple Temperatures; Normalized to 25°C

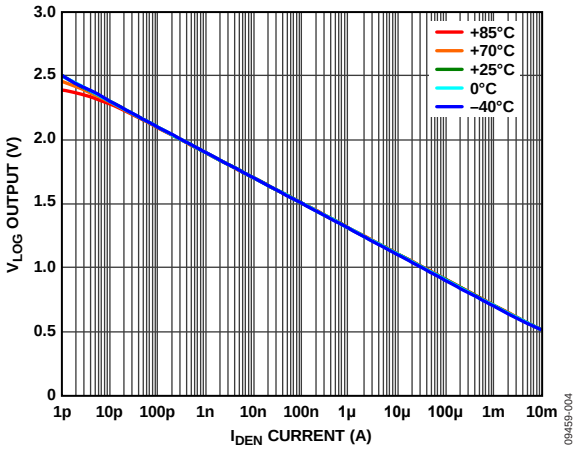


Figure 4. V_{LOG} vs. I_{DEN} for Multiple Temperatures; I_{NUM} = 100 nA

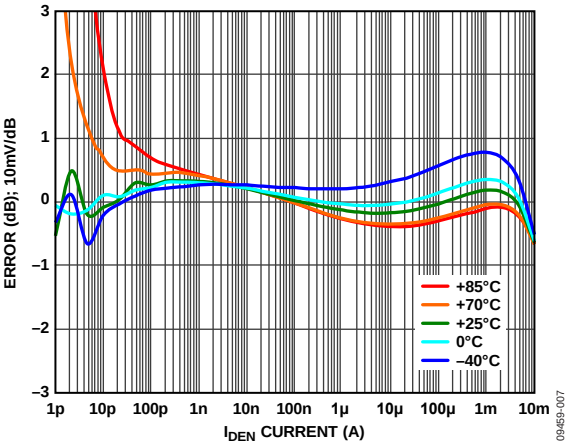


Figure 7. Law Conformance Error vs. I_{DEN} for Multiple Temperatures; I_{NUM} = 100 nA; Normalized to 25°C

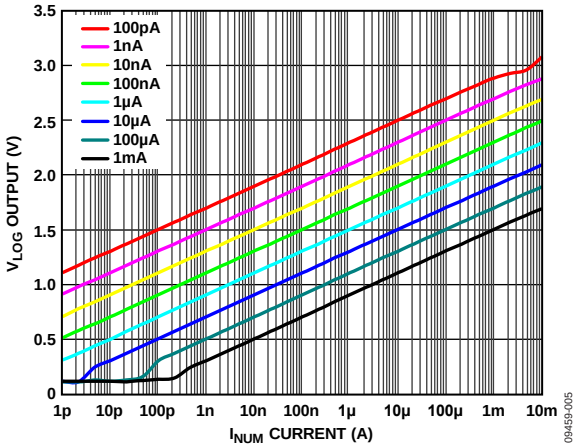


Figure 5. V_{LOG} vs. I_{NUM} for Multiple Values of I_{DEN} (Decade Steps from 100 pA to 1 mA)

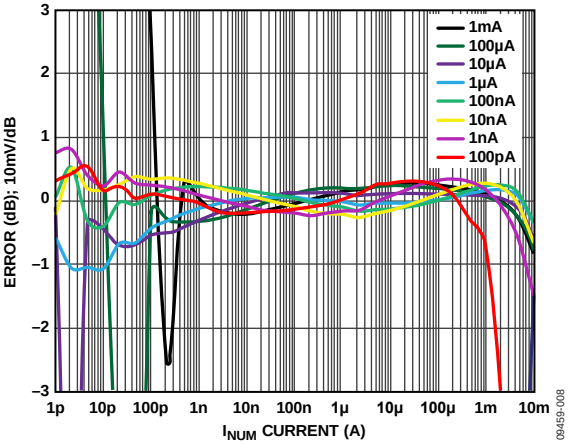


Figure 8. Law Conformance Error vs. I_{NUM} for Multiple Values of I_{DEN} (Decade Steps from 100 pA to 1 mA)

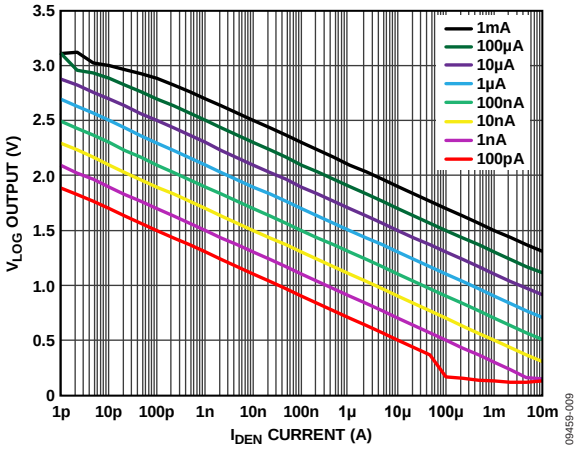


Figure 9. V_{LOG} vs. I_{DEN} for Multiple Values of I_{NUM} (Decade Steps from 100 pA to 1 mA)

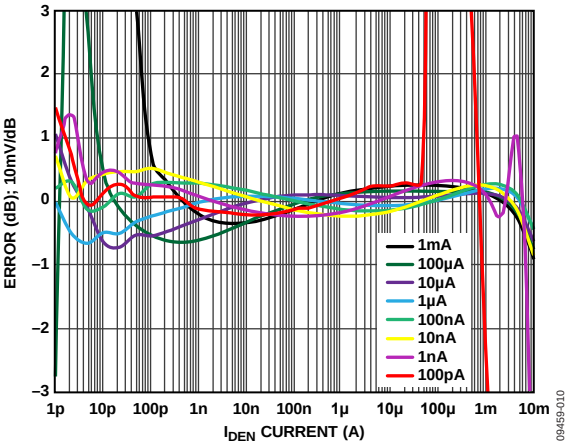


Figure 12. Law Conformance Error vs. I_{DEN} for Multiple Values of I_{NUM} (Decade Steps from 100 pA to 1 mA)

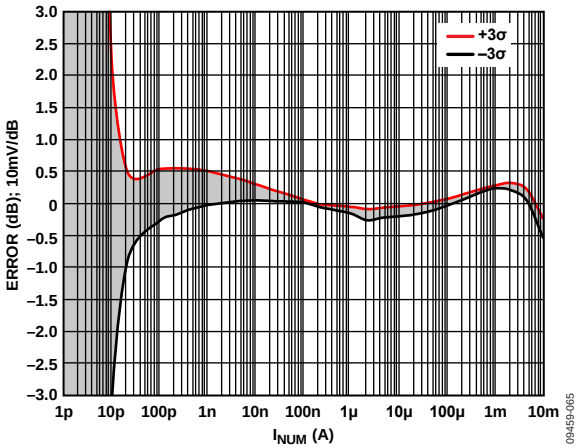


Figure 10. Law Conformance Error Distribution vs. I_{NUM} (3 σ Either Side of Mean)

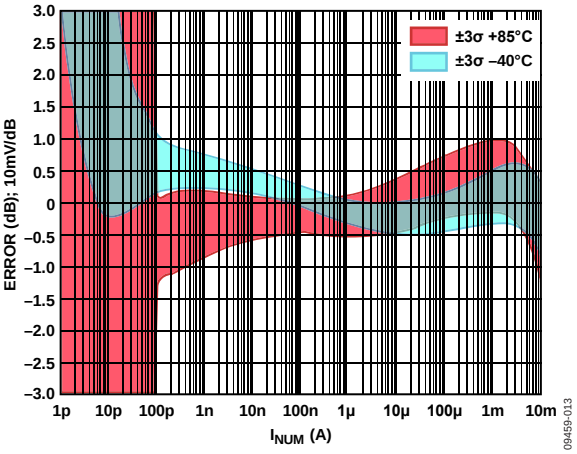


Figure 13. Law Conformance Error Distribution vs. I_{NUM} for –40°C and +85°C (3 σ Either Side of Mean)

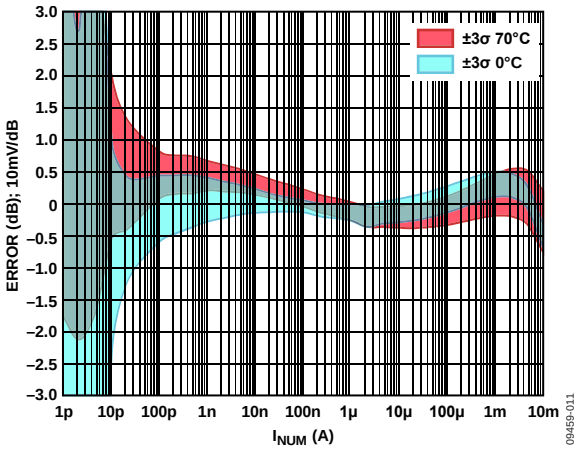


Figure 11. Law Conformance Error Distribution vs. I_{NUM} for 0°C and 70°C (3 σ Either Side of Mean)

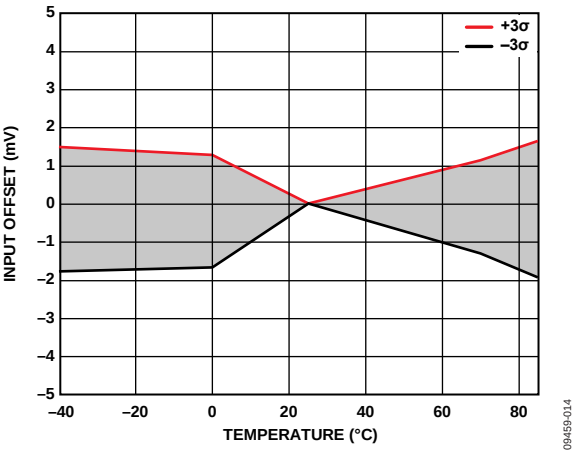


Figure 14. (V_{INUM} – V_{SUM}) vs. I_{NUM} for Multiple Temperatures

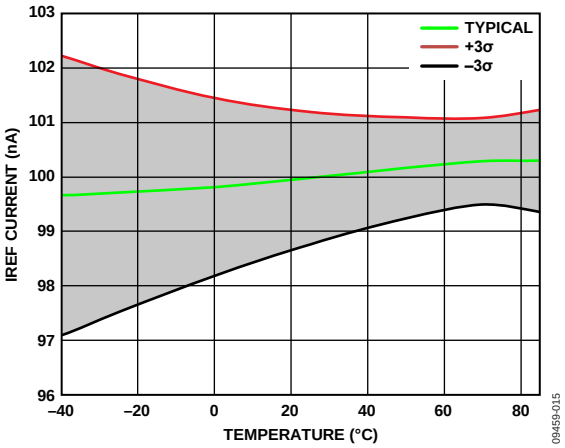


Figure 15. IREF Current vs. Temperature

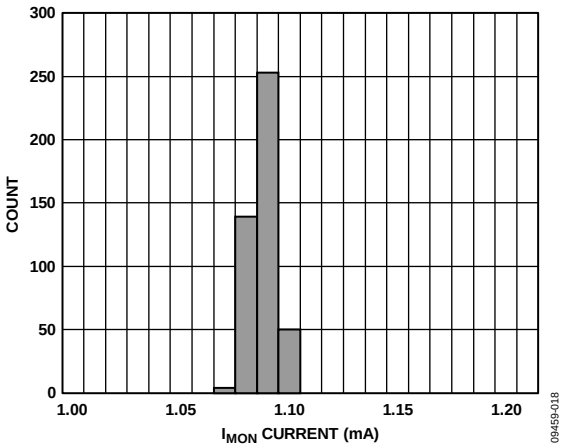


Figure 18. I_{MON} Histogram at I_{NUM} = 1 mA

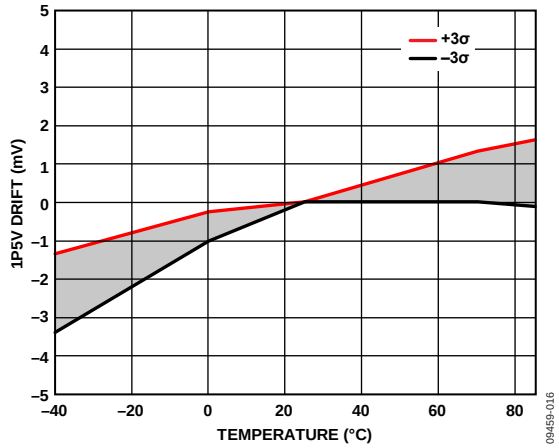


Figure 16. 1P5V Drift vs. Temperature

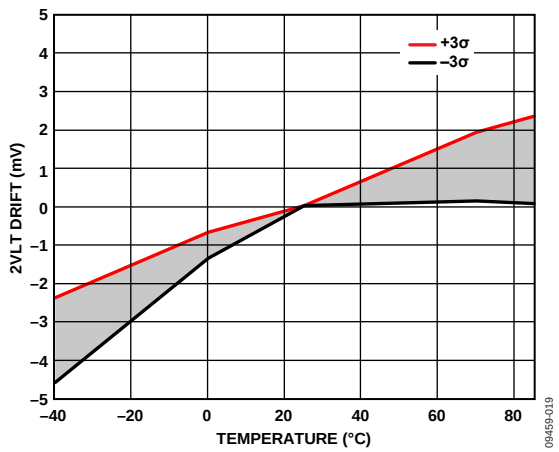


Figure 19. 2VLT Drift vs. Temperature

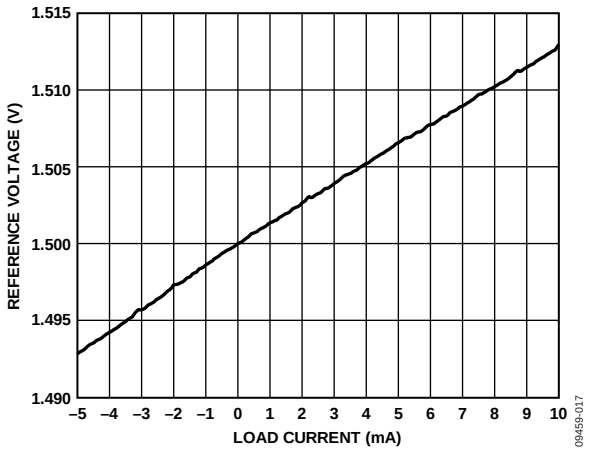


Figure 17. 1P5V vs. I_{LOAD} (Positive Current Defined into 1P5V Pin)

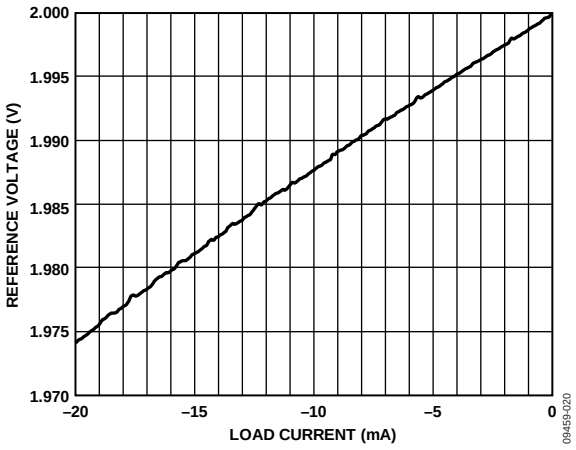


Figure 20. 2VLT vs. I_{LOAD} (Positive Current Defined into 2VLT Pin)

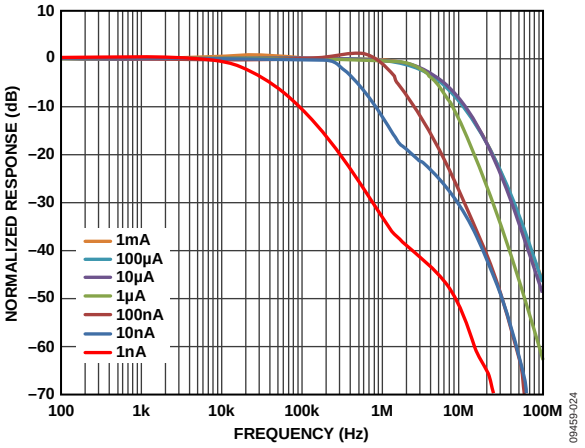


Figure 21. Small Signal AC Response from I_{NUM} to V_{LOG} for I_{NUM} in Decade Steps from 1 nA to 1 mA, I_{DEN} = 100 nA

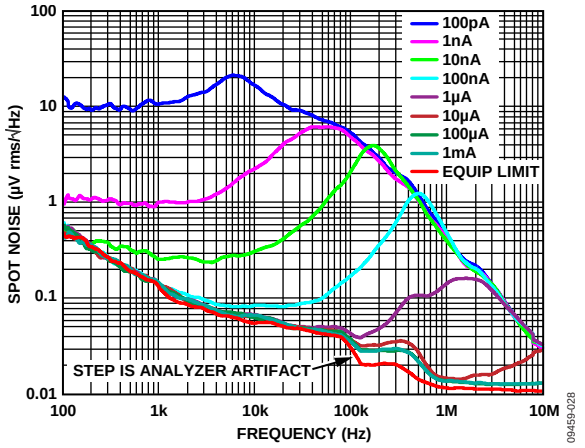


Figure 22. Spot Noise Spectral Density at VLOG vs. Frequency for I_{NUM} in Decade Steps from 1 nA to 1 mA (Noise at lower frequencies, where NSD is flat, is limited by resistance used to generate dc I_{NUM} current. See the Noise vs. Current section for further explanation.)

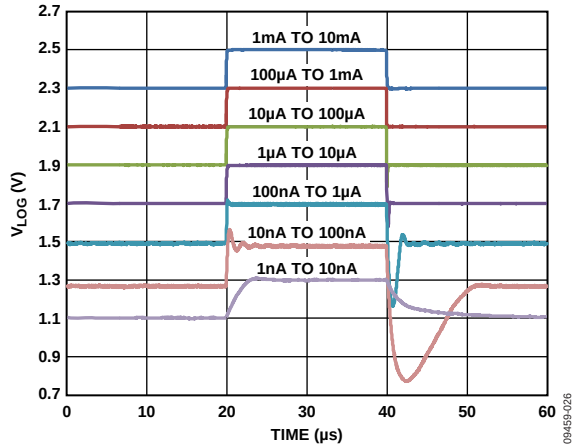


Figure 23. Pulse Response for I_{NUM} in Decade Steps from 1 nA to 1 mA, I_{DEN} = 100 nA

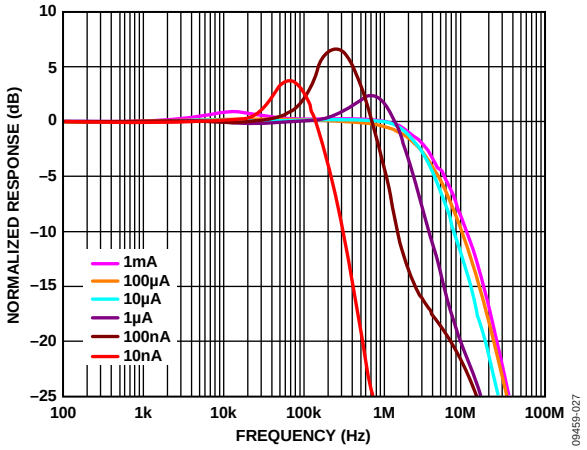


Figure 24. Small Signal AC Response from I_{DEN} to V_{LOG} for I_{DEN} in Decade Steps from 10 nA to 1 mA; I_{NUM} = 100 nA

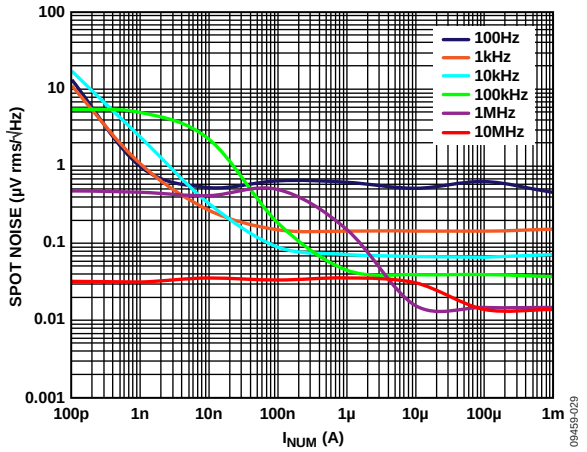


Figure 25. Spot Noise Spectral Density at VLOG vs. I_{NUM} in Decade Frequency Steps from 100 Hz to 10 MHz

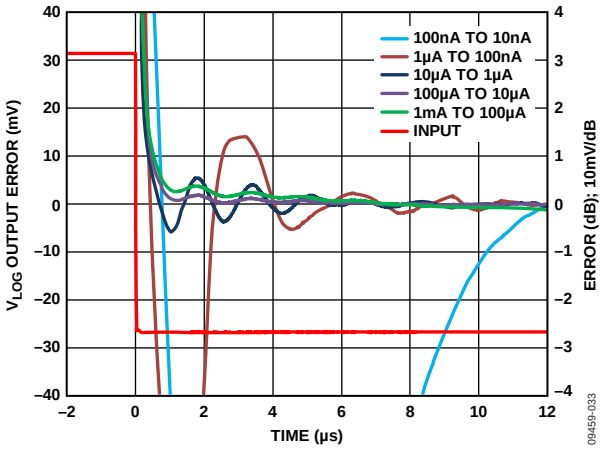


Figure 26. Normalized Falling Edge Settling of I_{NUM} to Within 1 dB (Error = 10 mV/dB)

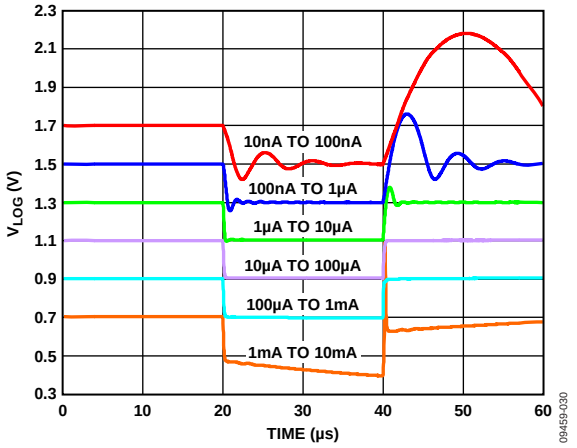


Figure 27. Pulse Response for I_{DEN} in Decade Steps from 1 nA to 1 mA; I_{NUM} = 100 nA

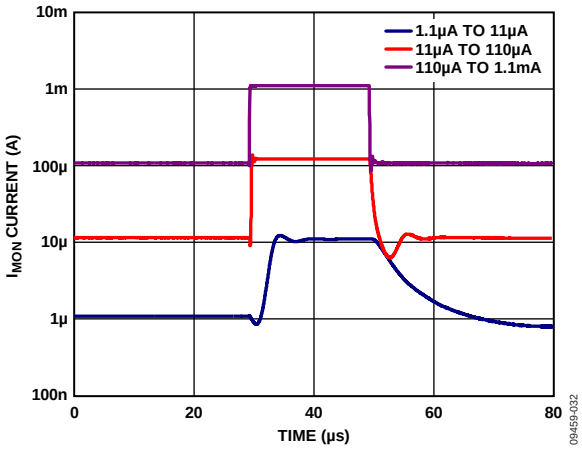


Figure 28. I_{MON} Pulse Response vs. I_{NUM}

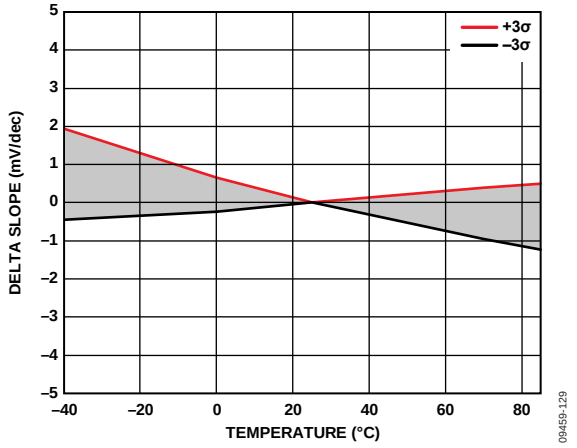


Figure 29. Slope Drift vs. Temperature for 200 mV/dec (3 σ to Either Side of Mean)

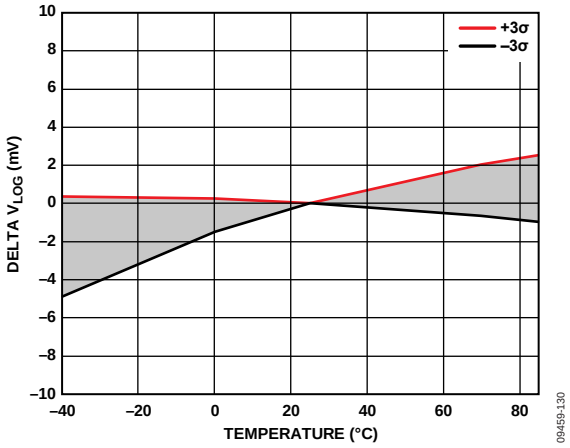


Figure 30. Logarithmic Offset Drift vs. Temperature (3 σ to Either Side of Mean)

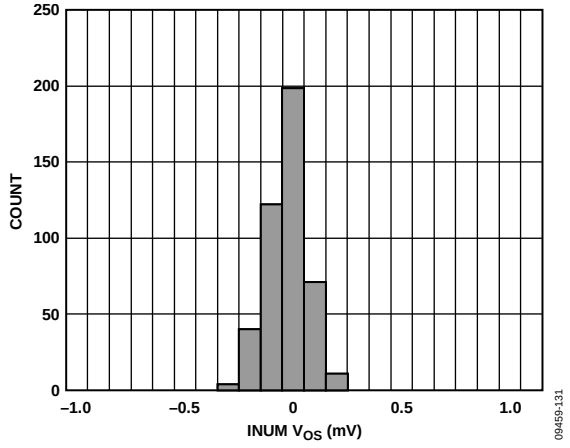


Figure 31. (V_{NUM} – V_{SUM}) Histogram at 25°C

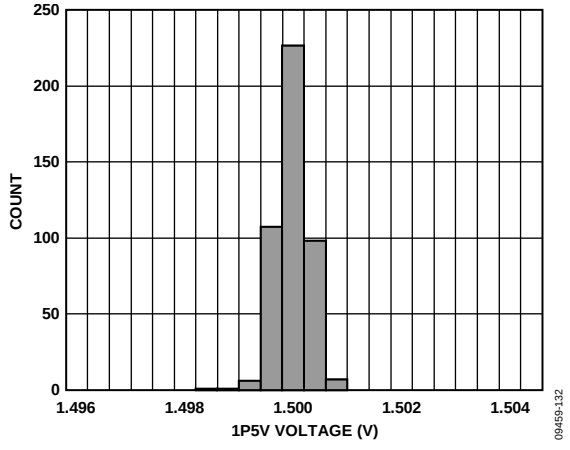


Figure 32. 1P5V Histogram

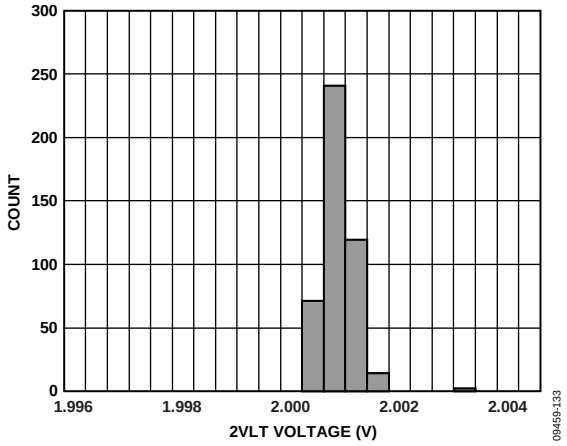


Figure 33. 2VLT Histogram

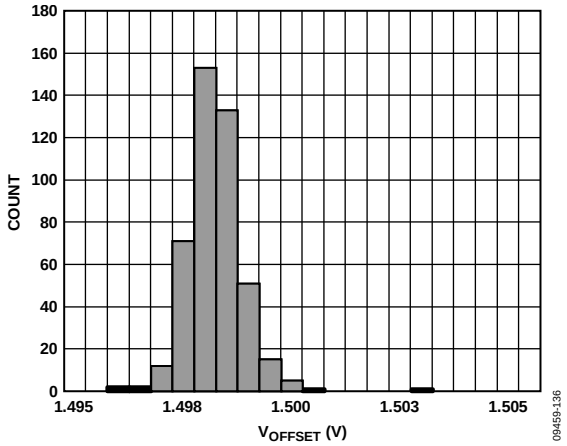


Figure 36. Distribution of V_{LOG} for $I_{NUM} = I_{DEN} = 100$ nA (Nominally 1.500 V)

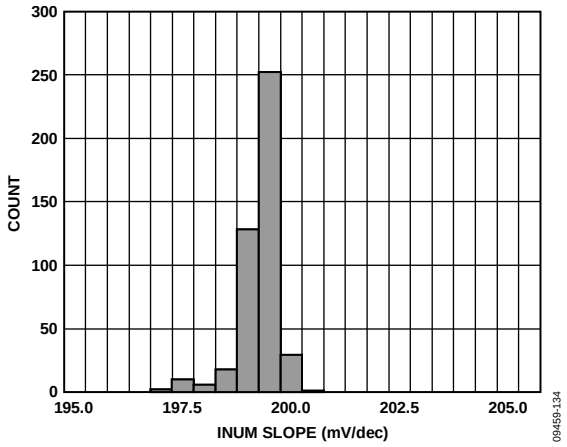


Figure 34. Distribution of Logarithmic Slope (Nominally 200 mV/dec)

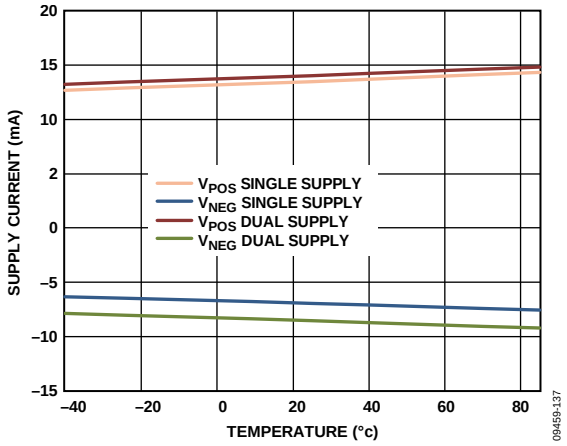


Figure 37. Supply Current vs. Temperature ($|V_{POS}|$, $|V_{VNEG}|$)

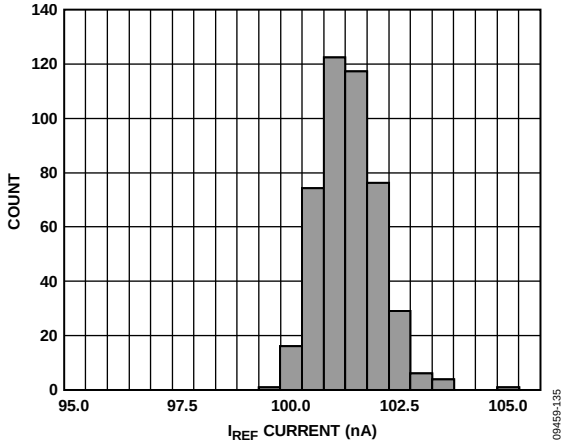


Figure 35. Distribution of I_{REF} (Nominally 100 nA)

TEST CIRCUITS

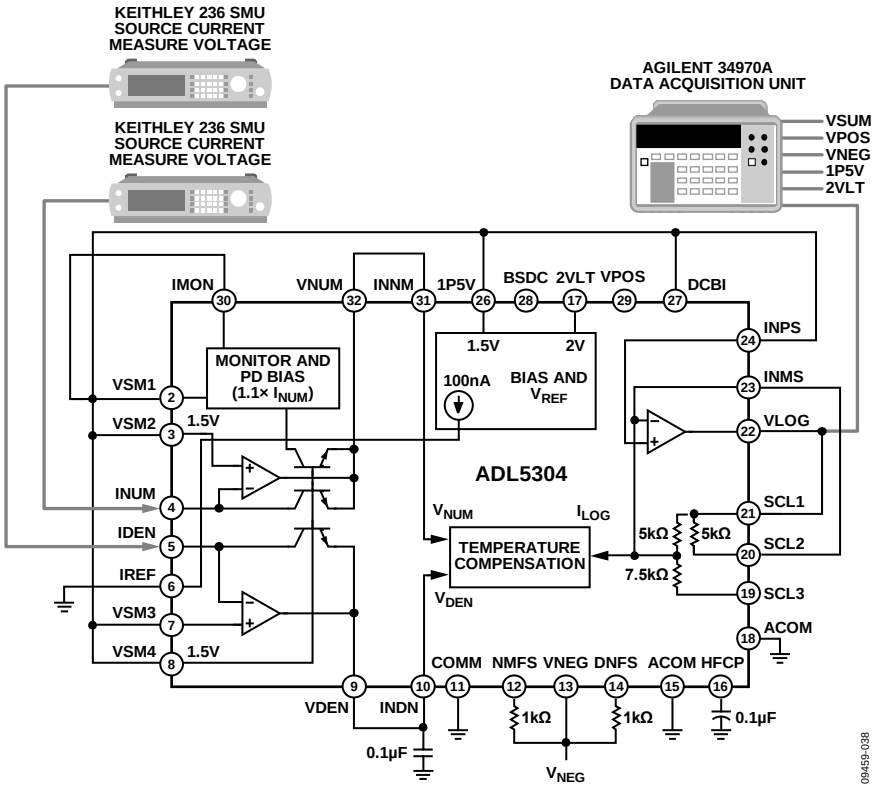


Figure 38. Setup for Measuring Logarithmic/Slope/Offset Conformance

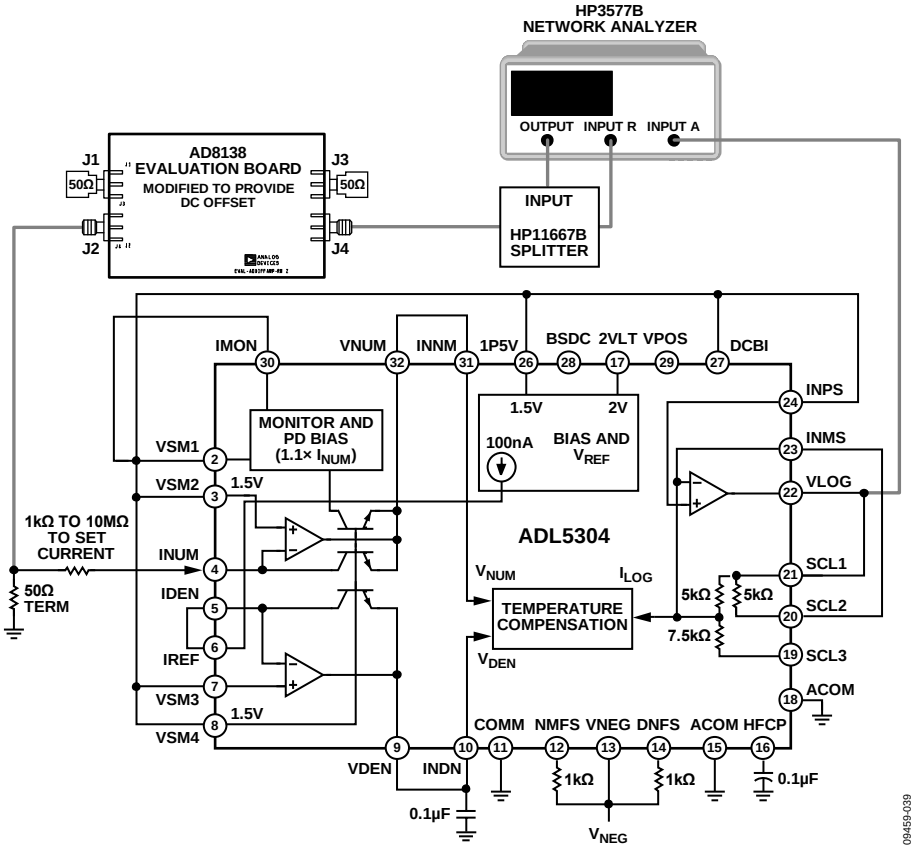


Figure 39. Setup for Measuring Bandwidth

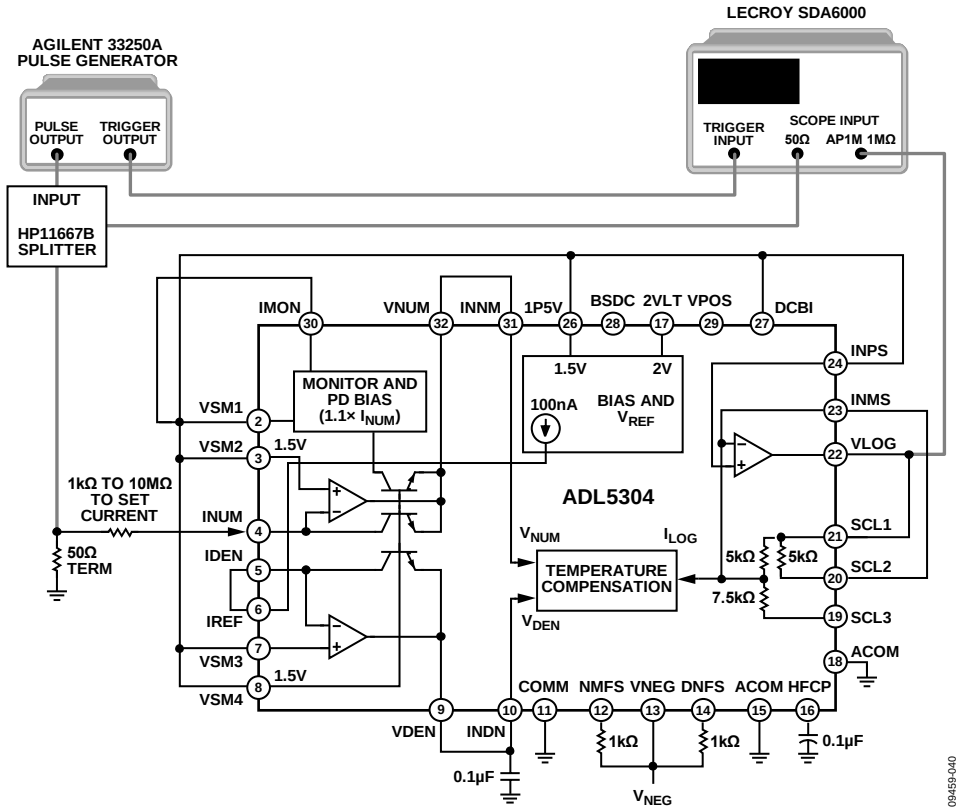


Figure 40. Setup for Measuring Pulse Settling

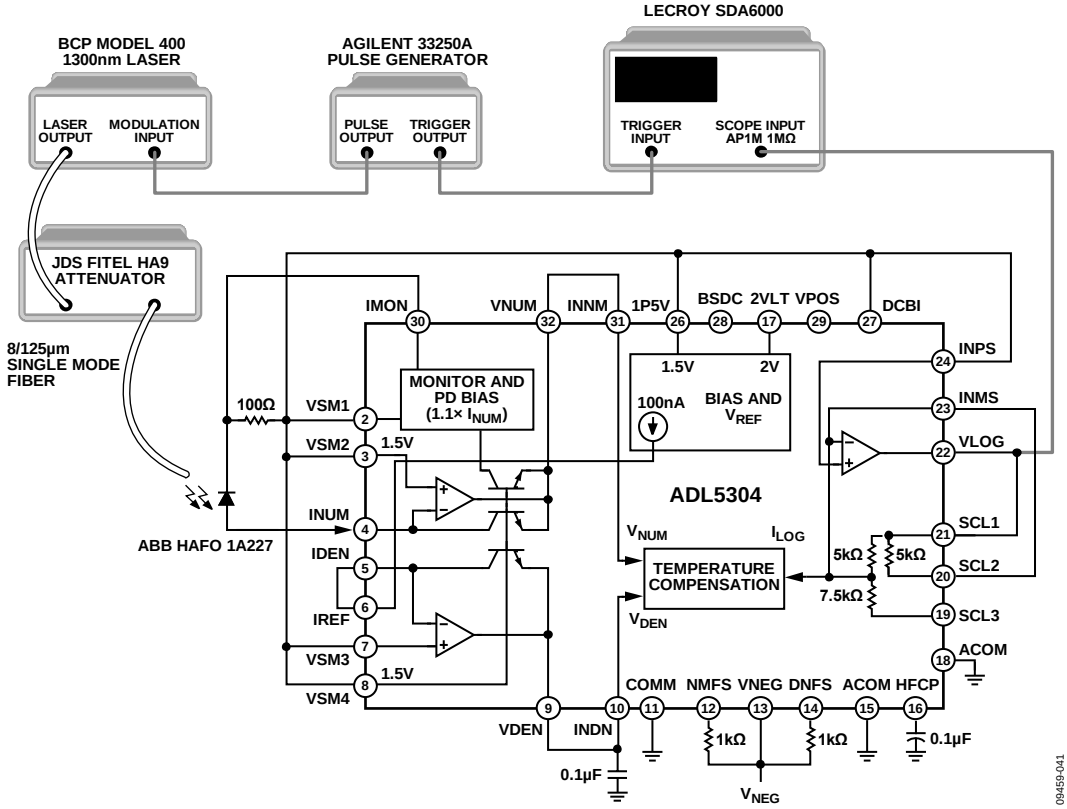


Figure 41. Setup for Measuring Photodiode Pulse Response

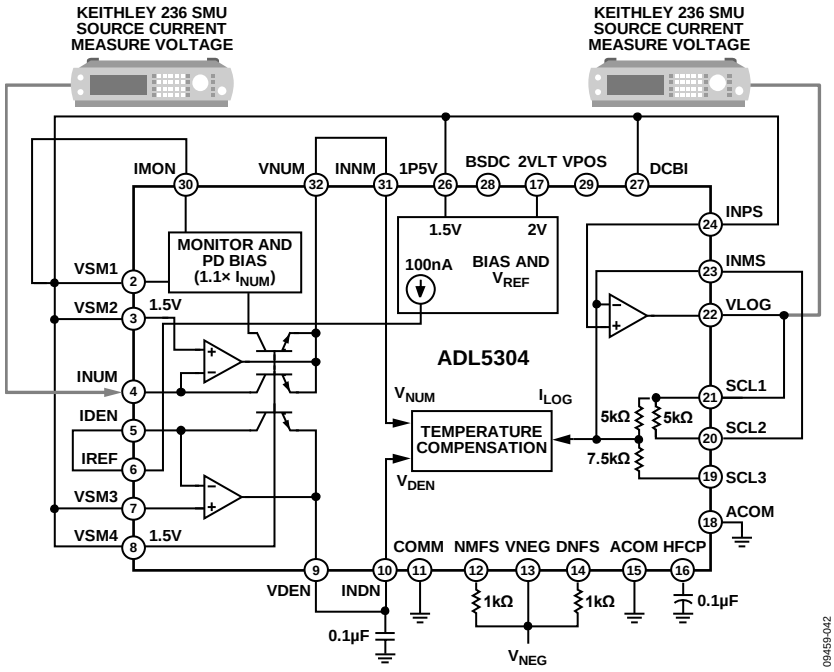


Figure 42. Setup for Measuring Output

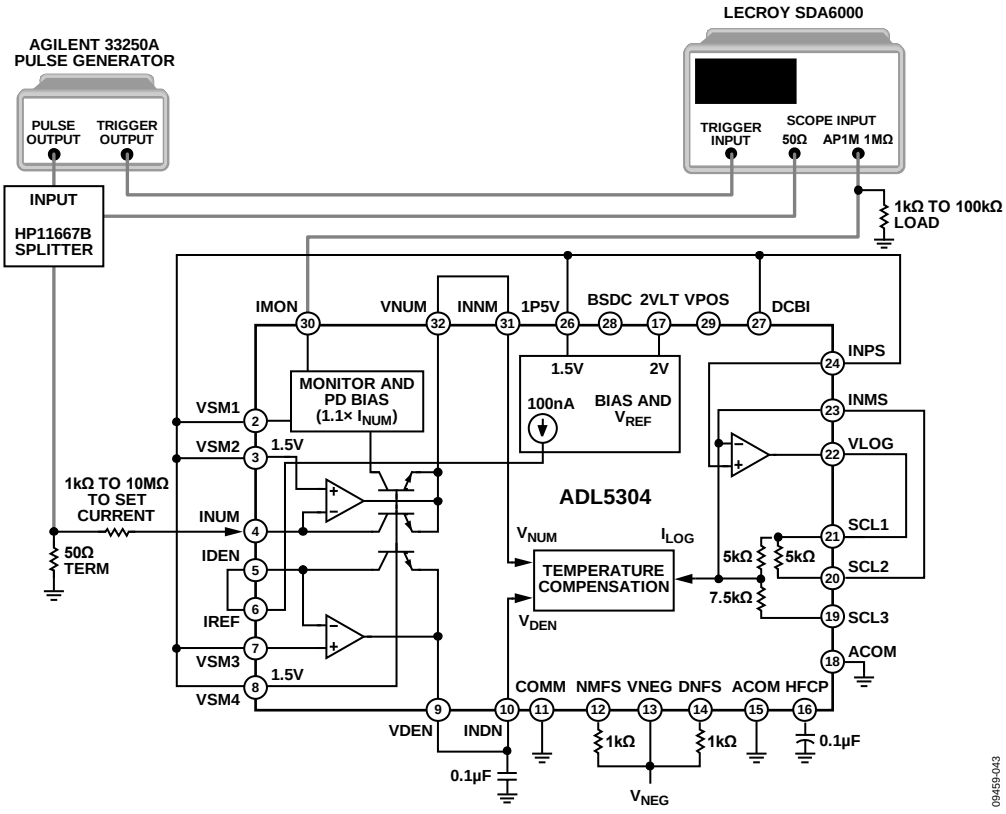


Figure 43. Setup for Measuring IMON Pulse Response

TERMINOLOGY

Optical Power
Optical power is defined as photon energy per unit of time measured as radiant flux (Φ) or radiant power, which is radiant energy (Q) per unit time.

Photodiode Responsivity
Photodiode (PD) responsivity, ρ, is a constant that correlates optical power (P_{OPT}) with PD current (I_{PD}).

$$I_{PD} = \rho \times P_{OPT} \quad (1)$$

where typical values for ρ of InGaAs p-intrinsic-n (PIN) photodiodes are in the range of 0.6 A/W to 1 A/W. In the case of 1 A/W, this means that for 1 mW of incident optical power, P_{OPT}, the PD delivers 1 mA of current, I_{PD}.

When the photodiode current input to the ADL5304 is divided by the responsivity, the log slope directly represents the change in input optical power, P_{OPT}.

Dark Current
All reverse-biased diodes develop a current due to the random generation of electrons/holes in the depletion region. In photodiodes, this current occurs with no incident light falling on the diode and is called the dark current, I_{DK}. Dark current limits the minimum signal that can be reliably detected. For high speed InGaAs PIN photodiodes, the I_{DK} is typically around 5 nA. For a photodiode with a responsivity of 1 A/W, a 5 nA I_{DK} limits minimum measureable optical power to −53 dBm.

Logarithmic Function
The logarithmic function is

$$V_{LOG} = V_Y \times \log_{10}\left(\frac{I_{NUM}}{I_Z}\right) \quad (2)$$

Logarithmic Slope
Logarithmic slope is the change in output voltage (V_{LOG}) for a given change in input current usually shown as a semi-log graph where one input current (I_{NUM} or I_{DEN}) is plotted on a log scale, and the output voltage (V_{LOG}) is plotted on a linear scale. The other input current is fixed. Typically, slope is denoted as V_Y with units of mV/decade or mV/dB. For the ADL5304, in the default configuration, V_Y = 200 mV/decade (10 mV/dB).

Logarithmic Intercept
Logarithmic intercept, I_Z, is an extrapolated value representing the input current where V_{LOG} = 0 V. In single-supply operation (the VSMx pins = DCBI = INPS = 1P5V), V_{LOG} is always positive, and when the ADL5304 is operating in the default configuration of $I_{DEN} = I_{REF}$ = 100 nA, the logarithmic intercept occurs at I_{NUM} = 3.162 fA.

In the case of dual-supply operation of the device, the intercept can be shifted to different values depending on where the VSM1 to VSM4, DCBI, and INPS pins are biased; the only recommended values are either 1.5 V via connection to the 1P5V pin, as in the case of single-supply operation, or ground when a dual supply is used.

For example, if connected to ground, then the intercept is at $I_Z = I_{DEN} = I_{NUM}$ for which $\log(I_{NUM}/I_{DEN}) = 0$. This is how most people interpret the function log(x).

The most practical way to define intercept is to simply always use $\log_{10}(I_{NUM}/I_{DEN}) = 0$ as the reference point. The only consequence is that a V_{OFS} needs to be introduced depending on how the output buffer gain and offset is set up.

$$V_{LOG} = V_Y \times \log_{10}\left(\frac{I_{NUM}}{I_{DEN}}\right) + V_{OFS} \quad (3)$$

For the default single-supply setup, as shown in Figure 1, V_Y = 0.2 V/decade and V_{OFS} = 1.5 V (derived from the 1P5V pin), and I_{DEN} is supplied by the on-chip trimmed I_{REF} = 100 nA.

The relationship between I_Z and V_{OFS} is as follows:

$$I_Z = \frac{I_{DEN}}{10^{\left(\frac{V_{OFS}}{V_Y}\right)}} = \frac{I_{REF}}{10^{\left(\frac{V_{1P5V}}{V_Y}\right)}} = \frac{100\text{ nA}}{10^{\left(\frac{1.5\text{V}}{0.2\text{V/dec}}\right)}} \quad (4)$$

Because I_{REF} and V_Y are trimmed for the default setup with V_{OFS} = 1.500 V, I_Z should also be a stable quantity; however, because it is a calculated value determined by the I_{REF}, V_{1P5V}, and V_Y parameters, its distribution is the combination of the three parameters and wider than the original parameters.

The ideal single- and dual-supply ADL5304 responses are shown in Figure 44.

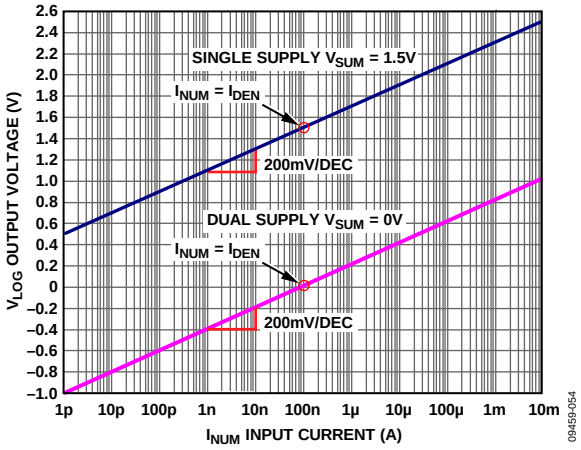


Figure 44. Ideal Transfer Function

THEORY OF OPERATION

BASIC CONCEPTS

The ADL5304 exploits the logarithmic relationship between base emitter voltage, V_{BE}, and the collector current, I_C, of a bipolar junction transistor (see Equation 5). This is the fundamental basis of the extended class of translinear circuits. A log amp based on this unique property of the bipolar transistor is called a translinear log amp to distinguish it from log amps designed for RF applications, which use different principles while having similar objectives.

$$V_{BE} = V_T \log(I_C/I_S) \quad (5)$$

Two scaling quantities appear in Equation 5: the thermal voltage, $V_T = kT/q$, and the saturation current, I_S. The thermal voltage is of crucial importance in determining the logarithmic slope in a translinear log amp. V_T has a process invariant value of 25.69 mV at T = 25°C and varies in proportion to the absolute temperature (PTAT). Saturation current, unlike V_T, is a process and device dependent parameter. Saturation current is typically approximately 10^{-16} A at 25°C, but exhibits enormous variation over temperature, by a factor of more than a billion.

The temperature dependence of saturation current is compensated in the ADL5304 by using a second reference transistor, having an identical variation, to stabilize the intercept by using the difference between the two V_{BE}s.

Input currents, I_{NUM} and I_{DEN}, are the numerator and denominator of the logarithmic argument that follows:

$$\Delta V_{BE} = V_T \log (I_{NUM}/I_{DEN}) \quad (6)$$

In log ratio applications, both I_{NUM} and I_{DEN} may each vary over the full specified range of 1 pA to 10 mA. However, in default operation, I_{DEN} takes the internally preset current of I_{REF} = 100 nA.

Equation 6 shows that the ΔV_{BE} is still PTAT, but the required logarithmic slope must be temperature stable; therefore, this is corrected using proprietary circuit techniques. Using this correction the relationship between a photodiode current, I_{PD}, applied to INUM, and the voltage appearing at the output at VLOG is

$$V_{LOG} = V_Y \log_{10}(I_{PD}/I_Z) \quad (7)$$

where:

V_Y is the log slope voltage (and, for the case of base-10 logarithms, it is also the volts per decade).
I_Z is the extrapolated log intercept.

The relationship between V_Y and ΔV_{BE} is a factor close to 3.333 in the default configuration from (V_{NUM} – V_{DEN}) to the output of VLOG. Because a decade change in the input current ratio results in close to a 60 mV/decade change in ΔV_{BE}; multiplying this by 3.333 results in 0.2 V/decade. During fabrication, V_Y is trimmed to 0.2 V/decade (10 mV/dB), I_{REF} to 100 nA, V_{OFS} to 1.500 V, and I_Z to 3.162 fA. When I_{PD} = 1 pA, the output V_{LOG} has a value of 0.5 V (see Figure 44). I_Z is small because V_{LOG} is always above ground potential even at the lowest end of the dynamic range, when using V_{OFS} = 1.500 V. If a negative supply is used, this voltage can cross zero at the intercept value.

The output for the value of I_{PD} can be calculated using Equation 8. For example, with an input current of 100 nA,

$$V_{LOG} = 0.2 \text{ V} \log_{10}(100 \text{ nA}/3.162 \text{ fA}) = 1.500 \text{ V} \quad (8)$$

The slope and intercept can be adjusted to suit the application, to either higher or lower values, without significant loss of calibration accuracy.

OPTICAL MEASUREMENTS

It is important to understand the transducer aspects of a photodiode when interpreting the photodiode current relative to the incident optical power.

In purely electrical circuits, current applied to a resistive load results in a power proportional to the square of the current. For a photodiode interface, however, there is a difference in scaling because photon-generated photodiode current (I_{PD}) flows in an element biased at a fixed voltage. I_{PD} is equal to the optical power (P_{OPT}) absorbed in the detector times the responsivity of the photodiode (ρ).

$$I_{PD} = \rho \times P_{OPT} \quad (9)$$

A similar relationship exists between the intercept current, I_Z, and effective intercept power, P_Z.

$$I_Z = \rho \times P_Z \quad (10)$$

Therefore, the V_{OUT} equation for the ADL5304 may be written as

$$V_{LOG} = V_Y \log_{10}(P_{OPT}/P_Z) \quad (11)$$

For the ADL5304 operating in its default mode, an I_Z of 3.162 fA corresponds to a P_Z of 3.95 fW for a diode having a responsivity of 0.8 A/W. An optical power of 12.5 µW therefore generates

$$V_{LOG} = 0.2 \text{ V} \log_{10}(12.5 \text{ µW}/3.95 \text{ fW}) = 1.900 \text{ V} \quad (12)$$

In optical applications, the interpretation of V_{LOG} is as an equivalent optical power; therefore, the slope for calculation purposes remains 10 mV/dB (for either current or power).

Decibel Scaling

When signal power is expressed in decibels above a reference level (for example, dBm, when the reference is 1 mW), logarithmic conversion has already been implicitly performed. Therefore, the log ratio in the previous expressions becomes a simple difference. Be careful in assigning variable names, because P is often used to denote actual power as well as this same power expressed in decibels. These are very different quantities. Misunderstandings can be avoided by using D to denote decibel powers.

When V_Y (the volts/decade) is converted to its decibel value, $V_Y' = V_Y/10$ (because there are 10 dB per decade in the context of a power measurement), it can be written

$$V_{LOG} = 20 \text{ mV}(D_{OPT} - D_Z) \quad (13)$$

where:

D_{OPT} is the optical power expressed in decibels above a reference level.
D_Z denotes the equivalent intercept power relative to the same level.

Using the previous example and assuming a reference power of 1 mW, a P_{OPT} of 12.5 µW corresponds to a D_{OPT} of $10 \log_{10}(12.5 \text{ µW}/1 \text{ mW}) = -19.03$ dBm; the equivalent intercept power of 3.95 fW corresponds to a D_Z of −114.03 dBm. Therefore,

$$V_{LOG} = 20 \text{ mV } (-19.03 - (-114.03)) = 1.900 \text{ V} \quad (14)$$

the same result calculated with Equation 12.

CIRCUIT DESCRIPTION

The ADL5304 addresses a wide variety of interfacing conditions to meet the needs of fiber optic supervisory systems, as well as many nonoptical applications. This section explains the general structure of this log amp. The ADL5304 is an order of magnitude faster than any previous log amp that Analog Devices, Inc., has made, through careful FET amp design; the key limitation in the speed at low currents.

Figure 45 is a simplified schematic of the front-end section of the ADL5304. The numerator current, I_{NUM}, is received at the INUM pin. The voltage at this node is equal to that on the two adjacent guard pins, VSM2 and IDEN, differing only by the offset voltage of the JFET op amp that supports the operation of the Translinear Device Q1 that converts the I_{NUM} current to a logarithmic voltage. VSM2 is needed to provide the collector-emitter bias for Q1, and it is preset to 1.5 V via the external connection to Pin 1P5V.

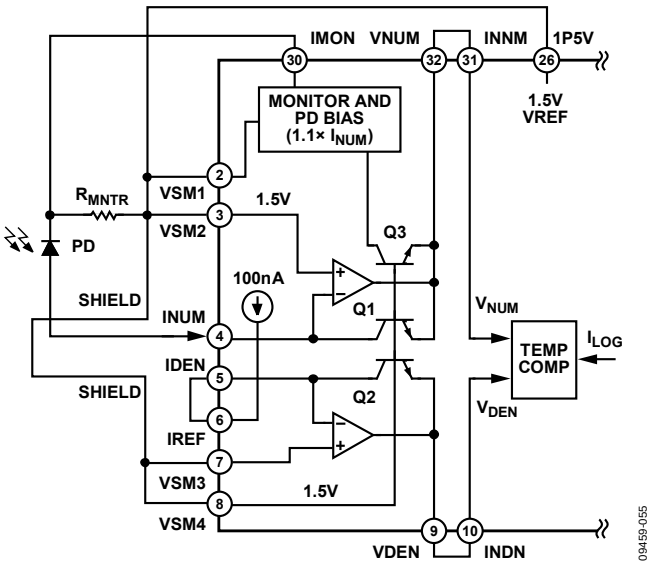


Figure 45. Simplified Front-End Schematic

In conventional translinear log amps, the collector and base of Q1 are both held at ground potential, this is not possible in a single-supply part.

A second transistor, Q2, operates at a collector current of I_{DEN}. In most applications, this is the reference of I_{REF} = 100 nA, supplied internally and laser trimmed.

The difference between the two V_{BE}s with Q1 accepting a photodiode current of $I_{NUM} = I_{PD}$ is

$$V_{BE1} - V_{BE2} = V_T \log_{10}(I_{PD}/I_{REF}) \quad (15)$$

By adding an accurate PTAT voltage of magnitude,

$$V_{OFS} = V_T \log_{10}(I_{REF}/I_Z) = 1.500 \text{ V} \quad (16)$$

resulting in

$$V_{BE1} - V_{BE2} + V_{OFS} = V_T [\log_{10}(I_{PD}/I_{REF}) + \log_{10}(I_{REF}/I_Z)]$$
$$= (kT/q) \log_{10}(I_{PD}/I_Z) \quad (17)$$

The temperature variation of kT/q is then eliminated by an analog divider that essentially puts a variable proportional to temperature underneath the T in Equation 17 and raising the magnitude of kT/q to a stable value of 0.2 V. Therefore, for photodiode applications,

$$V_{LOG} = 0.2 \text{ V} \log_{10}(I_{PD}/I_Z) \quad (18)$$

When the VSM1to VSM4, DCBI, and INPS pins are tied to ground and $V_{NEG} < -2$ V, the offset (V_{OFS}) is removed, leaving the more general form.

$$V_{LOG} = 0.2 \text{ V} \log_{10}(I_{NUM}/I_{DEN}) \quad (19)$$

Bandwidth vs. Current

Both the response time and wideband noise of translinear log amps are functions of the transistor collector current, I_C, and only slightly amenable to improvement by circuit design. The bandwidth falls at low values of I_C due to the effects of junction capacitances in Q1 and the decrease in transconductance (g_m) of a bipolar transistor, which is a linear function of I_C, or in the case of a photodiode application, the photocurrent, I_{PD}. The corresponding incremental emitter resistance is

$$r_e = 1/g_m = V_T/I_{PD} = kT/qI_{PD} \quad (20)$$

and becomes extremely high at low currents (260 MΩ at I_C = 100 pA). Therefore, even minute capacitances associated with the transistor can generate very long time constants.

If the net effect of these capacitances is represented loosely as C_J, the corresponding low-pass corner frequency is

$$f_{-3dB} = qI_{PD}/2\pi kTC_J \quad (21)$$

showing the proportionality of bandwidth to current. Using a value of 0.3 pF for C_J, this becomes 20 MHz/μA. The small signal bandwidth at I_{PD} = 100 pA is thus only 2 kHz. However, whereas this simple model can be useful in making the basic point, it excludes many other effects that limit its accuracy. At high currents, the subsequent signal processing limits the maximum overall bandwidth.

Noise vs. Current

For an ideal bipolar transistor, the voltage noise spectral density, S_{NSD}, referred to V_{BE}, and caused by shot-noise mechanisms, evaluates to

$$S_{NSD} = 14.6/\sqrt{I_C}\ \text{nV}/\sqrt{\text{Hz}}\ (T_A = 27°\text{C}) \quad (22)$$

where I_C is in μA. For example, at an I_C of 1 nA, S_{NSD} evaluates to approximately 0.5 μV/√Hz.

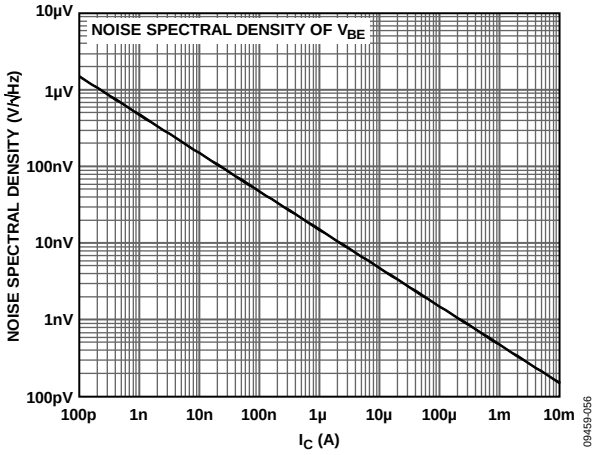


Figure 46. Noise Spectral Density of V_{BE} vs. I_C

Assuming a 20 kHz net system bandwidth at this current, the integrated noise voltage is 70 μV rms. The theoretical noise of V_{BE} vs. I_C is shown in Figure 46. However, the log scaling of the V_{BE} is approximately 3 mV/dB, and in the ADL5304, this is increased to a slope of 10 mV/dB at the VLOG pin. Therefore, the noise at VLOG, predicted by Equation 22, is multiplied by a factor of 3.33. Secondary sources of noise, mostly in the analog divider used for temperature stabilization of the slope and the input FET buffer amplifiers, add to this basic noise. The measured data are shown in Figure 22.

Note how at low frequencies the NSD flattens for input currents less than 10 nA, this noise is limited by the resistor that makes the dc current. A 10 MΩ resistor was used for these three currents with a dc bias voltage across the resistor of 1 mV, 10 mV, and 100 mV, respectively.

A 10 MΩ resistor makes a noise current of 40.7 fA/√Hz, which is converted via the g_m of the logging transistor into a noise voltage. This voltage adds to the noise voltage of the bipolar transistor itself, as shown in Figure 46. The r_e of the transistor is $1/g_m$ and equal to 25.85 MΩ at I_C equals 1 nA. Together with the noise current of the source resistor, this makes a noise voltage at the emitter of the logging transistor (VNUM) of 1.05 μV/√Hz; this contrasts with the noise voltage of the transistor itself of 0.46 μV/√Hz (approximately 0.5 μV/√Hz). The total combined noise is approximately 1.15 μV/√Hz.

The effect of the 10 MΩ resistor at 100 pA of dc current becomes even more pronounced because the noise at VNUM due to the source resistor is 10.5 μV/√Hz, whereas the transistor only contributes 1.46 μV/√Hz for a total of 10.6 μV/√Hz.

Therefore, unless the resistor that makes the dc current becomes very large, in general, measurement at the lower currents is limited by the noise of the source resistor. This problem does not exist when using a photodiode because the resistance of the photodiode increases at the same rate as the logging transistor (see Figure 47).

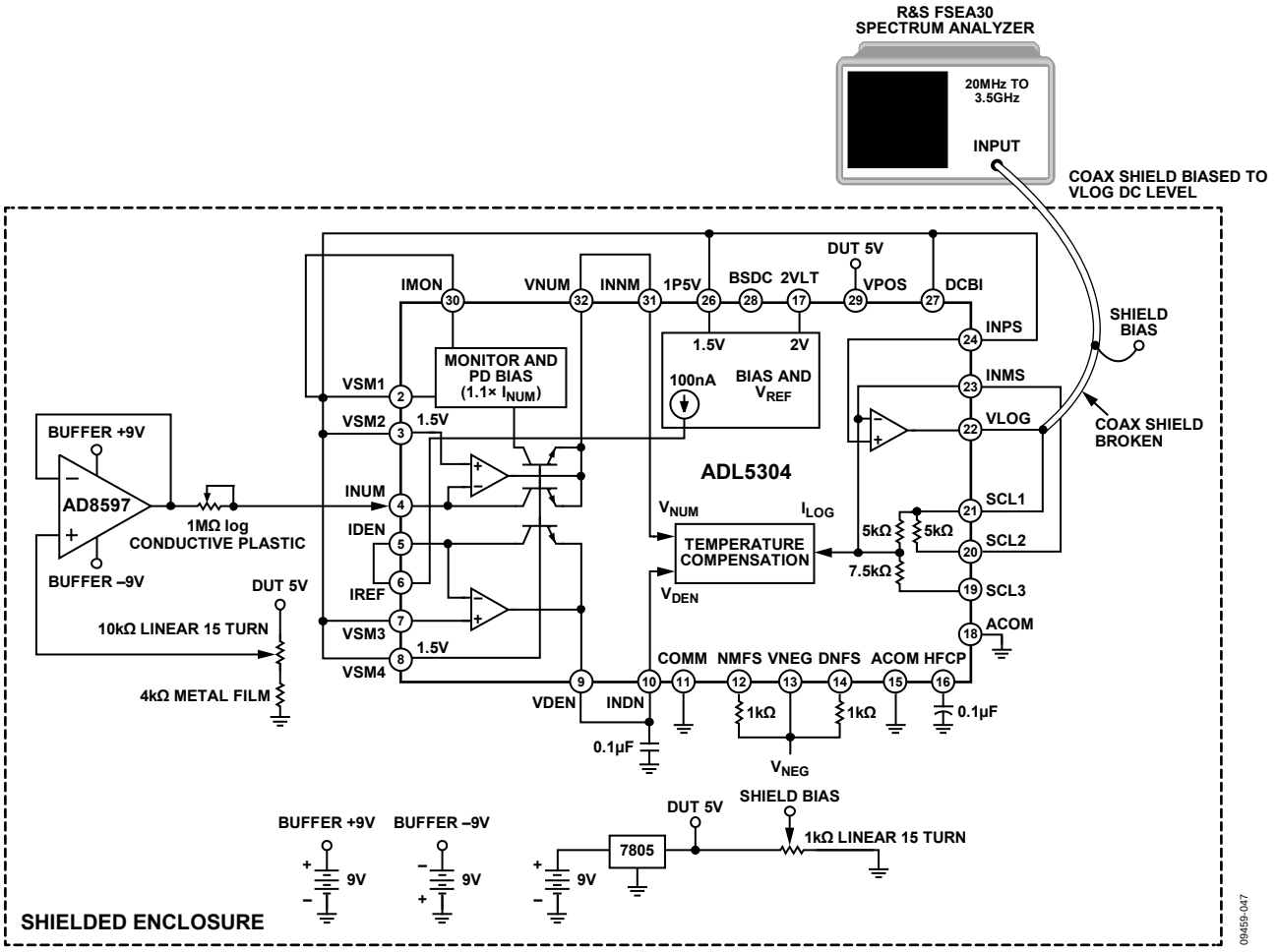


Figure 47. Setup for Measuring Noise for I_{NUM} = 100 pA, I_{NUM} = 1 nA, and I_{NUM} = 10 nA

Filtering to Improve Noise and Dynamic Behavior

The noise at the output of a log amp, particularly at low current levels, leads to uncertainty in the measurement. Noise amplitude is limited by the finite bandwidth.

If measurement speed is not of primary concern, additional filtering can reduce noise. Figure 48 shows the recommended locations for additional external filtering. Note the ADL5304 consists of a current-to-voltage (transimpedance) conversion (I_{NUM} or I_{DEN} to $V_{NUM} - V_{DEN}$), followed by a voltage-to-current conversion ($V_{NUM} - V_{DEN}$ to I_{LOG}), and then followed by another current-to-voltage conversion (I_{LOG} to V_{LOG}).

Typically, capacitors are not used on the numerator side (I_{NUM}) to keep the speed of the device as high as possible. On the denominator side (I_{DEN}), additional filtering is useful to reduce noise. In applications where I_{NUM} is used as the reference to the logarithmic equation and I_{DEN} is a variable, for example, where a reverse logarithmic slope is desired, filtering can be done on the numerator side (I_{NUM}).

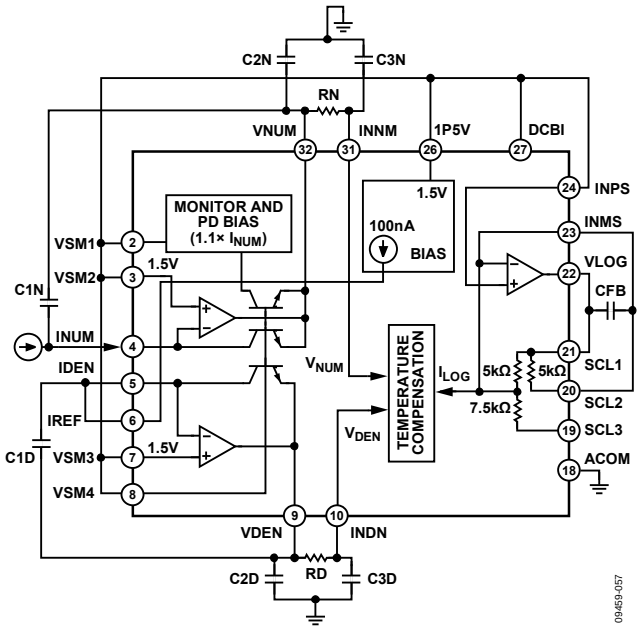


Figure 48. Possible External Filtering Locations

The C1D capacitor effectively reduces the bandwidth of the denominator input stage. A few picofarads of capacitance (<5 pF) reduce the bandwidth significantly for currents below approximately 1 μA, though whereas 1 nF to 10 nF are normally enough to reduce the bandwidth up to the maximum 10 mA of input current. When measurement speed is of primary importance, it is better to add filtering after the FET amp outputs, in which case, C2D, RD, and C3D are the best locations. The resistor in this case should not be much larger than 1 kΩ because there is a bias current that is approximately 35 μA that flows from the temperature compensation block into each of the VDEN and VNUM pins. Inserting a resistor, as shown in Figure 48, lifts up the voltages at the INNM and/or INDN pins and potentially causes headroom problems in the temperature compensation block.

When I_{DEN} is used as the reference, as is normally done, then it is recommended that C1D is zero, C2D is a 0.1 μF ceramic decoupling capacitor, RD is a short, and C3D is not placed.

Adding a capacitor, CFB, adds additional filtering at the buffer output. This capacitor also helps to optimize the pulse response by placing a zero across the feedback resistor (2.5 kΩ in the default configuration). A good value to start with is 22 pF, this introduces a zero at 2.9 MHz that can improve the pulse responses for input currents above approximately 100 μA.

Photodiode Bias

The ADL5304 provides for adaptive photodiode bias. A monitoring transistor, Q3, connected in parallel with Q1 (see Figure 49), samples 1/10th the input current, I_{NUM}. This sampled current is multiplied by a factor of 11 to give an effective output current at the IMON pin of 1.1 times I_{NUM}. Because the photodiode produces I_{NUM}, the additional current has to flow in an external resistor, R_{MNTR}, equal to 10 × R_S, where R_S is the value of the internal parasitic series resistance of the photodiode. This ensures that the actual junction of the photodiode is biased as close as possible to 0 V to minimize dark current. The CMON capacitor provides potential filtering and dynamic currents during fast transients. The value for best bias response depends on the photodiode used and should be determined experimentally. Nominally, CMON = 0.

If the adaptive bias is not used, the IMON pin must be connected to ground. It is easy to provide a 0.5 V reverse bias across the diode by using the 2VLT reference and connecting it to the cathode. Because the ADL5304 forces the voltage at INUM very close to 1.500 V, the trimmed 2.000 V ensures a precise 0.5 V reverse bias for the PD.

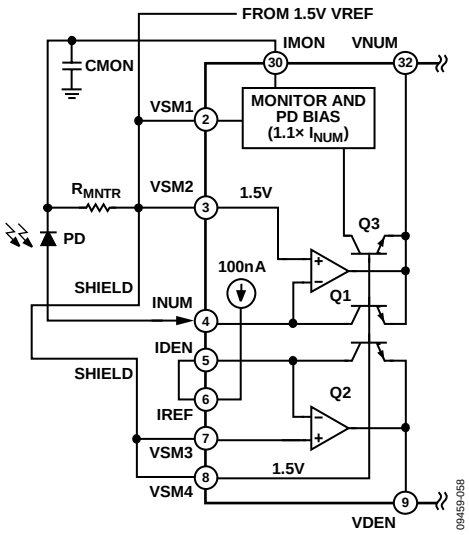


Figure 49. Adaptive Photodiode Bias

One example of dual-supply operation is shown in Figure 50, where the 2.000 V (the 2VLT pin) reference ensures a precisely controlled, reverse bias across the PD. The user can use other reverse bias voltages but needs to provide them separately. Note that when the VSMx pins are grounded, the DCBI and INPS pins must also be grounded.

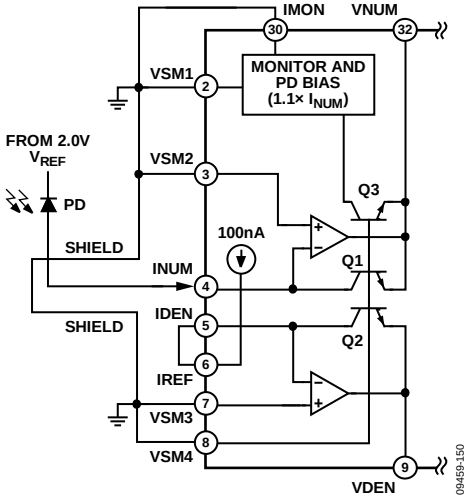


Figure 50. PD Bias with V_{SUM} at Ground and Using 2.000 V

Reference Outputs

The ADL5304 has three trimmed precision references, two voltages, and one current (I_{REF}). The voltages are 1.500 V and 2.000 V at the 1P5V and 2VLT pins, respectively. The 1P5V reference is intended to provide the bias to the VSM1 to VSM4, DCBI, and INPS pins; it can sink up to 10 mA and source a maximum of about 5 mA.

The 2VLT reference can source up to 20 mA of current, but it cannot sink any current. The primary use of the 2.0 V reference is for photodiode bias, or to generate reference currents other than the 100 nA provided by I_{REF}. Together with a precision resistor, the 1.5 V and 2.0 V references can reliably generate any current up to approximately 5 mA.

The I_{REF} current, nominally 100 nA, flows out of the IREF pin and is primarily used as an input to the IDEN pin to provide the denominator current, I_{DEN}. The choice of 100 nA places it in the middle of the 1 pA to 10 mA range. I_{REF} can also be used as the input to the INUM pin and thereby invert the basic log response of the ADL5304. If $I_{DEN} = I_{REF}$, V_{LOG} increases with increasing I_{NUM}. Whereas if $I_{NUM} = I_{REF}$ and the input current is applied to IDEN, V_{LOG} decreases with increasing I_{DEN}.

Buffer Amplifier

A buffer amplifier completes the signal chain that takes the I_{LOG} current from the temperature compensation block and converts it to a voltage at the VLOG pin. The buffer amplifier gain and offset can be configured to provide different logarithmic slope and intercept at the V_{LOG} output. On-chip resistors provide optimized scale factors and intercepts via the SCL1, SCL2, and SCL3 pins.

For example, in Figure 51, the default setup provides a scale of 0.2 V/decade and an intercept of 3.162 fA. $V_{OFS} = V_{LOG} = 1.5$ V when the internal $I_{LOG} = 0$ A, which corresponds to $I_{NUM} = I_{DEN}$. I_{LOG} varies from −400 µA to +400 µA with a scale of 80 µA/decade over the full 200 dB input current range. In the default configuration, I_{LOG} is negative for $I_{NUM} > I_{DEN}$ and positive for $I_{NUM} < I_{DEN}$. If the input current is applied to the IDEN pin and the reference current (I_{REF}) to the INUM pin, the slope of V_{LOG} is negative and the range is inverted, that is, V_{LOG} is 2.5 V for I_{DEN} = 1 pA, and V_{LOG} is 0.5 V for I_{DEN} = 10 mA.

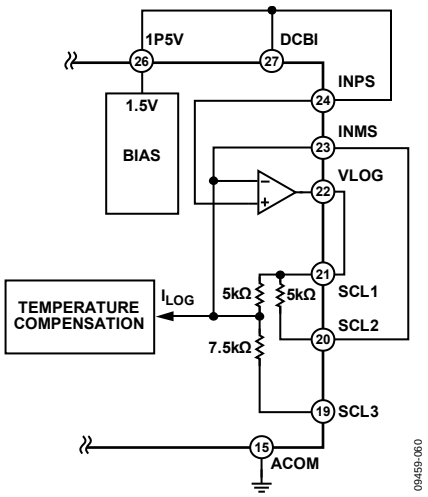


Figure 51. Buffer Amplifier in Default Configuration

The buffer amplifier is a voltage feedback op amp with supplies between VPOS and VNEG. For single-supply operation, the VNEG pin is tied to ground, and the INPS pin, the positive input of the op amp, to the 1P5V pin.

If a ground referenced input is desired at the INUM or IDEN pins, then the INPS and DCBI pins together with the VSMx pins must be tied to ground, and VNEG needs to be less than −2 V. If larger slopes are required, VPOS can increase to +5 V, and VNEG can increase to −5 V. For example, if the SCL3 pin is connected to VLOG, and SCL1 and SCL2 remain open, the internal 7.5 kΩ resistor, together with the 80 µA/decade I_{LOG}, provides a slope of 0.6 V/decade at the VLOG pin. Implementation of slopes of 0.2 V/decade to 0.8 V/decade is easily accomplished.

Setting the Log Slope and Intercept

The choice of optimal slope and intercept depends on the application and supply voltage(s). For example, when an input current range of less than the full 200 dB is desired, a higher slope can be chosen to better use the full voltage span available at VLOG, and perhaps optimally position it to suit the input capacity of a subsequent analog-to-digital converter (ADC). Very high slopes, such as 0.8 V/decade, can be realized, allowing a smaller range of I_{PD} to be measured at high sensitivity.

Any other intercept and slope can be realized using external resistors, but these do not, in general, form accurate ratios to the on-chip resistors. Therefore, some inaccuracies should be expected. If the SCL1, SCL2, and SCL3 pins are not connected and a resistor is placed between the INMS and VLOG pins, the I_{LOG} current is forced through the external resistor and thereby has a log slope that is 80 µA/decade times R_{EXT}; V_{OFS} is equal to the voltage applied to the INPS pin.

Table 4. VLOG Scaling Options

Option	Pin SCL1	Pin SCL2	Pin SCL3	Pin INPS	Pin INMS	V_Y (V/dec)	I_Z (A)	V_{OFS} (V)
Single-Supply Operation (VNEG = 0 V; VSMx = DCBI = INPS = 1P5V)								
1[1]	VLOG	INMS	Open	1P5V	SCL2	0.2	3.16 f	1.5
2	VLOG	INMS	VLOG	1P5V	SCL2	0.15	0.01 f	1.5
3	VLOG	INMS	Ground	1P5V	SCL2	0.2	0.01 f	2.0
4	VLOG	Open	Ground	1P5V	Open	0.4	56.2 f	2.5
5	VLOG	Open	Open	1P5V	Open	0.4	17.8 p	1.5
6	Open	Open	VLOG	1P5V	Open	0.6	316 p	1.5
7	Open	VLOG	Open	1P5V	Open	0.8	1.33 n	1.5
8	VLOG	INMS	2VLT	1P5V	SCL2	0.2	21.6 f	1.333
Dual-Supply Operation (VNEG < −2 V; VSMx = DCBI = INPS = Ground)								
9[2]	VLOG	INMS	Open	Ground	SCL2	0.2	100 n	0
10	VLOG	INMS	VLOG	Ground	SCL2	0.15	100 n	0
11	VLOG	Open	Open	Ground	Open	0.4	100 n	0
12	Open	Open	VLOG	Ground	Open	0.6	100 n	0
13	Open	VLOG	Open	Ground	Open	0.8	100 n	0

[1] Default setup for single supply and VSMx = 1.5 V.
[2] Default setup for dual supply and VSMx = ground.

The default setups are noted in Table 4.

Other intercepts are achieved by injecting different currents into the IDEN pin, for example, if I_{DEN} = 1 µA, as shown in Figure 52, the VLOG transfer function is simply shifted by one decade to the right. One way of doing this is to put a precision 500 kΩ resistor between the 2VLT and IDEN pins in the single-supply default setup. The intercept is moved up to 31.62 fA, and all output voltages for a given I_{NUM} are lowered by one decade, that is, by 0.2 V at V_{LOG}. For example, the new I_{DEN} = 1 µA, and V_{LOG} = 1.3 V for I_{NUM} = 100 nA.

This is particularly useful if the slope is already as desired but the desired intercept cannot be achieved with the on-chip resistors. Only a shift toward the right makes sense because a shift to the left requires excessively large resistors.

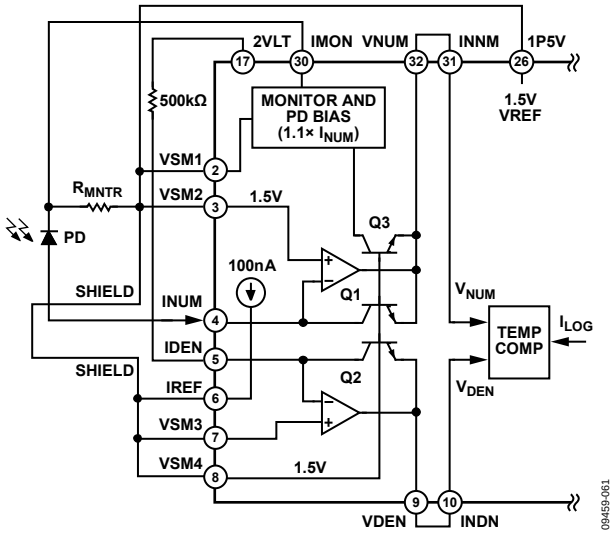


Figure 52. Intercept Shifted One Decade Right via External Resistor, Reference Current I_{DEN} = 1 µA

Slope Inversion

Table 4 lists only those slopes that are positive because this is the expected normal operation in measurement mode. The slopes can be inverted by two methods. By using $I_{NUM} = I_{REF}$ = 100 nA, in which case, the intercepts, I_Z, are at larger currents mirrored from the values shown in Table 4 around the 100 nA reference current. For example, for the default setup with V_Y = 0.2 V/decade and I_Z = 3.162 fA, swapping INUM and IDEN connections result in V_Y = −0.2 V/decade and I_Z = 3.162 A.

The second method is to simply swap the connections between the VNUM and VDEN pins and the inputs to the temperature compensation cell (INNM and INDN), as shown in Figure 53 (compare to Figure 52). This technique is particularly useful if both negative log slope and adaptive photodiode biasing via I_{MON} are desired together.

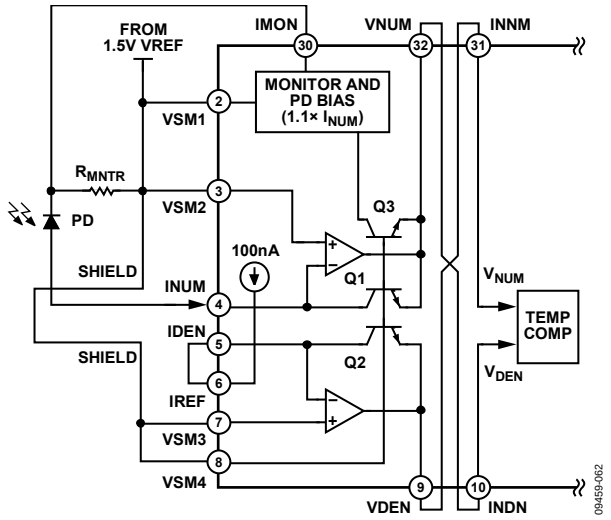


Figure 53. Simple Slope Inversion Method

Log Ratio Operation

Because the ADL5304 has two equal inputs, I_{NUM} and I_{DEN}, log ratio operation is possible. The only difference between I_{NUM} and I_{DEN} is that the I_{MON} current derives from the I_{NUM} signal and allows adaptive photodiode bias at this input only. Assuming that the ratio I_{NUM}/I_{DEN} can, in general, be either greater or less than unity, V_{LOG} can be of either polarity, requiring a negative supply in some cases. The value of V_{LOG} depends on the minimum ratio and the slope chosen for the application.

For example, if the ratio can vary from 1:1000 to 1000:1 and a slope of 20 mV/dB is required, the peak swing is ±1.2 V around V_{OFS}.

Option 5 in Table 4 provides this with an intercept I_Z of 17.8 pA (V_{OFS} = 1.5 V) with V_{LOG} = ±1.2 V around V_{OFS} = 1.5 V, which results in 0.3 V ≤ V_{LOG} ≤ 2.7 V.

APPLICATIONS INFORMATION

USING THE ADL5304

The basic connections for single-supply operation are shown in Figure 55. Supply decoupling is not critical and the suggested values are conservative; however, it is recommended that a ferrite bead be placed in the supply lines together with a 0.1 µF decoupling capacitor. Ferrite beads are preferable to resistors because they do not produce a dc voltage drop that can affect reference levels. In Figure 55, the slope is 10 mV/dB or 0.2 V/decade, and the intercept is 3.162 fA. For the full dynamic range of 200 dB (100 dB optical), V_{LOG} varies from 0.5 V to 2.5 V (see small diagram at the output in Figure 55) with $V_{LOG} = V_{OFS} = 1.5$ V, when $I_{NUM} = I_{DEN}$. Because the IDEN pin is connected to the IREF pin, $I_{DEN} = 100$ nA. Figure 55 also shows the setup for the adaptive photodiode bias. If this is not desired, ground the IMON pin, remove R_{MNTR}, and provide the desired bias voltage greater than 1.5 V to the cathode of the PD. As noted in the Photodiode Bias section, the on-chip 2 V reference can be used for this purpose and provides an exact 0.5 V reverse bias together with the 1.5 V that is forced by the FET amp to the anode via the INUM pin.

Using the Adaptive Bias

The positive bias on the photodiode cathode must be adequate to support the peak current, which is limited by its internal series resistance, R_S. Typical values of R_S are 5 Ω. A model of a representative photodiode (JDSU EPM 605) is shown in Figure 54.

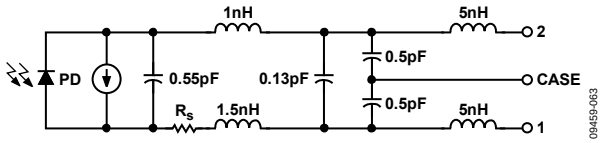


Figure 54. Photodiode Model

It is desirable to use a small bias at very low levels of illumination to minimize the error due to current leakage across the diode terminals. The adaptive bias achieves this automatically even for larger currents through the addition of the external resistor, R_{MNTR}, that is 10 times R_S. In case of uncertainty in R_S, an R_{MNTR} that is slightly greater than 10 times R_S is recommended. In the limit, when R_{MNTR} is not present at all, the voltage at the IMON pin increases until the current source saturates and absorbs the excess 10% of current that the IMON output generates. However, this defeats the purpose of the adaptive bias; therefore, users must ensure that R_{MNTR} is present when using the adaptive bias.

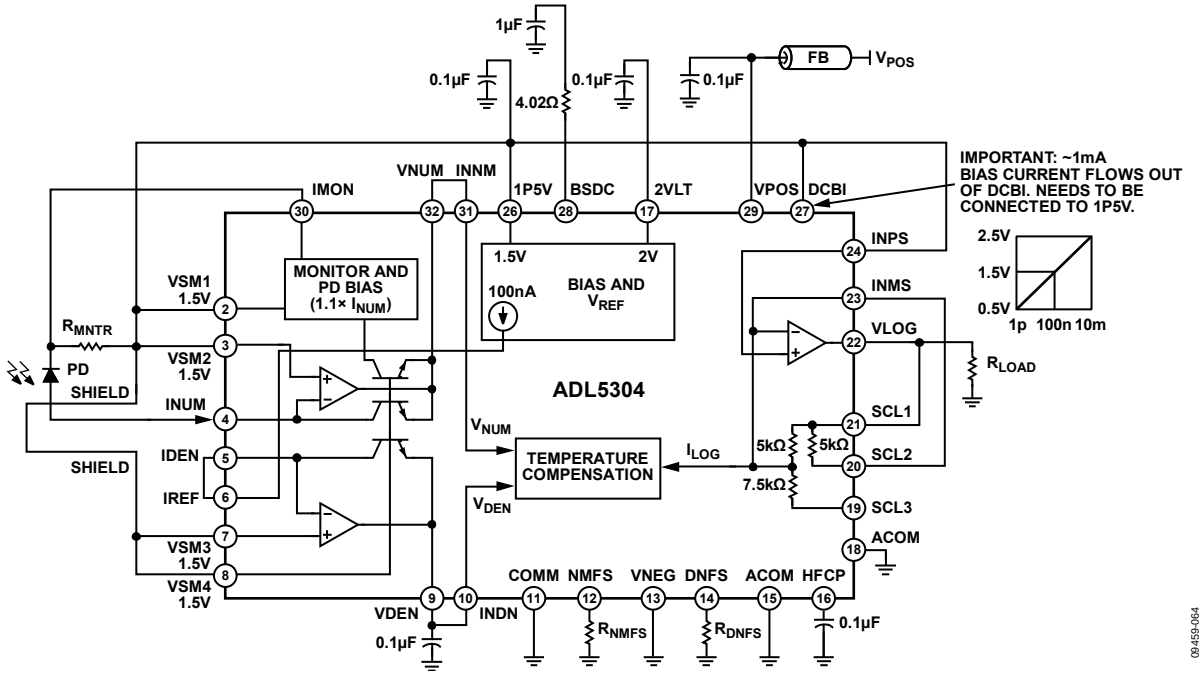


Figure 55. Basic Connections for Single-Supply Operation

Summing Node Voltage

It is important to reiterate that the VSM1 to VSM4, DCBI, and INPS pins always need to be tied together. Failure to do so results in erroneous outputs at VLOG.

The VSMx pins must be well decoupled to provide a good ac ground.

Leakage

VSM2 and VSM3 are critical nodes because they are used by the FET amplifiers to define the voltages on the INUM and IDEN pins. Furthermore, the voltage applied to VSM2 and VSM3 is also used to drive the shield around the inputs, which becomes critical at low currents (<1 nA) to minimize leakage. A voltage difference between the INUM and VSM2 pins of 1 mV together with a leakage resistor of 100 MΩ results in a current of 10 pA. If the current flows into the device, this leakage current limits the lowest measurable input current.

Even worse, if the current is negative (that is, pulls current out of the input pin), the input voltage pulls low, and the FET amp output rails positive. This can happen rather easily when the input is biased at 1.5 V. For example, a 1 GΩ resistor between the input pin and ground generates a 1.5 nA current that flows from the input pin to ground and thereby pulls the input nodes low. A log amp input is unidirectional, and it can accept current in only one direction. A current that flows in the wrong direction breaks the loop that biases the inputs. For this reason, if currents of less than about 1 nA are to be measured, it is critical that a guard be used, and that the boards are cleaned of any contaminants including solder flux. In the case where the leakage is so large that it cannot be overcome by the input current, the V_{LOG} output rails to the negative or positive ends of the output range, depending on whether it is INUM or IDEN that has the leakage.

VLOG Output

The VLOG output is somewhat sensitive to loading and does not like to drive large capacitances or very small resistors, for this reason, it is recommended to keep C_{LOAD} < 5 pF and R_{LOAD} > 10 kΩ.

Dynamic Response

The ADL5304 does not require input compensation networks to stabilize the circuit. However, a negative going current can happen during normal dynamic operation, for example, during current steps that decreases from larger to smaller values. During a large step, the input loop can temporarily open causing a transient invalid V_{LOG} output. Loop recovery time is directly related to the input current; therefore, the smaller the input current, the longer it takes for the ADL5304 to recover. Careful design that reduces parasitic capacitance at the INUM and IDEN inputs helps to reduce this recovery time; however, this behavior cannot be eliminated because it is characteristic of translinear log amps.

Some pulse response measurement results with an actual photodiode (1A227, 0.8 A/W, 0.7 pF) are shown in Figure 56 and Figure 57 for the setup in Figure 55.

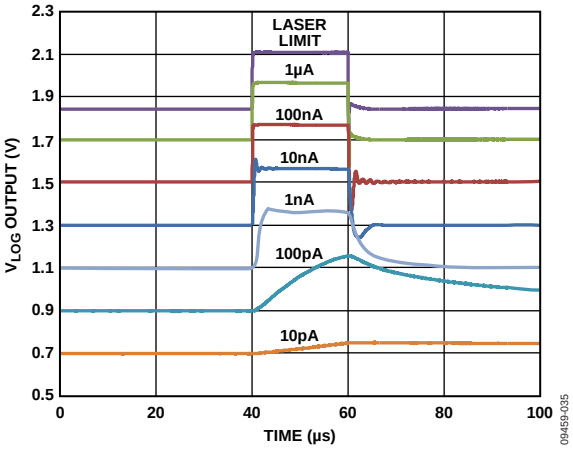


Figure 56. Photodiode Response for Input Currents of Approximately 10 pA to >1 µA Where Laser Limit Encountered

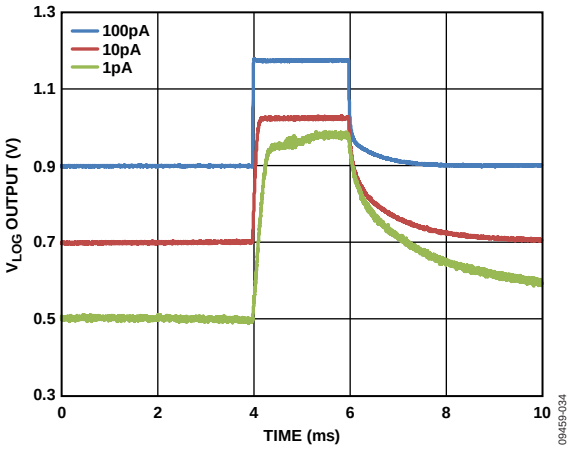


Figure 57. Increased Time Scale to Show Measurements Down to I_{NUM} Approximately 1 pA (Approximately 1.25 pW; −89.03 dBm)

USING A NEGATIVE SUPPLY

In most applications of the ADL5304, a single supply is adequate. A single supply also provides the lowest power operation. Dual supplies are needed if the user wants to bias the anode of the photodiode at ground, as was shown in Figure 50.

The negative supply needs to absorb the device bias current, the load current of the buffer, and the maximum input currents.

With the summing node moved to ground, the ADL5304 can be used as a voltage-input log amp, using a suitably scaled resistor from the voltage source to the INUM pin. The logarithmic accuracy for small voltages is limited by the offset of the JFET op amp, appearing between this pin and VSUM. The IDEN pin can likewise be driven from a voltage signal.

When very large input currents (INUM or IDEN greater than approximately 5 mA) and very low temperatures (−40°C) are expected, use a negative voltage on VNEG.

EVALUATION BOARD SCHEMATIC AND SILKSCREENS

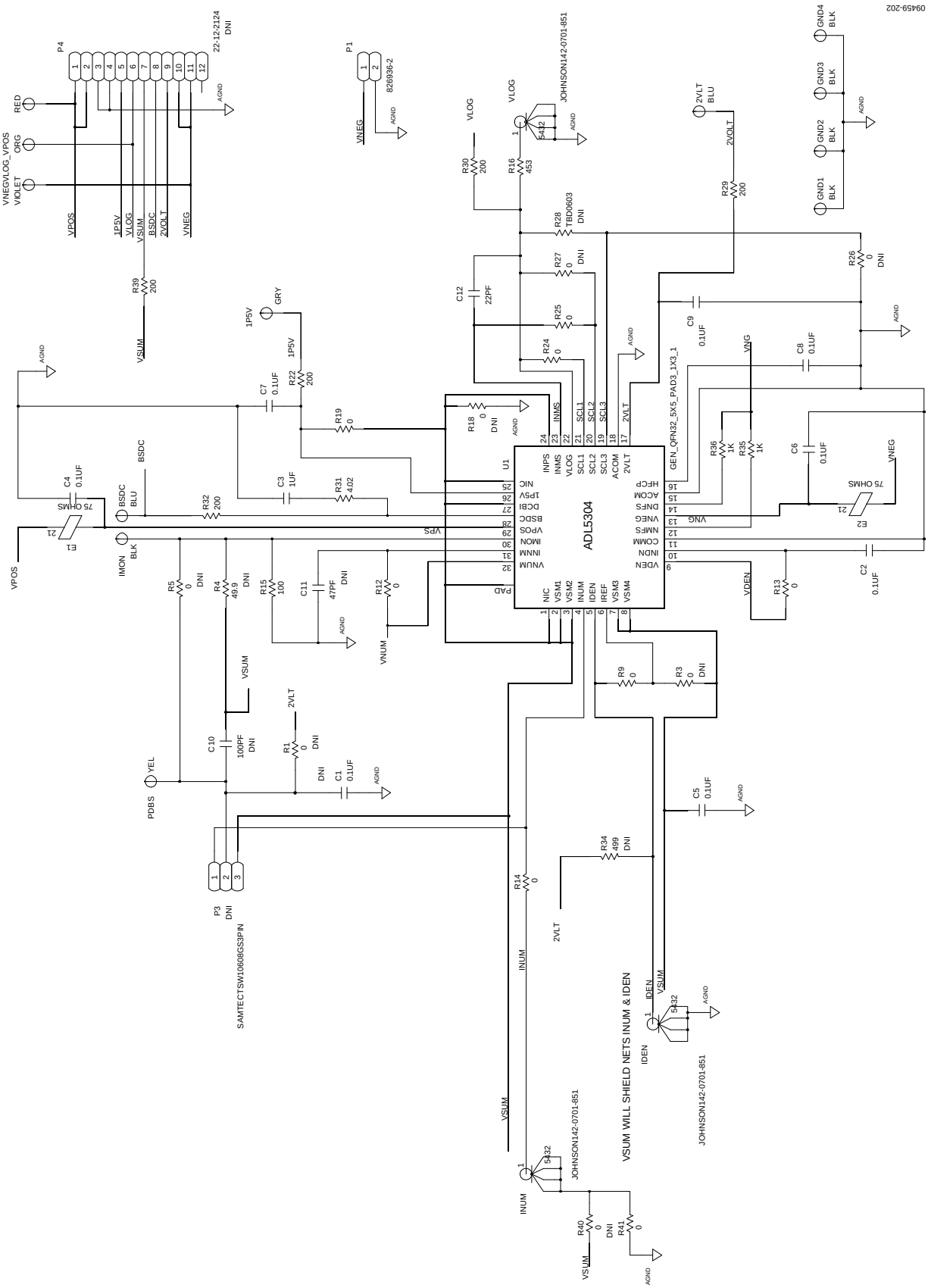


Figure 58. Evaluation Board Schematic

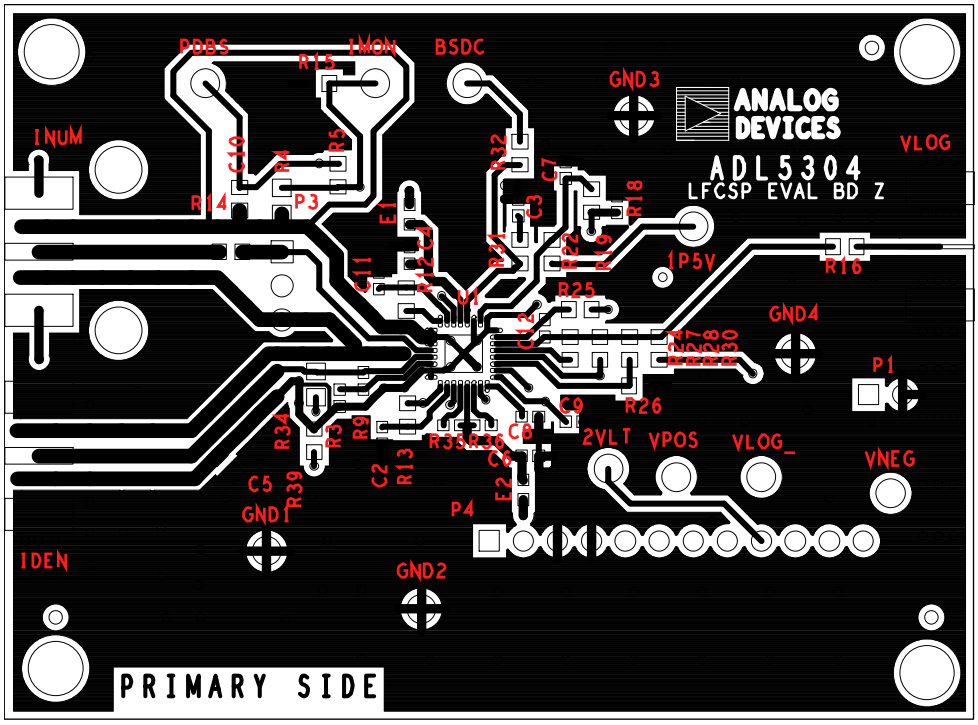


Figure 59. Evaluation Board, Primary Side

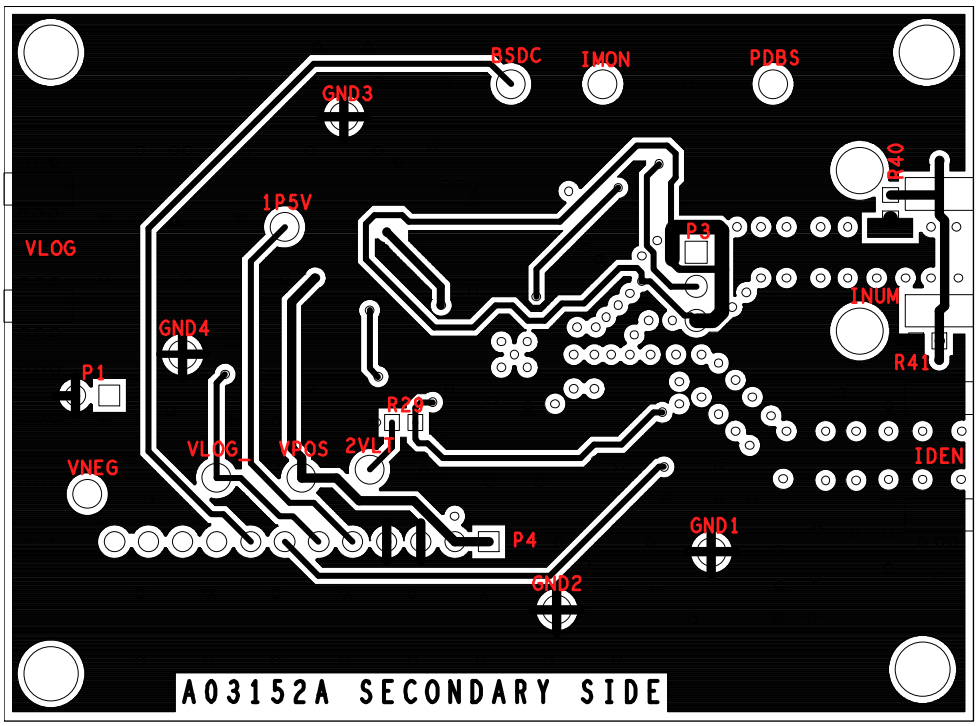


Figure 60. Evaluation Board, Secondary Side

OUTLINE DIMENSIONS

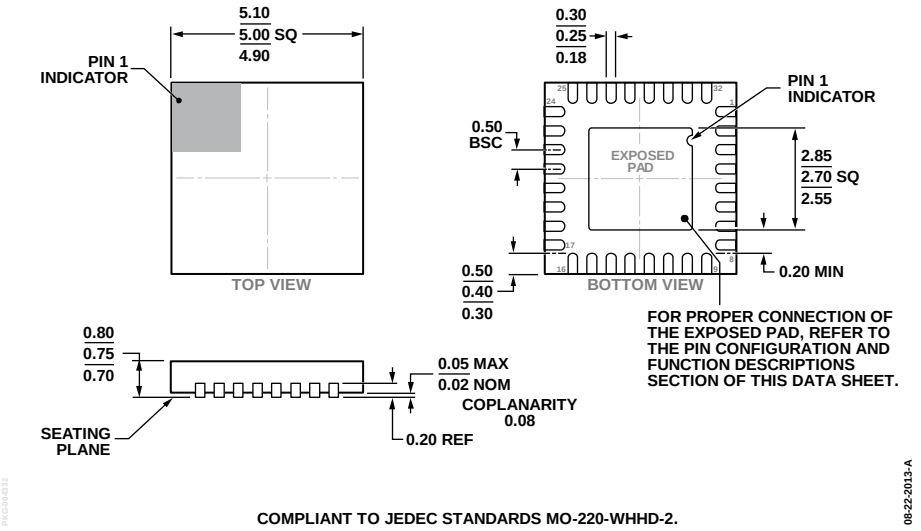


Figure 61. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-21)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Ordering Quantity	Package Option
ADL5304ACPZ-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	250	CP-32-21
ADL5304ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP], 7″ Tape and Reel	1500	CP-32-21
ADL5304ACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP], 13″ Tape and Reel	5000	CP-32-21
ADL5304-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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