

TPS1100, TPS1100Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

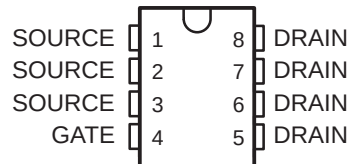
- Low $r_{DS(on)}$. . . 0.18 Ω Typ at $V_{GS} = -10$ V
- 3 V Compatible
- Requires No External V_{CC}
- TTL and CMOS Compatible Inputs
- $V_{GS(th)} = -1.5$ V Max
- Available in Ultrathin TSSOP Package (PW)
- ESD Protection Up to 2 kV Per MIL-STD-883C, Method 3015

description

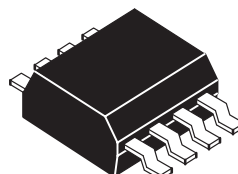
The TPS1100 is a single P-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of -1.5 V and an I_{DSS} of only 0.5 μ A, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version with its smaller footprint and reduction in height fits in places where other P-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for a small-outline integrated circuit (SOIC) package.

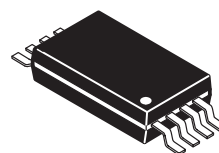
D OR PW PACKAGE
(TOP VIEW)



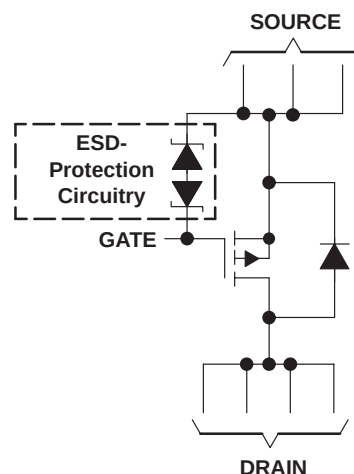
D PACKAGE



PW PACKAGE



schematic



NOTE A: For all applications, all source pins should be connected and all drain pins should be connected.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
-40°C to 85°C	TPS1100D	TPS1100PWLE	TPS1100Y

The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE). The chip form is tested at 25°C .



Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

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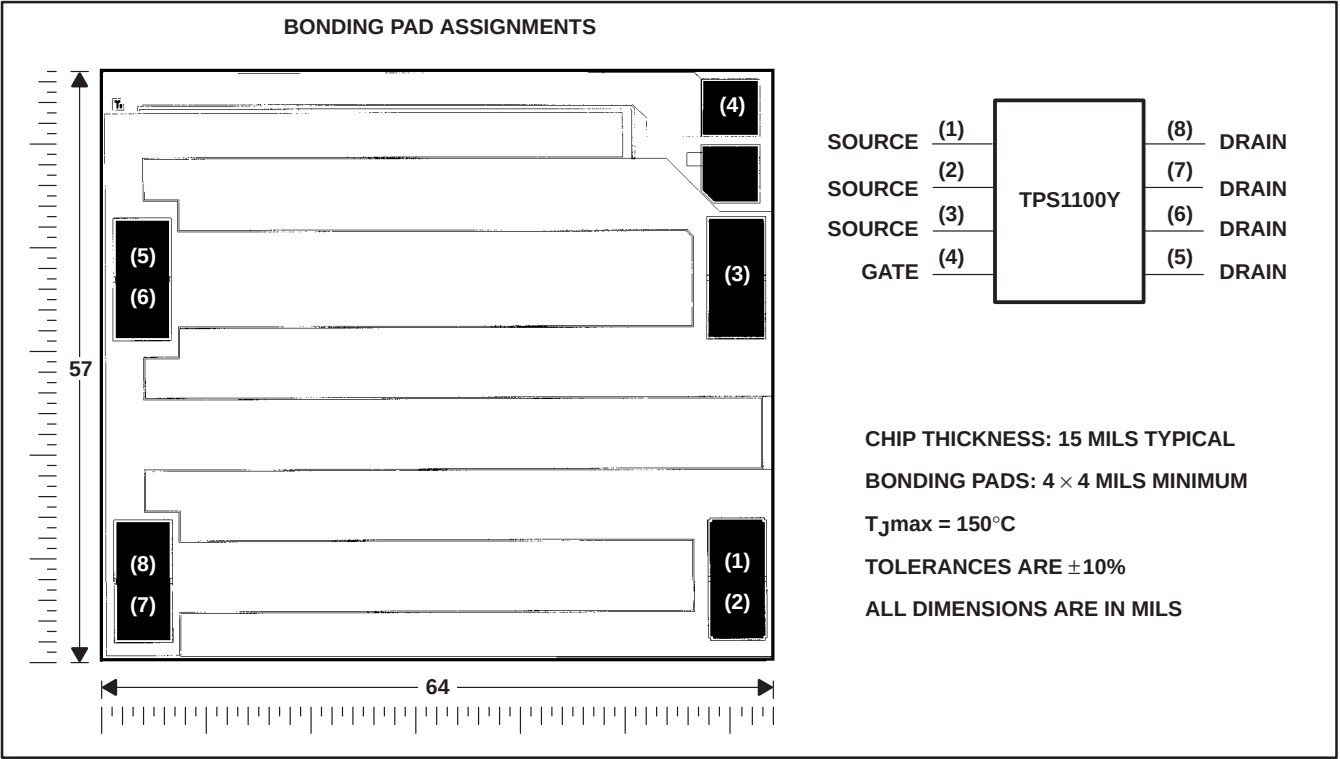
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description (continued)

Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

TPS1100Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1100. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



TPS1100, TPS1100Y

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

					UNIT
Drain-to-source voltage, V_{DS}				–15	V
Gate-to-source voltage, V_{GS}				2 or –15	V
Continuous drain current ($T_J = 150^{\circ}\text{C}$), $I_D^{\ddagger}$	$V_{GS} = -2.7\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 0.41	A
			$T_A = 125^{\circ}\text{C}$	± 0.28	
		PW package	$T_A = 25^{\circ}\text{C}$	± 0.4	
			$T_A = 125^{\circ}\text{C}$	± 0.23	
	$V_{GS} = -3\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 0.6	
			$T_A = 125^{\circ}\text{C}$	± 0.33	
		PW package	$T_A = 25^{\circ}\text{C}$	± 0.53	
			$T_A = 125^{\circ}\text{C}$	± 0.27	
	$V_{GS} = -4.5\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 1	
			$T_A = 125^{\circ}\text{C}$	± 0.47	
		PW package	$T_A = 25^{\circ}\text{C}$	± 0.81	
			$T_A = 125^{\circ}\text{C}$	± 0.37	
	$V_{GS} = -10\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 1.6	
			$T_A = 125^{\circ}\text{C}$	± 0.72	
		PW package	$T_A = 25^{\circ}\text{C}$	± 1.27	
			$T_A = 125^{\circ}\text{C}$	± 0.58	
Pulsed drain current, $I_D^{\ddagger}$			$T_A = 25^{\circ}\text{C}$	± 7	A
Continuous source current (diode conduction), I_S			$T_A = 25^{\circ}\text{C}$	–1	A
Storage temperature range, T_{Stg}				–55 to 150	$^{\circ}\text{C}$
Operating junction temperature range, T_J				–40 to 150	$^{\circ}\text{C}$
Operating free-air temperature range, T_A				–40 to 125	$^{\circ}\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	$^{\circ}\text{C}$

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 158^\circ\text{C/W}$ for the D package and $R_{\theta JA} = 248^\circ\text{C/W}$ for the PW package. These devices are mounted on a FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	791 mW	6.33 mW/ $^\circ\text{C}$	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/ $^\circ\text{C}$	323 mW	262 mW	101 mW

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 158^\circ\text{C/W}$ for the D package and $R_{\theta JA} = 248^\circ\text{C/W}$ for the PW package. These devices are mounted on an FR4 board with no special thermal considerations when tested.

TPS1100, TPS1100Y

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electrical characteristics at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS		TPS1100			TPS1100Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = −250 μA		−1	−1.25	−1.50	−1.25			V
V _{SD}	Source-to-drain voltage (diode-forward voltage) [†]	I _S = −1 A, V _{GS} = 0 V		−0.9			−0.9			V
I _{GSS}	Reverse gate current, drain short circuited to source	V _{DS} = 0 V, V _{GS} = −12 V		±100						nA
I _{DSS}	Zero-gate-voltage drain current	V _{DS} = −12 V, V _{GS} = 0 V	T _J = 25°C	−0.5						μA
			T _J = 125°C	−10						
r _{DS(on)}	Static drain-to-source on-state resistance [†]	V _{GS} = −10 V	I _D = −1.5 A	180		180		mΩ		
		V _{GS} = −4.5 V	I _D = −0.5 A	291	400	291				
		V _{GS} = −3 V	I _D = −0.2 A	476	700	476				
		V _{GS} = −2.7 V		606	850	606				
g _{fs}	Forward transconductance [†]	V _{DS} = −10 V, I _D = −2 A		2.5		2.5		S		

[†] Pulse test: pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

dynamic

PARAMETER		TEST CONDITIONS			TPS1100, TPS1100Y			UNIT
					MIN	TYP	MAX	
Qg	Total gate charge	VDS = −10 V, VGS = −10 V, ID = −1 A	5.45			nC		
Qgs	Gate-to-source charge		0.87					
Qgd	Gate-to-drain charge		1.4					
td(on)	Turn-on delay time	VDD = −10 V, RL = 10 Ω, ID = −1 A, RG = 6 Ω, See Figures 1 and 2	4.5			ns		
td(off)	Turn-off delay time		13			ns		
tr	Rise time		10			ns		
tf	Fall time		2					
trr(SD)	Source-to-drain reverse recovery time		16					

PARAMETER MEASUREMENT INFORMATION

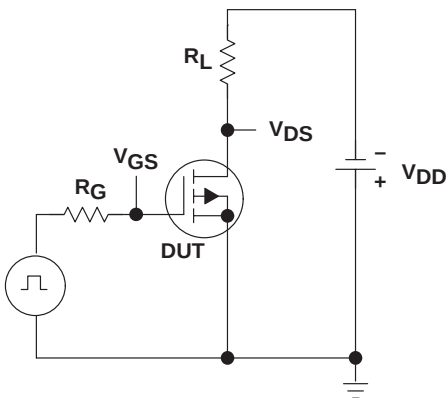


Figure 1. Switching-Time Test Circuit

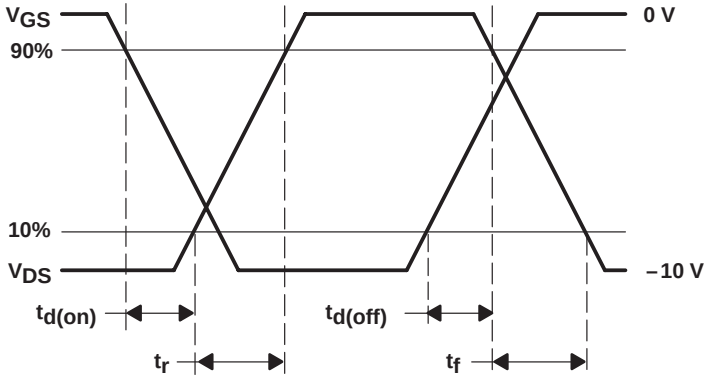


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

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TYPICAL CHARACTERISTICS

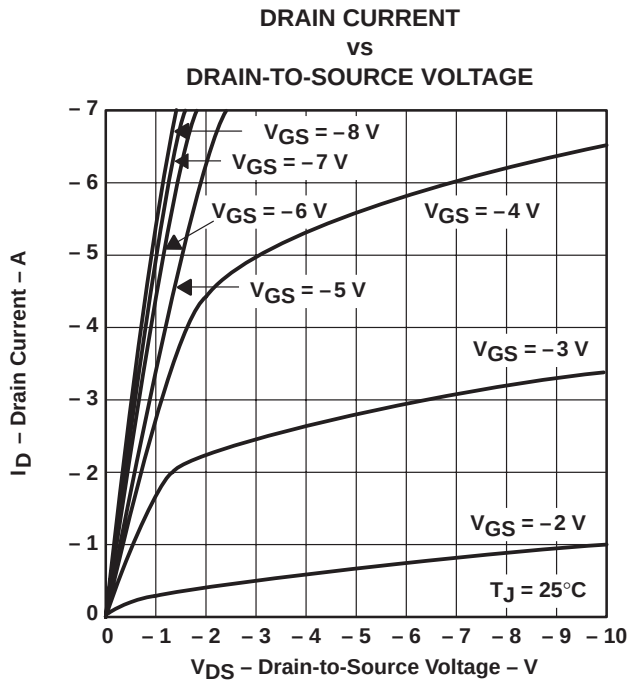


Figure 3

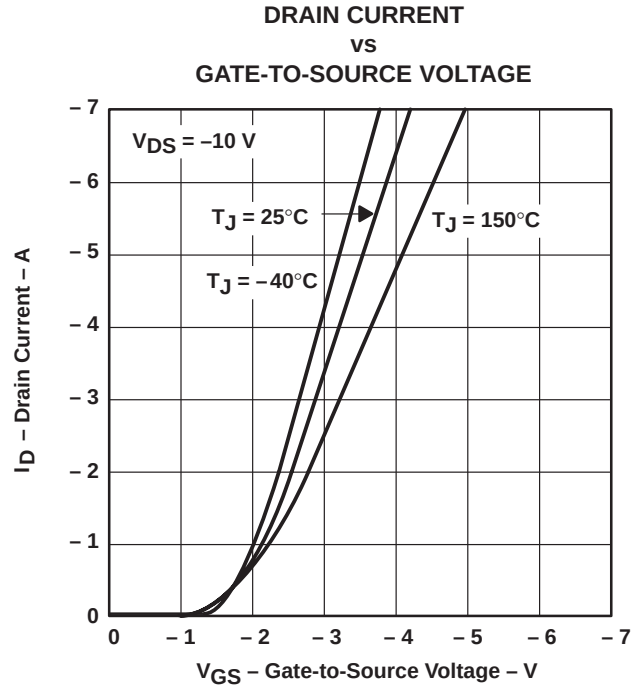


Figure 4

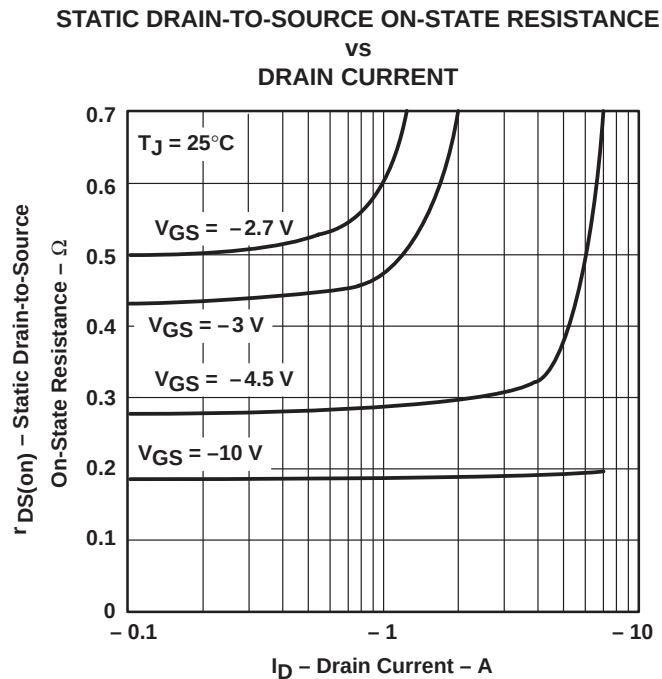


Figure 5

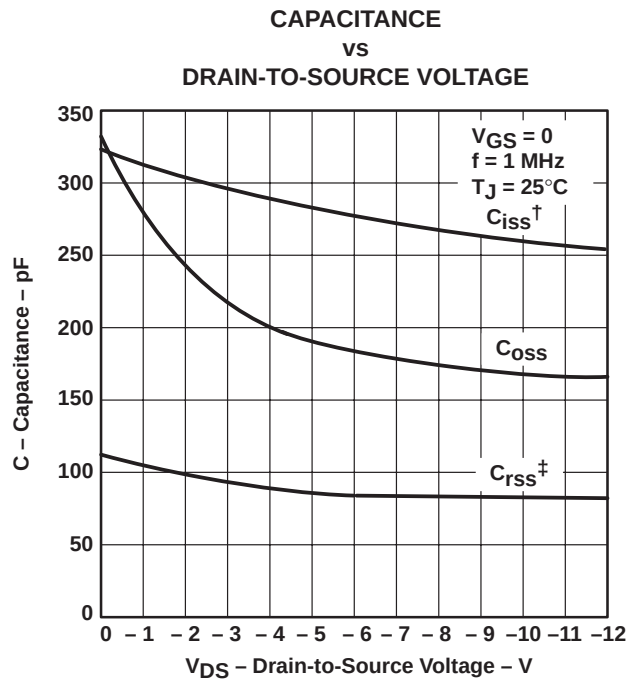


Figure 6

$$\dagger C_{iss} = C_{gs} + C_{gd} \text{ (} C_{ds} \text{ shorted)}$$

$$\ddagger C_{rss} = C_{gd}, C_{oss} = C_{ds} + \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$$

TYPICAL CHARACTERISTICS

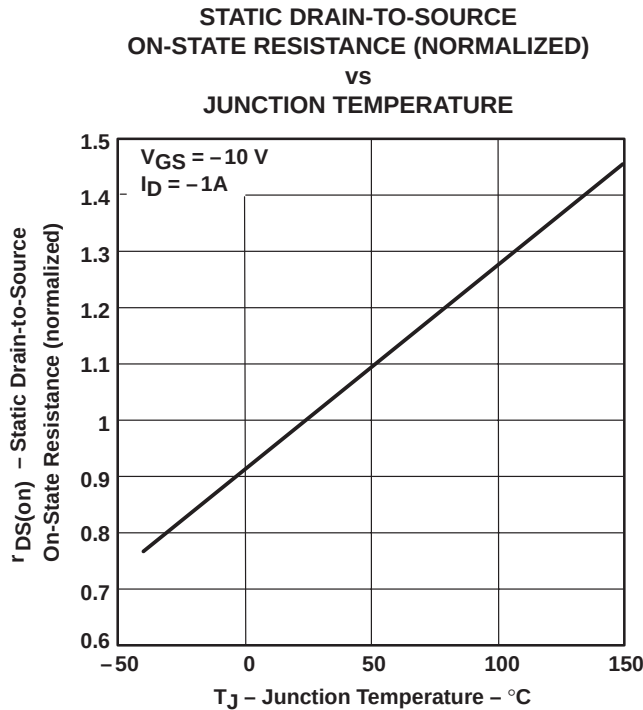


Figure 7

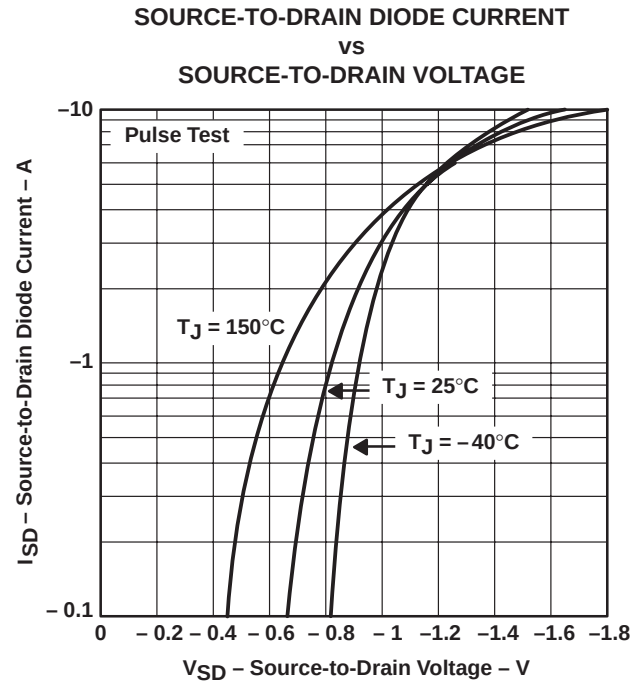


Figure 8

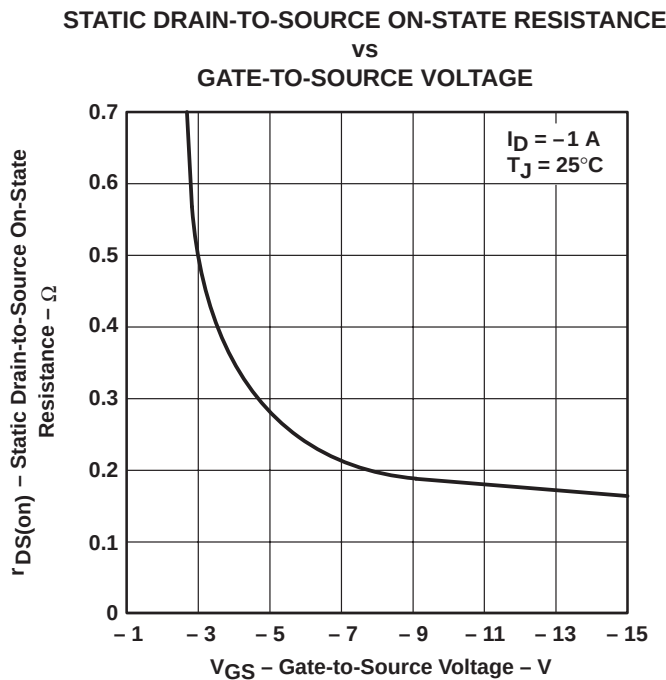


Figure 9

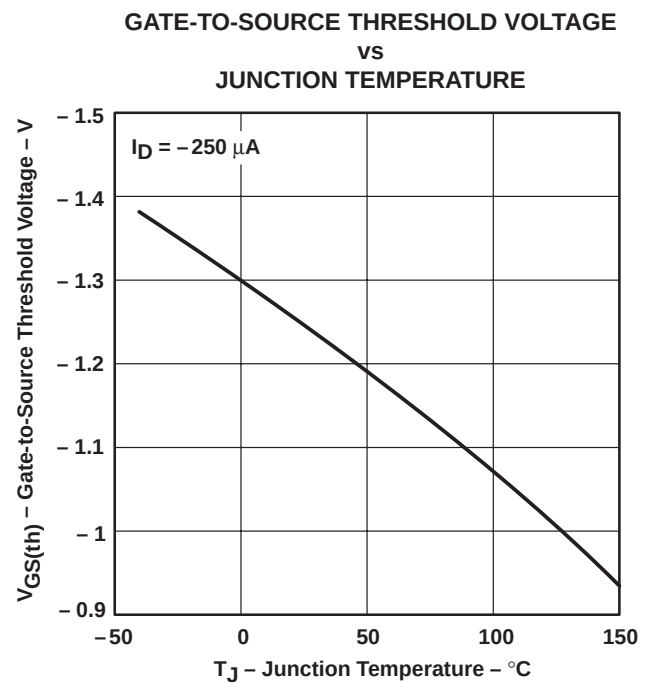


Figure 10

TPS1100, TPS1100Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

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TYPICAL CHARACTERISTICS

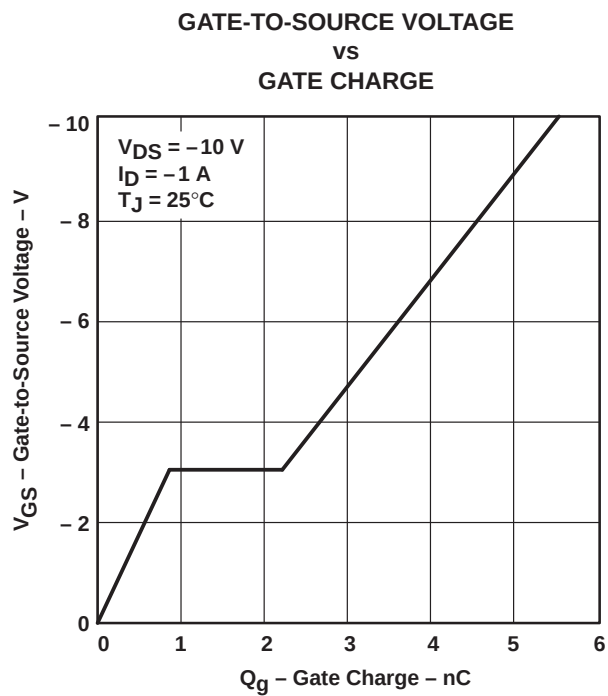
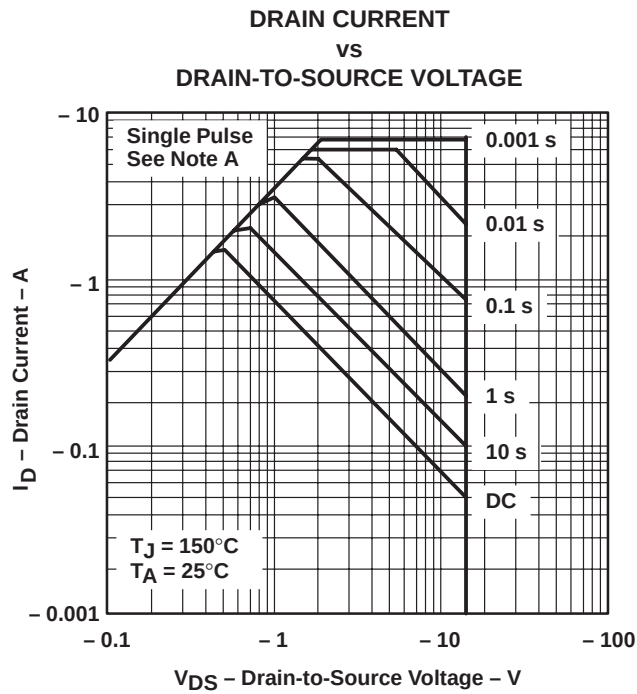
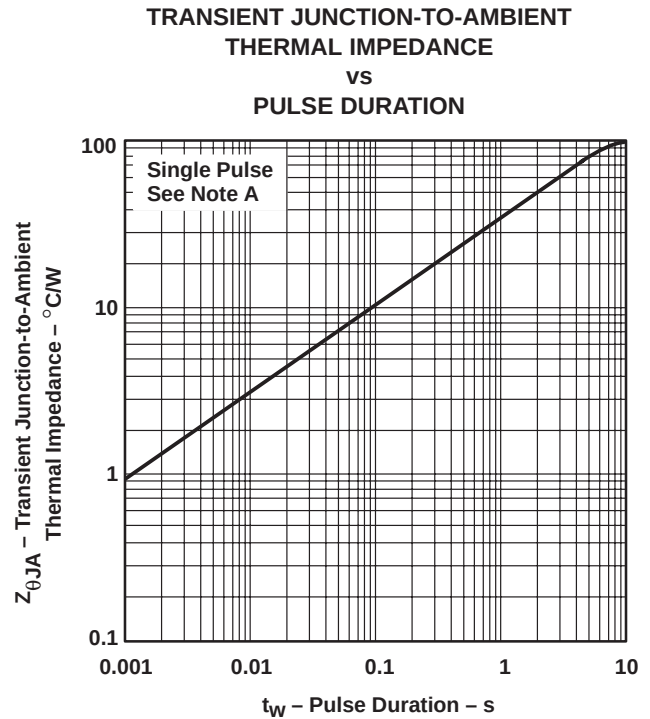


Figure 11

THERMAL INFORMATION



NOTE A: Values are for the D package and are FR4-board mounted only.

APPLICATION INFORMATION

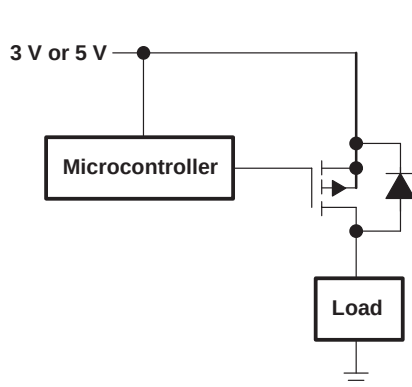


Figure 14. Notebook Load Management

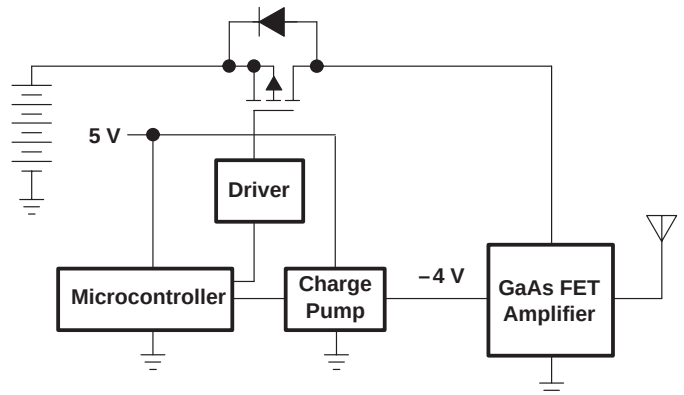


Figure 15. Cellular Phone Output Drive

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS1100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		PS1100	Samples
TPS1100PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		PS1100	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

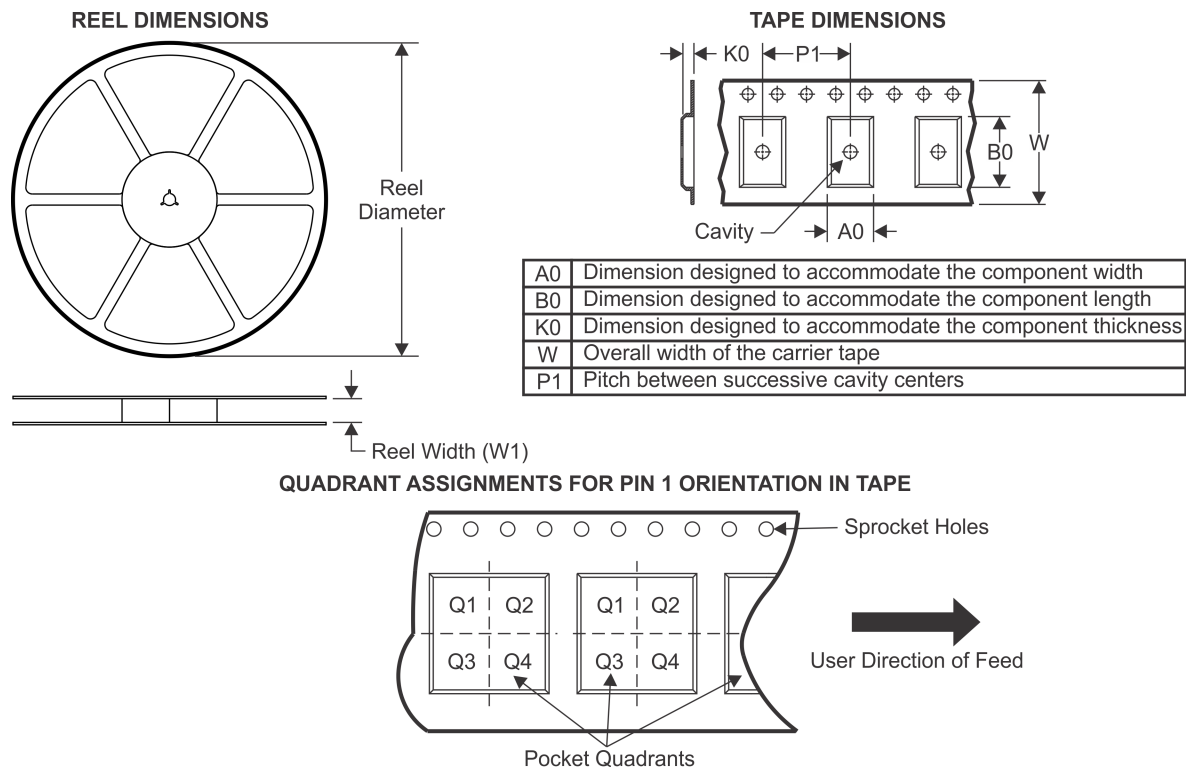
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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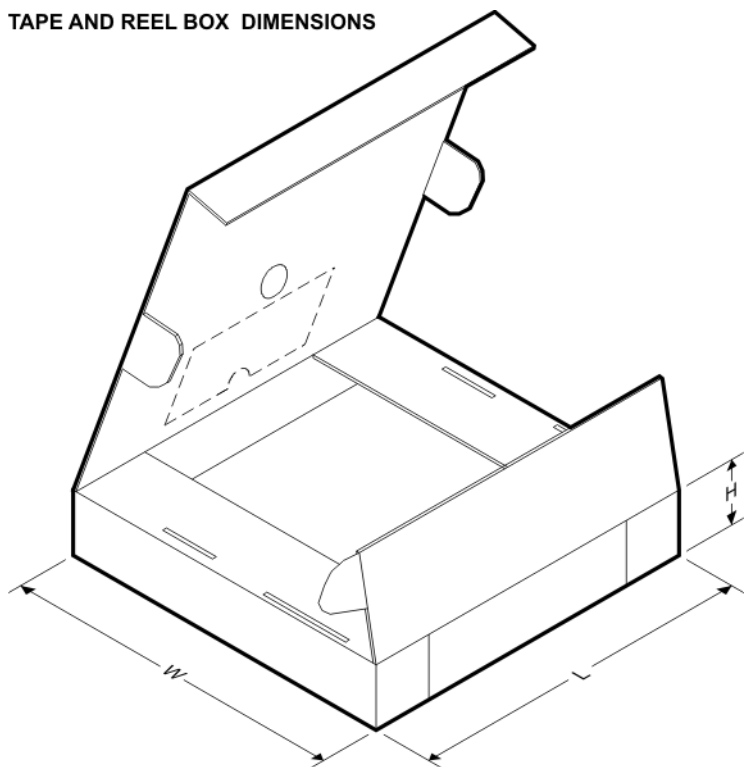
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS1100PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1100DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS1100PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

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