Low Phase Noise, Fast Settling, 6 GHz PLL Frequency Synthesizer

Data Sheet

ADF4196

FEATURES

- Fast settling, fractional-N PLL architecture
- Single PLL replaces ping-pong synthesizers
- Frequency hop across GSM band in 5 µs with phase settled within 20 µs
- 1 degree rms phase error at 4 GHz RF output
- Digitally programmable output phase
- RF input range up to 6 GHz
- 3-wire serial interface
- On-chip, low noise differential amplifier
- Phase noise figure of merit: −216 dBc/Hz

APPLICATIONS

- GSM/EDGE base stations
- PHS base stations
- Pulse Doppler radar
- Instrumentation and test equipment
- Beam-forming/phased array systems

GENERAL DESCRIPTION

The ADF4196 frequency synthesizer can be used to implement local oscillators (LO) in the upconversion and downconversion sections of wireless receivers and transmitters. Its architecture is specifically designed to meet the GSM/EDGE lock time requirements for base stations, and the fast settling feature makes the ADF4196 suitable for pulse Doppler radar applications.

The ADF4196 consists of a low noise, digital phase frequency detector (PFD) and a precision differential charge pump. A differential amplifier converts the differential charge pump output to a single-ended voltage for the external voltage controlled oscillator (VCO). The sigma-delta (Σ-Δ) based fractional interpolator, working with the N divider, allows programmable modulus fractional-N division. Additionally, the 4-bit reference (R) counter and on-chip frequency doubler allow selectable reference signal (REF_{IN}) frequencies at the PFD input.

A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a VCO. The switching architecture ensures that the PLL settles within the GSM time slot guard period, removing the need for a second PLL and associated isolation switches. This decreases the cost, complexity, PCB area, shielding, and characterization found on previous ping-pong GSM PLL architectures.

FUNCTIONAL BLOCK DIAGRAM

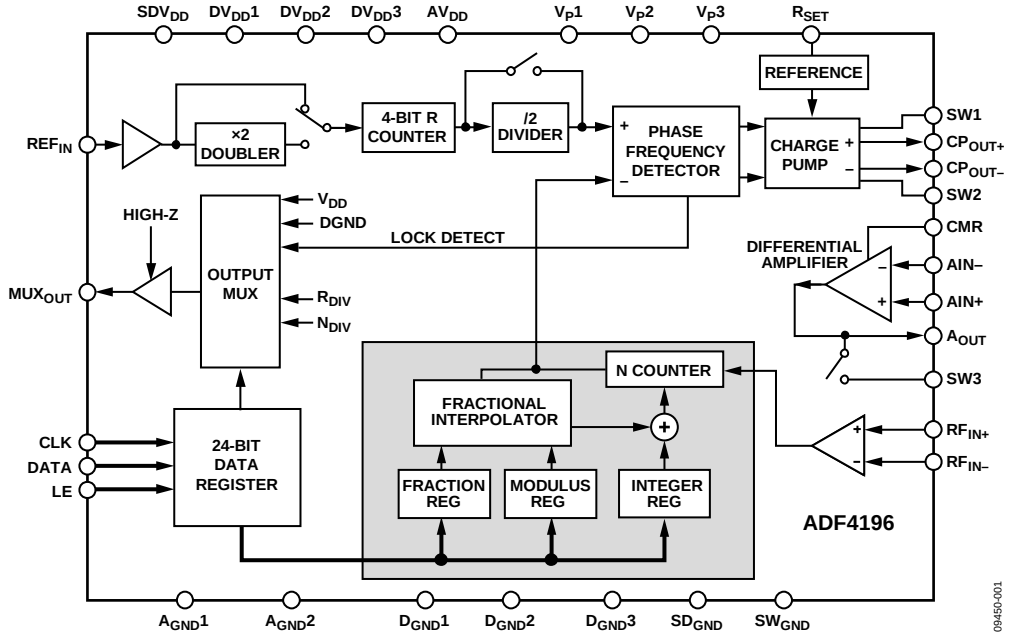


Figure 1.

Rev. D

Document Feedback

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REVISION HISTORY

5/15—Rev. C to Rev. D

Changed LFCSP_VQ to LFCSP_WQ ... Throughout
Changes to Figure 3 ... 6
Changed ADuC70xx Interface Section to Analog Microcontroller Interface Section ... 27
Changes to Analog Microcontroller Interface Section and Figure 38 ... 27
Updated Outline Dimensions ... 28
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1/13—Rev. B to Rev. C

Change to Power-Up Initialization Section ... 23
Changes to Ordering Guide ... 28

12/11—Rev. A to Rev. B

Changes to Figure 10, Figure 11, Figure 13, and Figure 14 ... 9
Change to Figure 31 ... 17

10/11—Revision A: Initial Version

SPECIFICATIONS

AV_{DD} = $DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$ = SDV_{DD} = 3 V ± 10%; V_P1, V_P2 = 5 V ± 10%; V_P3 = 5.35 V ± 5%; $A_{GND}1$, $A_{GND}2$ = $D_{GND}1$, $D_{GND}2$, $D_{GND}3$ = 0 V; R_{SET} = 2.4 kΩ; dBm referred to 50 Ω; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range = −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
RF Input Frequency ($RF_{IN±}$)	0.4		6	GHz	See Figure 21 for input circuit
RF Input Sensitivity	−10		0	dBm	
Maximum Allowable Prescaler Output Frequency[1]			750	MHz	
REF_{IN} CHARACTERISTICS					
REF_{IN} Input Frequency			300	MHz	For f > 120 MHz, set REF/2 bit = 1 (Register R1)
REF_{IN} Edge Slew Rate	300			V/µs	
REF_{IN} Input Sensitivity	0.7		V_{DD}	V p-p	AC-coupled
			0 to V_{DD}	V	CMOS compatible
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency			26	MHz	
CHARGE PUMP					
I_{CP} Up/Down					
High Value		6.6		mA	R_{SET} = 2.4 kΩ
Low Value		104		µA	R_{SET} = 2.4 kΩ
Absolute Accuracy		5		%	
R_{SET} Range	1		4	kΩ	Nominally R_{SET} = 2.4 kΩ
I_{CP} Three-State Leakage		1		nA	
I_{CP} Up vs. Down Matching		0.1		%	0.75 V ≤ V_{CP} ≤ V_P1, V_P2, V_P3 − 1.5 V
I_{CP} vs. V_{CP}		1		%	0.75 V ≤ V_{CP} ≤ V_P1, V_P2, V_P3 − 1.5 V
I_{CP} vs. Temperature		1		%	0.75 V ≤ V_{CP} ≤ V_P1, V_P2, V_P3 − 1.5 V
DIFFERENTIAL AMPLIFIER					
Input Current		1		nA	
Output Voltage Range	1.4		V_P3 − 0.3	V	
VCO Tuning Range	1.8		V_P3 − 0.8	V	
Output Noise		7		nV/√Hz	At 20 kHz offset
LOGIC INPUTS					
Input High Voltage, V_{IH}	1.4			V	
Input Low Voltage, V_{IL}			0.7	V	
Input Current, I_{INH}, I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DD} − 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
$DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$		AV_{DD}		V	
V_P1, V_P2	4.5		5.5	V	AV_{DD} ≤ V_P1, V_P2 ≤ 5.5 V
V_P3	5.0		5.65	V	V_P1, V_P2 ≤ V_P3 ≤ 5.65 V
I_{DD} (AV_{DD} + $DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$ + SDV_{DD})		22	27	mA	
I_{DD} (V_P1 + V_P2)		22	27	mA	
I_{DD} (V_P3)		24	30	mA	
I_{DD} Power-Down		10		µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SW1, SW2, AND SW3					
On Resistance					
SW1 and SW2		65		Ω	
SW3		75		Ω	
NOISE CHARACTERISTICS					
Output					
900 MHz[2]		−108		dBc/Hz	At 5 kHz offset and 26 MHz PFD frequency
1800 MHz[3]		−102		dBc/Hz	At 5 kHz offset and 13 MHz PFD frequency
Phase Noise					
Normalized Phase Noise Floor (PN_{SYNTH})[4]		−216		dBc/Hz	At VCO output with dither off, PLL loop bandwidth = 500 kHz
Normalized 1/f Noise (PN_{1_f})[5]		−110		dBc/Hz	Measured at 10 kHz offset, normalized to 1 GHz

[1] Choose a prescaler value that ensures that the frequency on the RF input is less than the maximum allowable prescaler frequency (750 MHz).
[2] $f_{REF_{IN}}$ = 26 MHz; f_{STEP} = 200 kHz; f_{RF} = 900 MHz; loop bandwidth = 40 kHz.
[3] $f_{REF_{IN}}$ = 13 MHz; f_{STEP} = 200 kHz; f_{RF} = 1800 MHz; loop bandwidth = 60 kHz.
[4] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the N divider value) and 10 log(f_{PFD}). $PN_{SYNTH} = PN_{TOT} - 10\log(f_{PFD}) - 20\log(N)$.
[5] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at an offset frequency, f, is given by $PN = P_{1_f} + 10\log(10\text{ kHz}/f) + 20\log(f_{RF}/1\text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL™.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD}1, DV_{DD}2, DV_{DD}3 = 3\text{ V} \pm 10\%$; $V_P1, V_P2 = 5\text{ V} \pm 10\%$; $V_P3 = 5.35\text{ V} \pm 5\%$; $A_{GND}1, A_{GND}2 = D_{GND}1, D_{GND}2, D_{GND}3 = 0\text{ V}$; $R_{SET} = 2.4\text{ k}\Omega$; dBm referred to 50 Ω; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Operating temperature = −40°C to +85°C.

Table 2.

Parameter	Limit	Description
t_1	10 ns min	LE setup time
t_2	10 ns min	DATA to CLK setup time
t_3	10 ns min	DATA to CLK hold time
t_4	15 ns min	CLK high duration
t_5	15 ns min	CLK low duration
t_6	10 ns min	CLK to LE setup time
t_7	15 ns min	LE pulse width

Timing Diagram

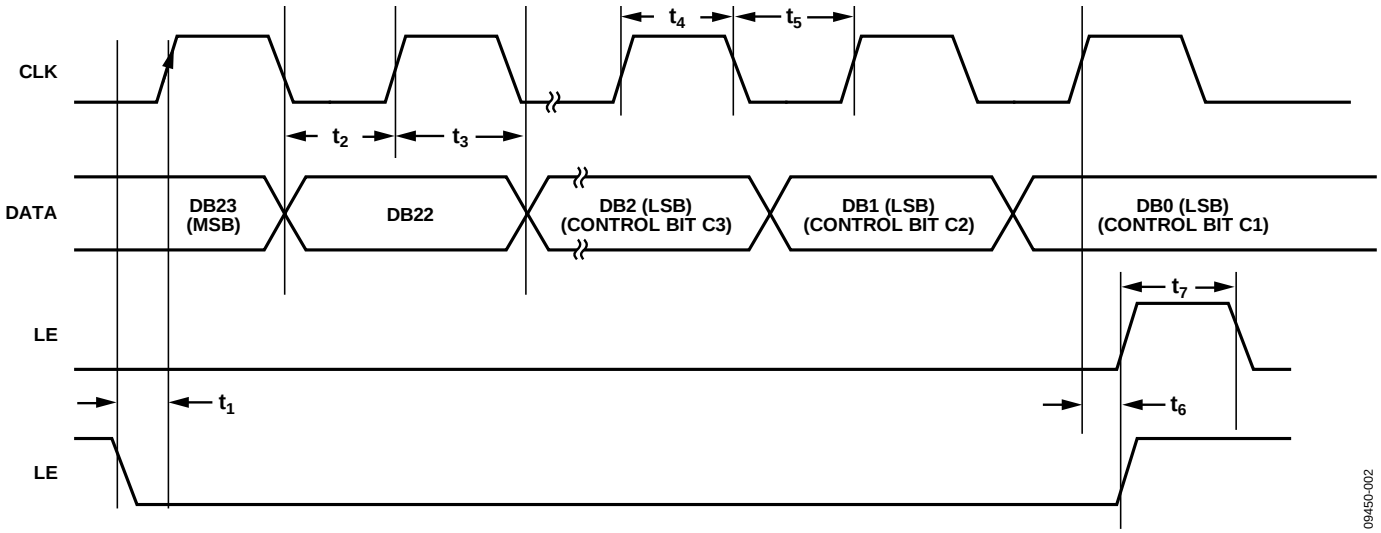


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to Ground	−0.3 V to +3.6 V
AV_{DD} to $DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$, SDV_{DD}	−0.3 V to +0.3 V
V_P1, V_P2, V_P3 to Ground	−0.3 V to +5.8 V
V_P1, V_P2, V_P3 to AV_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to Ground	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to Ground	−0.3 V to V_P1, V_P2, V_P3 + 0.3 V
REF_{IN}, RF_{IN+}, RF_{IN-} to Ground	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Take proper precautions for handling and assembly.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead LFCSP (Paddle Soldered)	27.3	°C/W

TRANSISTOR COUNT

This device includes 75,800 metal oxide semiconductors (MOS) and 545 bipolar junction transistors (BJT).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

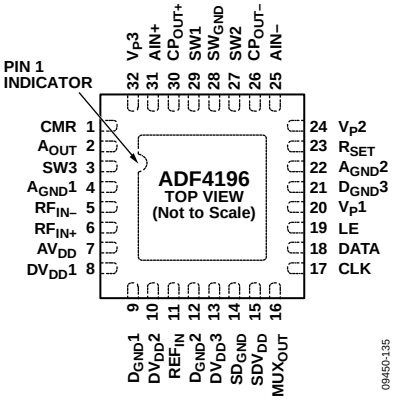


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CMR	Common-Mode Reference Voltage for the Output Voltage Swing of the Differential Amplifier. Internally biased to three-fifths of V_P3. Requires a 0.1 µF capacitor to the ground plane.
2	A_{OUT}	Differential Amplifier Output. This pin is the differential amplifier output to tune the external VCO.
3	SW3	Fast Lock Switch 3. This switch is closed when the SW3 timeout counter is active.
4	$A_{GND}1$	Analog Ground. This is the ground return pin for the differential amplifier and the RF section.
5	RF_{IN-}	Complementary Input to the RF Prescaler. This pin must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	RF_{IN+}	Input to the RF Prescaler. This small-signal input is ac-coupled to the external VCO.
7	AV_{DD}	Power Supply Pin for the RF Section. Nominally 3 V. Place a 100 pF decoupling capacitor to the ground plane as close as possible to this pin.
8	$DV_{DD}1$	Power Supply Pin for the N Divider. $DV_{DD}1$ should be at the same voltage as AV_{DD}. Place a 0.1 µF decoupling capacitor to the ground plane as close as possible to this pin.
9	$D_{GND}1$	Ground Return Pin for $DV_{DD}1$.
10	$DV_{DD}2$	Power Supply Pin for the REF_{IN} Buffer and R Divider. Nominally 3 V. Place a 0.1 µF decoupling capacitor to the ground plane as close as possible to this pin.
11	REF_{IN}	Reference Input. This CMOS input has a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
12	$D_{GND}2$	Ground Return Pin for $DV_{DD}2$ and $DV_{DD}3$.
13	$DV_{DD}3$	Power Supply Pin for the Serial Interface Logic. Nominally 3 V.
14	SD_{GND}	Ground Return Pin for the Digital Σ-Δ Modulator.
15	SDV_{DD}	Power Supply Pin for the Digital Σ-Δ Modulator. Nominally 3 V. Place a 0.1 µF decoupling capacitor to the ground plane as close as possible to this pin.
16	MUX_{OUT}	Multiplexer Output. This multiplexer output allows the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally (see Figure 35 for details).
17	CLK	Serial Clock Input. Data is clocked into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
18	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs as the control bits. This input is a high impedance CMOS input.
19	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the three LSBs.
20	V_P1	Power Supply Pin for the Phase Frequency Detector (PFD). Nominally 5 V, V_P1 should be at the same voltage as V_P2. Place a 0.1 µF decoupling capacitor to the ground plane as close as possible to this pin.
21	$D_{GND}3$	Ground Return Pin for V_P1.
22	$A_{GND}2$	Ground Return Pin for V_P2.

Pin No.	Mnemonic	Description
23	R_{SET}	Connecting a resistor between this pin and GND sets the charge pump output current. The nominal voltage bias at the R_{SET} pin is 0.55 V. The relationship between I_{CP} and R_{SET} is $$I_{CP} = \frac{0.25}{R_{SET}}$$ Therefore, with R_{SET} = 2.4 kΩ, I_{CP} = 104 μA.
24	V_P2	Power Supply Pin for the Charge Pump. Nominally 5 V, V_P2 should be at the same voltage as V_P1. Place a 0.1 μF decoupling capacitor to the ground plane as close as possible to this pin.
25	AIN−	Negative Input Pin for the Differential Amplifier.
26	CP_{OUT-}	Differential Charge Pump Negative Output Pin. Connect this pin to AIN− and the loop filter.
27	SW2	Fast Lock Switch 2. This switch is closed to SW_{GND} when the SW1/SW2 timeout counter is active.
28	SW_{GND}	Ground for SW1 and SW2 Switches. Connect this pin to the ground plane.
29	SW1	Fast Lock Switch 1. This switch is closed to SW_{GND} when the SW1/SW2 timeout counter is active.
30	CP_{OUT+}	Differential Charge Pump Positive Output Pin. Connect this pin to AIN+ and the loop filter.
31	AIN+	Positive Input Pin for the Differential Amplifier.
32	V_P3	Power Supply Pin for the Differential Amplifier. Ranges from 5.0 V to 5.5 V. Place a 0.1 μF decoupling capacitor to the ground plane as close as possible to this pin. V_P3 also requires a 10 μF decoupling capacitor to the ground plane.
	EP	Exposed Paddle. The exposed paddle must be connected to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ. UNIT GHz KEYWORD R
PARAM TYPE S IMPEDANCE 50
DATA FORMAT MA

FREQ.	MAGS11	ANGS11	FREQ.	MAGS11	ANGS11
0.5	0.8897	–16.6691	2.3	0.67107	–75.8206
0.6	0.87693	–19.9279	2.4	0.66556	–77.6851
0.7	0.85834	–23.561	2.5	0.6564	–80.3101
0.8	0.85044	–26.9578	2.6	0.6333	–82.5082
0.9	0.83494	–30.8201	2.7	0.61406	–85.5623
1.0	0.81718	–34.9499	2.8	0.5977	–87.3513
1.1	0.80229	–39.0436	2.9	0.5655	–89.7605
1.2	0.78917	–42.3623	3.0	0.5428	–93.0239
1.3	0.77598	–46.322	3.1	0.51733	–95.9754
1.4	0.75578	–50.3484	3.2	0.49909	–99.1291
1.5	0.74437	–54.3545	3.3	0.47309	–102.208
1.6	0.73821	–57.3785	3.4	0.45694	–106.794
1.7	0.7253	–60.695	3.5	0.44698	–111.659
1.8	0.71365	–63.9152	3.6	0.43589	–117.986
1.9	0.70699	–66.4365	3.7	0.42472	–125.62
2.0	0.7038	–68.4453	3.8	0.41175	–133.291
2.1	0.69284	–70.7986	3.9	0.41055	–140.585
2.2	0.67717	–73.7038	4.0	0.40983	–147.97

09450-038

Figure 4. S-Parameter Data for the RF Input

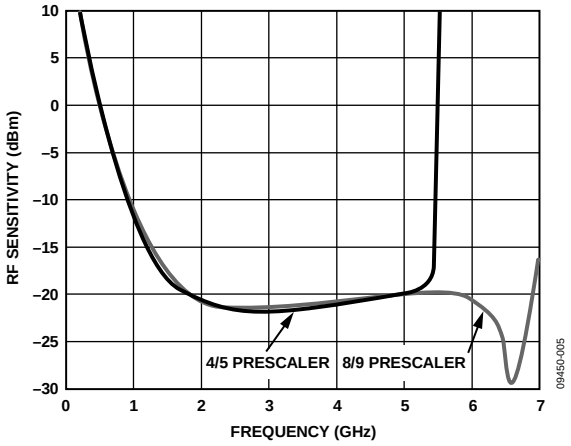


Figure 7. RF Input (RF_{IN}) Sensitivity

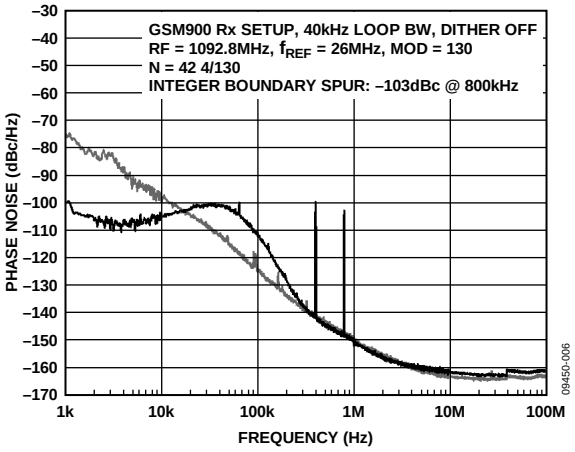


Figure 5. Single-Sideband (SSB) Phase Noise Plot at 1092.8 MHz (GSM900 Rx Setup) vs. Free Running VCO Noise

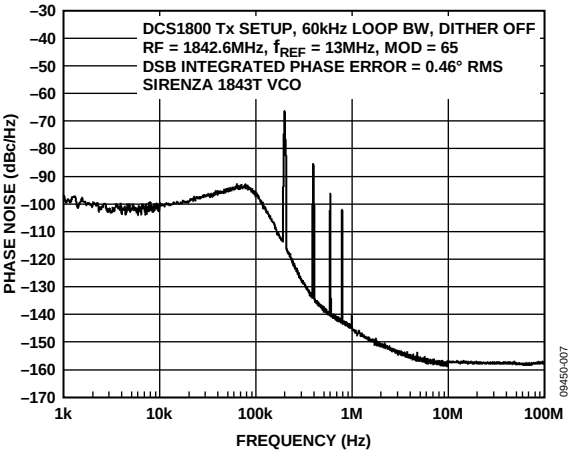


Figure 8. Single-Sideband (SSB) Phase Noise Plot at 1842.6 MHz (DCS1800 Tx Setup)

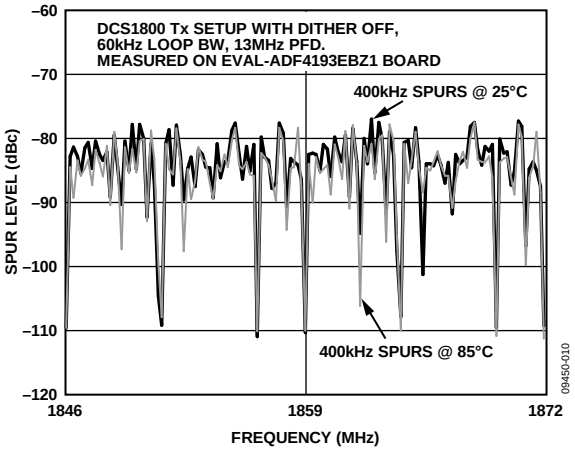


Figure 6. 400 kHz Fractional Spur Levels Across All DCS1800 Tx Channels over Two Integer Multiples of the PFD Reference

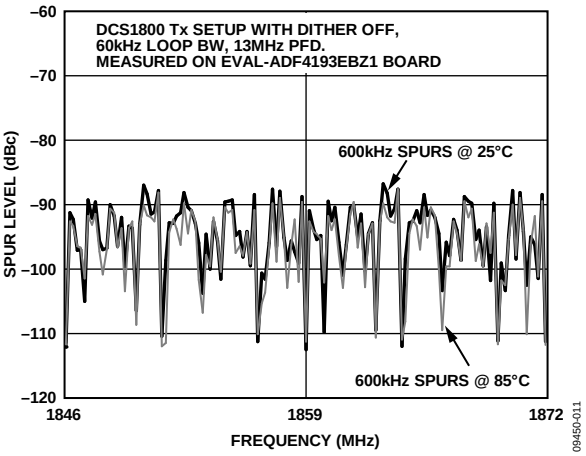


Figure 9. 600 kHz Fractional Spur Levels Across All DCS1800 Tx Channels over Two Integer Multiples of the PFD Reference

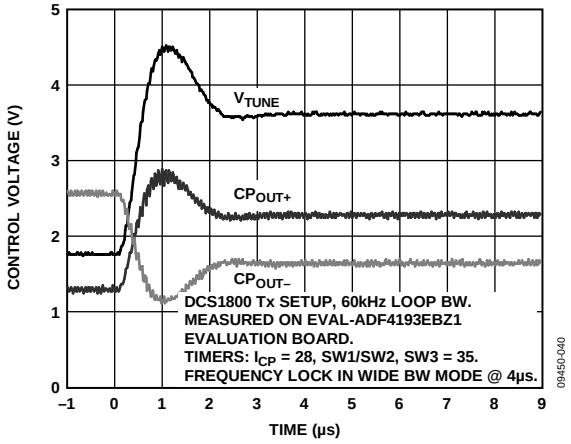


Figure 10. V_{TUNE} Settling Transient for a 75 MHz Jump from 1818 MHz to 1893 MHz with Sirenza 1843T VCO

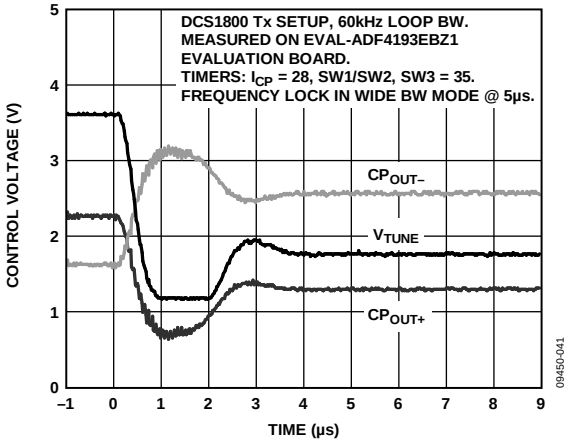


Figure 13. V_{TUNE} Settling Transient for a 75 MHz Jump Down from 1893 MHz to 1818 MHz (Bottom of Allowed Tuning Range) with Sirenza 1843T VCO

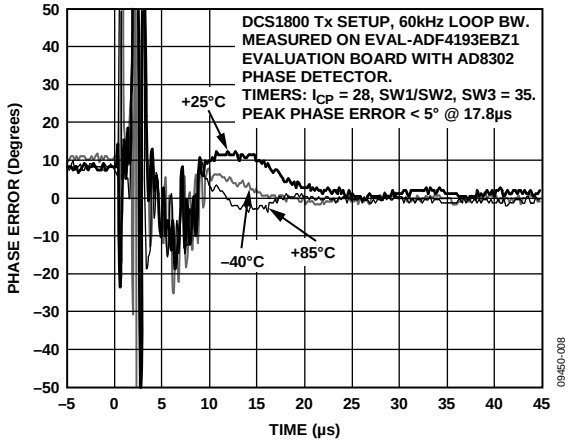


Figure 11. Phase Settling Transient for a 75 MHz Jump from 1818 MHz to 1893 MHz (V_{TUNE} = 1.8 V to 3.7 V with Sirenza 1843T VCO)

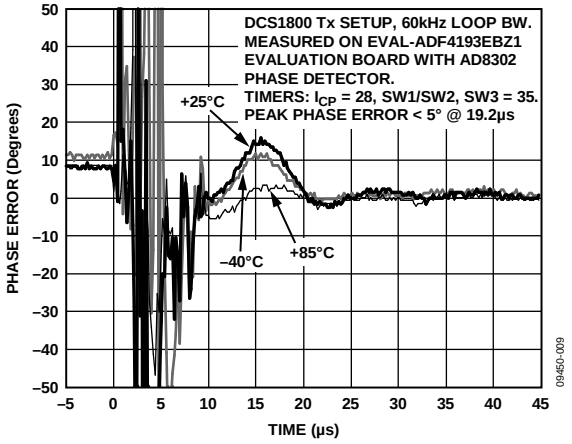


Figure 14. Phase Settling Transient for a 75 MHz Jump Down from 1893 MHz to 1818 MHz (V_{TUNE} = 3.7 V to 1.8 V with Sirenza 1843T VCO)

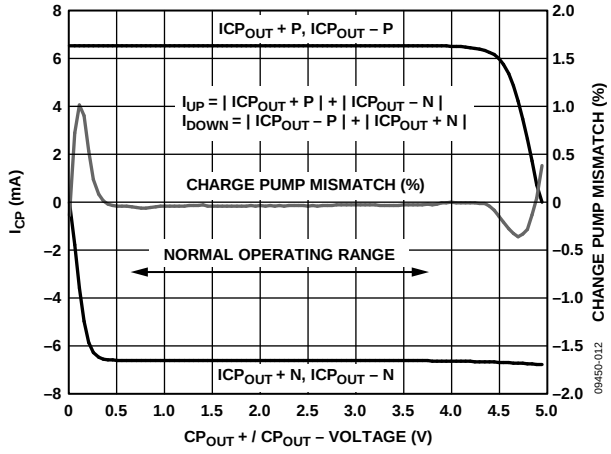


Figure 12. Differential Charge Pump Output Compliance Range and Charge Pump Mismatch with $V_P1 = V_P2$ = 5 V

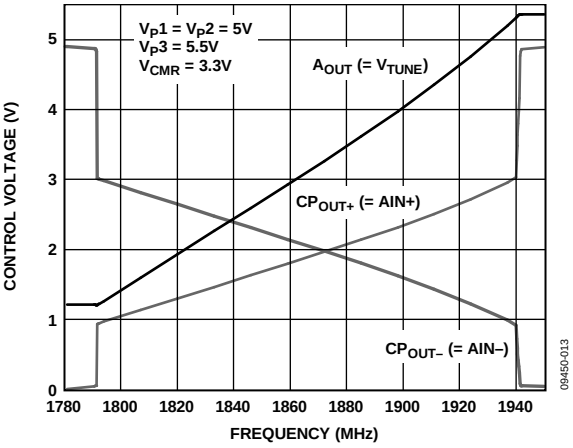


Figure 15. Tuning Range with a Sirenza 1843T VCO and a 5.5 V Differential Amplifier Power Supply Voltage

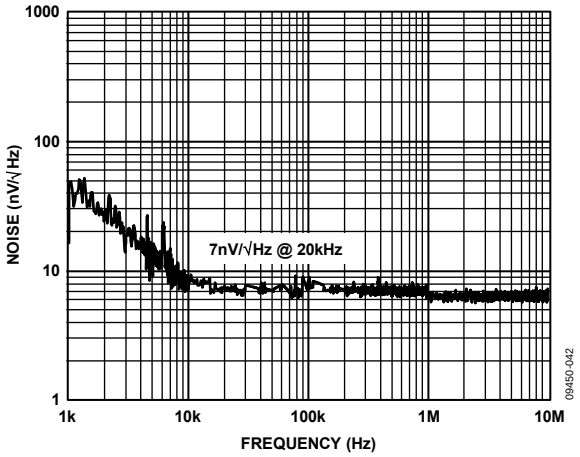


Figure 16. Voltage Noise Density Measured at the Differential Amplifier Output

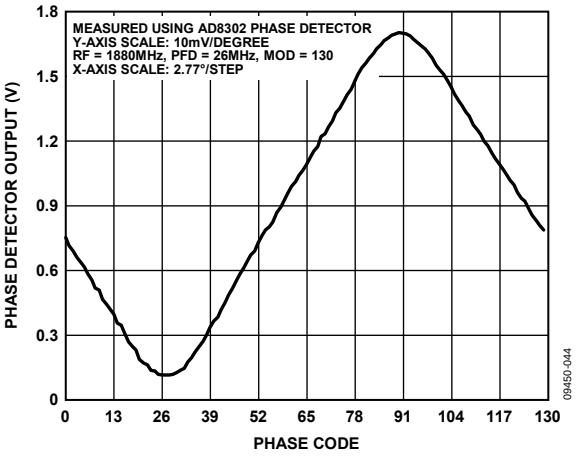


Figure 18. Detected RF Output Phase for Phase Code Sweep from 0 to MOD

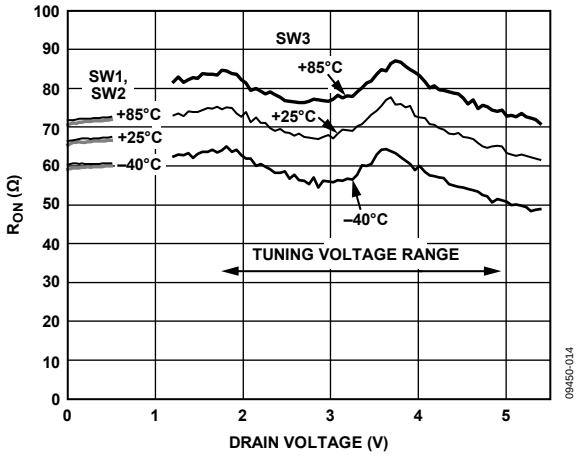


Figure 17. On Resistance of the SW1, SW2, and SW3 Loop Filter Switches

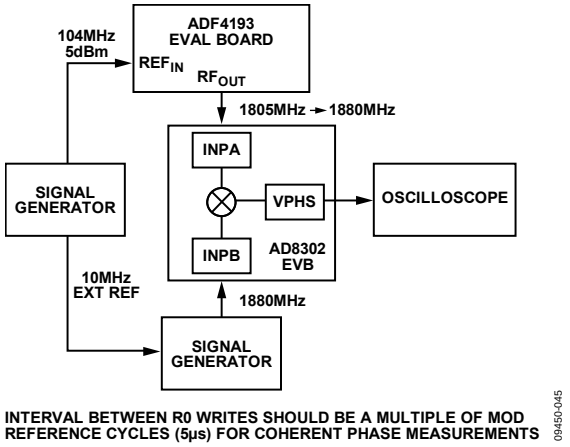


Figure 19. Test Setup for Phase Lock Time Measurements

THEORY OF OPERATION

GENERAL DESCRIPTION

The ADF4196 is targeted at GSM base station requirements, specifically to eliminate the need for ping-pong solutions. It can also be used in pulse Doppler radar applications. The ADF4196 works on the basis of fast lock, using a wide loop bandwidth during a frequency change and narrowing the loop bandwidth when frequency lock is achieved.

Widening the loop bandwidth is achieved by increasing the charge pump current. To maintain stability with the changing charge pump current, the ADF4196 includes switches that change the loop filter component values.

The narrow loop bandwidth ensures that phase noise and spur specifications are met. A differential charge pump and loop filter topology ensure that the fast lock time benefit obtained from widening the loop bandwidth is maintained when the loop is restored to narrow bandwidth mode for normal operation.

REFERENCE INPUT

The reference input stage is shown in Figure 20. Switch SW1 and Switch SW2 are normally closed, and Switch SW3 is normally open. During power-down, SW3 is closed, and SW1 and SW2 are opened to ensure that there is no loading of the REF_{IN} pin. The falling edge of REF_{IN} is the active edge at the positive edge triggered PFD.

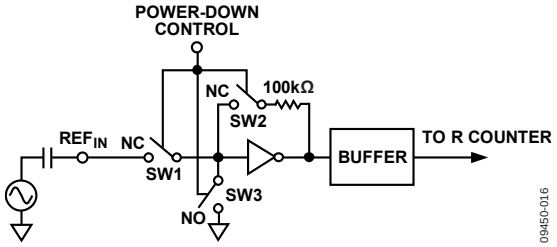


Figure 20. Reference Input Stage

R Counter and Doubler

The 4-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the PFD. A toggle flip-flop can be inserted after the R counter to provide an additional divide-by-2. Using this option has the added advantage of ensuring that the PFD reference clock has a 50/50 mark-to-space ratio. This ratio gives the maximum separation between the fast lock timer clock, which is generated off the falling edge of the PFD reference, and the rising edge, which is the active edge in the PFD. It is recommended that this toggle flip-flop be enabled for all even R divide values that are greater than 2. The flip-flop must be enabled if dividing down a REF_{IN} frequency that is greater than 120 MHz.

An optional doubler before the 4-bit R counter can be used for low REF_{IN} frequencies, up to 20 MHz. With these programmable options, reference division ratios from 0.5 to 30 between REF_{IN} and the PFD are possible.

RF INPUT STAGE

The RF input stage is shown in Figure 21. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the prescaler. Two prescaler options are available: 4/5 and 8/9. Select the 8/9 prescaler for N divider values that are greater than 80.

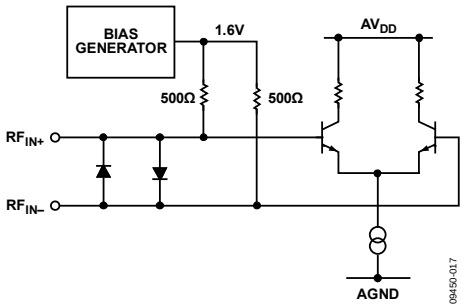


Figure 21. RF Input Stage

RF N Divider

The RF N divider allows a fractional division ratio in the PLL feedback path. The integer and fractional parts of the division are programmed using separate registers, as shown in Figure 22 and described in the INT, FRAC, and MOD Relationship section. Integer division ratios from 26 to 511 are allowed, and a third-order Σ-Δ modulator interpolates the fractional value between the integer steps.

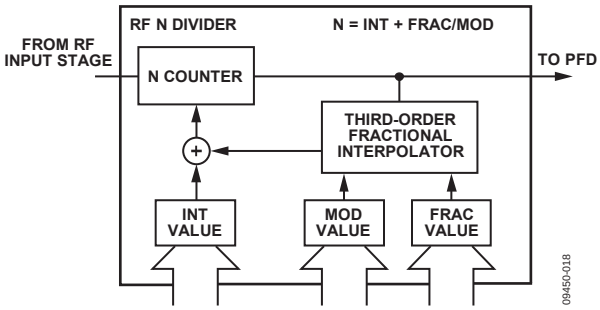


Figure 22. Fractional-N RF Divider

INT, FRAC, and MOD Relationship

The INT, FRAC, and MOD values, programmed through the serial interface, make it possible to generate RF output frequencies that are spaced by fractions of the PFD reference frequency. The N divider value, shown inside the brackets of the following equation for the RF VCO frequency (RF_{OUT}), is composed of an integer part (INT) and a fractional part (FRAC/MOD).

$$RF_{OUT} = f_{PFD} \times [INT + (FRAC/MOD)] \quad (1)$$

where:
RF_{OUT} is the output frequency of the external VCO.
f_{PFD} is the PFD reference frequency.

The value of MOD is chosen to give the desired channel step with the available reference frequency. Then, program the INT and FRAC words for the desired RF output frequency. See the Worked Example section for more information.

PFD AND CHARGE PUMP

The PFD takes inputs from the R divider and N divider and produces up and down outputs with a pulse width difference that is proportional to the phase difference between the inputs. The charge pump outputs a net up or down current pulse of a width that is equal to this difference, to pump up or pump down the voltage that is integrated into the loop filter, which in turn increases or decreases the VCO output frequency. If the N divider phase lags the R divider phase, a net up-current pulse is produced that increases the VCO frequency (and, thus, the phase). If the N divider phase leads the R divider edge, a net down-current pulse is produced to reduce the VCO frequency and phase. Figure 23 is a simplified schematic of the PFD and charge pump. The charge pump is made up of an array of 64 identical cells, each of which is fully differential. All 64 cells are active during fast lock, and only one cell is active during normal operation.

Because a single-ended control voltage is required to tune the VCO, an on-chip differential-to-single-ended amplifier is provided for this purpose. In addition, because the phase-locked loop controls only the differential voltage generated across the charge pump outputs, an internal common-mode feedback (CMFB) loop biases the charge pump outputs at a common-mode voltage of approximately 2 V.

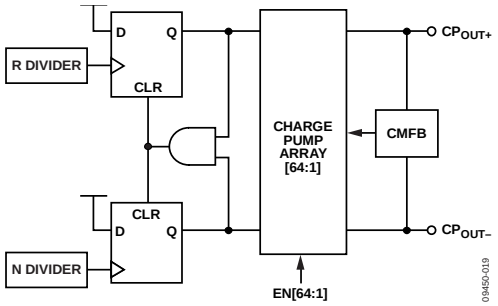


Figure 23. PFD and Differential Charge Pump Simplified Schematic

DIFFERENTIAL CHARGE PUMP

The charge pump cell has a fully differential design for best up-to-down current matching (see Figure 24). Good matching is essential to minimize the phase offset created when switching the charge pump current from its high value (in fast lock mode) to its nominal value (in normal mode).

To pump up, the up switches are on, and the PMOS current sources out through CP_{OUT+}, which increases the voltage on the external loop filter capacitors that are connected to CP_{OUT+}. Similarly, the NMOS current sink on CP_{OUT-} decreases the voltage on the external loop filter capacitors that are connected to CP_{OUT-}. Therefore, the differential voltage between CP_{OUT+} and CP_{OUT-} increases.

To pump down, PMOS current sources out through CP_{OUT-} and NMOS current sinks in through CP_{OUT+}, which decreases the (CP_{OUT+}, CP_{OUT-}) differential voltage. The charge pump up/down matching is improved by an order of magnitude over the conventional single-ended charge pump that depends on the matching of two different device types. The up/down matching in this structure depends on how a PMOS matches a PMOS, and how an NMOS matches an NMOS.

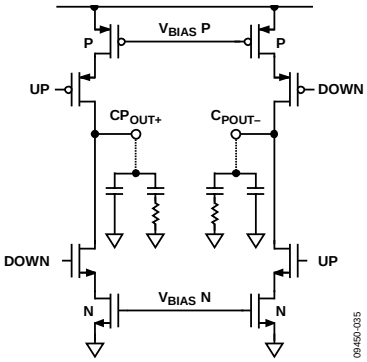


Figure 24. Differential Charge Pump Cell with External Loop Filter Components

FAST LOCK TIMEOUT COUNTERS

Timeout counters, clocked at one-quarter of the PFD reference frequency, are provided to precisely control the fast locking operation (see Figure 25). When a new frequency is programmed, the fast lock timers start and the PLL locks into wide bandwidth mode with the 64 identical 100 µA charge pump cells active (for a total of 6.4 mA).

When the I_{CP} counter times out, the charge pump current is reduced to 1× by deselecting cells in binary steps over the next six timer clock cycles, until only one 100 µA cell is active. The switching of the charge pump current, from 6.4 mA to 100 µA, equates to an 8-to-1 change in loop bandwidth; when this happens, the loop filter must be changed to ensure stability. The SW1, SW2, and SW3 switches change the loop filter.

The applications circuit shown in Figure 37 shows how the switches can be used to reconfigure the loop filter time constants. They close to short out external loop filter resistors during fast lock and open when their counters time out to restore the filter time constants to their normal values for the 100 µA charge pump current. Because it takes six timer clock cycles to reduce the charge pump current to 1×, it is recommended that both switch timers be programmed to the value of the I_{CP} timer plus 7.

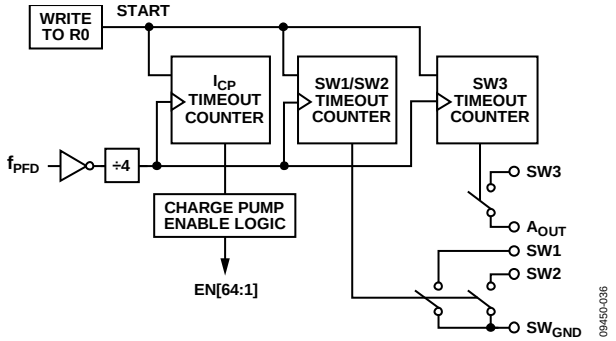


Figure 25. Fast Lock Timeout Counters

DIFFERENTIAL AMPLIFIER

The internal, low noise, differential-to-single-ended amplifier converts the differential charge pump output to a single-ended control voltage for the tuning port of the VCO. Figure 26 shows a simplified schematic of the differential amplifier. The output voltage is equal to the differential voltage, offset by the voltage on the CMR pin, according to the following equation:

$$V_{AOUT} = (V_{AIN+} - V_{AIN-}) + V_{CMR} \quad (2)$$

The CMR offset voltage is internally biased to three-fifths of V_P3, the differential amplifier power supply voltage, as shown in Figure 26. Connect a 0.1 µF capacitor to the ground plane from the CMR pin to roll off the thermal noise of the biasing resistors.

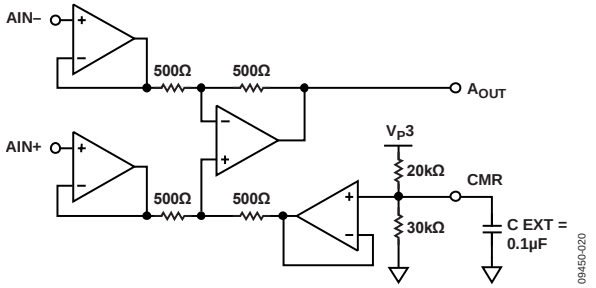


Figure 26. Differential Amplifier Block Diagram

As shown in Figure 15, the differential amplifier output voltage behaves according to Equation 2 over a 4 V range from ~1.2 V minimum up to V_P3 – 0.3 V maximum. However, fast settling is guaranteed over a tuning voltage range from 1.8 V up to V_P3 – 0.8 V only. This range allows sufficient room for overshoot in the PLL frequency settling transient.

Noise from the differential amplifier is suppressed inside the PLL loop bandwidth. For loop bandwidths of >20 kHz, the 1/f noise has a negligible effect on the PLL output phase noise. Outside the loop bandwidth, the FM noise of the differential amplifier modulates the VCO. The passive filter network following the differential amplifier (see Figure 37) suppresses this noise contribution to below the VCO noise from offsets of 400 kHz and greater. This network has a negligible effect on lock time because it is bypassed when SW3 is closed while the loop is locking.

MUX_{OUT} AND LOCK DETECT

MUX_{OUT} Control

The output multiplexer on the ADF4196 allows the user to access various internal points on the chip. The state of MUX_{OUT} is controlled by Bits[M4:M1] in the mux register. Figure 35 shows the full truth table; see Figure 27 for a block diagram of the MUX_{OUT} circuit.

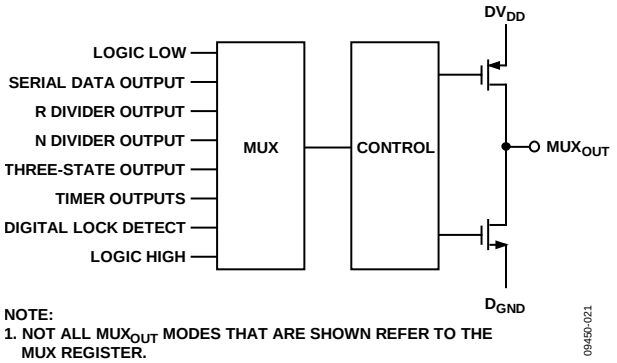


Figure 27. MUX_{OUT} Circuit

Lock Detect

MUX_{OUT} can be programmed to provide a digital lock detect signal. Digital lock detect is active high. Its output goes high if there are 40 successive PFD cycles with an input error of <3 ns. For reliable lock detect operation with RF frequencies of <2 GHz, it is recommended that this threshold be increased to 10 ns by programming Register R6. The digital lock detect goes low again when a new channel is programmed or when the error at the PFD input exceeds 30 ns for one or more cycles.

INPUT SHIFT REGISTER

The ADF4196 serial interface includes a 24-bit input shift register. Data is clocked in, MSB first, on each rising edge of CLK. Data from the shift register is latched into one of eight control registers, R0 to R7, on the rising edge of load enable (LE) The destination register is determined by the state of the three control bits: C3 (DB2), C2 (DB1), and C1 (DB0) in the shift register. DB2, DB1, and DB0 are the three LSBs, as shown in the timing diagram in Figure 2. The truth table for these bits is shown in Table 6. Figure 28 shows a summary of how the registers are programmed.

Table 6. C3, C2, and C1 Truth Table

Control Bits				
C3 (DB2)	C2 (DB1)	C1 (DB0)	Register Name	Register
0	0	0	FRAC/INT	R0
0	0	1	MOD/R	R1
0	1	0	Phase	R2
0	1	1	Function	R3
1	0	0	Charge pump	R4
1	0	1	Power-down	R5
1	1	0	Mux	R6
1	1	1	Test mode	R7

REGISTER MAP

FRAC/INT REGISTER (R0)

9-BIT RF INT VALUE									12-BIT RF FRAC VALUE												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

MOD/R REGISTER (R1)

DBB CP ADJ	DBB REF/2	RESERVED	PRESCALER	DBB DOUBLER ENABLE	DBB 4-BIT RF R COUNTER				DBB 12-BIT MODULUS												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F5	F4	0	F2	F1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3 (0)	C2 (0)	C1 (1)

PHASE REGISTER (R2)

RESERVED	DBB 12-BIT PHASE												CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3 (0)	C2 (1)	C1 (0)

FUNCTION REGISTER (R3)

RESERVED										CPO GND	RESERVED	PFD POLARITY	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	F3	1	F1	C3 (0)	C2 (1)	C1 (1)

CHARGE PUMP REGISTER (R4)

RESERVED										9-BIT TIMEOUT COUNTER									TIMER SELECT		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	C9	C8	C7	C6	C5	C4	C3	C2	C1	F2	F1	C3 (1)	C2 (0)	C1 (0)

POWER-DOWN REGISTER (R5)

PD DIFF AMP	PD CHARGE PUMP	CP 3-STATE	COUNTER RESET	CONTROL BITS		
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F5	F4	F3	F2	F1	C3 (1)	C2 (0)	C1 (1)

MUX REGISTER (R6)

SIGMA-DELTA AND LOCK DETECT MODES				RESERVED					MUX_{OUT}				CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M13	M12	M11	M10	0	0	0	0	1	M4	M3	M2	M1	C3 (1)	C2 (1)	C1 (0)

TEST MODE REGISTER (R7)

RESERVED													CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	C3 (1)	C2 (1)	C1 (1)

DBB = DOUBLE BUFFERED BIT(S)

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Figure 28. Bit Maps for Register R0 to Register R7

FRAC/INT REGISTER (R0) LATCH MAP

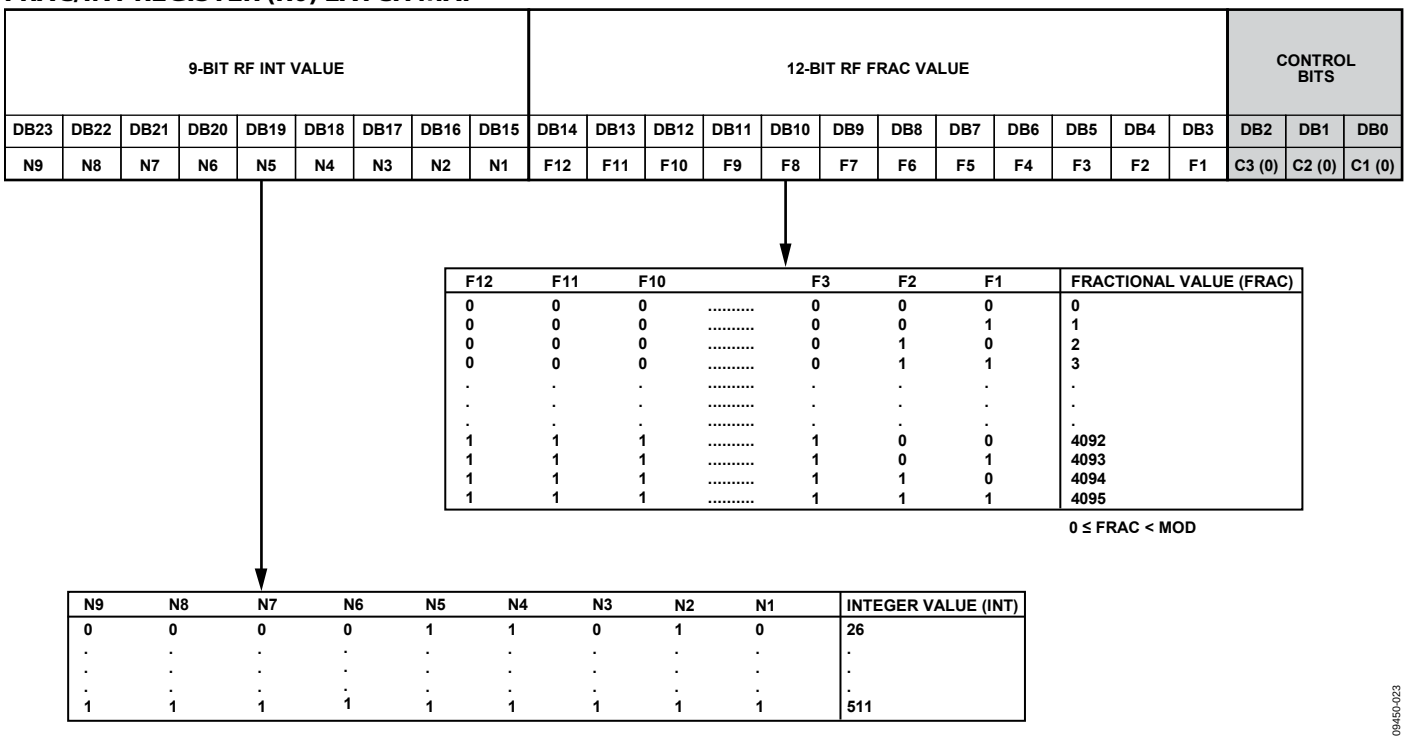


Figure 29. Bit Map for Register R0

R0, the FRAC/INT register, is used to program the synthesizer output frequency. On the PFD cycle following a write to R0, the N divider section is updated with the new INT and FRAC values, and the PLL automatically enters fast lock mode. The charge pump current is increased to its maximum value and remains at this value until the I_{CP} timeout counter times out; and the SW1, SW2, and SW3 switches close and remain closed until the SW1/SW2 and SW3 timeout counters time out.

After all the registers are programmed during the initialization sequence (see Table 9), a new channel can be programmed by performing a write to R0. However, as described in the Programming the ADF4196 section, it may also be desirable to program the R1 and R2 register settings on a channel-by-channel basis. These settings are double buffered by the write to Register R0. This means that, although the data is loaded through the serial interface on the respective R1 and R2 write cycles, the synthesizer is not updated with their data until the next write to Register R0.

Control Bits

To select R0, the FRAC/INT register, the three LSBs (C3, C2, and C1) should be set to 0, 0, 0.

9-Bit RF INT Value

Bits[DB23:DB15] set the INT value, which determines the integer part of the feedback division factor. All integer values from 26 to 511 are allowed (see the Worked Example section).

12-Bit RF FRAC Value

Bits[DB14:DB3] set the numerator of the fraction that is input to the Σ-Δ modulator. This fraction, along with INT, specifies the new frequency channel that the synthesizer locks to, as shown in the Worked Example section. FRAC values from 0 to MOD – 1 cover channels over a frequency range that is equal to the PFD reference frequency.

MOD/R REGISTER (R1) LATCH MAP

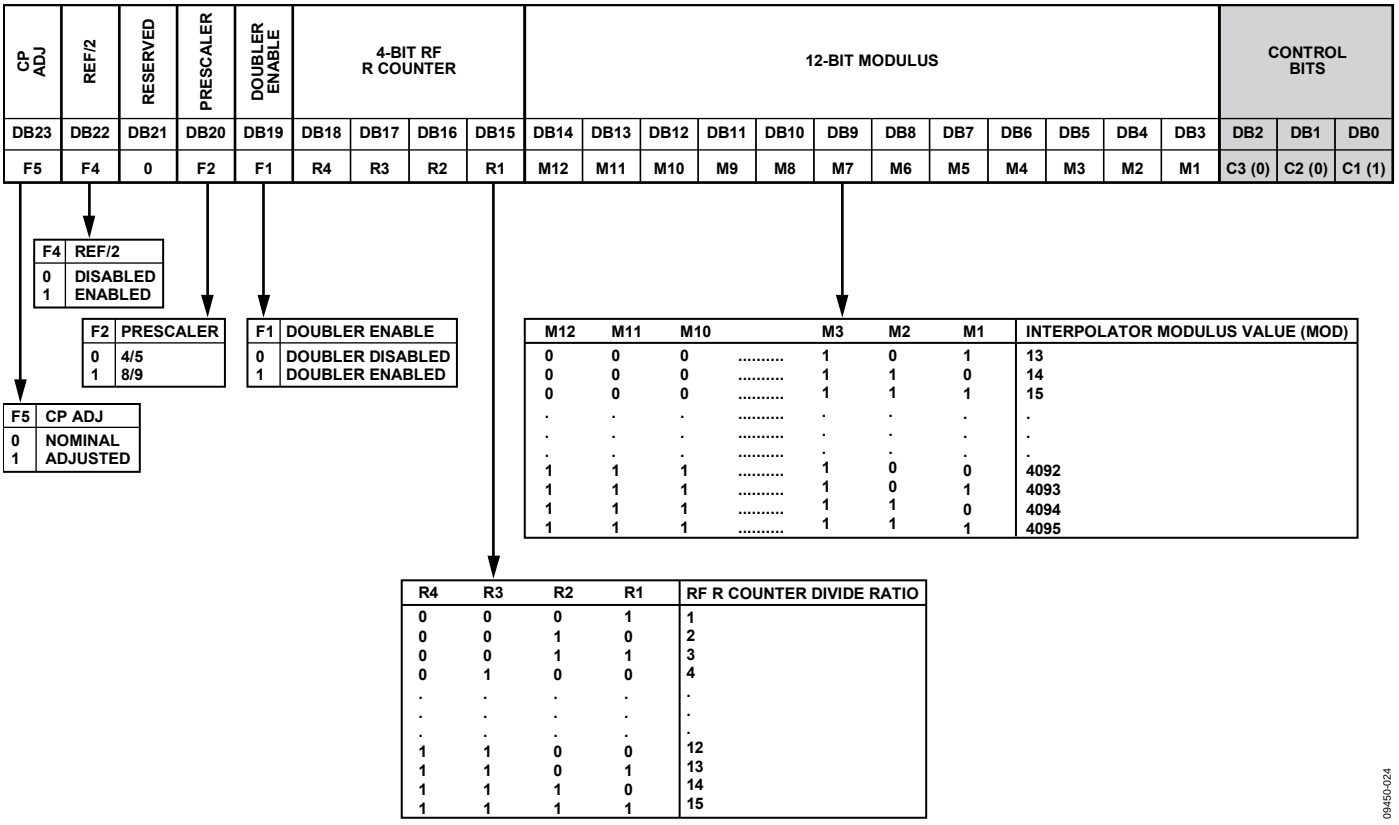


Figure 30. Bit Map for Register R1

R1, the MOD/R register, sets the PFD reference frequency and the channel step size, which is determined by the PFD frequency divided by the fractional modulus. Note that the 12-bit modulus, the 4-bit RF R counter, the doubler enable bits, REF/2, and CP ADJ are double buffered. They do not take effect until the next write to R0 (the FRAC/INT register) is complete.

Control Bits

Register R1 is selected with C3, C2, and C1 set to 0, 0, 1.

CP ADJ

When the CP ADJ bit is set to 1, the charge pump current is scaled up 25% from its nominal value on the next write to R0. When this bit is set to 0, the charge pump current remains at its nominal value on the next write to R0. See the Programming the ADF4196 section for more information on how this feature can be used.

REF/2

Setting the REF/2 bit to 1 inserts a divide-by-2 toggle flip-flop between the R counter and the PFD, which extends the maximum REF_{IN} input rate.

Reserved Bit

The reserved bit, DB21, must be set to 0.

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with INT, FRAC, and MOD, determine the overall division ratio from RF_{IN} to the PFD input. Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4196 above 3 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value. If P = 4/5, then N_{MIN} = 26. If P = 8/9, N_{MIN} = 80.

Doubler Enable

Setting the doubler enabler bit to 1 inserts a frequency doubler between REF_{IN} and the 4-bit RF R counter. Setting this bit to 0 bypasses the doubler.

4-Bit RF R Counter

The 4-bit RF R counter allows the REF_{IN} frequency to be divided down to produce the reference clock to the PFD. All integer values from 1 to 15 are allowed (see the Worked Example section).

12-Bit Modulus

For a given PFD reference frequency, the fractional denominator or modulus sets the channel step resolution at the RF output. All integer values from 13 to 4095 are allowed. See the Programming the ADF4196 section for a Worked Example and guidelines for selecting the value of MOD.

PHASE REGISTER (R2) BIT LATCH MAP

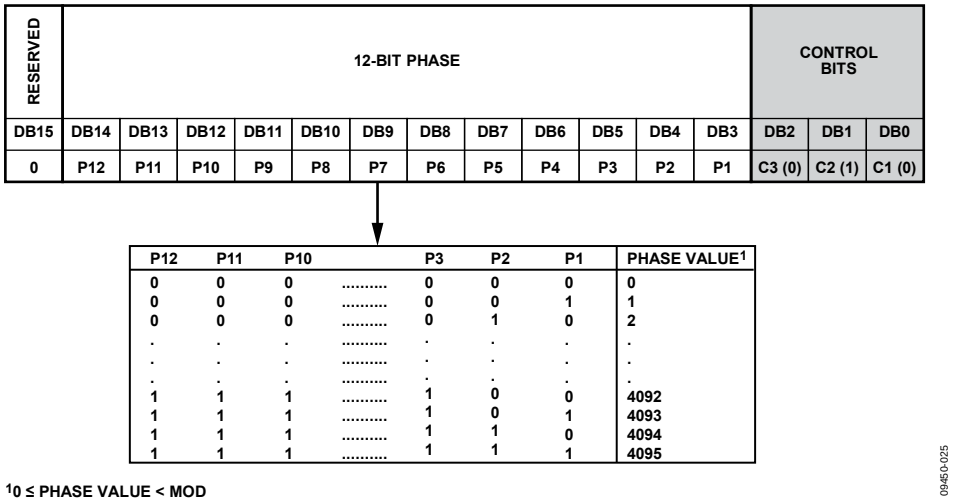


Figure 31. Bit Map for Register R2

R2, the phase register, is used to program the phase of the VCO output signal.

Control Bits

Register R2 is selected with C3, C2, and C1 set to 0, 1, 0.

12-Bit Phase

The 12-bit phase word sets the seed value of the Σ-Δ modulator. It can be programmed to any integer value from 0 to MOD, where MOD is the modulus value that is programmed in Register R1, Bits[DB14:DB3]. As the phase word is swept from 0 to MOD, the phase of the VCO output sweeps over a 360° range in steps of 360°/MOD.

Note that the phase bits are double buffered; they do not take effect until the load enable of the next write to R0 (the FRAC/INT register). Thus, to change the phase of the VCO output frequency, it is necessary to rewrite the INT and FRAC values to Register R0 following the write to Register R2.

The output of a fractional-N PLL can settle to any one of the MOD possible phase offsets with respect to the reference, where MOD is the fractional modulus.

To keep the output at the same phase offset with respect to the reference, each time that particular output frequency is programmed, the interval between writes to Register R0 must be an integer multiple of MOD reference cycles.

To keep the outputs of two ADF4196-based synthesizers phase coherent with each other (but not necessarily with the reference they have in common), the write to Register R0 on both chips must be performed during the same reference cycle. In this case, the interval between the R0 writes does not need to be an integer multiple of MOD cycles.

Reserved Bit

Set the reserved bit, DB15, to 0.

FUNCTION REGISTER (R3) LATCH MAP

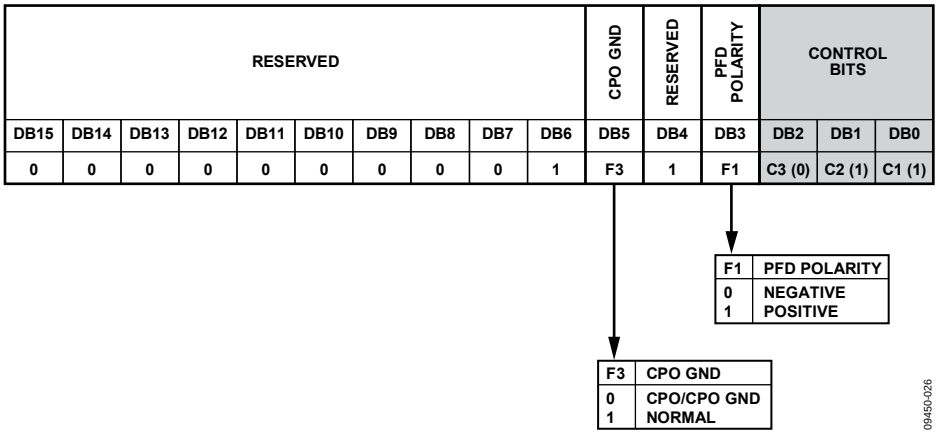


Figure 32. Bit Map for Register R3

R3, the function register, needs to be programmed only during the initialization sequence (see Table 9).

Control Bits

Register R3 is selected with C3, C2, and C1 set to 0, 1, 1.

CPO GND

When the CPO GND bit is low, the charge pump outputs are internally pulled to ground. This is invoked during the initialization sequence to discharge the loop filter capacitors. For normal operation, this bit should be set to 1.

PFD Polarity

Set the PFD polarity bit to 1 for positive polarity, and set it to 0 for negative polarity.

Reserved Bits

Program the DB15 to DB6 reserved bits to a hexadecimal code of 0x001, and set the DB4 reserved bit to 1.

CHARGE PUMP REGISTER (R4) LATCH MAP

RESERVED										9-BIT TIMEOUT COUNTER									TIMER SELECT		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	C9	C8	C7	C6	C5	C4	C3	C2	C1	F2	F1	C3 (1)	C2 (0)	C1 (0)

F2	F1	TIMER SELECT
0	0	SW1/SW2
0	1	SW3
1	0	I_{CP}
1	1	NOT USED

C9	C8	C7		C3	C2	C1	TIMEOUT COUNTER	xPFD CYCLES	DELAY µs[1]
0	0	0	.....	0	0	0	0	0	0
0	0	0	.....	0	0	1	1	4	0.15
0	0	0	.....	0	1	0	2	8	0.30
0	0	0	.....	0	1	1	3	12	0.46
.	.	.	.....	.	.	.	.	.	.
.	.	.	.....	.	.	.	.	.	.
.	.	.	.....	.	.	.	.	.	.
1	1	1	.....	1	0	0	508	2032	78.15
1	1	1	.....	1	0	1	509	2036	78.30
1	1	1	.....	1	1	0	510	2040	78.46
1	1	1	.....	1	1	1	511	2044	78.61

[1]DELAY WITH 26MHz PFD

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Figure 33. Bit Map for Register R4

R4, the charge pump register, is used for programming the timers for loop filter switches. These switches help maintain the stability of the loop filter after boosting the charge pump current.

Control Bits

Register R4 is selected with C3, C2, and C1 (Bits[DB2:DB0]) set to 1, 0, 0.

Reserved Bits

For normal operation, set the DB23 to DB14 reserved bits to a hexadecimal code of 0x001.

9-Bit Timeout Counter

These bits are used to program the fast lock timeout counters. The counters are clocked at one-quarter the PFD reference frequency; therefore, their time delay scales with the PFD frequency according to the following equation:

$$Delay(s) = (Timeout\ Counter\ Value \times 4)/(PFD\ Frequency)$$

For example, if 35 is loaded with timer select = 00, with a 13 MHz PFD, SW1 and SW2 switch after the following:

$$(35 \times 4)/13\ MHz = 10.8\ \mu s$$

Timer Select

The two timer select bits select the timeout counter that is to be programmed. Note that setting up the ADF4196 for correct operation requires setup of these three timeout counters: I_{CP}, SW1/SW2, and SW3. Therefore, three writes to this register are required in the initialization sequence. Table 7 shows example values for a GSM Tx synthesizer with a 60 kHz final loop bandwidth. See the Applications Information section for more information.

Table 7. Recommended Values for a GSM Tx LO

Timer Select	Timeout Counter	Value	Time (µs) with PFD = 13 MHz
10	I_{CP}	28	8.6
01	SW3	35	10.8
00	SW1/SW2	35	10.8

On each write to R0, the timeout counters start. Switch SW3 closes until the SW3 counter times out. Similarly, the SW1 and SW2 switches close until the SW1/SW2 counter times out. When the I_{CP} counter times out, the charge pump current is ramped down from 64× to 1× in six binary steps. It is recommended that the SW1/SW2 and SW3 timeout counter values be set equal to the I_{CP} timeout counter value plus 7, as in the example shown in Table 7.

POWER-DOWN REGISTER (R5) BIT MAP

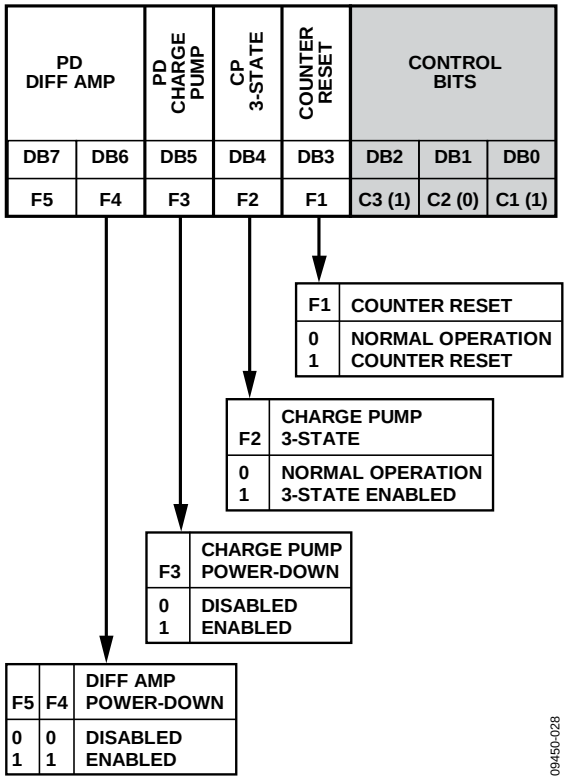


Figure 34. Bit Map for Register R5

R5, the power-down register, can be used to power down the PLL and differential amplifier sections. After power is initially applied, Register R5 must be programmed to clear the power-down bits. Then, before the ADF4196 comes out of power-down, the R2, R1, and R0 registers must be programmed.

Control Bits

Register R5 is selected with C3, C2, and C1 set to 1, 0, 1.

Power-Down Differential Amplifier

When the DB7 and DB6 bits are set to 1, the differential amplifier is put into power-down. When DB7 and DB6 are set to 0, normal operation resumes.

Power-Down Charge Pump

Setting Bit DB5 to 1 activates a charge pump power-down, and the following events occur:

- All active dc current paths are removed, except for the differential amplifier.
- The R and N divider counters are forced to their load state conditions.
- The charge pump is powered down with its outputs in three-state mode.
- The digital lock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The serial interface remains active and capable of loading and latching data.

For normal operation, set Bit DB5 to 0, followed by a write to R0.

CP Three-State

When the CP three-state bit is set to 1, the charge pump outputs enter three-state. Setting the CP three-state bit to 0 enables the charge pump outputs.

Counter Reset

When the counter reset bit is set to 1, the counters are held in reset. For normal operation, set this bit to 0, followed by a write to R0.

MUX REGISTER (R6) LATCH MAP AND TRUTH TABLE

SIGMA-DELTA AND LOCK DETECT MODES				RESERVED					MUX_{OUT}				CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M13	M12	M11	M10	0	0	0	0	1	M4	M3	M2	M1	C3 (1)	C2 (1)	C1 (0)

M13	M12	M11	M10	SIGMA-DELTA MODES
0	0	0	0	INIT STATE, DITHER OFF, 3ns LOCK DETECT THRESHOLD
0	0	1	1	DITHER ON
1	0	0	1	10ns LOCK DETECT THRESHOLD
ALL OTHER STATES				RESERVED

M4	M3	M2	M1	MUX_{OUT}
0	0	0	0	3-STATE
0	0	0	1	DIGITAL LOCK DETECT
0	0	1	0	N DIVIDER OUTPUT
0	0	1	1	LOGIC HIGH
0	1	0	0	R DIVIDER OUTPUT
0	1	0	1	RESERVED
0	1	1	0	SERIAL DATA OUTPUT
0	1	1	1	LOGIC LOW
1	0	0	0	R DIVIDER/2 OUTPUT
1	0	0	1	N DIVIDER/2 OUTPUT
1	0	1	0	RESERVED
1	0	1	1	RESERVED
1	1	0	0	I_{CP} TIMEOUT SIGNAL
1	1	0	1	SW1/SW2 TIMEOUT SIGNAL
1	1	1	0	SW3 TIMEOUT SIGNAL
1	1	1	1	RESERVED

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Figure 35. Bit Map and MUX_{OUT} Truth Table for Register R6

R6, the mux register, is used to program MUX_{OUT}, as well as Σ-Δ and lock detect modes.

Control Bits

Register R6 is selected with C3, C2, and C1 set to 1, 1, 0.

Σ-Δ and Lock Detect Modes

Bit DB15 to Bit DB12 are used to reconfigure certain PLL operating modes. In the initialization sequence after power is applied to the chip, the four bits must first be programmed to all zeros. This initializes the PLL to a known state with dither off in the Σ-Δ modulator and a 3 ns PFD error threshold in the lock detect circuit.

To turn on dither in the Σ-Δ modulator, an additional write should be made to Register R6 to program Bits[DB15:DB12] = 0011. However, for lowest noise operation, it is best to leave dither off.

To change the lock detect threshold from 3 ns to 10 ns, perform a separate write to R6 to program Bits[DB15:DB12] = 1001. This separate write is needed for reliable lock detect operation when the RF frequency is <2 GHz.

A write to R6 that programs Bits[DB15:DB12] = 0000 returns operation to the default state with both dither off and a 3 ns lock detect threshold.

Reserved Bits

For normal operation, the reserved bits (Bits[DB11:DB7]) must be set to 00001.

MUX_{OUT} Modes

These bits control the on-chip multiplexer, Pin 16 (see Figure 35 for the truth table). This pin is useful for diagnosis because it allows the user to look at various internal points of the chip, such as the R divider and the INT divider outputs.

In addition, it is possible to monitor the programmed timeout counter intervals on MUX_{OUT}. For example, if the I_{CP} timeout counter is programmed to 65 (with a 26 MHz PFD), then following the next write to R0, a pulse width of 10 µs is observed on the MUX_{OUT} pin.

Digital lock detect is available via the MUX_{OUT} pin.

PROGRAMMING THE ADF4196

The ADF4196 can synthesize output frequencies with a channel step or resolution that is a fraction of the input reference frequency. For a given input reference frequency and a desired output frequency step, the first choice to make is the PFD reference frequency and the MOD value. After these are chosen, the desired output frequency channels are set by programming the INT and FRAC values.

WORKED EXAMPLE

In this example of a GSM900 Rx system, the RF output frequencies must be generated with channel steps of 200 kHz. A reference frequency input (REF_{IN}) of 104 MHz is available. The R divider setting that determines the PFD reference is shown in Equation 3.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (3)$$

where:
REF_{IN} is the input reference frequency.
D is the doubler enable bit (0 or 1).
R is the 4-bit R counter code (1 to 15).
T is the REF/2 bit (0 or 1).

The maximum PFD reference frequency of 26 MHz is chosen, and the following settings are programmed to give an R divider value of 4:

- Doubler enable = 0
- R = 2
- REF/2 = 1

Next, the modulus is chosen to allow fractional steps of 200 kHz:

$$MOD = 26 \text{ MHz}/200 \text{ kHz} = 130 \quad (4)$$

When the channel step is defined, Equation 5 shows how output frequency channels are programmed.

$$RF_{OUT} = [INT + (FRAC/MOD)] \times f_{PFD} \quad (5)$$

where:
RF_{OUT} is the desired RF output frequency.
INT is the integer part of the division.
$FRAC$ is the numerator part of the fractional division.
MOD is the modulus or denominator part of the fractional division.

Thus, the frequency channel at 962.4 MHz is synthesized by programming the following values: INT = 37 and FRAC = 2.

SPUR MECHANISMS

The following sections describe the three different spur mechanisms that arise with a fractional-N synthesizer and how the ADF4196 can best be programmed to minimize them.

Fractional Spurs

The fractional interpolator in the ADF4196 is a third-order, Σ-Δ modulator (SDM) with a modulus MOD that is programmable to any integer value from 13 to 4095. If dither is enabled, the minimum allowed value of MOD is 50. The SDM is clocked at the PFD reference rate (f_{PFD}), which allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD.

With dither turned off, the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order modulator used in the ADF4196, the repeat length depends on the value of MOD, as shown in Table 8.

Table 8. Fractional Spurs with Dither Off

Condition (Dither Off)	Repeat Length	Spur Interval
MOD Is Divisible by 2 but Not by 3	2 × MOD	Channel step/2
MOD Is Divisible by 3 but Not by 2	3 × MOD	Channel step/3
MOD Is Divisible by 6	6 × MOD	Channel step/6
All Other Divisors	MOD	Channel step

With dither enabled, the repeat length is extended to 2^{21} cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. This can degrade the in-band phase noise at the PLL output by as much as 10 dB. Therefore, for lowest noise, dither off is a better choice, particularly when the final loop bandwidth is low enough to attenuate even the lowest frequency fractional spur. The wide loop bandwidth range that is available with the ADF4196 allows the use of dither in most applications.

Integer Boundary Spurs

Another mechanism for fractional spur creation involves interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (which is the purpose of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter and are more noticeable on channels that are close to integer multiples of the reference, where the difference frequency can be inside the loop bandwidth (thus, the name integer boundary spurs).

The 8:1 loop bandwidth switching ratio of the ADF4196 makes it possible to attenuate all spurs to sufficiently low levels for most applications. The final loop bandwidth can be chosen to ensure that all spurs are far enough out of band and meet the lock time requirements with the 8× bandwidth boost.

The programmable modulus and R divider of the ADF4196 can also be used to avoid integer boundary channels. This option is described in the Avoiding Integer Boundary Channels section.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is feedthrough of low levels of on-chip reference switching noise out of the $RF_{IN\pm}$ pins back to the VCO, resulting in reference spur levels as high as −90 dBc. These spurs can be suppressed below −110 dBc by inserting sufficient reverse isolation, for example, through an RF buffer between the VCO and $RF_{IN\pm}$ pins. Also, take care in the printed circuit board (PCB) layout to ensure that the VCO is well separated from the input reference to avoid a possible feedthrough path on the board.

POWER-UP INITIALIZATION

After applying power to the ADF4196 for the first time, a 14-step sequence is recommended, as described in Table 9.

The divider and timer settings used in the example in Table 9 are for a DCS1800 Tx synthesizer with a 104 MHz REF_{IN} frequency.

The ADF4196 powers up after Step 13 and locks to the programmed channel frequency after Step 14.

Table 9. Power-Up Initialization Sequence A and Initialization Sequence B

Step[1]	Register/ Bits	Hex Code	Description
1	R5 [7:0]	0xFD	Set all power-down bits.
2	R3 [15:0]	0x005B	PFD polarity = 1, ground CP_{OUT+}/CP_{OUT-}.
Wait 10 ms			Allow time for loop filter capacitors to discharge.
3	R7 [15:0]	0x0007	Clear test modes.
4	R6 [15:0]	0x000E	Initialize PLL modes, digital lock detect on MUX_{OUT}.
5A	R6 [15:0]	0x900E	10 ns lock detect threshold, digital lock detect on MUX_{OUT}.
5B	R6 [15:0]	0x000E	Add 16 PFD cycle delay after LE before starting hop to next frequency.
6	R4 [23:0]	0x004464	SW1/SW2 timer = 10.8 µs.
7	R4 [23:0]	0x00446C	SW3 timer = 10.8 µs.
8	R4 [23:0]	0x004394	I_{CP} timer = 8.6 µs.
9	R2 [15:0]	0x00D2	Phase = 26.
10	R1 [23:0]	0x520209	8/9 prescaler, doubler disabled, R = 4, toggle FF on, MOD = 65.
11	R0 [23:0]	0x480140	INT = 144, FRAC = 40 for 1880 MHz output frequency.
12	R3 [15:0]	0x007B	PFD polarity = 1, release CP_{OUT}+/CP_{OUT-}.
13	R5 [7:0]	0x05	Clear all power-down bits.
14	R0 [23:0]	0x480140	INT = 144, FRAC = 40 for 1880 MHz output frequency.

[1] Initialization Sequence A includes Step 5A and omits Step 5B; Initialization Sequence B includes Step 5B and omits Step 5A.

Two initialization sequences are available for the ADF4196: Initialization Sequence A and Initialization Sequence B. One or the other must be selected. Initialization Sequence A consists of Step 1 through Step 14 in Table 9, including Step 5A (but not Step 5B). (For Initialization Sequence B, Step 5A is replaced by Step 5B.) In Initialization Sequence A, the frequency hop starts immediately after the rising edge of LE, whereas in Initialization Sequence B, the ADF4196 waits 16 PFD cycles and then starts the hop. Initialization Sequence B reduces the overshoot of a frequency jump, but the start of a jump is delayed by 16 PFD cycles. Figure 36 shows this phenomenon.

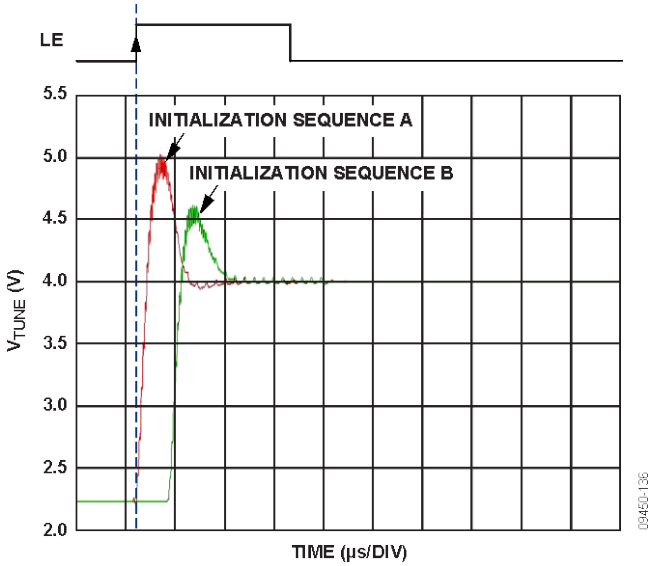


Figure 36. Frequency Jumps for Initialization Sequence A and Initialization Sequence B

CHANGING THE FREQUENCY OF THE PLL AND THE PHASE LOOKUP TABLE

After the ADF4196 is initialized, only a write to Register R0 is required to program a new output frequency. The N divider is updated with the values of INT and FRAC on the next PFD cycle following the LE edge that latches in the R0 word. However, the settling time and spurious performance of the synthesizer can be further optimized by modifying the R1 and R2 register settings on a channel-by-channel basis. These settings are double buffered by the write to R0. This means that, although the data is loaded through the serial interface on the respective R1 and R2 write cycles, the synthesizer is not updated with the new data until the next write to Register R0.

Register R2 can be used to digitally adjust the phase of the VCO output relative to the reference edge. The phase can be adjusted over the full 360° range at RF with a resolution of 360°/MOD. In most frequency synthesizer applications, the actual phase offset of the VCO output with respect to the reference is unknown and is irrelevant. In such applications, the phase adjustment capability of R2 can, instead, be used to optimize the settling time performance as described in the Phase Lookup Table section.

Phase Lookup Table

The fast lock sequence of the ADF4196 is initiated after the write to Register R0. The fast lock timers are programmed so that after the PLL has settled into wide bandwidth mode, the charge pump current is reduced and the loop filter resistor switches are opened, which reduces the loop bandwidth. The reference cycle on which these events occur is determined by the values that are preprogrammed into the timeout counters.

The phase locking plots of Figure 11 and Figure 14 show that the lock time to final phase is dominated by the phase swing that occurs when the bandwidth is reduced. When the PLL settles to its final frequency and phase, in wide bandwidth mode, this phase swing is the same regardless of the size of the frequency jump of the synthesizer. The amplitude of the phase swing is related to the current flowing through the loop filter resistors on the PFD reference cycle that open the SW1 and SW2 switches.

In an integer-N PLL, this current is zero when the PLL has settled. In a fractional-N PLL, the current is zero, on average, but it varies from one reference cycle to the next, depending on the quantization error sequence output from the digital Σ-Δ modulator. Because the Σ-Δ modulator is all digital logic, clocked at the PFD reference rate for a given value of MOD, the actual quantization error on any given reference cycle is determined by the value of FRAC and the phase word with which the modulator is seeded, following the write to R0.

By choosing an appropriate value of phase corresponding to the value of FRAC that is programmed on the next write to R0, the size of the error current when the SW1 and SW2 switches are opened can be minimized. Thus, the phase swing that occurs when the bandwidth is reduced can be minimized.

With dither off, the fractional spur pattern that is due to the quantization noise of the SDM also depends on the phase word with which the modulator is seeded. Tables of optimized FRAC and phase values for popular SW1/SW2 and I_{CP} timer settings can be downloaded from the ADF4196 product page. If using a phase table, first write the phase to double buffered Register R2, and then write the INT and FRAC values to Register R0.

Avoiding Integer Boundary Channels

When programming a new frequency, another option involves a write to Register R1 to avoid integer boundary spurs. If the integer boundary spur level is too high, the integer boundary can be moved away from the desired channel by reprogramming the R divider to select a different PFD frequency. For example, if REF_{IN} = 104 MHz and R = 4 for a 26 MHz PFD reference, and MOD = 130 for 200 kHz steps, the frequency channel at 910.2 MHz has a 200 kHz integer boundary spur because it is offset by 200 kHz from 35 × 26 MHz.

An alternative way to synthesize this channel is to set R = 5 for a 20.8 MHz PFD reference and MOD = 104 for 200 kHz steps. The 910.2 MHz channel becomes a 5 MHz offset from the nearest integer multiple of 20.8 MHz, and the 5 MHz beat note spurs are well attenuated by the loop. Setting the double buffered DB23 bit (Bit CP ADJ in Register R1) to 1 increases the charge pump current by 25%, which compensates for the 25% increase in N with the change to the 20.8 MHz PFD frequency. This maintains constant loop dynamics and settling time performance for jumps between the two PFD frequencies. Clear the CP ADJ bit when returning to 26 MHz-based channels.

The Register R1 settings that are required for integer boundary spur avoidance are all double buffered and do not become active on the chip until the next write to Register R0. Always ensure that Register R0 is the last register written to when programming a new frequency.

Serial Interface Activity

The serial interface activity when programming the R2 or R1 register causes no noticeable disturbance to the synthesizer's settled phase or degradation in its frequency spectrum. Thus, in a GSM application, serial interface activity can be performed during the active part of the data burst. Because it takes only 10.2 µs to program the three registers (R2, R1, and R0) with the 6.5 MHz serial interface clock rate typically used, this programming can also be performed during the previous guard period with the LE edge to latch in the R0 data, delayed until it is time to switch the frequency.

APPLICATIONS INFORMATION

LOCAL OSCILLATOR FOR A GSM BASE STATION

Figure 37 shows the ADF4196 being used with a VCO to produce the LO for a GSM1800 base station. For GSM, the REF_{IN} signal can be any integer multiple of 13 MHz, but the main requirement is that the slew rate be at least 300 V/µs. The 104 MHz, 5 dBm input sine wave shown in Figure 37 satisfies this requirement.

Recommended parameters for the various GSM/DCS/PCS synthesizers are listed in Table 10.

Table 10. Recommended Setup Parameters

	GSM900		DCS1800/PCS1900	
Parameter	**Tx**	**Rx**	**Tx**	**Rx**
Loop BW	60 kHz	40 kHz	60 kHz	40 kHz
PFD	13 MHz	26 MHz	13 MHz	13 MHz
MOD	65	130	65	65
Dither	Off	Off	Off	Off
Prescaler	4/5	4/5	8/9	8/9
I_{CP} Timer	28	78	28	38
SW1, SW2, SW3 Timers	35	85	35	45
VCO K_V	18 MHz/V	18 MHz/V	38 MHz/V	38 MHz/V

Loop Bandwidth and PFD Frequency

A 60 kHz loop bandwidth is narrow enough to attenuate the PLL phase noise and spurs to the required level for a Tx low. A 40 kHz bandwidth is necessary to meet the GSM900 Rx synthesizer's particularly tough phase noise and spur requirements at ±800 kHz offsets. To get the lowest spur levels at ±800 kHz offsets for Rx, the Σ-Δ modulator should be run at the highest over-sampling rate possible. Therefore, for GSM900 Rx, a 26 MHz PFD frequency is chosen, and MOD = 130 is required for 200 kHz steps. Because this value of MOD is divisible by two, certain FRAC channels have a 100 kHz fractional spur. This is attenuated by the 40 kHz loop filter and, therefore, is not a concern. However, the 60 kHz loop filter that is recommended for Tx has a closed-loop response that peaks close to 100 kHz. Therefore, a 13 MHz PFD with MOD = 65, which avoids the 100 kHz spur, is the best choice for a Tx synthesizer.

Dither

Dither off should be selected for the lowest rms phase error.

Prescaler

The 8/9 prescaler should be selected for the DCS and PCS bands. The 4/5 prescaler allows an N divider range low enough to cover the GSM900 Tx and Rx bands with either a 13 MHz or 26 MHz PFD frequency.

Timer Values for Tx

To comply with the GSM spectrum due to switching requirements, the Tx synthesizer should not switch frequency until the PA output power has ramped down by at least 50 dB. If it takes 10 µs to ramp down to this level, only the last 20 µs of the 30 µs guard period is available for the Tx synthesizer to lock to final frequency and phase.

In fast lock mode, the Tx loop bandwidth is widened by a factor of 8 to 480 kHz and, therefore, the PLL achieves frequency lock for a jump across the entire band in <6 µs. After this, the PA power can start to ramp up again, and the loop bandwidth can be restored to the final value. With the I_{CP} timer = 28, the charge pump current reduction begins at ~8.6 µs. When the SW1, SW2, and SW3 timers = 35, the current reaches its final value before the loop filter switches open at ~10.8 µs.

With these timer values, the phase disturbance created when the bandwidth is reduced settles back to its final value by 20 µs, in time for the start of the active part of the GSM burst. If faster phase settling is desired with the 60 kHz bandwidth setting, the timer values can be reduced further but should not be brought less than the 6 µs that is required to achieve frequency lock in wide bandwidth mode.

Timer Values for Rx

The 40 kHz Rx loop bandwidth is increased by a factor of 8 to approximately 320 kHz during fast lock. With the Rx timer values shown in Table 10, the bandwidth is reduced after ~12 µs, which allows sufficient time for the phase disturbance to settle back before the start of the active part of the Rx time slot at 30 µs. As in the Tx synthesizer case, faster Rx settling can be achieved by reducing these timer values, their lower limit being determined by the time it takes to achieve frequency lock in wide bandwidth mode. In addition, the DCS and PCS Rx synthesizers have relaxed 800 kHz blocker specifications and, thus, can tolerate a wider loop bandwidth, which allows correspondingly faster settling.

VCO K_V

In general, the VCO gain, K_V, should be set as low as possible to minimize the reference and integer boundary spur levels that arise due to feedthrough mechanisms. When deciding on the optimum VCO K_V, a good choice is to allow 2 V to tune across the desired band, centered on the available tuning range. With V_P3 regulated to 5.5 V ± 100 mV, the tuning range available is 2.8 V.

Loop Filter Components

For good settling performance, it is important that capacitors with low dielectric absorption be used in the loop filter. Ceramic NPO C0G capacitors are a good choice for this application. A 2% tolerance is recommended for loop filter capacitors and 1% for resistors. A 10% tolerance is adequate for the inductor, L1.

ADIsimPLL Support

The ADF4193 loop filter design is supported on ADIsimPLL v2.7 or later. Example files for popular applications are available for download from the ADF4193 and ADF4196 product pages.

Also available is a technical note (ADF4193-TN-001, *ADF4193 Loop Filter Design Using ADIsimPLL*) that outlines a loop filter design procedure that takes full advantage of the new degree of freedom in the filter design that the differential amplifier and loop filter switches provide.

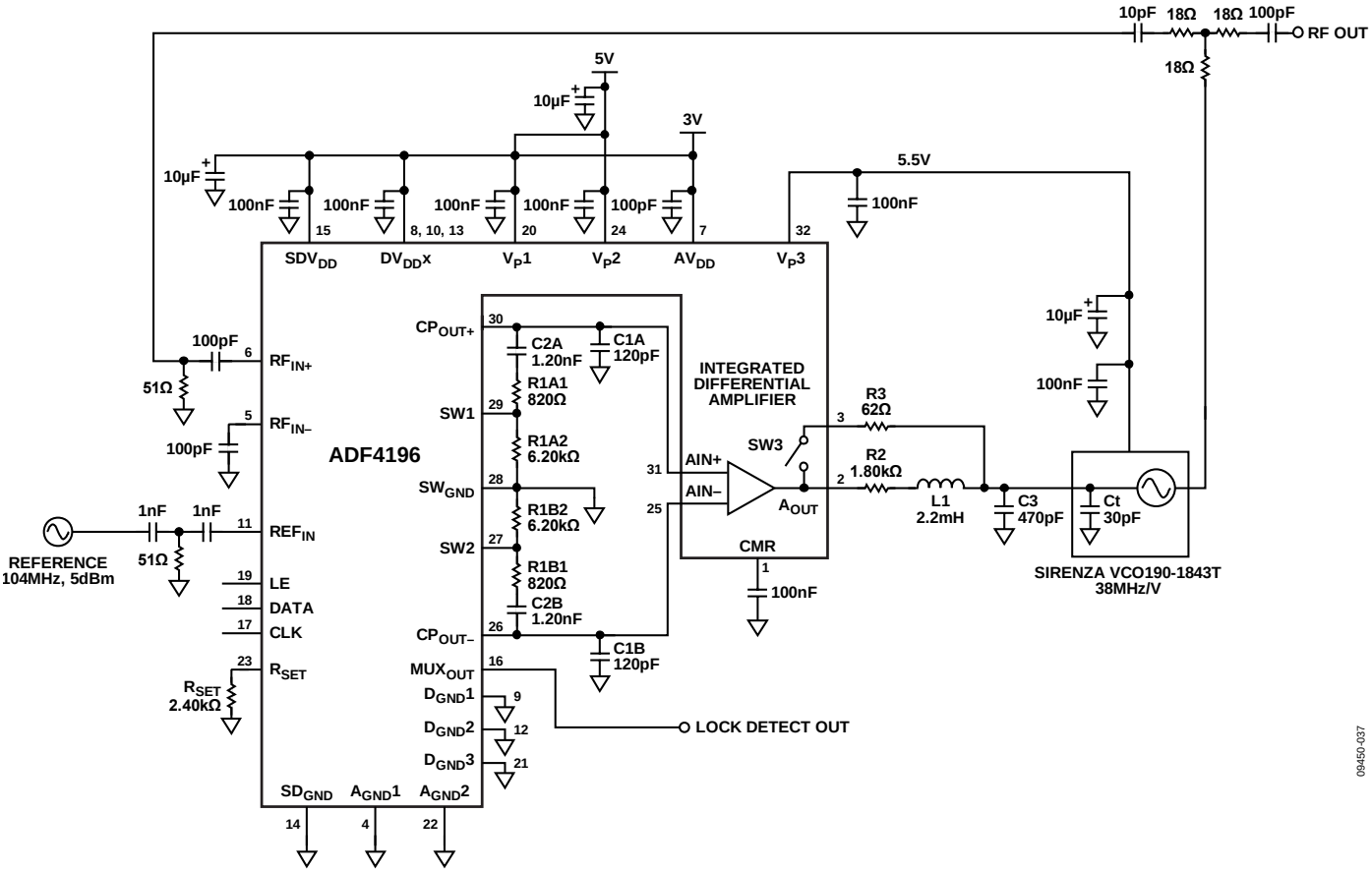


Figure 37. LO for DCS1800 Tx Using the ADF4196

INTERFACING

The ADF4196 has a simple SPI-compatible serial interface for writing to the device. The CLK, DATA, and LE pins control the data transfer. When LE goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are latched into the appropriate register. See Figure 2 for the timing diagram and Table 6 for the register address table.

The maximum allowable serial clock rate is 33 MHz.

Analog Microcontroller Interface

Figure 38 shows the interface between the ADF4196 and the following analog microcontrollers: the ADuC7019, ADuC7020, ADuC7021, ADuC7022, ADuC7023, ADuC7024, ADuC7025, ADuC7027, ADuC7028, ADuC7029, ADuC7033, ADuC7034, ADuC7036, ADuC7039, ADuc7060, and ADuC7061. (These microcontrollers are represented by the ADuC7019 in Figure 38.) These analog microcontrollers are based on an ARM7™ core, although the same interface can be used with any 8051-based microcontroller. The microcontroller is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4196 needs a 24-bit word. This is achieved by writing three 8-bit bytes from the microcontroller to the device. When the third byte is written, bring the LE input high to complete the transfer.

When power is first applied to the ADF4196, an initialization sequence is required for the output to become active (see Table 9).

I/O port lines on the microcontroller are also used to detect lock (MUX_{OUT} configured as lock detect and polled by the port input).

When operating in the SPI master mode, the maximum SPI transfer rate of the ADuC7023, for example, is 20 Mbps. This means that the maximum rate at which the output frequency can be changed is 833 kHz. If using a faster SPI clock, ensure adherence to the SPI timing requirements that are listed in Table 2.

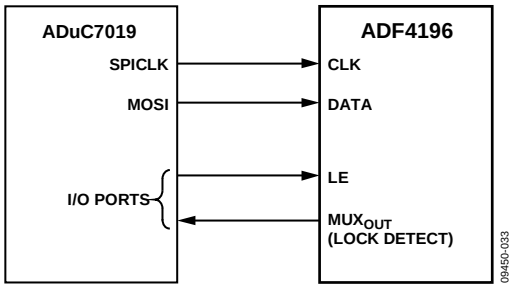


Figure 38. ADuC7019-to-ADF4196 Interface

Blackfin ADSP-BF527 Interface

Figure 39 shows the interface between the ADF4196 and the Blackfin® ADSP-BF527 digital signal processor (DSP). The ADF4196 needs a 24-bit serial word for each latch write. The easiest way to accomplish this, when using the Blackfin family, is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

Set up the word length for eight bits, and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer. Ensure that the clock speeds are within the maximum limits that are outlined in Table 2.

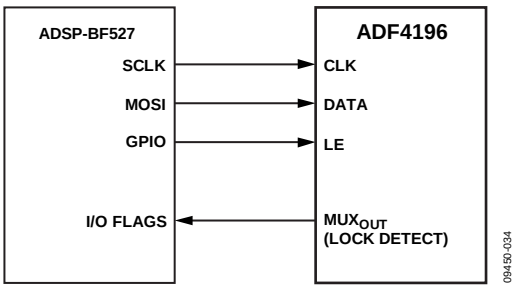


Figure 39. ADSP-BF527-to-ADF4196 Interface

PCB DESIGN GUIDELINES

The lands on the chip scale package (CP-32-7) are rectangular. The printed circuit board (PCB) pad for these lands should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. To ensure that the solder joint size is maximized, center the land on the pad.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the PCB should be at least as large as the exposed pad. To avoid shorting, provide a clearance on the PCB of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern.

Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, incorporate them into the thermal pad at a 1.2 mm pitch grid. Provide a via diameter between 0.3 mm and 0.33 mm, and plate the via barrel with 1 oz copper to plug the via. Connect the PCB thermal pad to $A_{GND}1$ or $A_{GND}2$.

OUTLINE DIMENSIONS

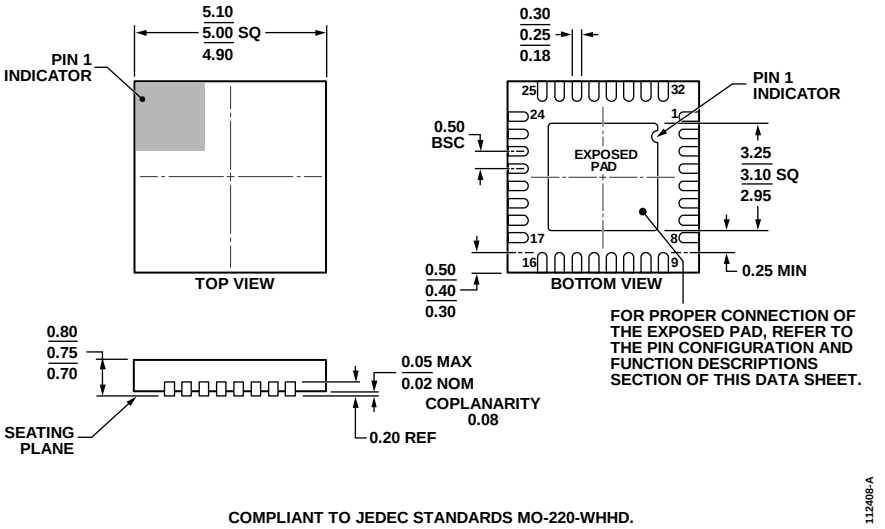


Figure 40. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4196BCPZ	−40°C to +85°C	32-Lead LFCSP_WQ	CP-32-7
ADF4196BCPZ-RL7	−40°C to +85°C	32-Lead LFCSP_WQ	CP-32-7
EV-ADF4196SD1Z		Evaluation Board (No VCO or Loop Filter)	

[1] Z = RoHS Compliant Part.

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