# HMC625HFLP5E

v00.0311

## 0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 0.5 - 6 GHz

### Typical Applications

The HMC625HFLP5E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

### Features

-13.5 to +18 Gain Control in 0.5 dB Steps

Power-up State Selection

High Output IP3: +33 dBm

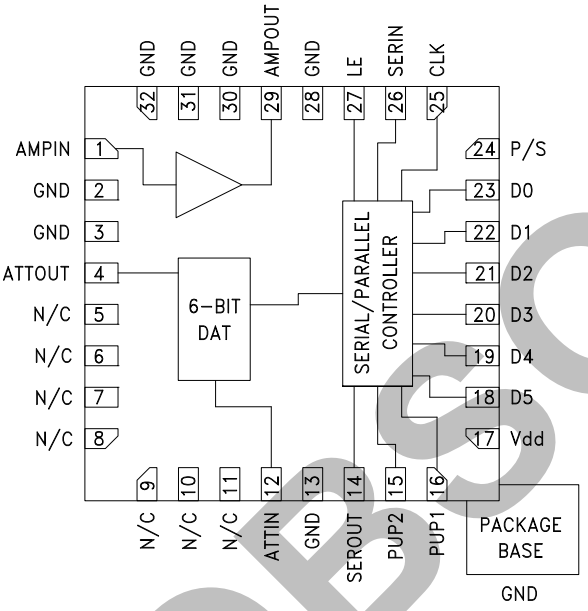
TTL/CMOS Compatible
Serial, Parallel, or latched Parallel Control

±0.25 dB Typical Gain Step Error

Single +5V Supply

32 Lead 5 x 5 mm SMT Package: 25 $mm^2$

### Functional Diagram




### General Description

The HMC625HFLP5E is a digitally controlled variable gain amplifier which operates from 0.5 - 6 GHz, and can be programmed to provide anywhere from 13.5 dB attenuation, to 18 dB of gain, in 0.5 dB steps. The HMC625HFLP5E delivers noise figure of 6 dB in its maximum gain state, with output IP3 of up to +33 dBm in any state. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 6 bit parallel word. The HMC625HFLP5E also features a user selectable power up state and a serial output port for cascading other Hittite serial controlled components. The HMC625HFLP5E is housed in a RoHS compliant 5 x 5 mm QFN leadless package, and requires no external matching components.

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### Electrical Specifications, $T_A$ = +25 °C, 50 Ohm System Vdd = +5V, Vs = +5V

| Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Frequency Range | | 500 - 2700 | | | 2700 - 4000 | | | 4000 - 6000 | | MHz |
| Gain (Maximum Gain State) | 13 | 18 | | 11 | 14 | | 5 | 10 | | dB |
| Gain Control Range | | 31.5 | | | 31.5 | | | 31.5 | | dB |
| Input Return Loss | | 15 | | | 12 | | | 10 | | dB |
| Output Return Loss | | 12 | | | 12 | | | 14 | | dB |
| Gain Accuracy: (Referenced to Maximum Gain State) All Gain States | | ± (0.3 + 3% of relative gain setting) Max | | | ± (0.3 + 3% of relative gain setting) Max | | | ± (0.4 + 5% of relative gain setting) Max | | dB |
| Output Power for 1 dB Compression | 16 | 19 | | 14 | 17 | | 11 | 14 | | dBm |
| Output Third Order Intercept Point (Two-Tone Output Power= 12 dBm Each Tone) | | 33 | | | 29 | | | 27 | | dBm |
| Noise Figure (Max Gain State) | | 6 | | | 7 | | | 8 | | dB |
| Switching Characteristics tRISE, tFall (10 / 90% RF) | | 30 | | | 30 | | | 30 | | ns |
| tON, tOFF (Latch Enable to 10 / 90% RF) | | 60 | | | 60 | | | 60 | | ns |
| Supply Current (Amplifier) | 60 | 86 | 100 | 60 | 86 | 100 | 60 | 86 | 100 | mA |
| Supply Current (Controller) Idd | | 0.12 | 0.25 | | 0.12 | 0.25 | | 0.12 | 0.25 | mA |

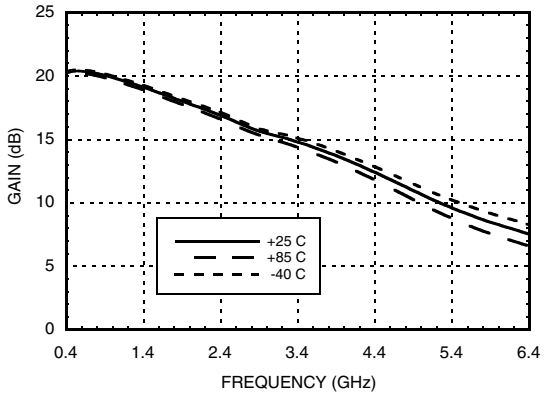
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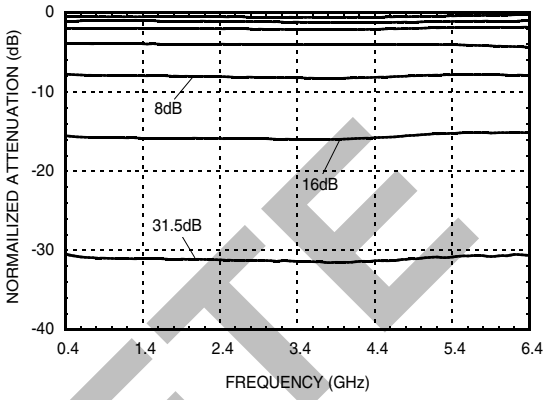
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### Maximum Gain vs. Frequency



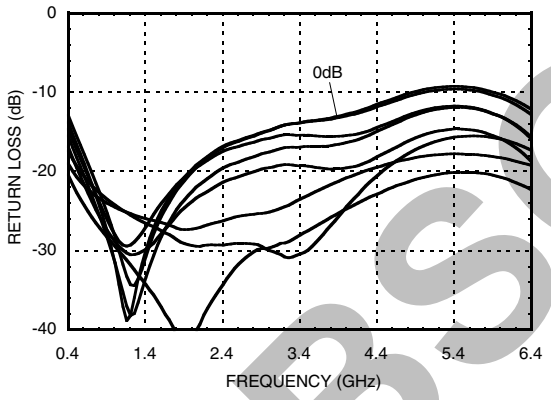

### Normalized Attenuation

*(Only Major States are Shown)*



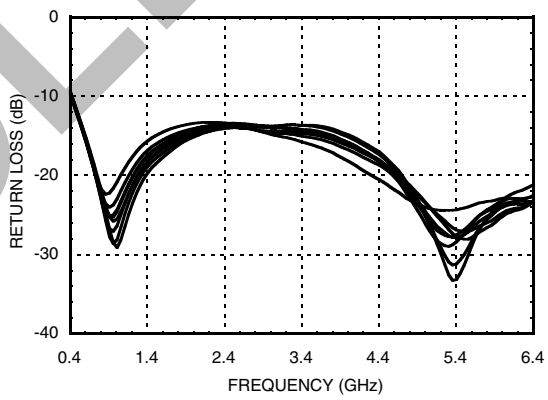

### Input Return Loss

*(Only Major States are Shown)*



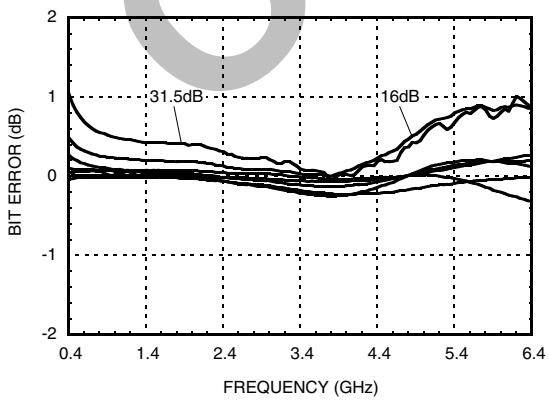

### Output Return Loss

*(Only Major States are Shown)*

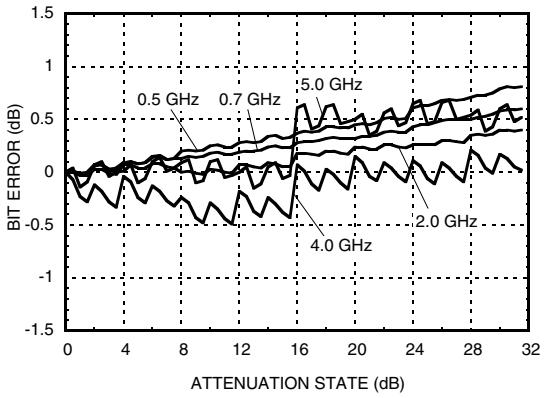



### Bit Error vs. Frequency

*(Only Major States are Shown)*




### Bit Error vs. Attenuation State




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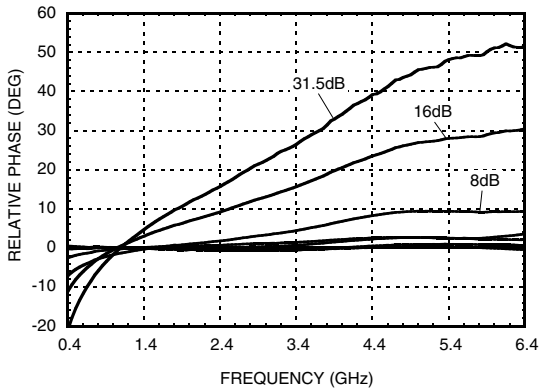
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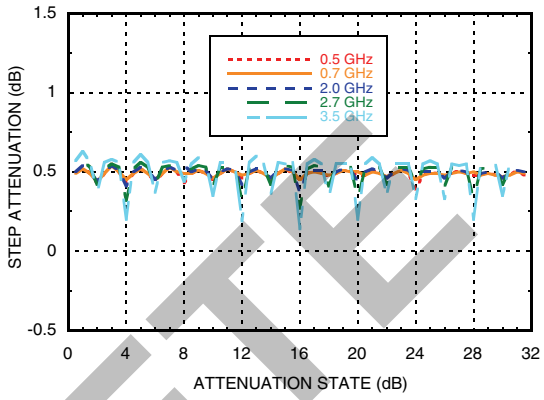
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### Normal Relative Phase vs. Frequency

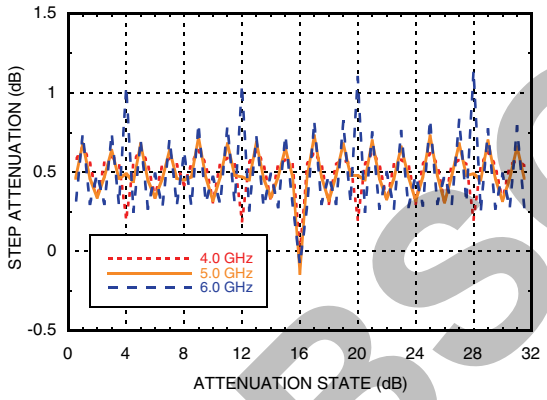
*(Only Major States are Shown)*



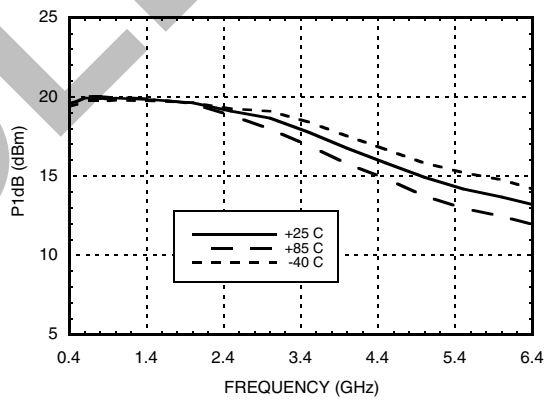

### Step Attenuation vs. Attenuation State, 0.5 - 3.5 GHz



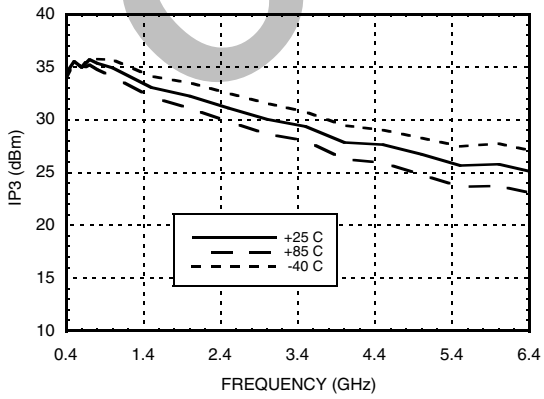

### Step Attenuation vs. Attenuation State, 4.0 - 6.0 GHz



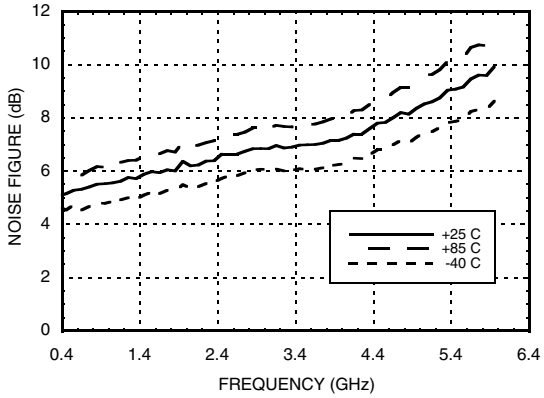

### Output P1dB vs. Temperature




### Output IP3 vs. Temperature




### Noise Figure




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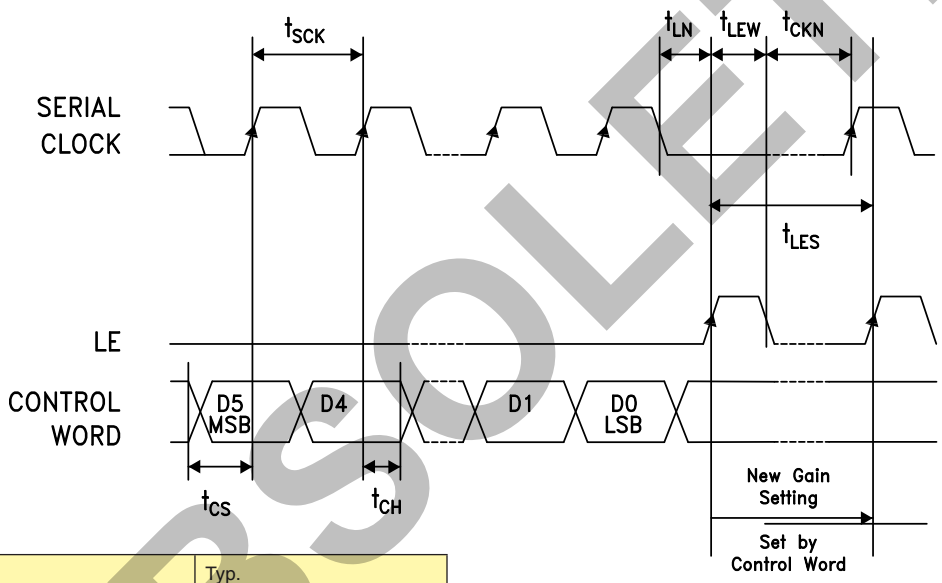


## Serial Control Interface

The HMC625HFLP5E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

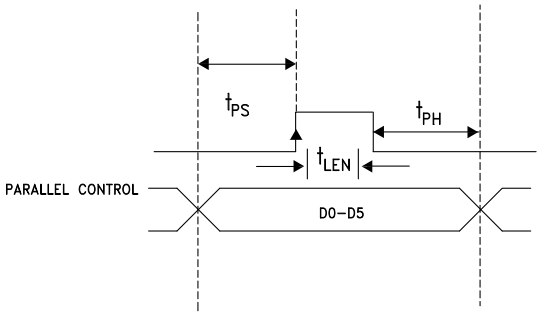
When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and serial input register is loaded asynchronously with parallel digital inputs (D0 - D5). When LE is high, 6-bit parallel data is transferred to the attenuator.

For all modes of operations, the DVGA state will stay constant while LE is kept low.




**Timing Diagram** *(Latched Parallel Mode)*

| Parameter | Typ. |
|---|---|
| Min. serial period, $t_{SCK}$ | 100 ns |
| Control set-up time, $t_{CS}$ | 20 ns |
| Control hold-time, $t_{CH}$ | 20 ns |
| LE setup-time, $t_{LN}$ | 10 ns |
| Min. LE pulse width, $t_{LEW}$ | 10 ns |
| Min LE pulse spacing, $t_{LES}$ | 630 ns |
| Serial clock hold-time from LE, $t_{CKN}$ | 10 ns |
| Hold Time $t_{PH}$ | 0 ns |
| Latch Enable Minimum width, $t_{LEN}$ | 10 ns |
| Setup Time, $t_{PS}$ | 2 ns |




## Parallel Mode *(Direct Parallel Mode & Latched Parallel Mode)*

**Note:** The parallel mode is enabled when P/S is set to low.

**Direct Parallel Mode** - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

**Latched Parallel Mode** - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

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## Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table. The DVGA latches in the desired power-up state approximately 200 ms after power-up.

## Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

## Absolute Maximum Ratings

| | |
|---|---|
| RF Input Power [1] | 11.5 dBm (T = 85 °C) |
| Digital Inputs (LE, SERIN, CLK, P/S, DO-D5, PUP1, PUP2) | -0.5 to Vdd +0.5V |
| Controller Bias Voltage (Vdd) | 5.6V |
| Amplifier Bias Voltage (Vcc) | 5.5V |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T = 85 °C) (derate 15.1 mW/°C above 85 °C) [1] | 0.98 W |
| Thermal Resistance | 66.3 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |

[1] At max gain settling

## Bias Voltage

| Vdd (V) | Idd (Typ.) (mA) |
|---|---|
| 5V | 0.12 |
| Vs (V) | Is (Typ.) (mA) |
| 5V | 86 |

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## PUP Truth Table

| LE | PUP1 | PUP2 | Gain Relative to Maximum Gain |
|---|---|---|---|
| 0 | 0 | 0 | -31.5 |
| 0 | 1 | 0 | -24 |
| 0 | 0 | 1 | -16 |
| 0 | 1 | 1 | Insertion Loss |
| 1 | X | X | 0 to -31.5 dB |

Note: The logic state of D0 - D5 determines the power-up state per truth table shown below when LE is high at power-up.

## Truth Table

| Control Voltage Input | | | | | | Gain Relative to Maximum Gain |
|---|---|---|---|---|---|---|
| D5 | D4 | D3 | D2 | D1 | D0 | |
| High | High | High | High | High | High | 0 dB |
| High | High | High | High | High | Low | -0.5 dB |
| High | High | High | High | Low | High | -1 dB |
| High | High | High | Low | High | High | -2 dB |
| High | High | Low | High | High | High | -4 dB |
| High | Low | High | High | High | High | -8 dB |
| Low | High | High | High | High | High | -16 dB |
| Low | Low | Low | Low | Low | Low | -31.5 dB |
| Any combination of the above states will provide a reduction in gain approximately equal to the sum of the bits selected. | | | | | | |

## Control Voltage Table

| State | Vdd = +3V | Vdd = +5V |
|---|---|---|
| Low | 0 to 0.5V @ <1 µA | 0 to 0.8V @ <1 µA |
| High | 2 to 3V @ <1 µA | 2 to 5V @ <1 µA |

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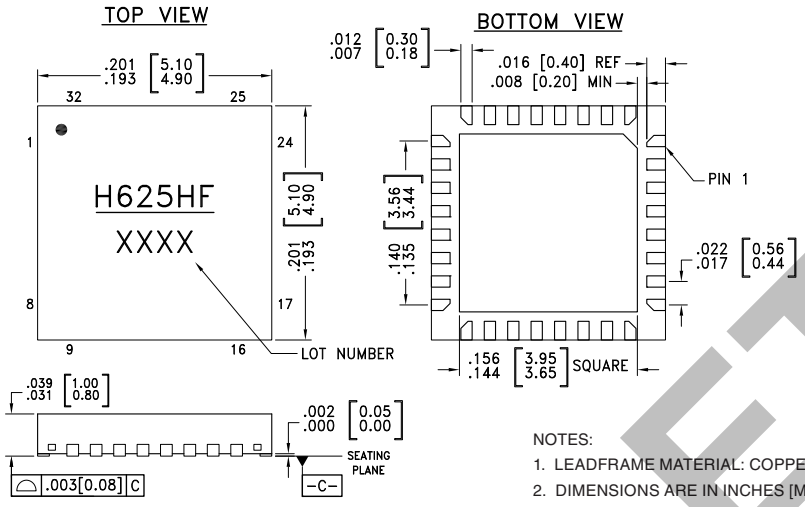
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## Outline Drawing




NOTES:

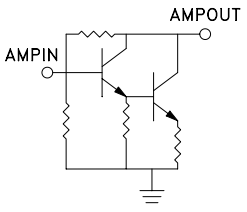
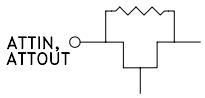
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15 mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05 mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

## Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [2] |
|---|---|---|---|---|
| HMC625HFLP5E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [1] | H625HF<br>XXXX |

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1 | AMPIN | This pin is DC coupled.<br>An off chip DC blocking capacitor is required. |  |
| 29 | AMPOUT | RF output and DC bias (Vcc) for the output stage of the amplifier. | |
| 2, 3, 13, 28, 30 - 32 | GND | These pins and package bottom must be connected to RF/DC ground. |  |
| 4, 12 | ATTIN, ATTOUT | These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation. |  |

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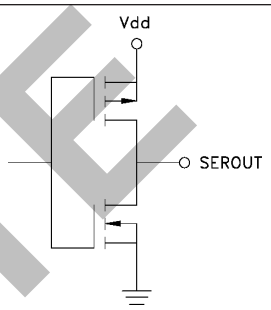
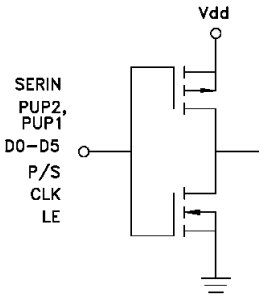
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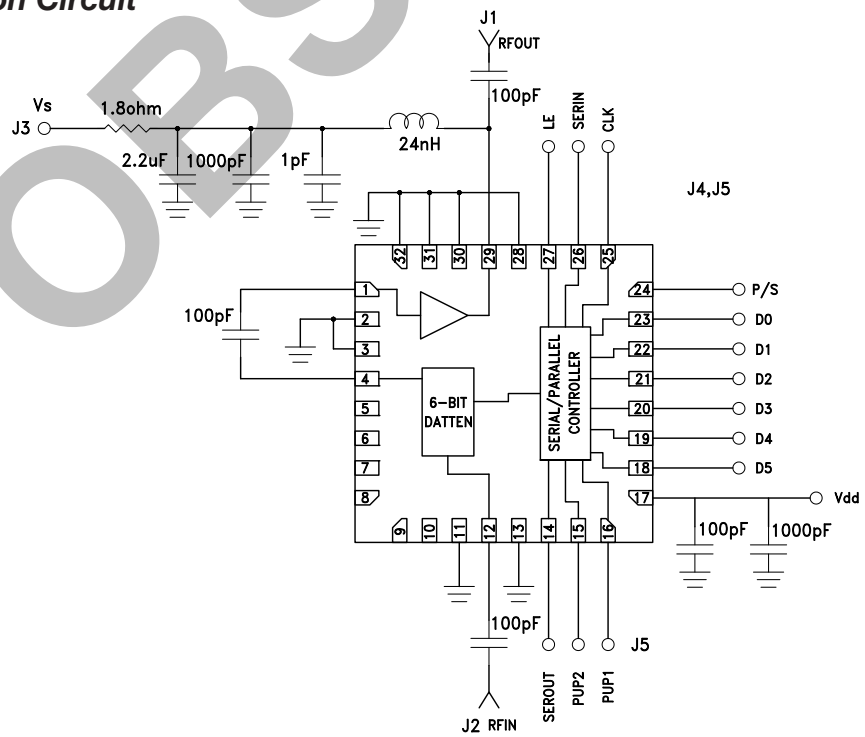
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## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 5-11 | N/C | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 14 | SEROUT | Serial input data delayed by 6 clock cycles. |   |
| 15, 16 | PUP2, PUP1 | |   |
| 18 - 23 | D5, D4, D3, D2, D1, D0 | | |
| 24 | P/S | | |
| 25 | CLK | | |
| 26 | SERIN | | |
| 27 | LE | | |
| 17 | Vdd | Supply Voltage | |

## Application Circuit




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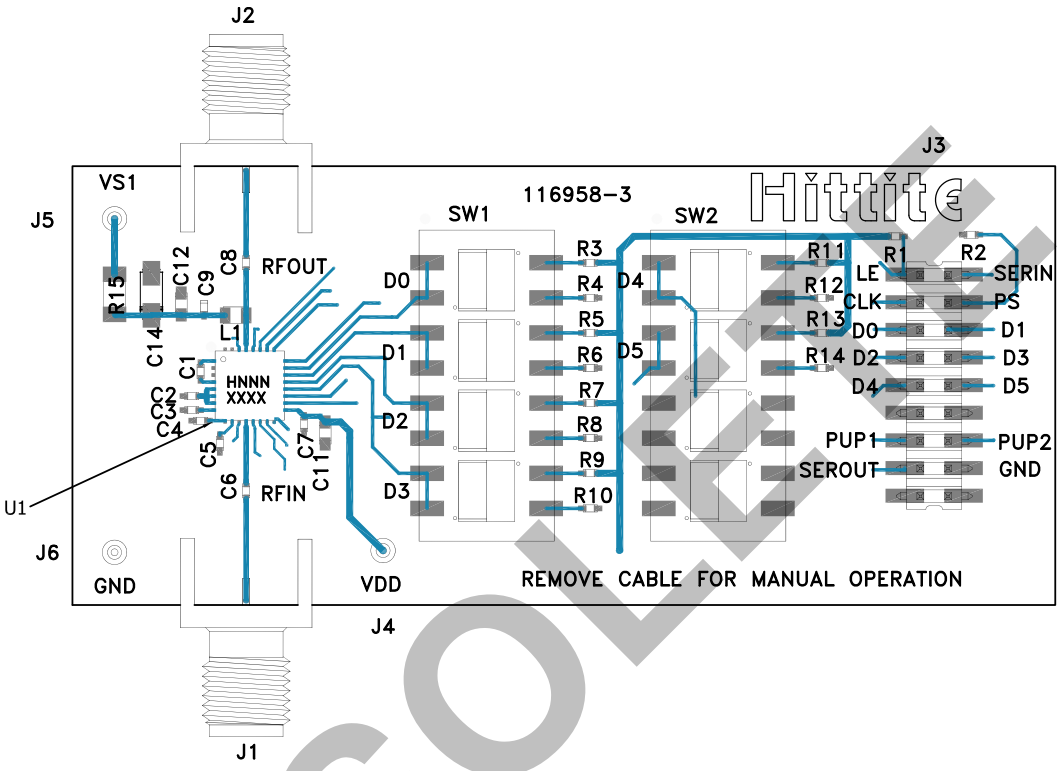
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## Evaluation PCB




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## List of Materials for Evaluation PCB 116960 [1]

| Item | Description |
|---|---|
| J1 - J2 | PCB Mount SMA Connector |
| J3 | 18 Pin DC Connector |
| J4 - J6 | DC Pin |
| C1 - C9 | 100 pF Capacitor, 0402 Pkg. |
| C11 - C12 | 1000 pF Capacitor, 0402 Pkg. |
| C14 | 2.2 µF Capacitor, CASE A Pkg. |
| R1 - R14 | 100 kOhm Resistor, 0402 Pkg. |
| R15 | 1.8 Ohm Resistor, 1206 Pkg. |
| SW1, SW2 | SPDT 4 Position DIP Switch |
| L1 | 24 nH Inductor, 0603 Pkg. |
| U1 | HMC625HFLP5E Variable Gain Amplifier |
| PCB [2] | 116958 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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