TPS63036 High-Efficiency Buck-Boost Converter in Tiny Wafer Chip Scale Package

1 Features

- Input voltage range: 1.8 V to 5.5 V (>2 V for device start-up)
- Adjustable output voltage range: 1.2 V to 5.5 V
- High efficiency over the entire load range
  - Operating quiescent current: 25 µA
  - Power save mode with seamless transition
- Average current mode buck-boost architecture
  - Automatic transition between modes
  - Fixed frequency operation at 2.4 MHz
  - Synchronization to external clock possible
- Safety and robust operation features
  - Overtemperature, overvoltage protection
  - Load disconnect during shutdown
- Tiny 8-pin wafer chip scale package (WCSP): 1.814 mm × 1.076 mm

2 Applications

- Battery voltage regulation (headsets and earbuds, cameras, augmented reality glasses, electronic and robotic toys, personal medical products)
- Wi-Fi® or Bluetooth® module supply (IP network camera, wireless access point, single board computer, portable POS, wireless sensors)
- LED/Laser supply (barcode scanner, laser distance meter)

3 Description

The TPS63036 is a non-inverting buck-boost converter able to provide a regulated output voltage from an input supply that can be higher or lower than the output voltage. The buck-boost converter is based on a fixed frequency, pulse width modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters power save mode to maintain high efficiency over a wide load current range. The power save mode can be disabled, forcing the converter to operate at a fixed switching frequency.

The maximum average current in the switches is limited to a typical value of 1000 mA. The output voltage is programmable using an external resistor divider.

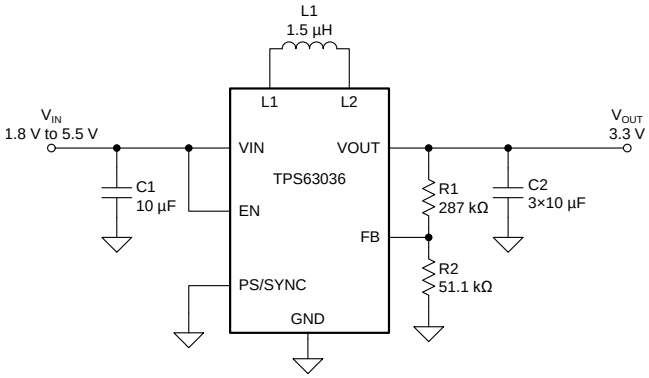
The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the supply.

Device Information(1)

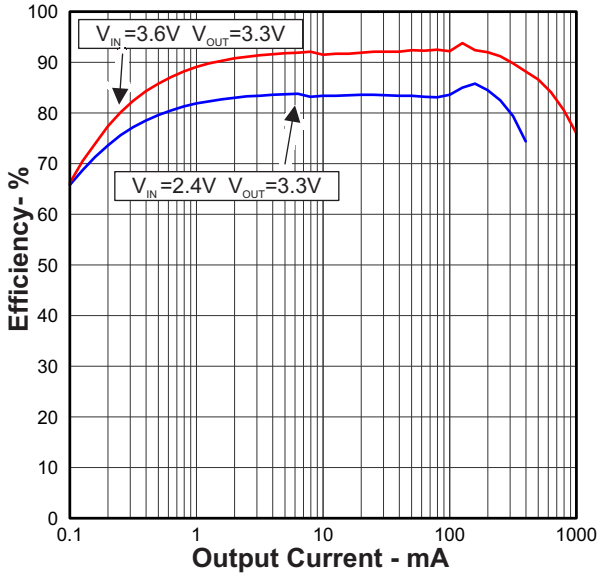
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63036	WCSP (8)	1.814 mm × 1.076 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2015) to Revision B — **Page**

- Updated *Features* and *Applications* ... 1
- Corrected the body size in *Features* and the *Device Information* table ... 1
- Corrected efficiency graph ... 1
- Removed hints to fixed output voltage versions (for example, in the *Pin Functions* table) ... 3

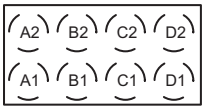
Changes from Original (August 2012) to Revision A — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Available Output Voltage Options* table ... 3
- Removed *Packaging Information* section ... 17

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5 Pin Configuration and Functions

YFG Package
8-Pin WCSP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	A2	Input	Enable input (1 enabled, 0 disabled)
FB	D2	Input	Voltage feedback pin
GND	C2	—	Control/logic ground
PS/SYNC	B2	Input	Enable/disable power-save mode (1 disabled, 0 enabled, clock signal for synchronization)
L1	B1	Input	Connection for inductor
L2	C1	Input	Connection for inductor
VIN	A1	Input	Supply voltage for power stage
VOUT	D1	Output	Buck-boost converter output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage on VIN, L1, L2, VOUT, PS/SYNC, EN, FB	–0.3	7	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage at VIN	1.8	5.5	V
Operating free air temperature, T_A	–40	85	°C
Operating virtual junction temperature, T_J	–40	125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS63036 YFG (WCSP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.8[1]		5.5	V
V_{OUT}	Output voltage range			1.2		5.5	V
	Duty cycle in step-down conversion			20%			
V_{FB}	Feedback voltage		PS/SYNC = VIN I_{OUT} < 5 mA	495	500	505	mV
V_{FB}	Feedback voltage		PS/SYNC = GND referenced to 500 mV I_{OUT} < 5 mA	-3%		+6%	
	Load regulation		PS/SYNC = GND		0.008		%/mA
f	Oscillator frequency			1800	2000	2200	kHz
	Frequency range for synchronization			2200	2400	2600	kHz
I_{SW}	Average input current limit		V_{IN} = 3.6 V, T_A = 25°C[2]		1000		mA
	High-side switch ON-resistance		V_{IN} = 3.6 V		200		mΩ
	Low-side switch ON-resistance		V_{IN} = 3.6 V		200		mΩ
	Line regulation				0.5%		
I_q	Quiescent current	VIN	I_{OUT}= 0 mA, V_{EN} = V_{IN} = 3.6 V, V_{OUT} = 3.3 V		25	35	µA
		VOUT			4	6	µA
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = 3.6 V		0.1	0.9	µA
CONTROL STAGE							
V_{UVLO}	Undervoltage lockout threshold falling			1.4	1.5	1.6	V
	Undervoltage lockout threshold raising			1.6	1.8	2.0	V
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped on GND or VIN		0.01	0.1	µA
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

(1) The typical required supply voltage for start-up is 2 V. The part is functional down to 1.8 V.
(2) For the minimum specified average input current limit at V_{OUT} = 2.5 V, 3.3 V and 4.5 V refer to curve in Figure 1. For the maximum specified average input current limit at V_{OUT} = 2.5 V, 3.3 V and 4.5 V refer to curve in Figure 2.

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6.6 Typical Characteristics

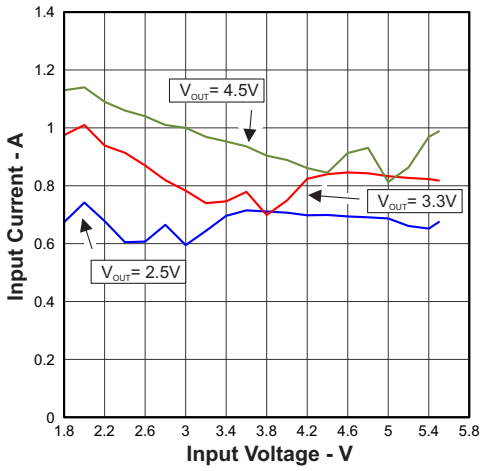


Figure 1. Minimum Input Current vs Input Voltage

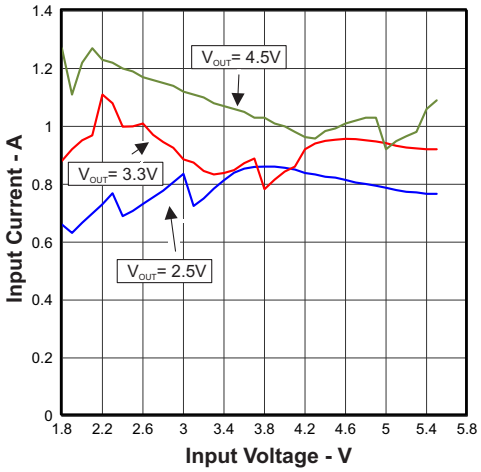


Figure 2. Maximum Input Current vs Input Voltage

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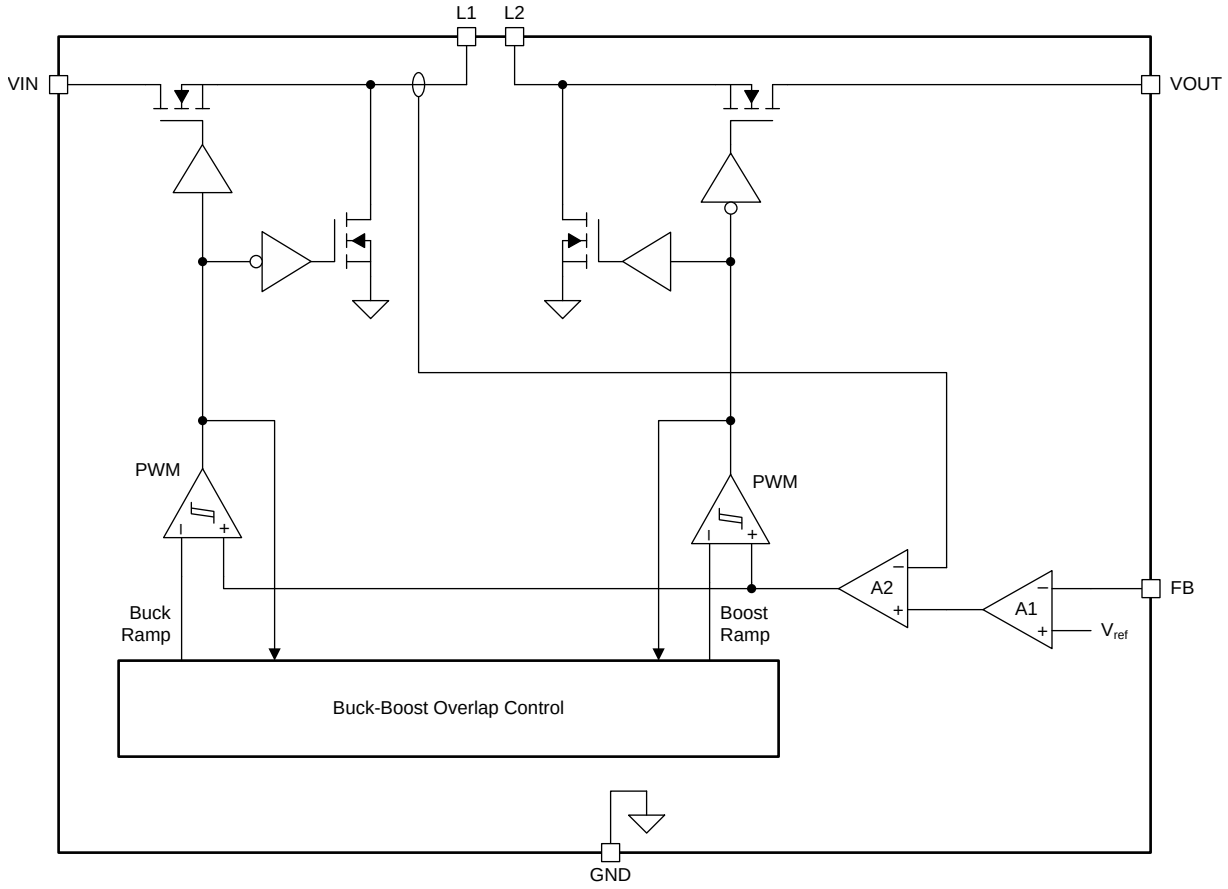
7 Detailed Description

7.1 Overview

The controller circuit of the device is based on an average current mode topology. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. A resistive voltage divider must be connected to that pin. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter. To protect the device from overheating an internal temperature sensor is implemented.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

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Feature Description (continued)

7.3.2 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. In case it reaches the overvoltage threshold the voltage amplifier regulates the output voltage to this value.

7.3.3 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage at VIN is lower than approximately its threshold (see *Electrical Characteristics* table). When in operation, the device automatically enters the shutdown mode if the voltage at VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

7.3.4 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see *Electrical Characteristics* table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

7.4 Device Functional Modes

7.4.1 Soft-Start and Short Circuit Protection

After being enabled, the device starts operating. The average input current limit ramps up from an initial 400 mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will also not increase. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. At a short on the output during operation, the current limit also is decreased accordingly.

7.4.2 Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from step-down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. For the remaining 2 switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

7.4.3 Control Loop

The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 3 shows the control loop.

The noninverting input of the trans-conductance amplifier Gmv can be assumed to be constant. The output of Gmv defines the average inductor current. The inductor current is reconstructed measuring the current through the high-side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the ON-time of the same MOSFET. During the OFF-time the current is reconstructed internally starting from the peak value reached at the end of the ON-time cycle. The average current is then compared to the desired value and the difference, or current error, is amplified and compared to the sawtooth ramp of either the buck or the boost.

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Device Functional Modes (continued)

The Buck-Boost Overlap Control makes sure that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Thanks to this block whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other, on the other hand when there is no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result the number of classical buck-boost cycles or no switching is reduced to a minimum and high-efficiency values have been achieved.

Slope compensation is not required to avoid subharmonic oscillation which are otherwise observed when working with peak current mode control with D > 0.5.

Nevertheless the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This purpose is reached limiting the gain of the current amplifier.

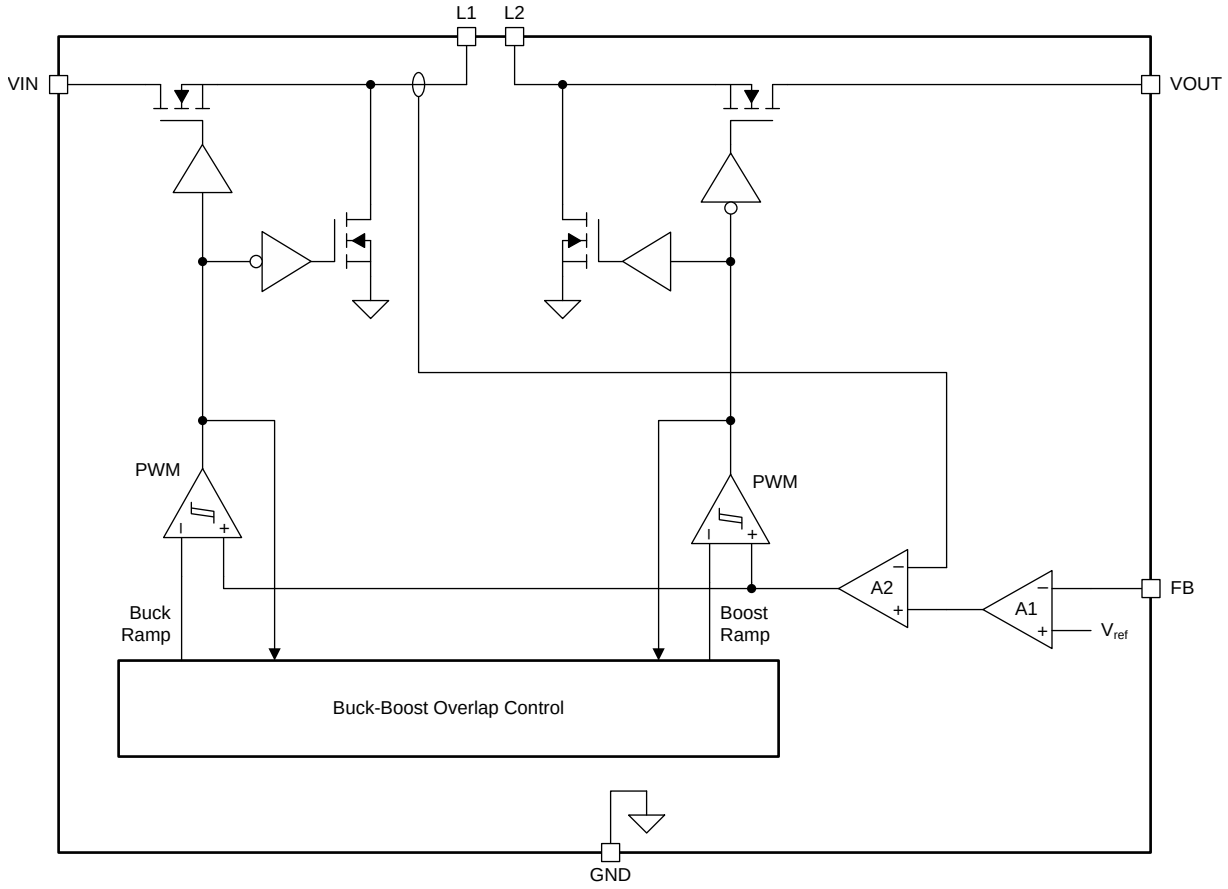


Figure 3. Average Current Mode Control

7.4.4 Power-Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. Power-save mode is used to improve efficiency at light load. To enable power-save mode, PS/SYNC must be set low. If PS/SYNC is set low then power-save mode is entered when the average inductor current gets lower than about 100 mA. At this point the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

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Device Functional Modes (continued)

During the power-save mode, the output voltage is monitored with a comparator by the threshold comp low and comp high. When the device enters power-save mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comp low threshold, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last one or several pulses. The converter continues these pulses until the comp high threshold is reached and the average inductance current gets lower than about 100 mA. When the load increases above the minimum forced inductor current of about 100 mA, the device will automatically switch to PWM mode.

The power-save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a phase-locked loop (PLL), so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS63036 device is a noninverting buck-boost converter that is suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. The device supports regulated output voltages from 1.2 V to 5.5 V.

8.2 Typical Application

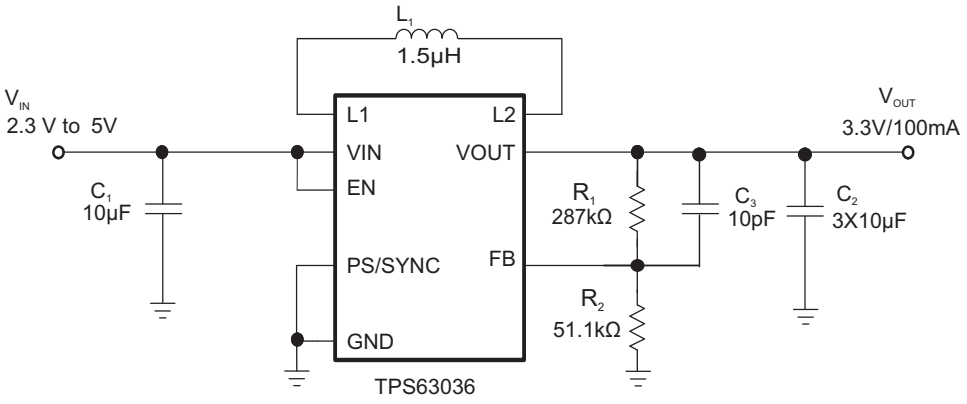


Figure 4. Typical Operating Circuit

8.2.1 Design Requirements

The design guidelines provide a component selection to operate the adjustable device within the *Recommended Operating Conditions*.

8.2.2 Detailed Design Procedure

The design guideline provides a component selection to operate the device within the recommended operating conditions.

Table 1 shows the list of components for the *Application Curves*.

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63036	Texas Instruments
L1	1.5 µH, 3 mm x 3 mm x 1.5 mm	Coilcraft, LPS3015-152MLC
C1	10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME84D, Murata
C2	3 × 10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME84D, Murata
R1, R2	Depending on the output voltage at TPS63036	

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The TPS63036 buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected to work with the internal compensation. As a general rule of thumb, the product L × C should not move over a wide range when selecting a different output filter. However, when selecting the output filter a low limit for the inductor value exists to avoid sub-harmonic oscillation which could be caused by a far too fast ramp up of the amplified inductor current. For the TPS63036 the minimum inductor value should be kept at 1 uH. To simplify this process Table 1 outlines possible inductor and capacitor value combinations.

Table 2. Output Filter Selection (Average Inductance Current up to 1 A)

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)		
	30	44	66
1.0	√	√	√
1.5	√(3)	√	√
2.2			√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check mark indicates recommended filter combinations

8.2.2.1 Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, with the chosen inductance value, the peak current for the inductor in steady-state operation can be calculated. Only the equation which defines the switch current in boost mode is reported because this is providing the highest value of current and represents the critical current value for selecting the right inductor.

Duty Cycle Boost

$$D = \frac{Vout - Vin}{Vout} \quad (1)$$

$$I_{PEAK} = I_{SW_MAX} + \frac{Vin \times D}{2 \times f \times L} \quad (2)$$

where

- D = Duty cycle in boost mode
- f = Converter switching frequency (typical 2 MHz)
- L = Selected inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
- I_{SW_MAX} = Maximum average input current (Figure 6)

NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode.

Consider the load transients and error conditions that can cause higher inductor currents. Consider when selecting an appropriate inductor. Please refer to Table 3 for typical inductors.

The size of the inductor can also affect the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inverse proportional to the inductor value and the load current. This means as higher the value of inductance and load current is the more possibilities has the right plane zero to be moved at lower frequency. This could degrade the phase margin of the feedback loop. TI recommends to choose the value of the inductor in order to have the frequency of the right half plane zero >400 kHz. The frequency of the RHPZ can be calculated using equation Equation 2.

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$$f_{RHPZ} = \frac{(1 - D)^2 \times Vout}{2\pi \times Iout \times L} \quad (3)$$

where

- D =Duty cycle in boost mode

NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode.

Table 3. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
1 µH	TOKO 1286AS-H-1R0M	2x1.6x1.2	2.3A/78mΩ
1 µH	Coilcraft XFL4020-102	4 x 4 x 2.1	5.1A/10.8 mΩ
1 µH	Coilcraft XFL3012-102	3 x 3 x 1.2	2.2 A/35 mΩ
1.5µH	TOKO, 1286AS-H-1R5M	2 x 1.6 x 1.2	4.4A/ 14.40mΩ
1.5µH	Coilcraft, LPS3015-152MLC	3 x 3 x 1.5	2.1A/100mΩ
1.5µH	TOKO, 1269AS-H-1R5M	2.5 x 2 x 1	2.1A/108mΩ
2.2µH	TOKO D1286AS-H-2R2M	2 x 1.6 x 1.2	1.6A/192mΩ

8.2.2.2 Capacitor Selection

8.2.2.2.1 *Input Capacitor*

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

8.2.2.2.2 *Output Capacitor*

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and GND pins of the IC. The recommended typical output capacitor value is 30 µF.

There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

When choosing input and output capacitors, it needs to be kept in mind, that the value of capacitance experiences significant losses from their rated value depending on the operating temperature and the operating DC voltage. It is not uncommon for a small surface mount ceramic capacitor to lose 50% and more of its rated capacitance. For this reason it could be important to use a larger value of capacitance or a capacitor with higher voltage rating in order to ensure the required capacitance at the full operating voltage.

8.2.2.3 Setting the Output Voltage

The output voltage of the TPS63036 is set by an external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between FB and GND, R2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 100 kΩ, in order to set the divider current at 5 µA or higher. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (4)$$

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A small capacitor C3 = 10 pF, in parallel with R1 needs to be placed when using the power-save mode, to improve considerably the output voltage ripple.

8.2.2.4 Current Limit

To protect the device and the application, the average input current is limited internally on the IC. At nominal operating conditions, this current limit is constant. The current limit value can be found in the *Electrical Characteristics* table. The current limit varies depending on the input voltage. A curve of the input current varying with the input voltage is shown in Figure 5 and Figure 6 respectively showing the minimum and the maximum current limit expected depending on input and output voltage.

Given the average input current in Figure 5 is then possible to calculate the output current reached in boost mode using Equation 5 and Equation 6 and in buck mode using Equation 7 and Equation 8.

Duty Cycle Boost $$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (5)$$

Maximum Output Current Boost $$I_{OUT} = \eta \times I_{SW} \times (1 - D) \quad (6)$$

Duty Cycle Buck $$D = \frac{V_{OUT}}{V_{IN}} \quad (7)$$

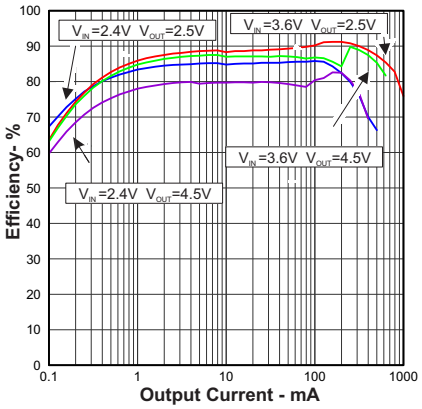
Maximum Output Current Buck $$Iout = \frac{\eta \times Isw}{D} \quad (8)$$

where

- η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
- f = Converter switching frequency (typical 2 MHz)
- L = Selected inductor value
- I_{SW} = Minimum average input current (Figure 5)

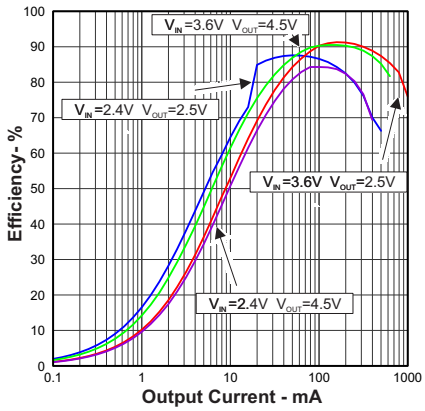
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8.2.3 Application Curves



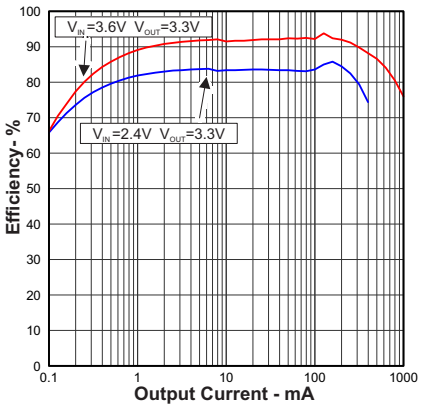
V_{OUT} = 2.5 V/ 4.5 V

Figure 5. Efficiency vs Output Current – Power-Save Mode Enabled



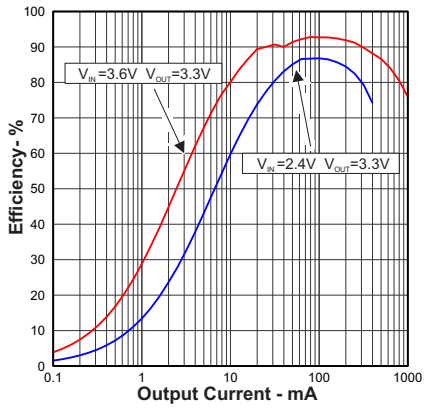
V_{OUT} = 2.5 V/ 4.5 V

Figure 6. Efficiency vs Output Current – Power-Save Mode Disabled



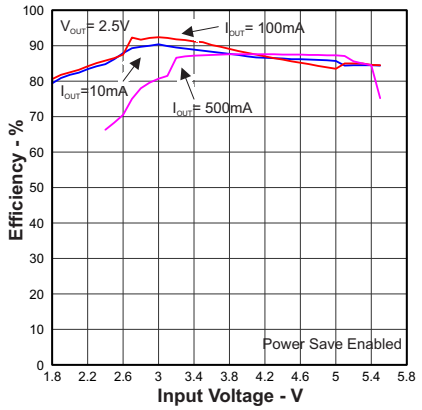
V_{OUT} = 3.3 V

Figure 7. Efficiency vs Output Current – Power-Save Mode Enabled



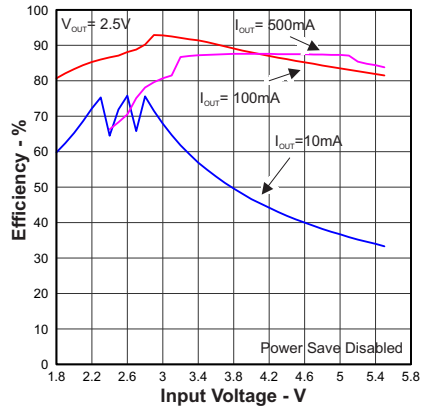
V_{OUT} = 3.3 V

Figure 8. Efficiency vs Output Current – Power-Save Mode Disabled



V_{OUT} = 2.5 V, I_{OUT} = 10 mA/100 mA/500 mA

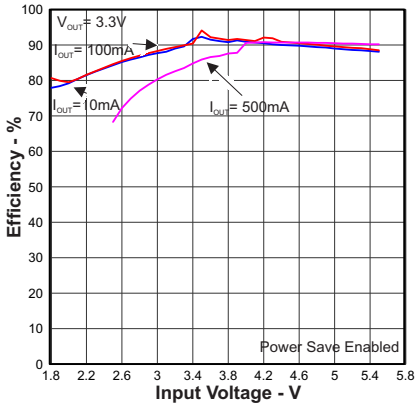
Figure 9. Efficiency vs Input Voltage – Power-Save Mode Enabled



V_{OUT} = 2.5 V, I_{OUT} = 10 mA/100 mA/500 mA

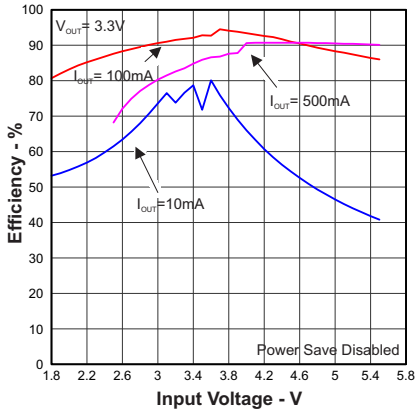
Figure 10. Efficiency vs Input Voltage – Power-Save Mode Disabled

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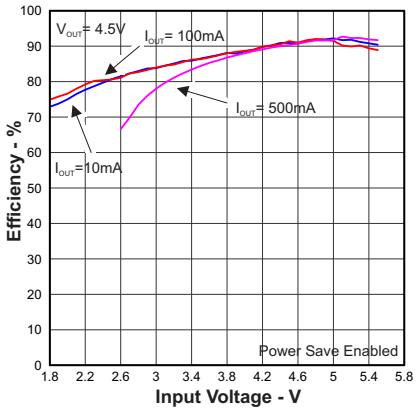
V_{OUT} = 3.3 V, I_{OUT} = 10 mA/100 mA/500 mA

Figure 11. Efficiency vs Input Voltage – Power-Save Mode Enabled



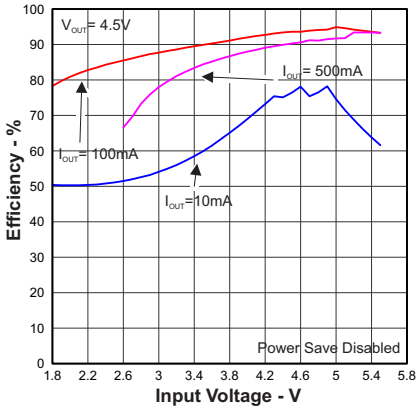
V_{OUT} = 3.3 V, I_{OUT} = 10 mA/100 mA/500 mA

Figure 12. Efficiency vs Input Voltage – Power-Save Mode Disabled



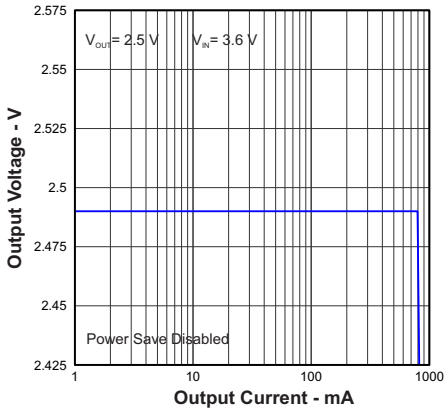
V_{OUT} = 4.5 V, I_{OUT} = 10 mA/100 mA/500 mA

Figure 13. Efficiency vs Input Voltage – Power-Save Mode Enabled



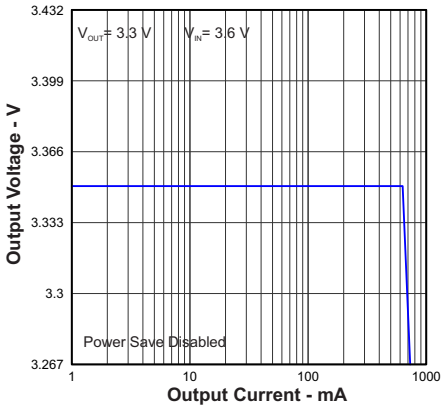
V_{OUT} = 4.5 V, I_{OUT} = 10 mA/100 mA/500 mA

Figure 14. Efficiency vs Input Voltage – Power-Save Mode Disabled



V_{OUT} = 2.5 V

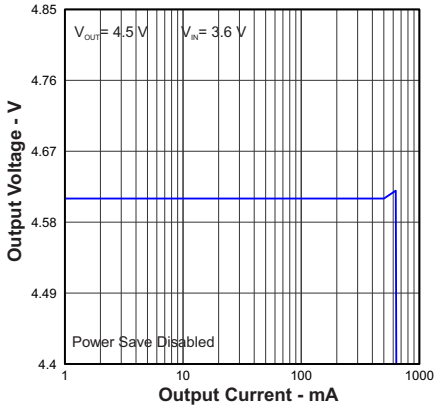
Figure 15. Output Voltage vs Output Current



V_{OUT} = 3.3 V

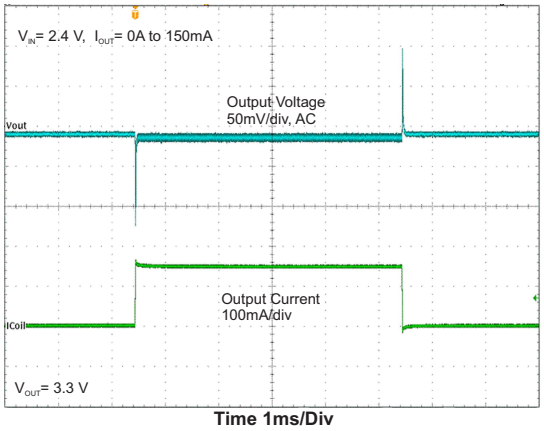
Figure 16. Output Voltage vs Output Current

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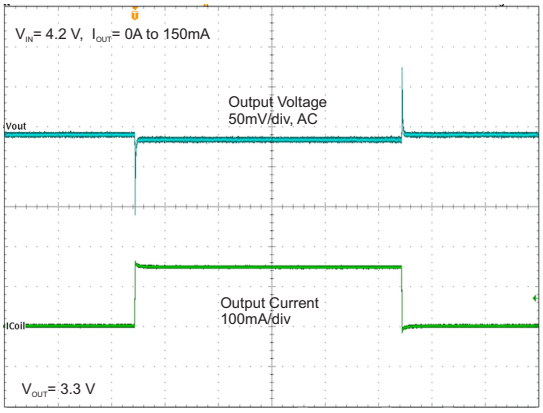
V_{OUT} = 4.5 V

Figure 17. Output Voltage vs Output Current



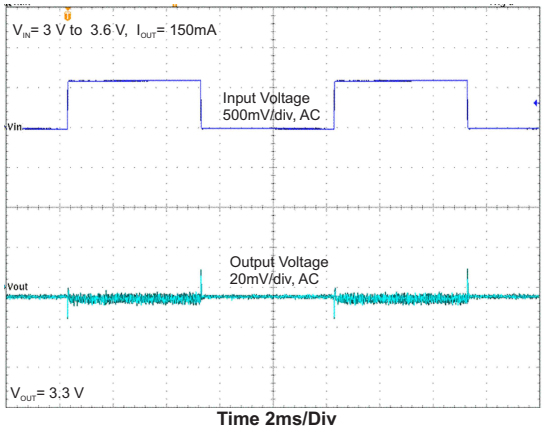
V_{IN} < V_{OUT}, Load Change from 0 mA to 150 mA

Figure 18. Load Transient Response



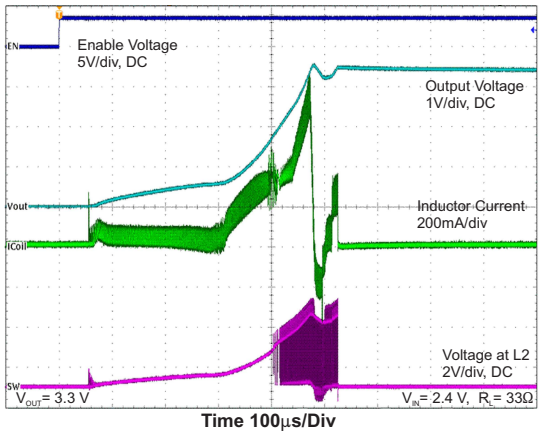
V_{IN} > V_{OUT}, Load Change from 0 mA to 150 mA

Figure 19. Load Transient Response



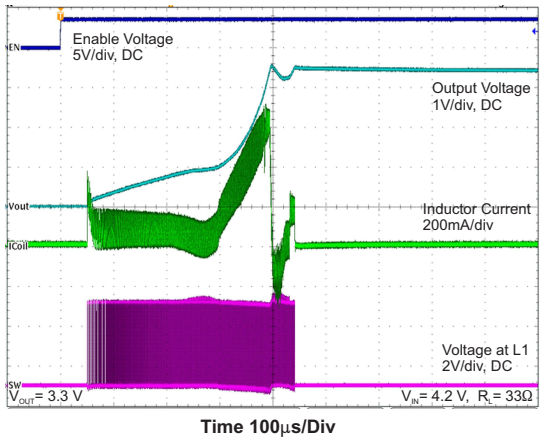
V_{OUT} = 3.3 V, I_{OUT} = 150 mA

Figure 20. Line Transient Response



V_{OUT} = 3.3 V, V_{IN} = 2.4 V, R_L = 33 Ω

Figure 21. Start-Up After Enable



V_{OUT} = 3.3 V, V_{IN} = 4.2 V, R_L = 33 Ω

Figure 22. Start-Up After Enable

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9 Power Supply Recommendations

The TPS63036 device has no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage and output current of the TPS63036.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC.

The feedback divider should be placed as close as possible to the ground pin of the IC.

10.2 Layout Example

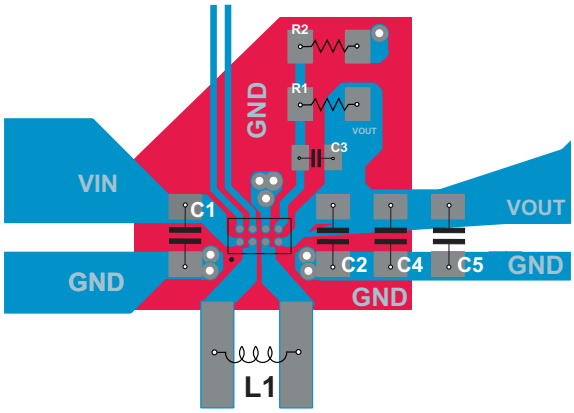


Figure 23. Layout Recommendation

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB by soldering all pins to traces as wide as possible.
3. Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS63036 device is 125°C. The thermal resistance of this 8-pin chip-scale package (YFG) is $R_{\theta JA}$ = 84°C/W, if all pins are soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 476 mW, as calculated in Equation 9. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125^\circ C - 85^\circ C}{84^\circ C/W} = 476\ mW \quad (9)$$

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11 Device and Documentation Support

11.1 Device Support

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63036YFGR	ACTIVE	DSBGA	YFG	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S63036	Samples
TPS63036YFGT	ACTIVE	DSBGA	YFG	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S63036	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

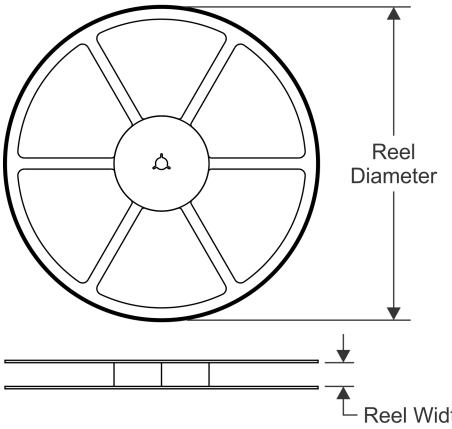
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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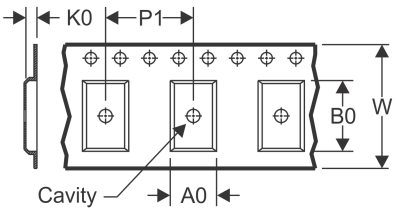
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

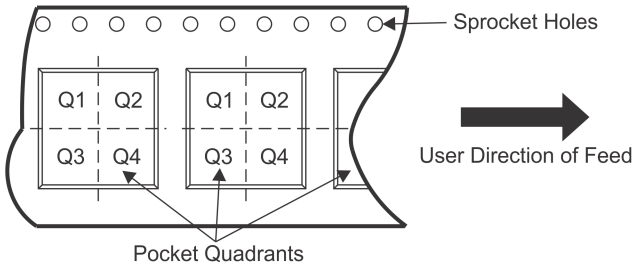


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

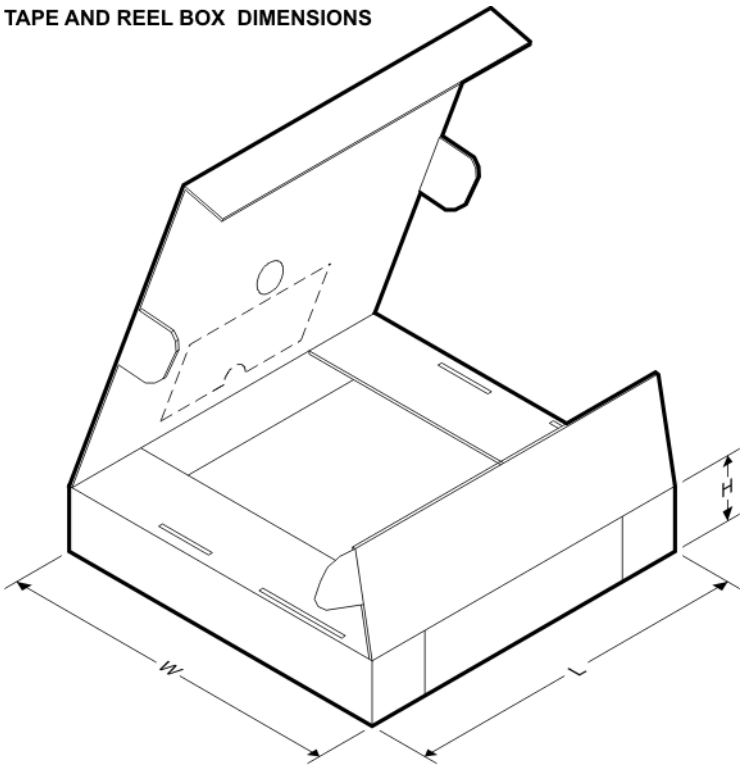
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63036YFGR	DSBGA	YFG	8	3000	180.0	8.4	1.2	2.0	0.7	4.0	8.0	Q1
TPS63036YFGT	DSBGA	YFG	8	250	180.0	8.4	1.2	2.0	0.7	4.0	8.0	Q1

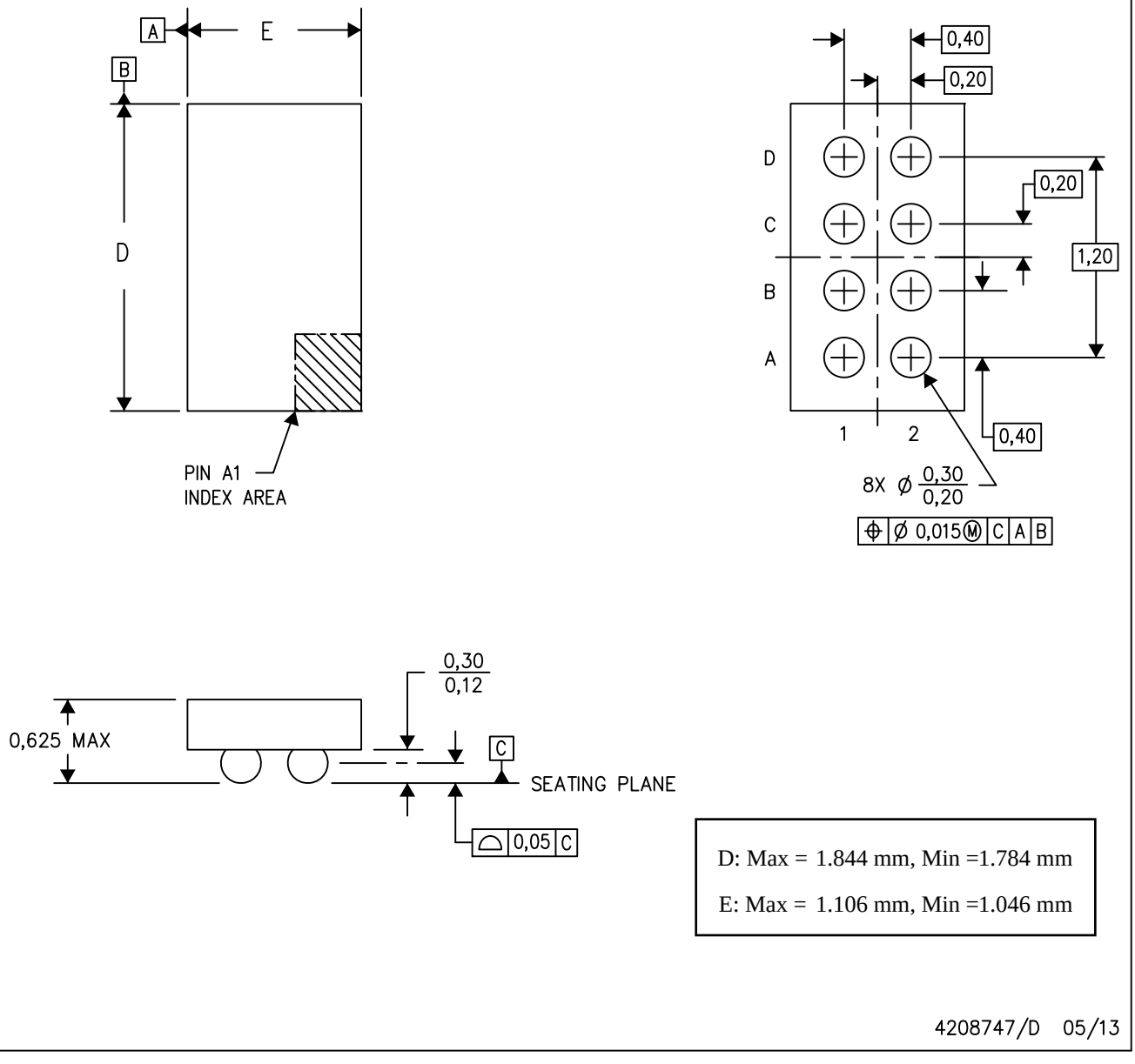
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63036YFGR	DSBGA	YFG	8	3000	182.0	182.0	20.0
TPS63036YFGT	DSBGA	YFG	8	250	182.0	182.0	20.0

YFG (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Die size package configuration.

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