MIC45404

19V 5A Ultra-Low Profile DC-to-DC Power Module

Features

- Input Voltage Range: 4.5V to 19V
- Output Current: Up to 5A
- 82% Peak Efficiency at 12 V_{IN}, 0.9 V_{OUT}
- Pin-Selectable Output Voltages: 0.7V, 0.8V, 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V
- ±1% Output Voltage Accuracy
- Supports Safe Pre-Biased Start-up
- Pin-Selectable Current Limit
- Pin-Selectable Switching Frequency
- Internal Soft Start
- Thermal Shutdown
- Hiccup Mode Short-Circuit Protection
- Available in a 54-Lead 6 mm x 10 mm QFN Package
- Ultra-Low Profile: 2.0 mm Height
- -40°C to +125°C Junction Temperature Range

Applications

- Servers, Data Storage, Routers and Base Stations
- FPGAs, DSP and Low-Voltage ASIC Power

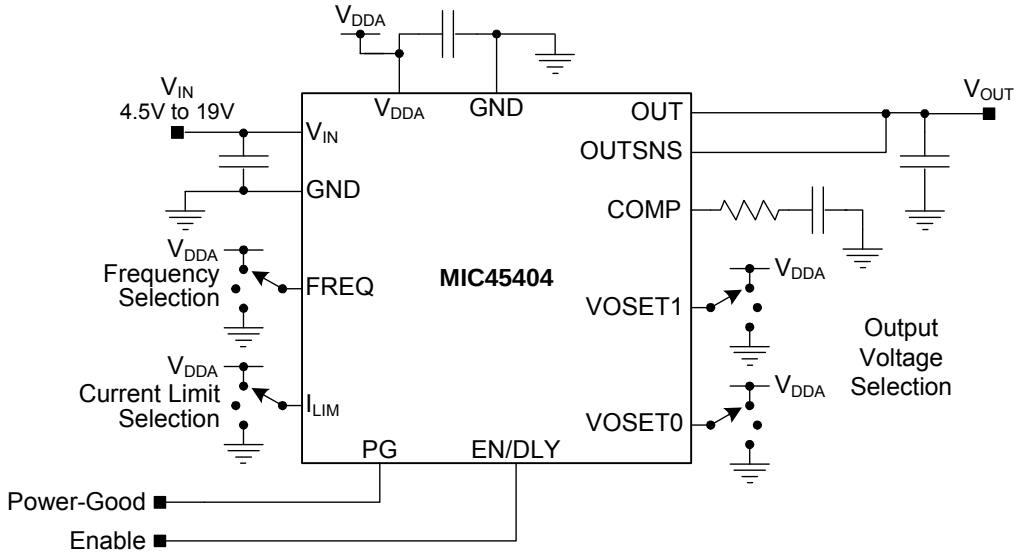
General Description

The MIC45404 device is an ultra-low profile, synchronous step-down regulator module, featuring a unique 2.0 mm height. The module incorporates a DC-to-DC regulator, bootstrap capacitor, high-frequency input capacitor and an inductor in a single package. The module pinout is optimized to simplify the Printed Circuit Board (PCB) layout process.

This highly integrated solution expedites system design and improves product time to market. The internal MOSFETs and inductor are optimized to achieve high efficiency at low output voltage. Due to the fully optimized design, MIC45404 can deliver up to 5A current with a wide input voltage range of 4.5V to 19V.

The MIC45404 is available in a 54-lead 6 mm x 10 mm x 2.0 mm QFN package with a junction operating temperature range from -40°C to +125°C, which makes an excellent solution for systems in which PCB real-estate and height are important limiting factors, and air flow is restricted.

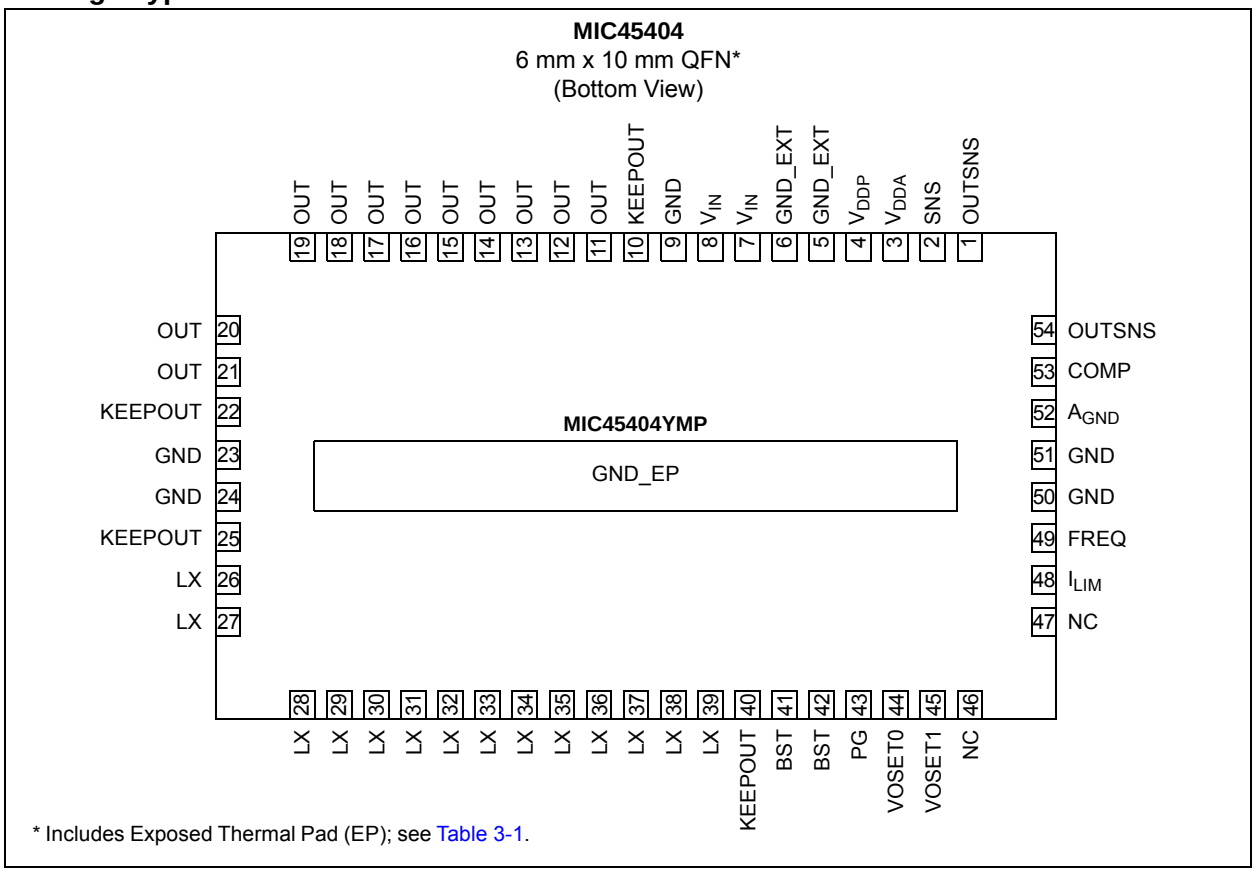
Typical Application



MIC45404 12V 5A DC-to-DC Converter

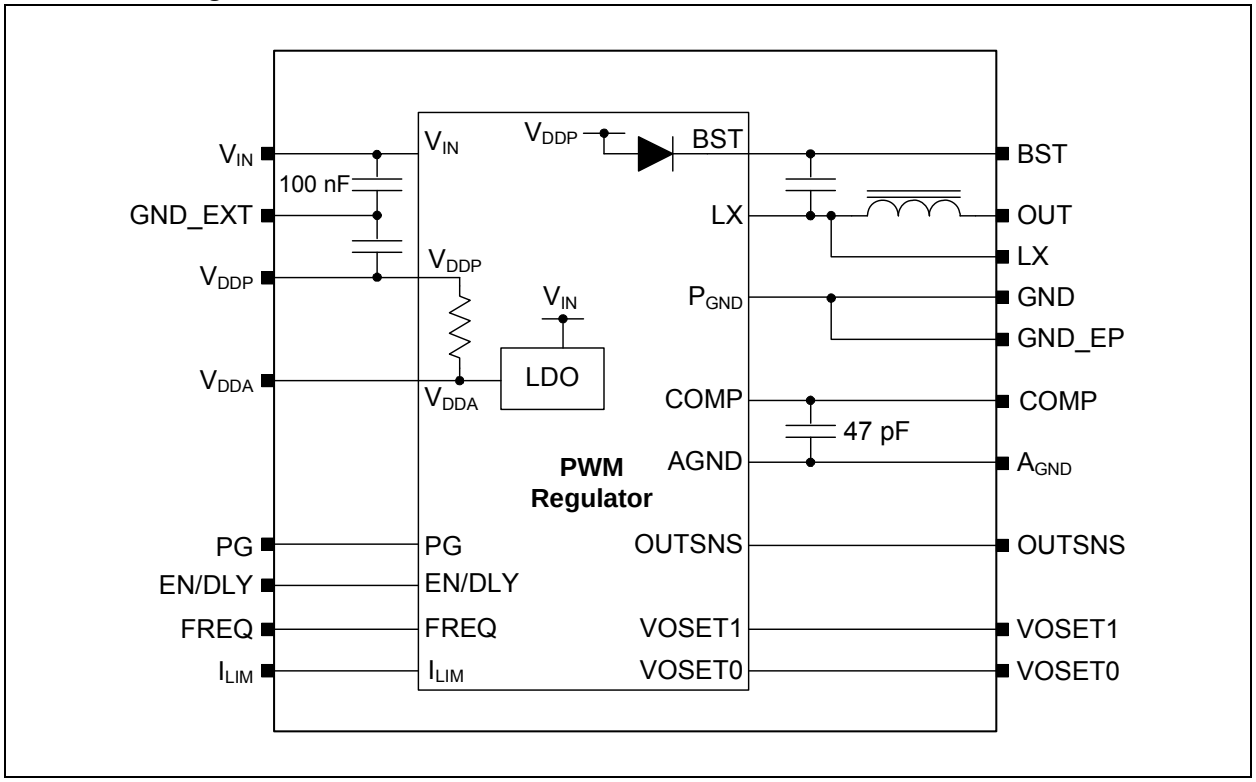
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Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} to A_{GND} ..... -0.3V to +20V
V_{DDP}, V_{DDA} to A_{GND} ..... -0.3V to +6V
V_{DDP} to V_{DDA} ..... -0.3V to +0.3V
VOSETX, FREQ, I_{LIM}, to A_{GND} ..... -0.3V to +6V
BST to LX ..... -0.3V to +6V
BST to A_{GND} ..... -0.3V to +26V
EN/DLY to A_{GND} ..... -0.3V to V_{DDA} + 0.3V, +6V
PG to A_{GND} ..... -0.3V to +6V
COMP, OUTSNS to A_{GND} ..... -0.3V to V_{DDA} + 0.3V, +6V
A_{GND} to GND ..... -0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... 260°C
ESD Rating(1)
HBM 2kV
MM 150V
CDM 1500V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings(1)

Supply Voltage (V_{IN}) ..... 4.5V to 19V
Externally Applied Analog and Drivers Supply Voltage (V_{IN} = V_{DDA} = V_{DDP}) ..... 4.5V to 5.5V
Enable Voltage (EN/DLY) ..... 0V to V_{DDA}
Power Good (PG) Pull-up Voltage (VPU_PG) ..... 0V to 5.5V
Output Current 5A
Junction Temperature (T_J) ..... -40°C to +125°C

Note 1: The device is not ensured to function outside the operating range.

ELECTRICAL CHARACTERISTICS[1]

Electrical Specifications: unless otherwise specified, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.
Boldface values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
V_{IN} Supply						
Input Range	V_{IN}	**4.5**	—	**19**	V	
Disable Current	I_{VINQ}	—	33	**60**	µA	EN/DLY = 0V
Operating Current	I_{VINOp}	—	5.35	**8.5**	mA	EN/DLY > 1.28V, OUTSNS = 1.15 x $V_{OUT(NOM)}$, no switching
V_{DDA} 5V Supply						
Operating Voltage	V_{DDA}	**4.8**	5.1	**5.4**	V	EN/DLY > 0.58V, I_{VDDA} = 0 mA to 10 mA
Dropout Operation		**3.6**	3.75	—	V	V_{IN} = 4.5V, EN/DLY > 0.58V, I_{VDDA} = 10 mA
V_{DDA} Undervoltage Lockout						
V_{DDA} UVLO Rising	UVLO_R	**3.1**	3.5	**3.9**	V	V_{DDA} Rising, EN/DLY > 1.28V
V_{DDA} UVLO Falling	UVLO_F	**2.87**	3.2	**3.45**	V	V_{DDA} Falling, EN/DLY > 1.28V
V_{DDA} UVLO Hysteresis	UVLO_H	—	300	—	mV	
EN/DLY Control						
LDO Enable Threshold	EN_LDO_R	—	515	**600**	mV	Turns on V_{DDA} LDO
LDO Disable Threshold	EN_LDO_F	**450**	485	—	mV	Turns off V_{DDA} LDO
LDO Threshold Hysteresis	EN_LDO_H	—	30	—	mV	
EN/DLY Rising Threshold	EN_R	**1.14**	1.21	**1.28**	V	Initiates power stage operation
EN/DLY Falling Threshold	EN_F	—	1.06	—	V	Stops power stage operation
EN/DLY Hysteresis	EN_H	—	150	—	mV	
EN/DLY Pull-up Current	EN_I	**1**	2	**3**	µA	
Switching Frequency						
Programmable Frequency (High Z)	f_{SZ}	**360**	400	**440**	kHz	FREQ = High Z (open)
Programmable Frequency 0	f_{S0}	**500**	565	**630**	kHz	FREQ= Low (GND)
Programmable Frequency 1	f_{S1}	**700**	790	**880**	kHz	FREQ = High (V_{DDA})
Overcurrent Protection						
HS Current Limit 0	I_{LIM_HS0}	**6.0**	7.1	**8.1**	A	I_{LIM} = Low (GND)
HS Current Limit 1	I_{LIM_HS1}	**8.1**	9.3	**10.3**	A	I_{LIM} = High (V_{DDA})
HS Current Limit High Z	I_{LIM_HSZ}	**9.3**	10.5	**11.9**	A	I_{LIM} = High Z (open)
Top FET Current Limit Leading-Edge Blanking Time	LEB	—	108	—	ns	
LS Current Limit 0	I_{LIM_LS0}	**3.0**	4.6	**6.3**	A	I_{LIM} = Low (GND)
LS Current Limit 1	I_{LIM_LS1}	**4.0**	6.2	**7.9**	A	I_{LIM} = High (V_{DDA})
LS Current Limit High Z	I_{LIM_LSZ}	**5.0**	6.8	**8.6**	A	I_{LIM} = High Z (Open)
OC Events Count for Hiccup	IN_{HICC_DE}	—	15	—	Clock Cycles	Number of subsequent cycles in current limit before entering hiccup overload protection
Hiccup Wait Time	t_{HICC_WAIT}	—	3 x Soft Start Time	—		Duration of the High Z state on LX before new soft start.

Note 1: Specification for packaged product only.

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ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: unless otherwise specified, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.
Boldface values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Pulse-Width Modulation (PWM)						
Minimum LX On Time	$T_{ON(MIN)}$	—	26	—	ns	$T_A = T_J$ = +25°C
Minimum LX Off time	$T_{OFF(MIN)}$	90	135	190	ns	$V_{IN} = V_{DDA}$ = 5V, OUTSNS = 3V, FREQ = Open (400 kHz setting), VOSET0 = VOSET1 = 0V (3.3V setting), $T_A = T_J$ = +25°C
Minimum Duty Cycle	D_{MIN}	—	0	—	%	OUTSNS > 1.1 x $V_{OUT(NOM)}$
Gm Error Amplifier						
Error Amplifier Transconductance	Gm_{EA}	—	1.4	—	mS	
Error Amplifier DC Gain	A_{EA}	—	50000	—	V/V	
Error Amplifier Source/Sink Current	I_{SR_SNK}	-400	—	+400	µA	$T_A = T_J$ = +25°C
COMP Output Swing High	COMP_H	—	2.5	—	V	
COMP Output Swing Low	COMP_L	—	0.8	—	V	
COMP-to-Inductor Current Transconductance	Gm_{PS}	—	12.5	—	A/V	V_{OUT} = 1.2V, I_{OUT} = 4A
Output Voltage DC Accuracy						
Output Voltage Accuracy for Ranges 1 and 2	OutErr12	**-1**	—	**1**	%	4.75V ≤ V_{IN} ≤ 19V, V_{OUT} = 0.7V to 1.8V, $T_A = T_J$ = -40°C to +125°C, I_{OUT} = 0A
Output Voltage Accuracy for Range 3	OutErr3	**-1.5**	—	**1.5**	%	4.75V ≤ V_{IN} ≤ 19V, V_{OUT} = 2.49V to 3.3V, $T_A = T_J$ = -40°C to +125°C, I_{OUT} = 0A
Load Regulation	LoadReg	—	0.03	—	%	I_{OUT} = 0A to 5A
Line Regulation	LineReg	—	0.01	—	%	6V < V_{IN} < 19V, I_{OUT} = 2A
Internal Soft Start						
Reference Soft Start Slew Rate	SS_SR	—	0.42	—	V/ms	V_{OUT} = 0.7V, 0.8V, 0.9V, 1.0V, 1.2V
Power Good (PG)						
PG Low Voltage	PG_V_{OL}	—	0.17	**0.4**	V	I_{PG} = 4 mA
PG Leakage Current	PG_I_{LEAK}	**-1**	0.02	**1**	µA	PG = 5V
PG Rise Threshold	PG_R	**90**	92	**95**	%	V_{OUT} Rising
PG Fall Threshold	PG_F	**87.5**	90	**92.5**	%	V_{OUT} Falling
PG Rise Delay	PG_R_DLY	—	0.45	—	ms	V_{OUT} Rising
PG Fall Delay	PG_F_DLY	—	80	—	µs	V_{OUT} Falling

Note 1: Specification for packaged product only.

ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: unless otherwise specified, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.
Boldface values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}	—	160	—	°C	
Thermal Shutdown Hysteresis	T_{SHDN_HYST}	—	25	—	°C	
Efficiency						
Efficiency	η	—	82	—	%	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 2A, f_S = f_{SZ} = 400 kHz, T_A = +25°C

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: unless otherwise specified, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.
Boldface values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Junction Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	-40	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 54 Lead, 6 mm x10 mm QFN	θ_{JA}	—	20	—	°C/W	See *"MIC45404 Evaluation Board User's Guide"*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.

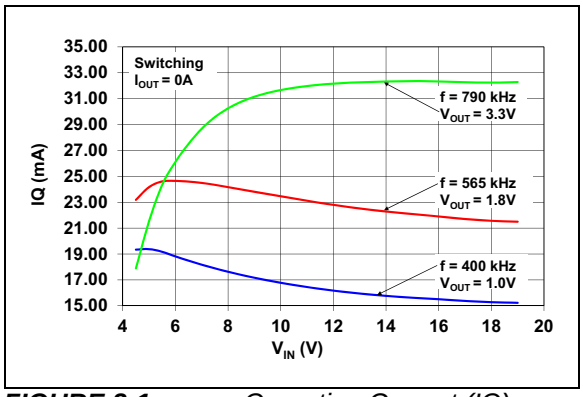


FIGURE 2-1: *Operating Current (IQ) vs. Input Voltage.*

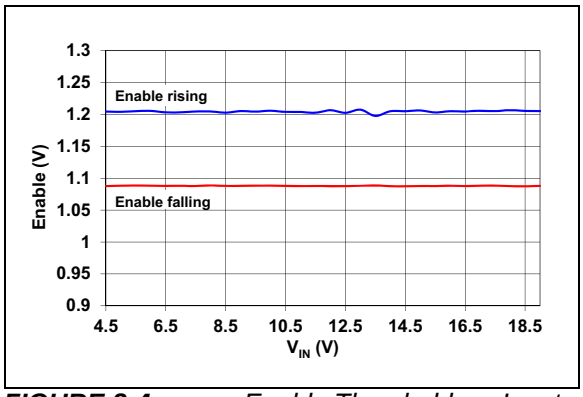


FIGURE 2-4: *Enable Threshold vs. Input Voltage.*

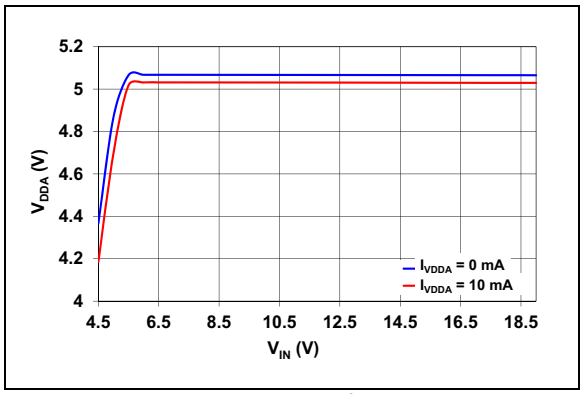


FIGURE 2-2: *V_{DDA} Voltage vs. Input Voltage.*

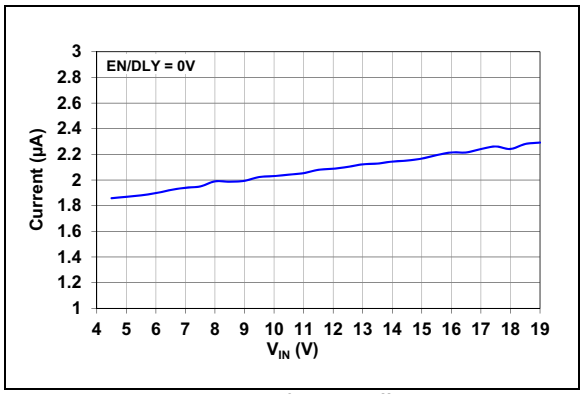


FIGURE 2-5: *EN/DLY Pull-up Current vs. Input Voltage.*

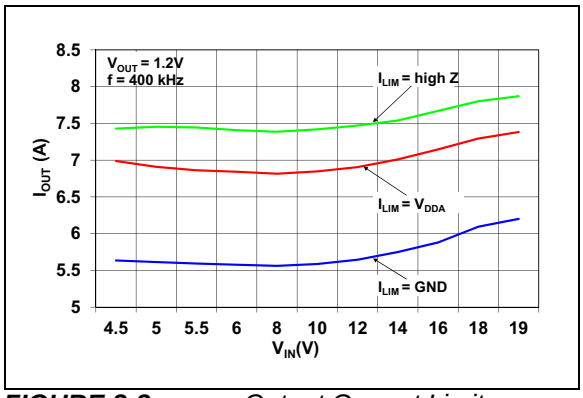


FIGURE 2-3: *Output Current Limit vs. Input Voltage.*

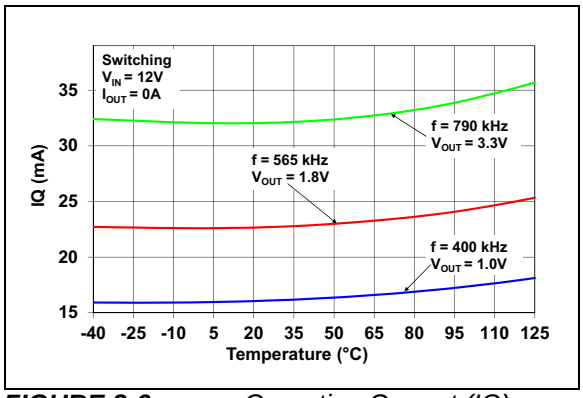


FIGURE 2-6: *Operating Current (IQ) vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.

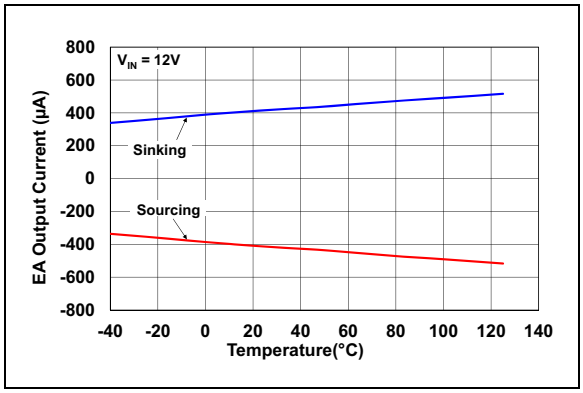


FIGURE 2-7: *EA Output Current vs. Temperature.*

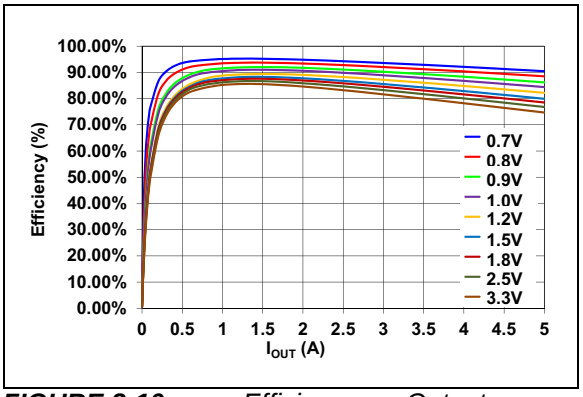


FIGURE 2-10: *Efficiency vs. Output Current (V_{IN} = 5V).*

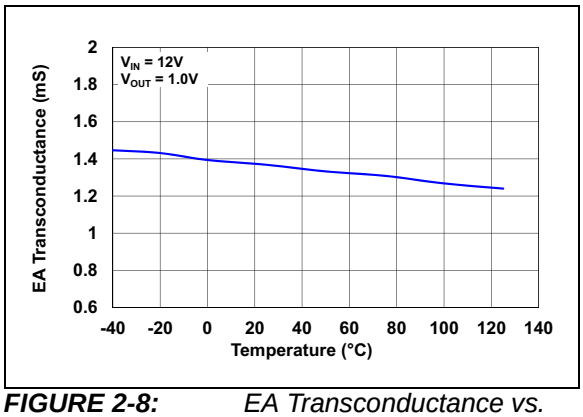


FIGURE 2-8: *EA Transconductance vs. Temperature.*

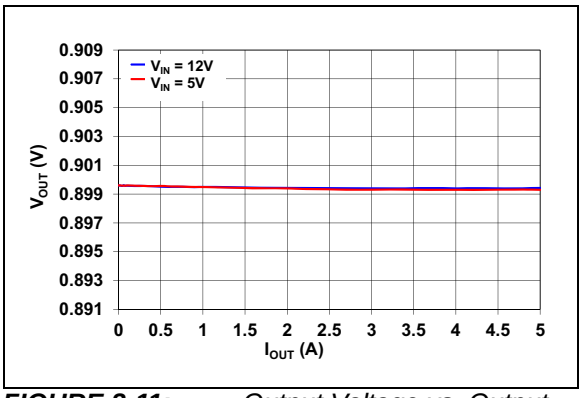


FIGURE 2-11: *Output Voltage vs. Output Current (V_{OUT} = 0.9V).*

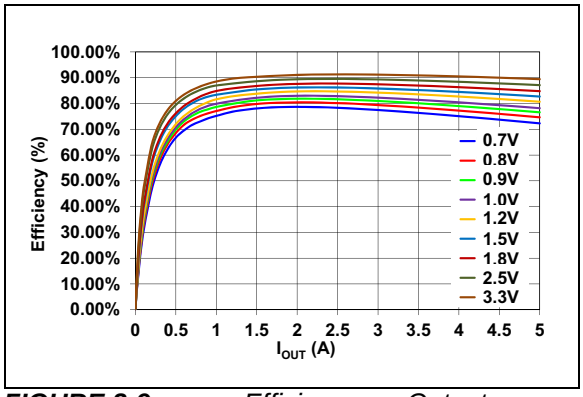


FIGURE 2-9: *Efficiency vs. Output Current (V_{IN} = 12V).*

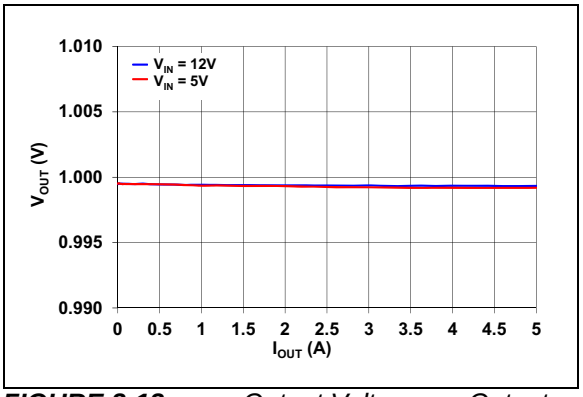


FIGURE 2-12: *Output Voltage vs. Output Current (V_{OUT} = 1.0V).*

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Note: Unless otherwise indicated, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.

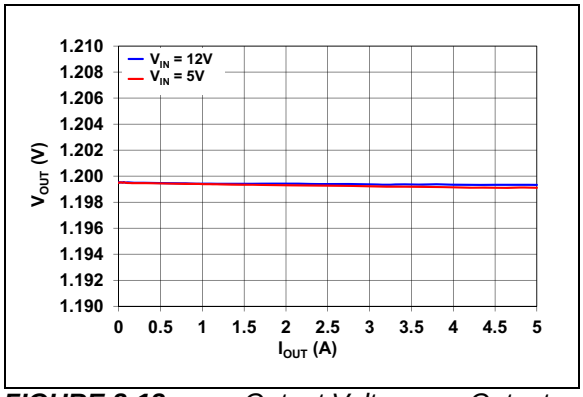


FIGURE 2-13: *Output Voltage vs. Output Current (V_{OUT} = 1.2V).*

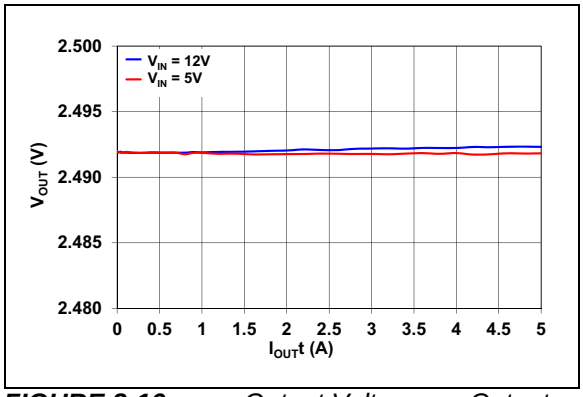


FIGURE 2-16: *Output Voltage vs. Output Current (V_{OUT} = 2.5V).*

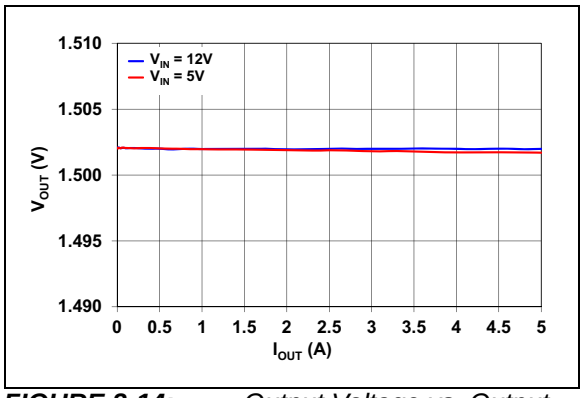


FIGURE 2-14: *Output Voltage vs. Output Current (V_{OUT} = 1.5V).*

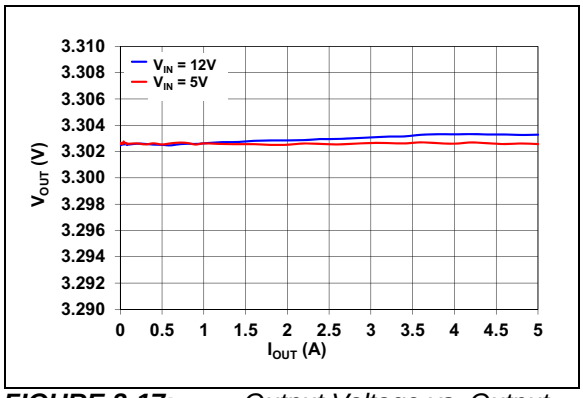


FIGURE 2-17: *Output Voltage vs. Output Current (V_{OUT} = 3.3V).*

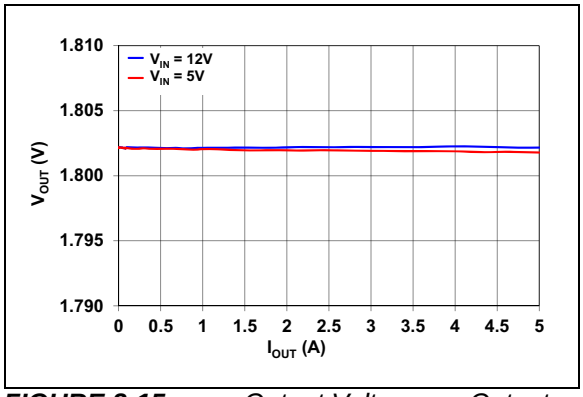


FIGURE 2-15: *Output Voltage vs. Output Current (V_{OUT} = 1.8V).*

Note: Unless otherwise indicated, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.

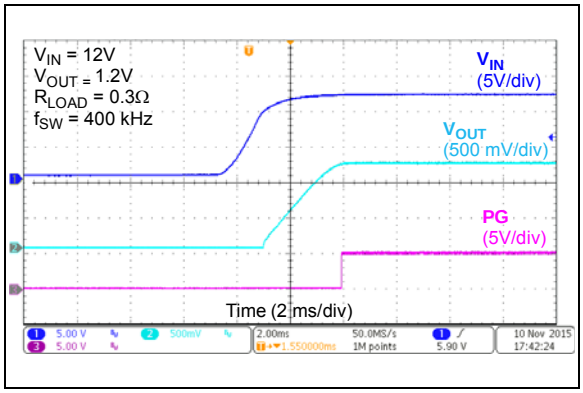


FIGURE 2-18: *V_{IN} Turn-On.*

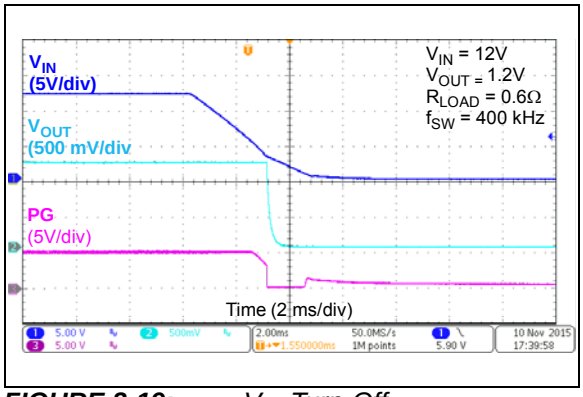


FIGURE 2-19: *V_{IN} Turn-Off.*

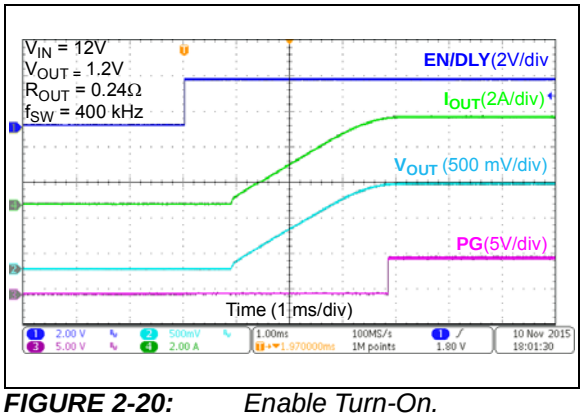


FIGURE 2-20: *Enable Turn-On.*

FIGURE 2-21: *Enable Turn-Off.*

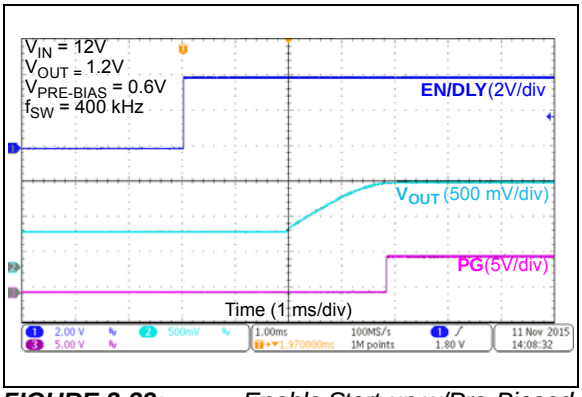


FIGURE 2-22: *Enable Start-up w/Pre-Biased Output.*

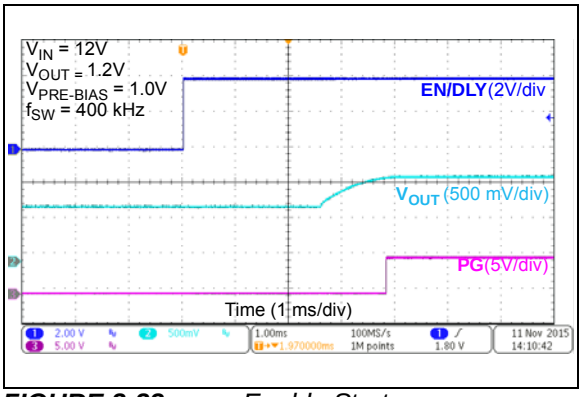


FIGURE 2-23: *Enable Start-up w/Pre-Biased Output.*

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Note: Unless otherwise indicated, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.

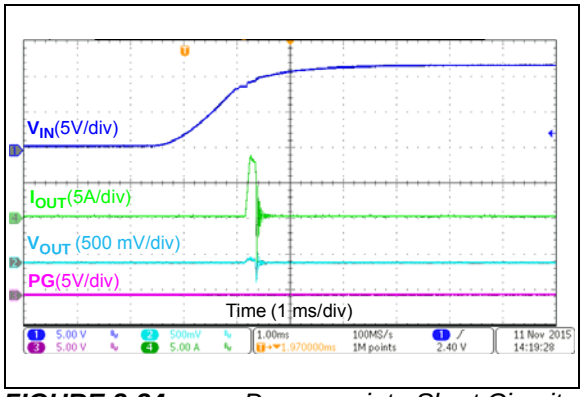


FIGURE 2-24: *Power-up into Short Circuit.*

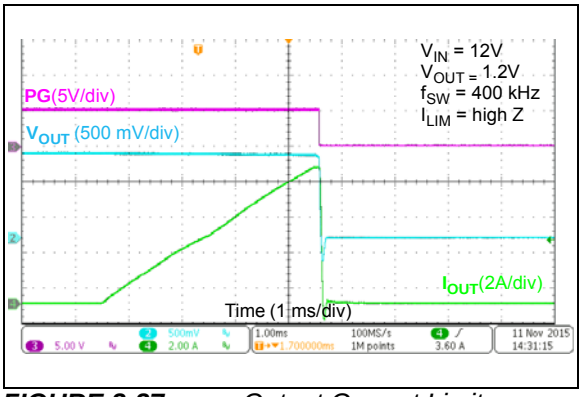


FIGURE 2-27: *Output Current Limit (I_{LIM} = High Z).*

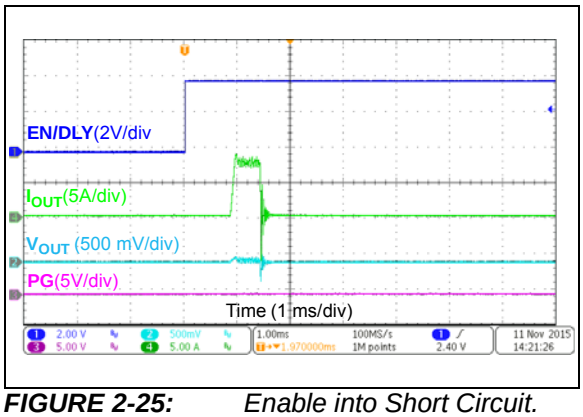


FIGURE 2-25: *Enable into Short Circuit.*

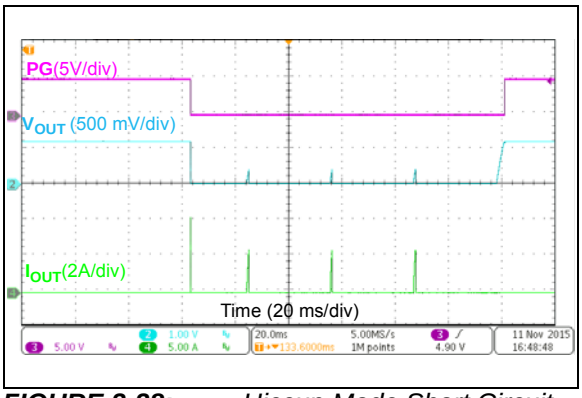


FIGURE 2-28: *Hiccup Mode Short Circuit and Output Recovery.*

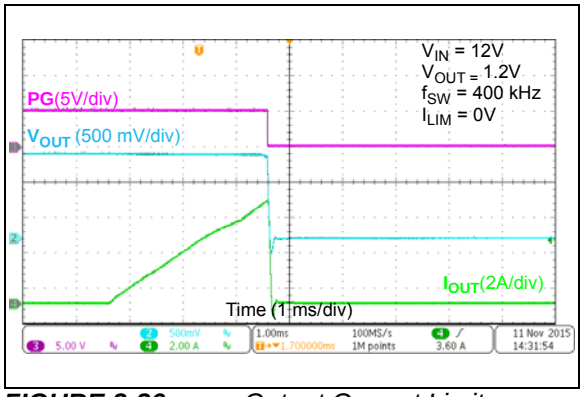


FIGURE 2-26: *Output Current Limit (I_{LIM} = 0V).*

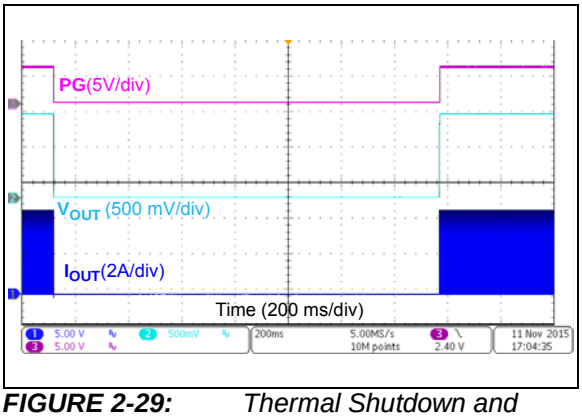


FIGURE 2-29: *Thermal Shutdown and Thermal Recovery.*

Note: Unless otherwise indicated, V_{IN} = 12V; C_{VDDA}= 2.2 µF, T_A = +25°C.

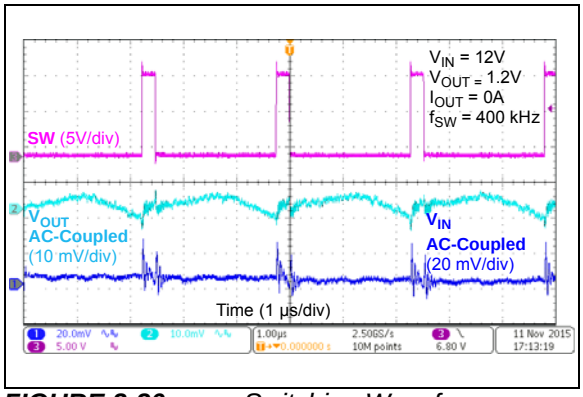


FIGURE 2-30: *Switching Waveforms (I_{OUT} = 0A).*

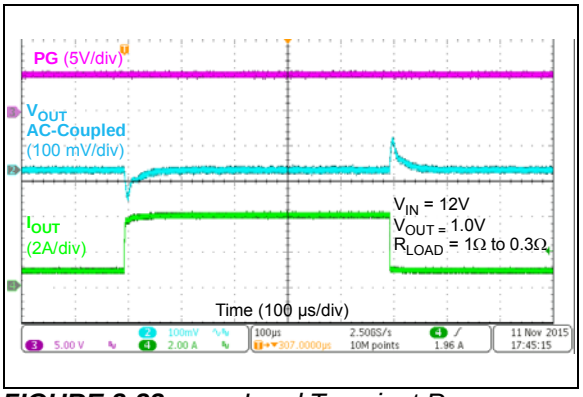


FIGURE 2-32: *Load Transient Response.*

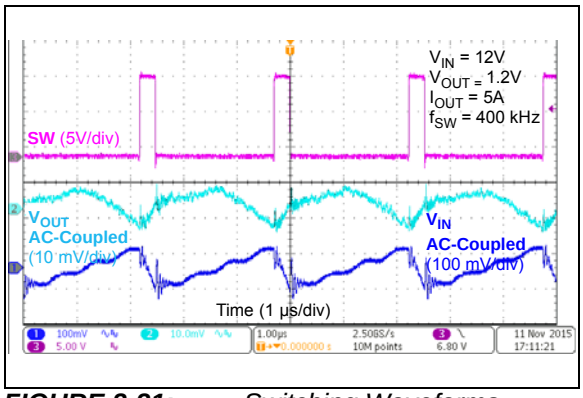


FIGURE 2-31: *Switching Waveforms (I_{OUT} = 5A).*

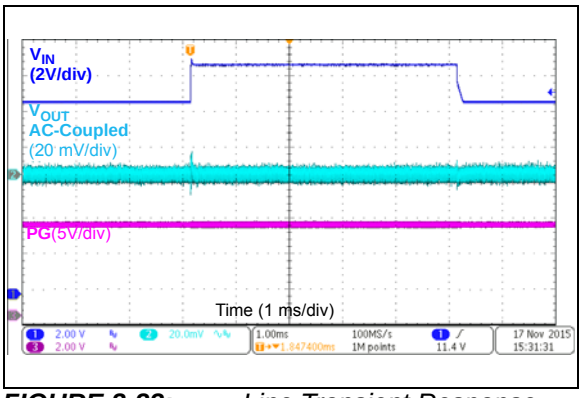


FIGURE 2-33: *Line Transient Response.*

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3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MIC45404	Symbol	Pin Function
1, 54	OUTSNS	Output Sensing Pin
2	EN/DLY	Precision Enable/Turn-On Delay Input Pin
3	V_{DDP}	MOSFET Drivers Internal Supply Pin
4	V_{DDA}	Internal LDO Output and Analog Supply Pin
5, 6	GND_EXT	Ground Extension Pins
7, 8	V_{IN}	Input Voltage Pins
9, 23, 24, 50, 51	GND	Power Ground Pins
11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21	OUT	Output Side Connection Pins
10, 22, 25, 40	KEEPOUT	Depopulated Pin Positions
26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39	LX	Switch Node Pins
41, 42	BST	Bootstrap Capacitor Pin
43	PG	Power Good Output Pin
44	VOSET0	Output Voltage Selection Pins
45	VOSET1	
46, 47	NC	Not Connected Pins
48	I_{LIM}	Current Limit Selection Pin
49	FREQ	Switching Frequency Selection Pin
52	A_{GND}	Analog Ground Pin
53	COMP	Compensation Network Pin
55	GND_EP	Ground Exposed Pad.

3.1 Output Sensing Pins (OUTSNS)

Connect these pins directly to the Buck Converter output voltage. These pins are the top side terminal of the internal feedback divider.

3.2 Precision Enable/Turn-On Delay Input Pin (EN/DLY)

The EN/DLY pin is first compared against a 515 mV threshold to turn on the on-board LDO regulator. The EN/DLY pin is then compared against a 1.21V (typical) threshold to initiate output power delivery. A 150 mV typical hysteresis prevents chattering when power delivery is started. A 2 µA (typical) current source pulls up the EN/DLY pin. Turn-on delay can be achieved by connecting a capacitor from EN/DLY to ground, while using an open-drain output to drive the EN/DLY pin.

3.3 MOSFET Drivers Internal Supply Pin (V_{DDP})

Internal supply rail for the MOSFET drivers, fed by the V_{DDA} pin. An internal resistor (10Ω) between the V_{DDP} and V_{DDA} pins, and an internal decoupling capacitor are provided in the module in order to implement an RC filter for switching noise suppression.

3.4 Internal Regulator Output Pin (V_{DDA})

Output of the internal linear regulator and internal supply for analog control. A 1 µF minimum ceramic capacitor should be connected from this pin to GND; a 2.2 µF nominal value is recommended.

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3.5 Ground Extension Pins (GND_EXT)

These pins are used for the bottom terminal connection of the internal V_{IN} and V_{DDP} decoupling capacitors. The GND_EXT pins should be connected to the GND net, directly at the top layer, using a wide copper connection.

3.6 Input Voltage Pins (V_{IN})

Input voltage for the Buck Converter power stage and input of the internal linear regulator. These pins are the drain terminal of the internal high-side N-channel MOSFET. A 10 µF (minimum) ceramic capacitor should be connected from V_{IN} to GND, as close as possible to the device.

3.7 Power Ground Pins (GND)

Connect the output capacitors to GND Pins 23 and 24, as close as possible to the module.

Connect the input capacitors to GND Pin 9, as close as possible to the module.

3.8 Output-Side Connection Pins (OUT)

Output side connection of the internal inductor. The output capacitors should be connected from this pin group to GND (Pins 23 and 24), as close to the module as possible.

3.9 Switch Node Pins (LX)

Switch Node: Drain (low-side MOSFET) and source (high-side MOSFET) connection of the internal power N-channel FETs. The internal inductor switched side and the bootstrap capacitor are connected to LX. Leave this pin floating.

3.10 Bootstrap Capacitor Pin (BST)

Connection to the internal bootstrap capacitor and high-side power MOSFET drive circuitry. Leave this pin floating.

3.11 Power Good Output Pin (PG)

When the output voltage is within 92.5% of the nominal set point, this pin will go from logic low to logic high through an external pull-up resistor. This pin is the drain connection of an internal N-channel FET.

3.12 Output Voltage Selection Pins (VOSET0 and VOSET1)

Three-state pin (low, high and High Z) for output voltage programming. Both VOSET0 and VOSET1 define 9 logic values, corresponding to nine output voltage selections.

3.13 Not Connected Pins (NC)

These pins are not internally connected. Leave them floating.

3.14 Current Limit Pin (I_{LIM})

This pin allows the selection of the current limit state: low, high and High Z.

3.15 Switching Frequency Pin (FREQ)

This pin allows the selection of the frequency state: low, high and High Z.

3.16 Analog Ground Pin (A_{GND})

This pin is a quiet ground for the analog circuitry of the internal regulator and a return terminal for the external compensation network.

3.17 Compensation Network Pin (COMP)

Connect a compensation network from this pin to A_{GND}.

3.18 GND Exposed Pad

Connect to ground plane with thermal vias.

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4.0 FUNCTIONAL DESCRIPTION

The MIC45404 is a pin-programmable, 5A Valley Current mode controlled power module, with an input voltage range from 4.5V to 19V.

The MIC45404 requires a minimal amount of external components. Only two supply decoupling capacitors and a compensation network are external. The flexibility in designing the external compensation allows the user to optimize the design across the entire input voltage and selectable output voltages range.

4.1 Theory of Operation

Valley Current mode control is a fixed frequency, leading-edge modulated Pulse-Width Modulation (PWM) Current mode control. Differing from the Peak Current mode, the Valley Current mode clock marks the turn-off of the high-side switch. Upon this instant, the MIC45404 low-side switch current level is compared against the reference current signal from the error amplifier. When the falling low-side switch current signal drops below the current reference signal, the high-side switch is turned on. As a result, the inductor valley current is regulated to a level dictated by the output of the error amplifier.

The feedback loop includes an internal programmable reference and output voltage sensing attenuator, thus removing the need for external feedback components and improving regulation accuracy. Output voltage feedback is achieved by connecting the OUTSNS pin directly to the output. The high-performance transconductance error amplifier drives an external compensation network at the COMP pin. The COMP pin voltage represents the reference current signal. This pin voltage is fed to the Valley Current mode modulator, which also adds slope compensation to ensure current loop stability.

Internal inductor, power MOSFETs and internal bootstrap diode complete the power train.

Overcurrent protection and thermal shutdown protect the MIC45404 from Faults or abnormal operating conditions.

4.2 Supply Rails (V_{IN}, V_{DDA}, V_{DDP}) and Internal LDO

V_{IN} pins represent the power train input. These pins are the drain connection of the internal high-side MOSFET and should be bypassed to GND, at least with a X5R or X7R 10 µF ceramic capacitor, placed as close as possible to the module. Multiple capacitors are recommended.

An internal LDO provides a clean supply (5.1V typical) for the analog circuits at the V_{DDA} pin. The internal LDO is also powered from V_{IN}, as shown in the Functional Diagram. The internal LDO is enabled when the voltage at the EN/DLY pin exceeds about 0.51V, and regulation takes place as soon as enough voltage has been established between the V_{IN} and V_{DDA} pins. An internal Undervoltage Lockout (UVLO) circuit monitors the level of V_{DDA}. The V_{DDA} pin needs external bypassing to GND by means of a 2.2 µF X5R or X7R ceramic capacitor, placed as close as possible to the module.

V_{DDP} is the power supply rail for the gate drivers and bootstrap circuit. This pin is bypassed to GND_EXT by means of an internal high-frequency ceramic capacitor. For this reason, the GND_EXT pins should be routed with a low-inductance path to the GND net. An internal 10Ω resistor is provided between V_{DDA} and V_{DDP}, allowing the implementation of a switching noise attenuation RC filter with the minimum amount of external components. It is possible, although typically not necessary, to lower the RC time constant by connecting an external resistor between V_{DDA} and V_{DDP}.

If the input rail is within 4.5V to 5.5V, it is possible to bypass the internal LDO by connecting V_{IN}, V_{DDA} and V_{DDP} together. Local decoupling of the V_{DDA} pin is still recommended.

4.3 Pin-Strapping Programmability (VOSET0, VOSET1, FREQ, I_{LIM})

The MIC45404 uses pin strapping to set the output voltage (VOSET0, VOSET1), switching frequency (FREQ) and current limit (I_{LIM}). No external passives are needed, therefore, the external component count is minimized. Each pin is a three-state input (connect to GND for LOW logic level, connect to V_{DDA} for HIGH logic level or leave unconnected for High Z). The logic level of the pins is read and frozen in the internal configuration logic immediately after the V_{DDA} rail comes up and becomes stabilized. After this instant, any change of the input logic level on the pins will have no effect until the V_{DDA} power is cycled again. The values corresponding to each particular pin strapping configuration are detailed in **Section 5.0 "Application Information"**.

4.4 Enable/Delay (EN/DLY)

The EN/DLY pin is a dual threshold pin that turns the internal LDO on/off and starts/stops the power delivery to the output, as shown in Figure 4-1.

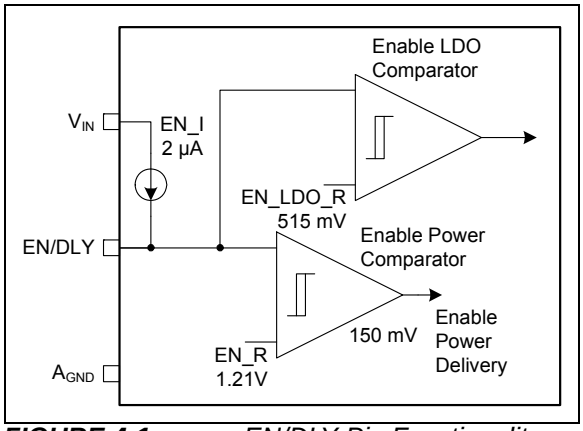


FIGURE 4-1: *EN/DLY Pin Functionality.*

The threshold for LDO enable is 515 mV (typical) with a hysteresis of approximately 30 mV. This hysteresis is enough because at the time of LDO activation, there is still no switching activity.

The threshold for power delivery is a precise 1.21V, ±70 mV. A 150 mV typical hysteresis prevents chattering due to switching noise and/or slow edges.

A 2 µA typical pull-up current, with ±1 µA accuracy, permits the implementation of a start-up delay by means of an external capacitor. In this case, it is necessary to use an open-drain driver to disable the MIC45404 while maintaining the start-up delay function.

4.5 Power Good (PG)

The PG pin is an open-drain output that requires an external pull-up resistor to a pull-up voltage (V_{PU_PG}), lower than 5.5V, for being asserted to a logic HIGH level. The PG pin is asserted with a typical delay of 0.45 ms when the output voltage (OUTSNS) reaches 92.5% of its target regulation voltage. This pin is deasserted with a typical delay of 80 µs when the output voltage falls below 90% of its target regulation voltage. The PG falling delay acts as a deglitch timer against very short spikes. The PG output is always immediately deasserted when the EN/DLY pin is below the power delivery enable threshold (EN_R/EN_F). The pull-up resistor should be large enough to limit the PG pin current to below 2 mA.

4.6 Inductor (LX, OUT) and Bootstrap (BST) Pins

The internal inductor is connected across the LX and OUT pins. The high-side MOSFET driver circuit is powered between BST and LX by means of an internal capacitor that is replenished from rail V_{DDP} during the low-side MOSFET on time. The bootstrap diode is internal.

4.7 Output Sensing (OUTSNS) and Compensation (COMP) Pins

OUTSNS should be connected exactly to the desired Point-of-Load (POL) regulation, avoiding parasitic resistive drops. The impedance seen into the OUTSNS pin is high (tens of kΩ or more, depending on the selected output voltage value), therefore, its loading effect is typically negligible. OUTSNS is also used by the slope compensation generator.

The COMP pin is the connection for the external compensation network. COMP is driven by the output of the transconductance error amplifier. Care must be taken to return the compensation network ground directly to A_{GND}.

4.8 Soft Start

The MIC45404 internal reference is ramped up at a 0.42 V/ms rate. Note that this is the internal reference soft start slew rate and that the actual slew rate seen at the output should take into account the internal divider attenuation, as detailed in the **Section 5.0 "Application Information"**.

4.9 Switching Frequency (FREQ)

The MIC45404 features three different selectable switching frequencies (400 kHz, 565 kHz and 790 kHz). Frequency selection is tied with a specific output voltage selection, as described in **Section 5.5 "Permissible MIC45404 Settings Combinations"**.

4.10 Pre-Biased Output Start-up

The MIC45404 is designed to achieve safe start-up into a pre-biased output without discharging the output capacitors.

4.11 Thermal Shutdown

The MIC45404 has a thermal shutdown protection that prevents operation at excessive temperature. The thermal shutdown threshold is typically set at +160°C, with a hysteresis of +25°C.

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4.12 Overcurrent Protection (I_{LIM}) and Hiccup Mode Short-Circuit Protection

The MIC45404 features instantaneous cycle-by-cycle current limit with current sensing, both on the low-side and high-side switches. It also offers a Hiccup mode for prolonged overloads or short-circuit conditions.

The low-side cycle-by-cycle protection detects the current level of the inductor current during the low-side MOSFET on time. The high-side MOSFET turn-on is inhibited as long as the low-side MOSFET current limit is above the overcurrent threshold level. The inductor current will continue decaying until the current falls below the threshold, where the high-side MOSFET will be enabled again, according to the duty cycle requirement from the PWM modulator.

The low-side current limit has three different programmable levels (for 3A, 4A and 5A loads) in order to fit different application requirements. Since the low-side current limit acts on the valley current, the DC output current level (I_{OUT}), where the low-side cycle-by-cycle current limit is engaged, will be higher than the current limit value by an amount equal to $\Delta IL_{PP}/2$, where ΔIL_{PP} is the peak-to-peak inductor ripple current.

The high-side current limit is approximately 1.4-1.5 times greater than the low-side current limit (typical values). The high-side cycle-by-cycle current limit immediately truncates the high-side on time without waiting for the off clocking event.

A Leading-Edge Blanking (LEB) timer (108 ns, typical) is provided on the high-side cycle-by-cycle current limit to mask the switching noise and to prevent falsely triggering the protection. The high-side cycle-by-cycle current limit action cannot take place before the LEB timer expires.

Hiccup mode protection reduces power dissipation in permanent short-circuit conditions. On each clock cycle, where a low-side cycle-by-cycle current limit event is detected, a 4-bit up/down counter is incremented. On each clock cycle without a concurrent low-side current limit event, the counter is decremented or left at zero. The counter cannot wraparound below '0000' and above '1111'. High-side current limit events do not increment the counter. Only detections from low-side current limit events trigger the counter.

If the counter reaches '1111' (or 15 events), the high and low-side MOSFETs become tri-stated, and power delivery to the output is inhibited for the duration of three times the soft start time. This digital integration mechanism provides immunity to momentary overloading of the output. After the wait time, the MIC45404 retries entering operation and initiates a new soft start sequence.

Figure 4-2 illustrates the Hiccup mode short-circuit protection logic flow. Note that Hiccup mode short-circuit protection is active at all times, including the soft start ramp.

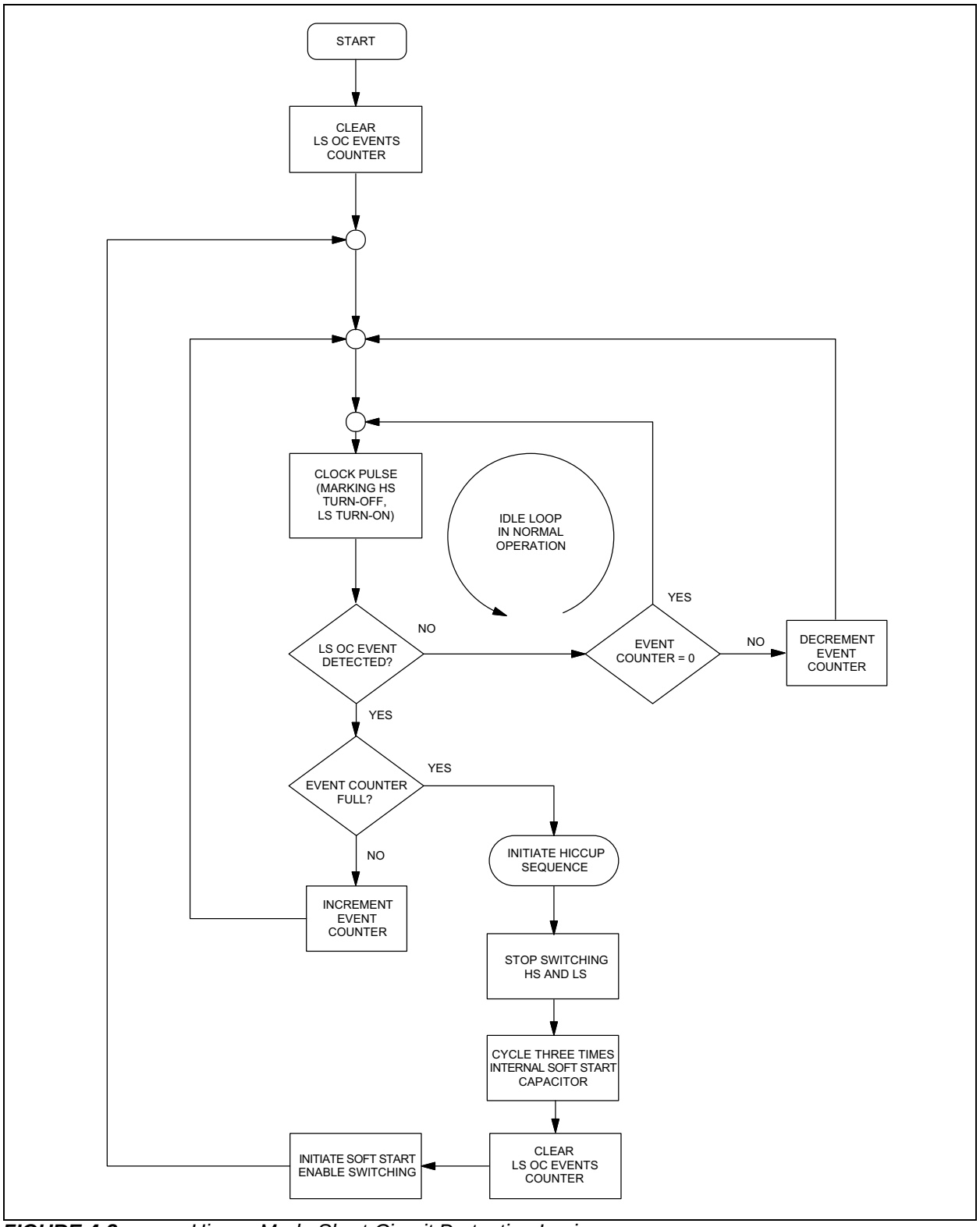


FIGURE 4-2: *Hiccup Mode Short-Circuit Protection Logic.*

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5.0 APPLICATION INFORMATION

5.1 Programming Start-up Delay and External UVLO

The EN/DLY pin allows programming an external start-up delay. In this case, the driver for the EN/DLY pin should be an open-drain/open-collector type, as shown in Figure 5-1.

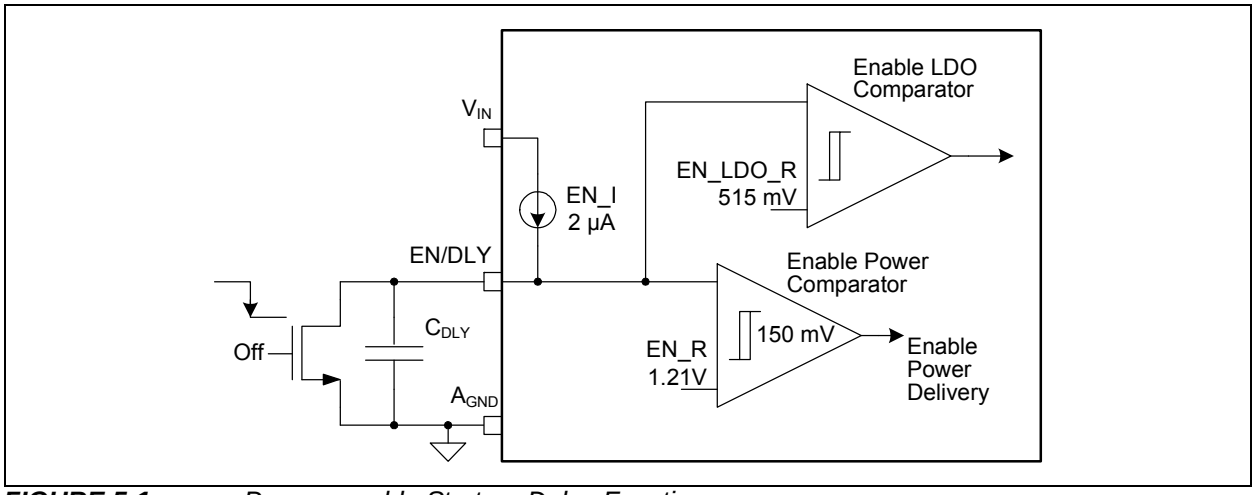


FIGURE 5-1: *Programmable Start-up Delay Function.*

The start-up delay is the delay time from the off falling edge to the assertion of the enable power delivery signal. It can be calculated as shown in Equation 5-1:

EQUATION 5-1:

$$t_{SU_DLY} = \frac{EN_R \times C_{DLY}}{EN_I}$$

Where:

EN_R = 1.21V
EN_I = 2 µA
C_{DLY} = Delay programming external capacitor

The EN/DLY pin can also be used to program a UVLO threshold for power delivery by means of an external resistor divider, as described in Figure 5-2.

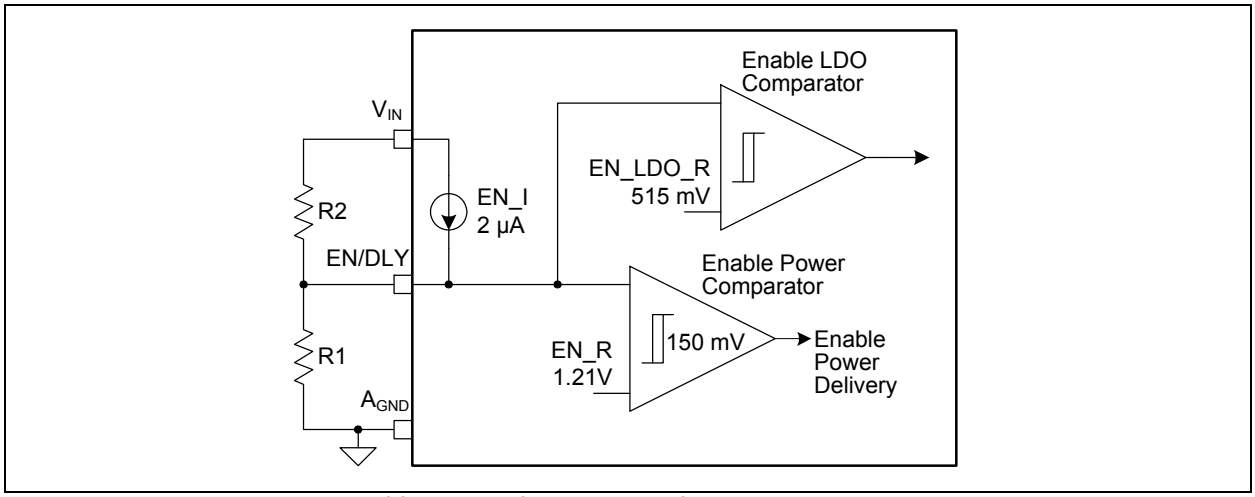


FIGURE 5-2: *Programmable External UVLO Function.*

The programmed V_{IN} UVLO threshold, V_{IN_RISE}, is given by:

EQUATION 5-2:

$$V_{IN_RISE} = EN_R \times \left(1 + \frac{R_2}{R_1}\right) - EN_I \times R_2$$

Where:

EN_R = 1.21V
EN_I = 2 µA
R_1 and R_2 = External resistors

To desensitize the V_{IN} UVLO threshold against variations of the pull-up current, EN_I, it is recommended to run the $R_1 – R_2$ voltage divider at a significantly higher current level than the EN_I current.

The corresponding V_{IN} UVLO hysteresis, V_{IN_HYS}, is calculated as follows:

EQUATION 5-3:

$$V_{IN_HYS} = 150\ mV \times \left(1 + \frac{R_2}{R_1}\right)$$

Similar calculations also apply to the internal LDO activation threshold.

5.2 Setting the Switching Frequency

The MIC45404 switching frequency can be programmed using FREQ, as shown in Table 5-1.

TABLE 5-1: SWITCHING FREQUENCY SETTINGS

FREQ Pin Setting	Frequency
High Z (open)	400 kHz
0 (GND)	565 kHz
1 (V_{DDA})	790 kHz

The switching frequency setting is not arbitrary, but it needs to be adjusted according to the particular output voltage selection due to peak-to-peak inductor ripple requirements. This is illustrated in **Section 5.5 "Permissible MIC45404 Settings Combinations"**.

5.3 Setting the Output Voltage

The MIC45404 output voltage can be programmed by setting pins, VOSET0 and VOSET1, as shown in Table 5-2.

TABLE 5-2: OUTPUT VOLTAGE SETTINGS

VOSET1	VOSET0	Output Voltage
0 (GND)	0 (GND)	3.3V
0 (GND)	1 (V_{DDA})	2.5V (2.49V)
1 (V_{DDA})	0 (GND)	1.8V
1 (V_{DDA})	1 (V_{DDA})	1.5V
0 (GND)	High Z (open)	1.2V
High Z (open)	0 (GND)	1.0V
1 (V_{DDA})	High Z (open)	0.9V
High Z (open)	1 (V_{DDA})	0.8V
High Z (open)	High Z (open)	0.7V

To achieve accurate output voltage regulation, the OUTSNS pin (internal feedback divider top terminal) should be Kelvin-connected as close as possible to the point of regulation top terminal. Since both the internal reference and the internal feedback divider's bottom terminal refer to A_{GND}, it is important to minimize voltage drops between the A_{GND} and the point of regulation return terminal.

5.4 Setting the Current Limit

The MIC45404's valley-mode current limit on the low-side MOSFET can be programmed by means of I_{LIM} as shown in Table 5-3.

TABLE 5-3: CURRENT LIMIT SETTINGS

I_{LIM}	Valley Current Limit (Typical Value)	Rated Output Current
0 (GND)	4.6 A	3A
1 (V_{DDA})	6.2 A	4A
High Z (open)	6.8 A	5A

Note that the programmed current limit values act as pulse-by-pulse, current limit thresholds on the valley inductor current. If the inductor current has not decayed below the threshold at the time the PWM requires a new on time, the high-side MOSFET turn-on is either delayed, until the valley current recovers below the threshold, or skipped. Each time the high-side MOSFET turn-on is skipped, a 4-bit up-down counter is incremented. When the counter reaches the configuration '1111', a hiccup sequence is invoked in order to reduce power dissipation under prolonged short-circuit conditions.

The highest current limit setting (6.8A) is intended to comfortably accommodate a 5A application. Ensure that the value of the operating junction temperature does not exceed the maximum rating in high output power applications.

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5.5 Permissible MIC45404 Settings Combinations

The MIC45404 allowable settings are constrained by the values in Table 5-4.

TABLE 5-4: PERMISSIBLE MIC45404 SETTINGS COMBINATIONS

Output Voltage	Frequency
3.3V	790 kHz
2.5V (2.49V)	
1.8V	565 kHz
1.5V	
1.2V	400 kHz
1.0V	
0.9V	
0.8V	
0.7V	

5.6 Output Capacitor Selection

Two main requirements determine the size and characteristics of the output capacitor, C_O:

- Steady-state ripple
- Maximum voltage deviation during load transient

For steady-state ripple calculation, both the ESR and the capacitive ripple contribute to the total ripple amplitude. The MIC45404 utilizes a low loss inductor, whose nominal value is 1.2 µH. From the switching frequency, input voltage, output voltage setting and load current, the peak-to-peak inductor current ripple and the peak inductor current can be calculated as:

EQUATION 5-4:

$$\Delta I_{L_PP} = V_O \times \left(\frac{1 - \frac{V_O}{V_{IN}}}{f_S \times L} \right)$$

EQUATION 5-5:

$$I_{L,PEAK} = I_O + \frac{\Delta I_{L_PP}}{2}$$

The capacitive ripple, $\Delta V_{r,C}$, and the ESR ripple, $\Delta V_{r,ESR}$, are given by:

EQUATION 5-6:

$$\Delta V_{R,C} = \frac{\Delta I_{L_PP}}{8 \times f_S \times C_O}$$

EQUATION 5-7:

$$\Delta V_{R,ESR} = ESR \times \Delta I_{L_PP}$$

The total peak-to-peak output ripple is then conservatively estimated as:

EQUATION 5-8:

$$\Delta V_R \cong \Delta V_{R,C} + \Delta V_{R,ESR}$$

The output capacitor value and ESR should be chosen such that ΔV_R is within specifications. Capacitor tolerance should be considered for worst-case calculations. In case of ceramic output capacitors, factor into account the decrease of effective capacitance versus applied DC bias.

The worst-case load transient for output capacitor calculation is an instantaneous 100% to 0% load release when the inductor current is at its peak value. In this case, all the energy stored in the inductor is absorbed by the output capacitor, while the converter stops switching and keeps the low-side FET on.

The peak output voltage overshoot (ΔV_O) happens when the inductor current has decayed to zero. This can be calculated with Equation 5-9:

EQUATION 5-9:

$$\Delta V_O = \sqrt{V_O^2 + \frac{L}{C_O} \times I_{L,PEAK}^2} - V_O$$

Equation 5-10 calculates the minimum output capacitance value ($C_{O(MIN)}$) needed to limit the output overshoot below ΔV_O.

EQUATION 5-10:

$$C_{O(MIN)} = \frac{L \times I_{L,PEAK}^2}{(\Delta V_O + V_O)^2 - V_O^2}$$

The result from the minimum output capacitance value for load transient is the most stringent requirement found for capacitor value in most applications. Low Equivalent Series Resistance (ESR) ceramic output capacitors, with X5R or X7R temperature ratings, are recommended.

For low output voltage applications with demanding load transient requirements, using a combination of polarized and ceramic output capacitors may be the most convenient option for smallest solution size.

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5.7 Input Capacitor Selection

Two main requirements determine the size and characteristics of the input capacitor:

- Steady-State Ripple
- RMS Current

The Buck Converter input current is a pulse train with very fast rising and falling times, so low-ESR ceramic capacitors are recommended for input filtering because of their good high-frequency characteristics.

By assuming an ideal input filter (which can be assimilated to a DC input current feeding the filtered buck power stage) and by neglecting the contribution of the input capacitor ESR to the input ripple (which is typically possible for ceramic input capacitors), the minimum capacitance value, $C_{IN(MIN)}$, needed for a given input peak-to-peak ripple voltage, $\Delta V_{r, IN}$, can be estimated as shown in Equation 5-11:

EQUATION 5-11:

$$C_{IN(MIN)} = \frac{I_O \times D \times (1-D)}{\Delta V_{r,IN} \times f_S}$$

Where:

D is the duty cycle at the given operating point.

The RMS current, $I_{IN,RMS}$, of the input capacitor is estimated as in Equation 5-12:

EQUATION 5-12:

$$I_{IN,RMS} = I_O \times \sqrt{D \times (1-D)}$$

Note that, for a given output current, I_O, worst-case values are obtained at D = 0.5.

Multiple input capacitors can be used to reduce input ripple amplitude and/or individual capacitor RMS current.

5.8 Compensation Design

As a simple first-order approximation, the Valley Current mode controlled buck power stage can be modeled as a voltage controlled current source, feeding the output capacitor and load. The inductor current state variable is removed and the power stage transfer function from COMP to the inductor current is modeled as a transconductance (Gm_{PS}). The simplified model of the control loop is shown in Figure 5-3. The power stage transconductance, Gm_{PS}, shows some dependence on current levels and it is also somewhat affected by process variations, therefore, some design margin is recommended against the typical value, Gm_{PS} = 12.5A/V (see **Section 1.0 "Electrical Characteristics"**).

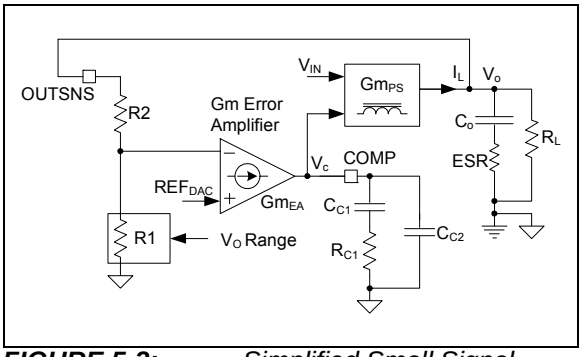


FIGURE 5-3: *Simplified Small Signal Model of the Voltage Regulation Loop.*

This simplified approach disregards all issues related to the inner current loop, like its stability and bandwidth. This approximation is good enough for most operating scenarios, where the voltage loop bandwidth is not pushed to aggressively high frequencies.

Based on the model shown in Figure 5-3, the control-to-output transfer function is:

EQUATION 5-13:

$$G_{CO(S)} = \frac{V_{O(S)}}{V_{C(S)}} = Gm_{PS} \times R_L \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)}$$

Where f_Z and f_P = the frequencies associated with the output capacitor ESR zero and with the load pole, respectively:

$$f_Z = \frac{1}{2\pi \times C_O \times ESR}$$

$$f_P = \frac{1}{2\pi \times C_O \times (ESR + R_L)}$$

The MIC45404 module uses a transconductance (Gm_{EA} = 1.4 mA/V) error amplifier. Frequency compensation is implemented with a Type-II network (R_{C1}, C_{C1} and C_{C2}) connected from the COMP to A_{GND}. The compensator transfer function consists of an integrator for zero DC voltage regulation error, a zero to boost the phase margin of the overall loop gain around the crossover frequency and an additional pole that can be used to cancel the output capacitor ESR zero, or to further attenuate switching frequency ripple. In both cases, the additional pole makes the regulation loop less susceptible to switching frequency noise. The additional pole is created by capacitor C_{C2} (internally provided, C_{C2} value is 47 pF). Equation 5-14 details the compensator transfer function, $H_{C(S)}$ (from OUTSNS to COMP).

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EQUATION 5-14:

$$H_{C(S)} = -\frac{R1}{R1 + R2} \times Gm_{EA} \times \frac{1}{S \times (C_{C1} + C_{C2})} \times \frac{(1 + S \times R_{C1} \times C_{C1})}{\left(1 + S \times R_{C1} \times \frac{C_{C1} \times C_{C2}}{C_{C1} + C_{C2}}\right)}$$

The overall voltage loop gain, $T_{V(S)}$, is the product of the control-to-output and the compensator transfer functions:

EQUATION 5-15:

$$T_{V(S)} = G_{CO(S)} \times H_{C(S)}$$

The value of the attenuation ratio, R1/(R1 + R2), depends on the output voltage selection and can be retrieved as illustrated in Table 5-5:

TABLE 5-5: INTERNAL FEEDBACK DIVIDER ATTENUATION VALUES

V_O Range	R1/(R1 + R2)	A (A = 1 + R2/R1)
0.7V-1.2V	1	1
1.5V-1.8V	0.5	2
2.5V(2.49V)-3.3V	0.333	3

The compensation design process is as follows:

1. Set the $T_{V(s)}$ loop gain crossover frequency, f_{XO}, in the range of $f_S/20$ to $f_S/10$. Lower values of f_{XO} allow a more predictable and robust phase margin. Higher values of f_{XO} would involve additional considerations about the current loop bandwidth in order to achieve a robust phase margin. Taking a more conservative approach is highly recommended.

EQUATION 5-16:

$$\frac{f_S}{20} \leq f_{XO} \leq \frac{f_S}{10}$$

2. Select R_{C1} to achieve the target crossover frequency, f_{XO}, of the overall voltage loop. This typically happens where the power stage transfer function, $G_{CO(S)}$, is rolling off at -20 dB/decade. The compensator transfer function, $H_{C(S)}$, is in the so-called midband gain region, where C_{C1} can be considered a DC blocking short circuit, while C_{C2} can still be considered as an open circuit, as calculated in Equation 5-17:

EQUATION 5-17:

$$R_{C1} = \left(\frac{R1 + R2}{R1}\right) \times \frac{2\pi \times C_O \times f_{XO}}{Gm_{EA} \times Gm_{PS}}$$

3. Select capacitor C_{C1} to place the compensator zero at the load pole. The load pole moves around with load variations, so to calculate the load pole use as a load resistance R_L, the value determined by the nominal output current, I_O, of the application, as shown in Equation 5-18 and Equation 5-19:

EQUATION 5-18:

$$R_L = \frac{V_O}{I_O}$$

EQUATION 5-19:

$$C_{C1} = \frac{C_O \times (ESR + R_L)}{R_{C1}}$$

4. Knowing that an internal C_{C2} capacitor of 47 pF is provided already, find out if any additional capacitance is needed to augment the overall value of the capacitor, C_{C2}.

The C_{C2} (total value) is intended for placing the compensator pole at the frequency of the output capacitor ESR zero and/or achieve additional switching ripple/noise attenuation.

If the output capacitor is a polarized one, its ESR zero will typically occur at low enough frequencies to cause the loop gain to flatten out and not roll off at a -20 dB/decade slope, around or just after the crossover frequency, f_{XO}. This causes undesirable scarce compensation design robustness and switching noise susceptibility. The compensator pole is then used to cancel the output capacitor ESR zero and achieve a well-behaved roll-off of the loop gain above the crossover frequency.

If the output capacitors are only ceramic, then the ESR zeros frequencies could be very high. In many cases, the frequencies could even be above the switching frequency itself. Loop gain roll-off at -20 dB/decade is ensured well beyond the crossover frequency, but even in this case, it is good practice to still make use of the compensator pole to further attenuate switching noise, while conserving phase margin at the crossover frequency.

For example, setting the compensator pole at 5 f_{XO} will limit its associated phase loss at the crossover frequency to about 11°. Placement at even higher frequencies, N × f_{XO} (N > 5), will reduce phase loss even further at the expense of less noise/ripple attenuation at the switching frequency. Some attenuation of the switching frequency noise/ripple is achieved as long as N × f_{XO} < f_S.

For the polarized output capacitor, compensator pole placement at the ESR zero frequency is achieved, as shown in Equation 5-20:

EQUATION 5-20:

$$C_{C2} = \frac{1}{\frac{R_{C1}}{C_O \times ESR} - \frac{1}{C_{C1}}}$$

For the ceramic output capacitor, compensator pole placement at N × f_{XO} (N ≥ 5, N × f_{XO} < f_S) is achieved, as detailed in Equation 5-21:

EQUATION 5-21:

$$C_{C2} = \frac{1}{2\pi \times R_{C1} \times N \times f_{XO} - \frac{1}{C_{C1}}}$$

The MIC45404 already provides an internal C_{C2} capacitor of 47 pF. Therefore, the external capacitance, C_{C2_EXT}, that should be added is given by Equation 5-22:

EQUATION 5-22:

$$C_{C2_EXT} = max(C_{C2} - 47\ pF, 0\ pF)$$

If the result, C_{C2} – 47 pF, yields to zero or to a negative number, no additional external capacitance is needed for C_{C2}.

5.9 Output Voltage Soft Start Rate

The MIC45404 features an internal analog soft start, such that the output voltage can be smoothly increased to the target regulation voltage. The soft start rate given in **Section 1.0 "Electrical Characteristics"** is referred to the error amplifier reference, and therefore, the effective soft start rate value, seen at the output of the module, has to be scaled according to the internal feedback divider attenuation values listed in Table 5-5. To calculate the effective output voltage soft start slew rate, SS_SR_{OUT}, based on the particular output voltage setting and the reference soft start slew rate, SS_SR, use the following formula:

EQUATION 5-23:

$$SS_SR_{OUT} = A \times SS_SR$$

Where:

A = Amplification

For the value of A, see the right column of Table 5-5.

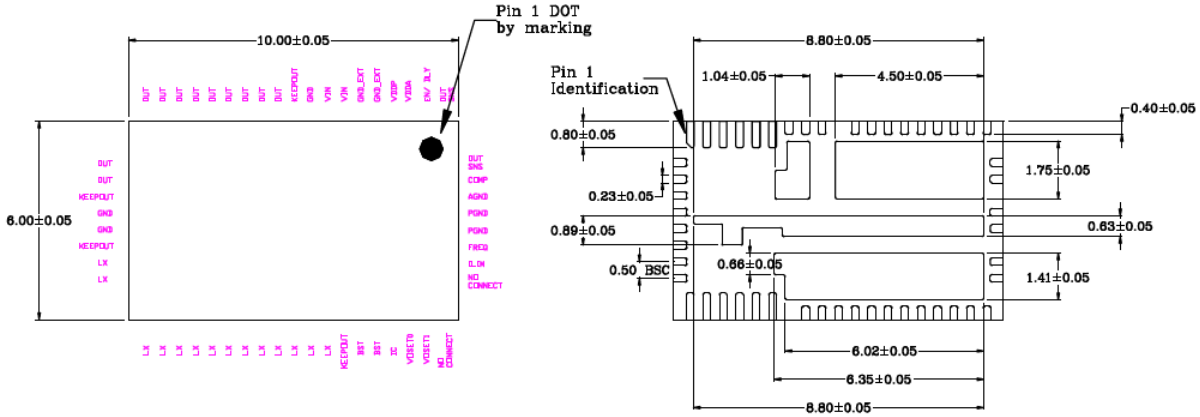
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6.0 PACKAGING INFORMATION

TITLE

54 LEAD P2QFN 10x6mm PACKAGE (PIP Module) OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	P2QFN106-54LD-PL-1	UNIT	MM
Lead Frame	Copper	Lead Finish	Matte Tin

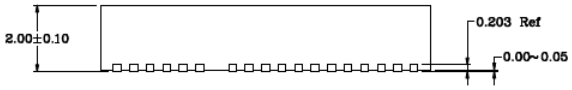


TOP VIEW

NOTE : 1, 2, 3

BOTTOM VIEW

NOTE : 1, 2, 3



SIDE VIEW

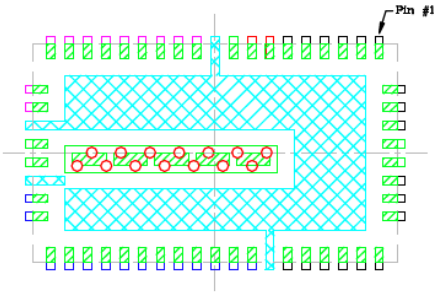
NOTE : 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLES IN LAND PATTERN REPRESENTS THERMAL VIA. RECOMMENDED SIZE IS 0.30-0.35mm, AT 0.80mm PITCH & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. CYAN COLORED (SHADED) PAD REPRESENT EXPOSED TRACE KEEP OUT AREA.
7. RECOMMENDED LAND PATTERN TOLERANCE IS 0.020mm UNLESS SPECIFIED.
8. SEE RECOMMENDED LAND PATTERN ON PAGE 2.

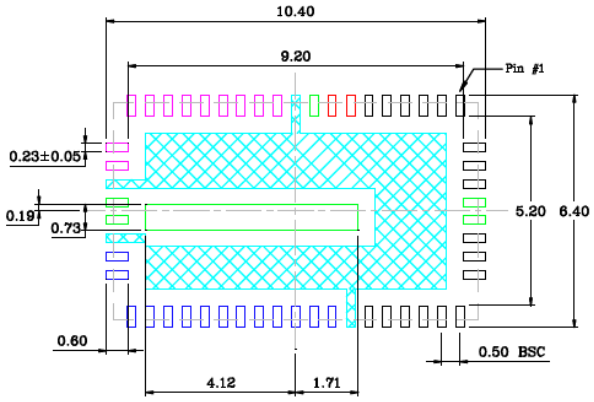
POD-Land Pattern Doc #: P2QFN106-54LD-PL-1-A

Recommended Land Pattern

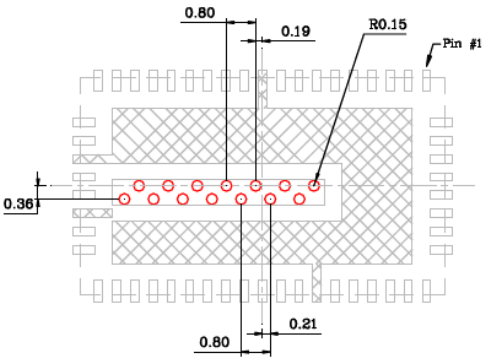
Note: 4,5,6,7,8



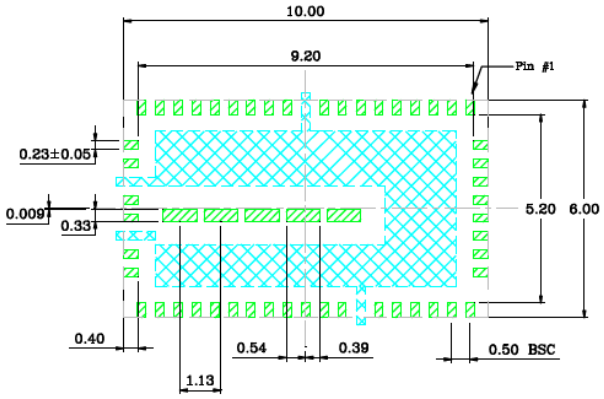
Stacked Up



Exposed Metal Trace



Thermal (filled) VIA



Solder Stencil Opening

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APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Original release of this document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	-XX[1]
Device	Lead Finish	Package Code	Tape and Reel Option

Device:	MIC45404: Ultra-low profile, synchronous step-down regulator module		
Lead Finish:	Y	=	Pb-Free with Industrial Temperature Grade
Package Code	MP	=	Module Package, thickness ≥ 2.0 mm
Tape and Reel Option:	TR	=	Tape and Reel[1]

Examples:

a) MIC45404YMP-TR: Pb-Free, 54 Lead 6 x 10 x 2 mm QFN Package, Tape and Reel.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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