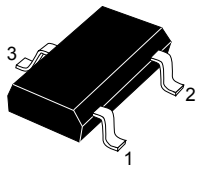
ESDA37W

Dual Transil™ array for ESD protection

Datasheet - production data



SOT323-3L

Features

- Unidirectional device
- Low leakage current (I_R max. < 1 µA at V_{RM})
- 300 W peak pulse power (8/20 µs)

Benefits

- High ESD protection level: up to 30 kV
- High integration
- Suitable for high density boards

Complies with the following standards

- IEC 61000-4-2 (exceeds level 4) :
  - 30 kV (air discharge)
  - 30 kV (contact discharge)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Entertainment
- Signal communications
- Connectivity
- Comfort and convenience

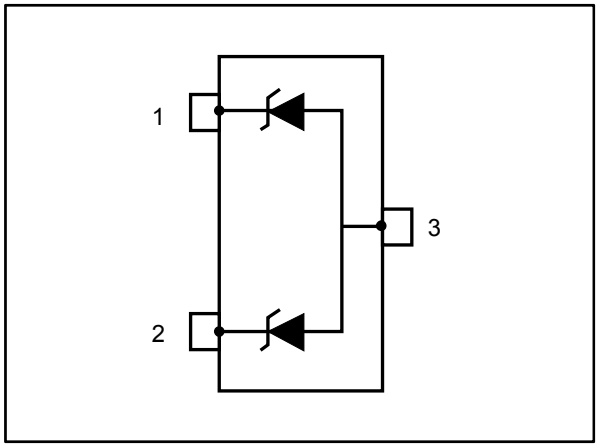
Description

This device is a diode array designed to protect 1 line or 2 lines against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

It can also be used a bidirectional suppressor by connecting only pin 1 and 2.

Figure 1: Functional diagram



This is information on a product in full production.

www.st.com

1 Characteristics

Table 1: Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage(1)	IEC 61000-4-2: Contact discharge Air discharge	 30 30	kV
P_{pp}	Peak pulse power (8/20 µs)		300	W
I_{pp}	Peak pulse current (8/20 µs)	ESDA37W	6.3	A
T_j	Operating junction temperature range		-40 to 150	°C
T_{stg}	Storage junction temperature range		-65 to 150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm from case		260	°C

Notes:

(1)For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2: Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
V_{RM}	=	Stand-off voltage
I_{RM}	=	Leakage current
I_F	=	Forward current
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward voltage drop
C	=	Capacitance
R_d	=	Dynamic impedance
αT	=	Voltage temperature

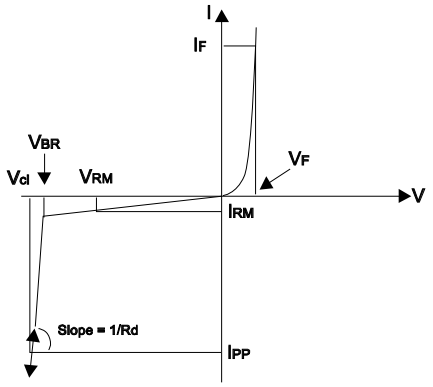


Table 2: Electrical characteristics (T_{amb} = 25 °C)

Order code	V_{BR} at I_R			I_{RM} at V_{RM}		R_d(1)	αT(2)	C_{line}	V_F at I_F	
	Min.	Max.		Max.		Typ.	Max.	Typ. at 0 V bias	Max.	
	V	V	mA	µA	V	mΩ	10^{-4}/°C	pF	V	mA
ESDA37W	37	43.3	1	1	36	2400	11	48	0.9	10

Notes:

(1)Square pulse I_{pp} = 15 A, t_p = 2.5 µs

(2)Δ V_{BR} = αT x (T_{amb} -25 °C) x V_{BR} (25 °C)

1.1 Characteristics (curves)

Figure 3: Peak pulse power dissipation versus initial junction temperature

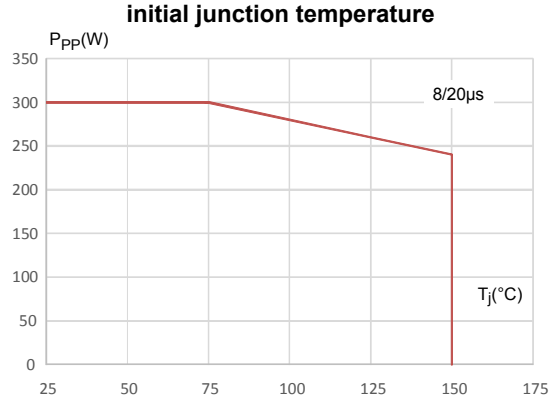


Figure 4: Peak pulse power versus exponential pulse duration (maximum values)

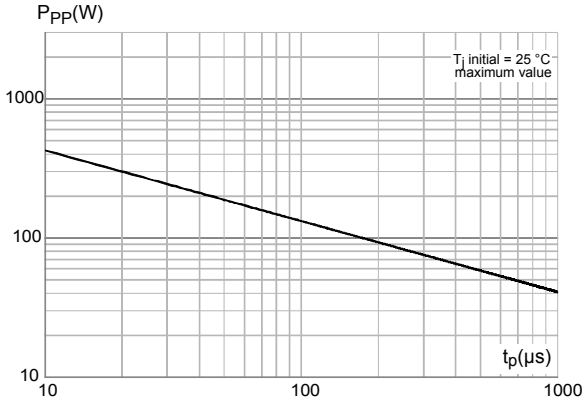


Figure 5: Variation of clamping voltage versus peak pulse current (maximum values)

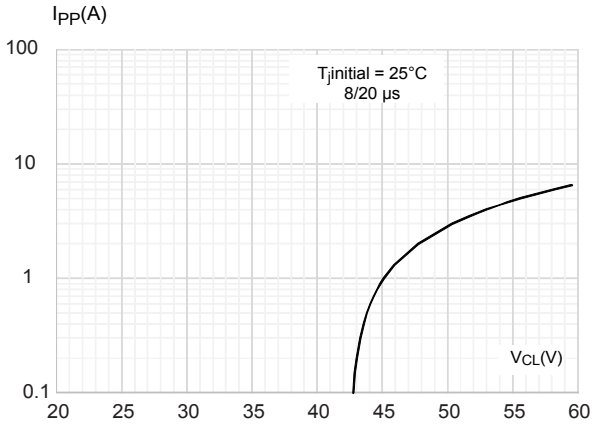
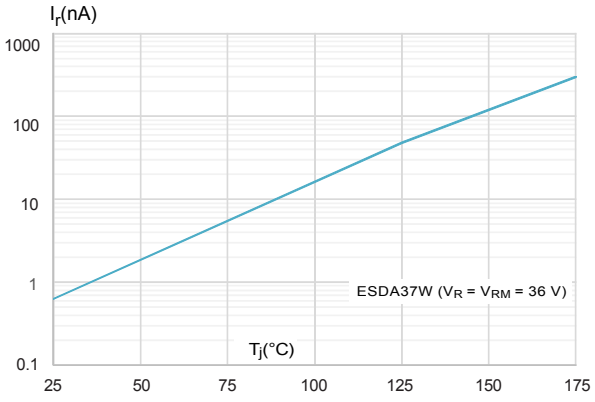


Figure 6: Variation of leakage current



2 Application and design guidelines

Refer to STMicroelectronics application note:

- AN2689: Protection of automotive electronics from electrical hazards, guidelines for design and component selection.

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

- Epoxy meets UL 94,V0
- Lead-free package

3.1 SOT323-3L package information

Figure 7: SOT323-3L package outline

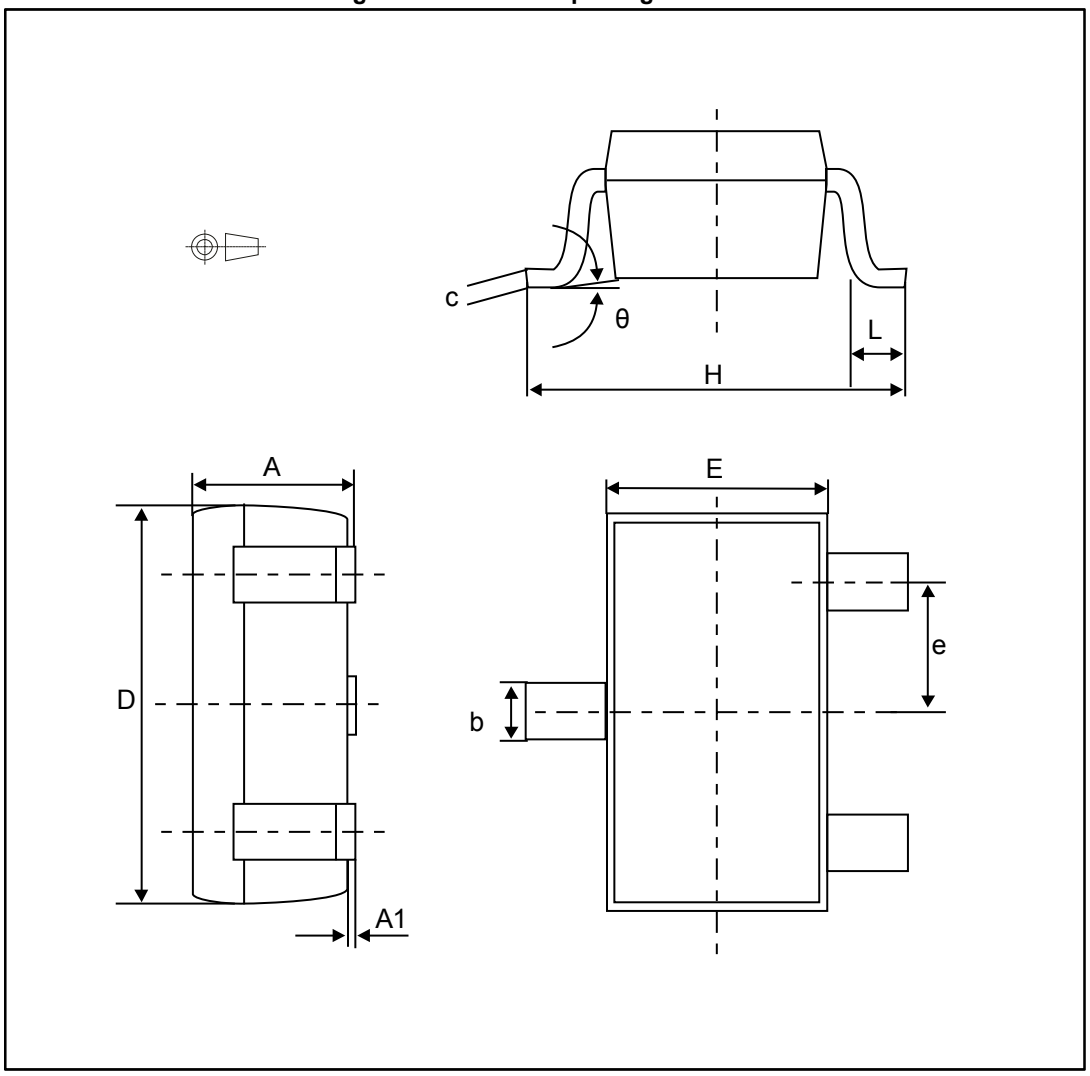
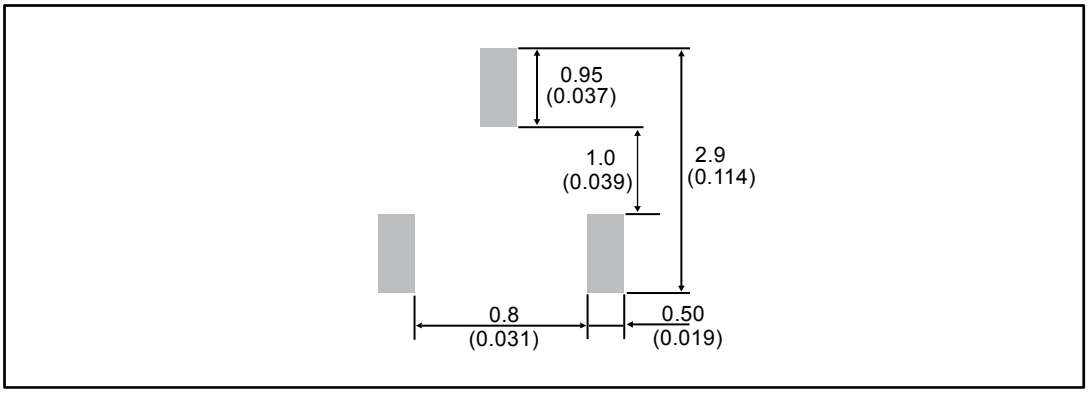


Table 3: SOT323-3L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.8		1.1	0.031		0.043
A1	0.0		0.1	0.000		0.003
b	0.25		0.4	0.0098		0.0157
c	0.1		0.26	0.003		0.0102
D	1.8	2.0	2.2	0.070	0.078	0.086
E	1.15	1.25	1.35	0.0452	0.0492	0.0531
e	0.60	0.65	0.70	0.024	0.026	0.028
H	1.8	2.1	2.4	0.070	0.082	0.094
L	0.1	0.2	0.30	0.004	0.008	0.012
Θ	0		30°	0		30°

Figure 8: SOT323-3L recommended footprint (dimensions in inches)



4 Recommendation on PCB assembly

4.1 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

4.2 Placement

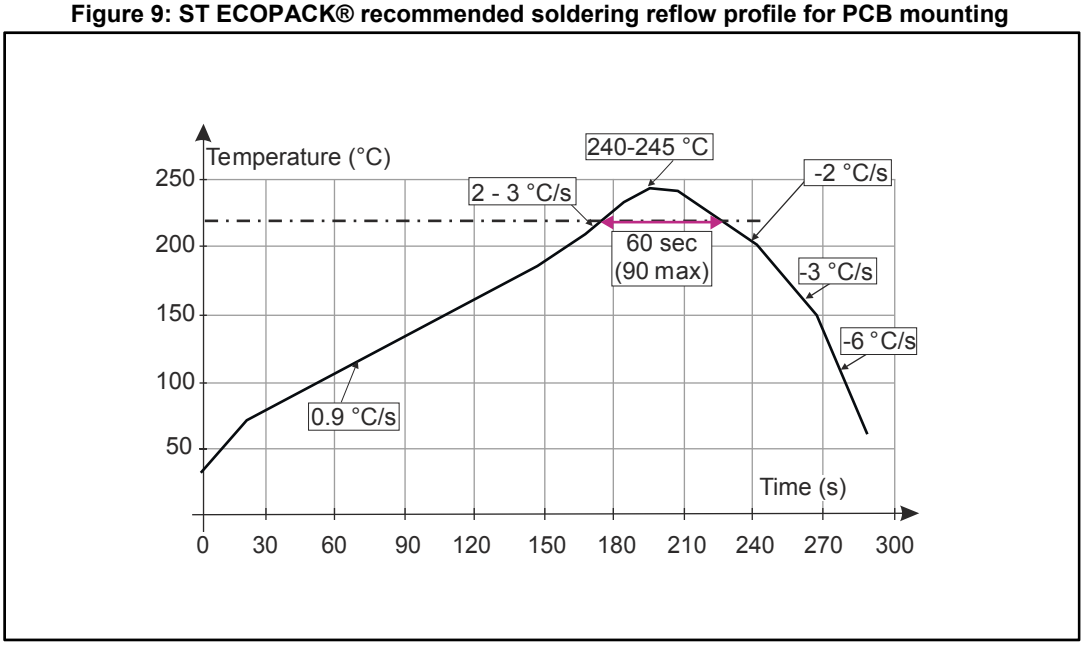
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.3 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

4.4 Reflow profile

Figure 9: ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Figure 10: Ordering information scheme

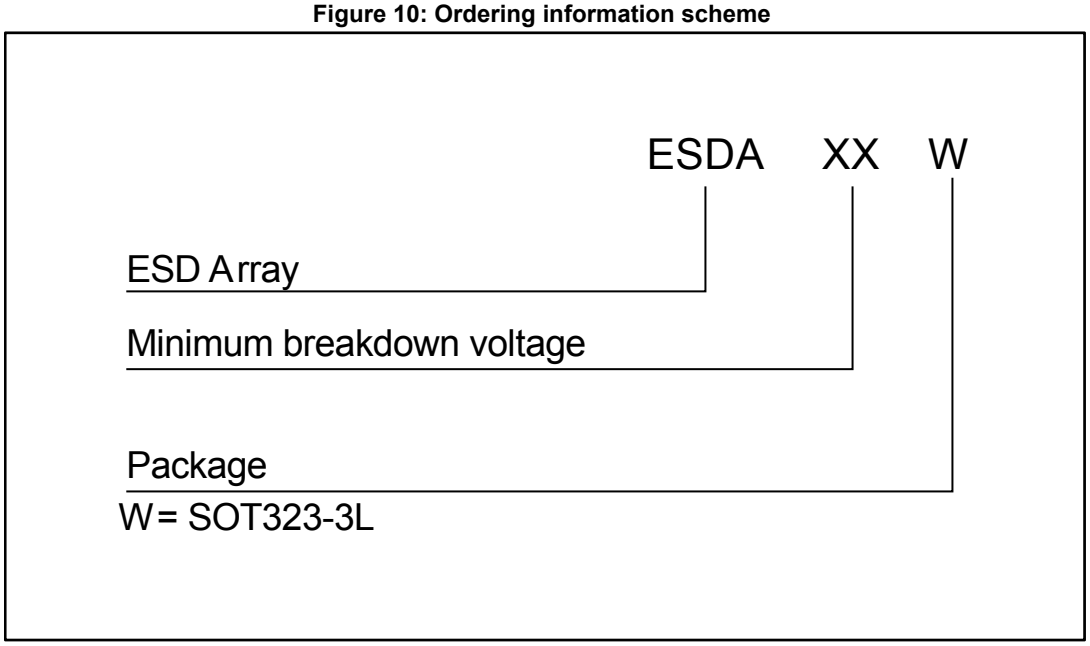


Table 4: Ordering information

Order code	Marking(1)	Package	Weight	Base qty.	Delivery mode
ESDA37W	E37	SOT323-3L	6.6 mg	3000	Tape and reel

Notes:

(1)The marking can be rotated by multiples of 90° to differentiate assembly location.

6 Revision history

Table 5: Document revision history

Date	Revision	Changes
18-Dec-2017	1	First issue.

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