

Evaluation Board for the **AD5791** 1 ppm 20-Bit, ± 1 LSB INL, Voltage Output DAC with Single and Dual Supply

FEATURES

Full-featured evaluation board for the **AD5791** with the **ADP5070** power solution

Power Solution generated from single 3.3 V supply.

PC control in conjunction with Analog Devices, Inc., **EVAL-SDP-CB1Z** SDP

PC software for control

EVALUATION KIT CONTENTS

EVAL-AD5791SDZ evaluation board

EV-ADR445-REFZ reference board

AD5791 evaluation software

GENERAL DESCRIPTION

This user guide supports the EVAL-AD5791SDZ evaluation board, Revision B. **UG-185** supports previous revisions of the evaluation board.

The EVAL-AD5791SDZ is a full-featured evaluation board, designed for the easy evaluation of all features of the **AD5791** voltage output, 20-bit digital-to-analog converter (DAC). The **AD5791** pins are accessible at on-board connectors for external connection. The evaluation board can be controlled by two means: via the on-board connector (J12) or via the system demonstration platform (SDP) connector (J14).

The evaluation board also integrates a power solution utilizing the **ADP5070** switching regulator and linear regulators (**ADP7118** and **ADP7182**) to generate a bipolar supply of up to -15 V and $+15$ V from a $+3.3$ V single supply. Alternatively, the DAC can be supplied with linear power supplies via the on-board connectors (J11 and J13).

A daughter board connected to the top right of the EVAL-AD5791SDZ includes a voltage reference to externally apply to the DAC.

The **EVAL-SDP-CB1Z** SDP board allows the EVAL-AD5791SDZ evaluation board to be controlled through the USB port of a Windows®-based PC featuring Windows XP or later when using the **AD5791** evaluation software.

The **AD5791** is a high precision, 20-bit DAC, designed to meet the requirements of precision control applications. The output range of the **AD5791** is configured by two reference voltage inputs. The device is specified to operate with a dual power supply of up to 33 V.

Complete specifications for the **AD5791** are available in the **AD5791** data sheet available from Analog Devices, which must be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD PHOTOGRAPH



Figure 1.

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REVISION HISTORY

6/2019—Rev. A to Rev. B

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6/2018—Rev. 0 to Rev. A

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1/2018—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES AND DEFAULT LINK OPTIONS

The EVAL-AD5791SDZ evaluation board can be powered using the on-board ADP5070 from a single voltage of 3.3 V to +5 V. The voltage sources available are an external single supply via the J11 connector and a supply sourced from the SDP controller board (EVAL-SDP-CB1Z).

Alternatively, the J13 connector can provide power to the board, instead of the ADP5070, and J13 is intended for use with well-regulated bench supplies. See Figure 2 for a functional block diagram.

With any of the possible options, set the link options on the evaluation board for the required operating setup first, before supplying the evaluation board.

Each supply is decoupled to the relevant ground plane with 10 μ F and 0.1 μ F capacitors. Each device supply pin is again decoupled with a 10 μ F and 0.1 μ F capacitor pair to the relevant ground plane.

The analog and digital planes are connected at one location close to the DAC. To avoid ground loop problems, do not connect AGND and DGND elsewhere in the system.

Table 1. Quick Start Jumper Configuration for ADP5070 and Bench Supply

Link No.	ADP5070 with LDOs	ADP5070	Bench Supply
LK2	Inserted	Inserted	Removed
LK5	Removed	Inserted	Inserted
LK6	Removed	Inserted	Not applicable
LK7	Removed	Inserted	Not applicable
LK8	B	B	B
LK9	B	B	A
LK10	B	B	A

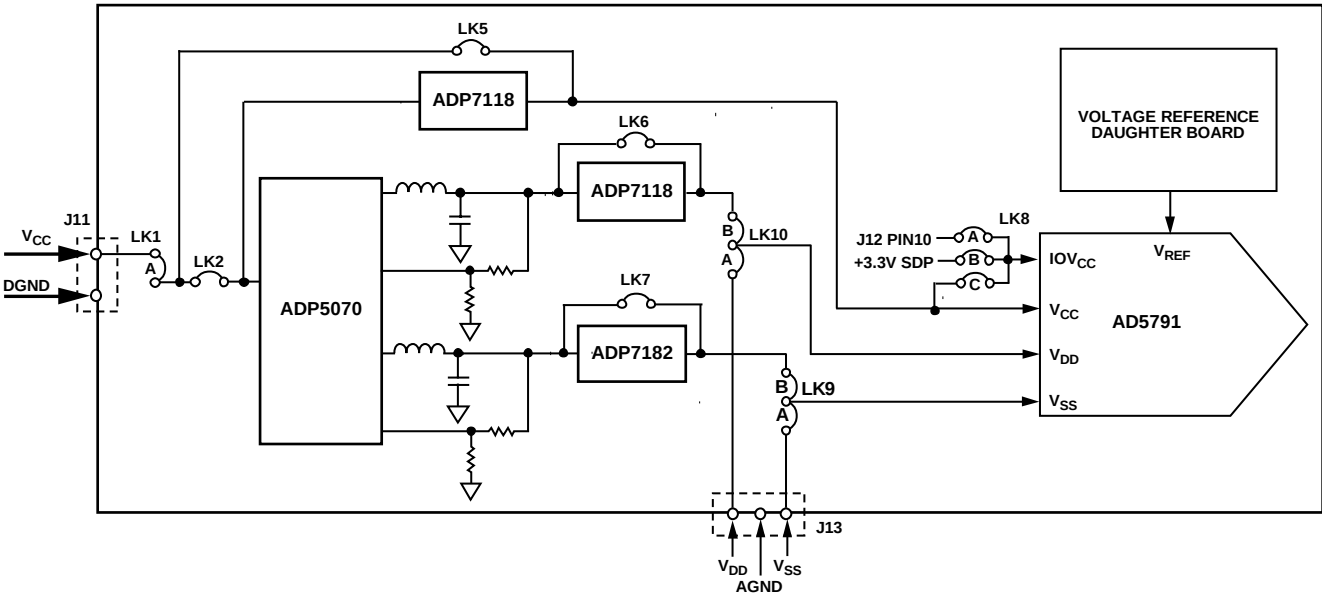


Figure 2. Powering the EVAL-AD5791SDZ Evaluation Board

POWER SOLUTION (ADP5070)—SINGLE-SUPPLY OPTION

The EVAL-AD5791SDZ board is populated with an [ADP5070](#) switching regulator. This regulator is preceded by voltage regulators ([ADP7118](#) and [ADP7182](#)) that can be bypassed if required. The supplies generated from the [ADP5070](#) alone or with the addition of the voltage regulators are -15 V and $+15\text{ V}$ from a $+3.3\text{ V}$ to $+5\text{ V}$ single supply. Link LK6 and Link LK7 must be inserted when the voltage regulators are bypassed.

The circuit was designed using the [ADIsimPower](#) toolset, which selects the components, generates the schematic and bill of materials, and displays the performance specifications. Visit the [ADP5070](#) product page to download the design tools.

The [ADP5070](#) requires a minimum voltage supply of 3.3 V for proper operation. Following the jumper configuration in Table 1 for the [ADP5070](#) alone or the [ADP5070](#) with low dropout regulators (LDOs) options, the evaluation board is supplied via the on-board J11 connector with an external 3.3 V single supply.

The J11 connector can be supplied with a range of 3.3 V to 5 V when Link LK5 is inserted, or with a range of 3.3 V to 18 V when Link LK5 is removed.

Link LK8 must be inserted to Position B if the board is supplied with a voltage larger than 3.3 V via the on-board J11 or J12 connectors.

Link LK1 must be inserted to Position A at all times. Refer to Table 3 for full link options.

BENCH POWER SUPPLY—DUAL SUPPLY OPTION

The evaluation board can be powered using a bench supply to allow all output voltage ranges of the [AD5791](#). A headroom and footroom of at least 2.5 V is required on the dual supply. It is important that the voltage across the negative analog supply (V_{SS}) and positive analog supply (V_{DD}) does not exceed the absolute maximum rating of 34 V . Otherwise, device reliability can be affected.

Following the jumper configuration in Table 1 for the bench supply configuration, supply the evaluation board with a dual supply of $V_{SS} = -15\text{ V}$ and $V_{DD} = 15\text{ V}$ via the J13 connector. The [AD5791](#) also requires users to apply a single supply of 3.3 V to 5 V to the V_{CC} pin and a single supply of 3.3 V to the IOV_{CC} pin that can be sourced via the J11 connector or the on-board J12 connector. Select the position of Link LK8 depending on the preferred source to supply the V_{CC} pin and the IOV_{CC} pin. Link LK8 must be inserted to Position B if the board is supplied with a voltage larger than 3.3 V via the on-board J11 or J12 connectors. Select the position of Link LK1 to Position A at all times. Refer to Table 3 for full link options.

VOLTAGE REFERENCE DAUGHTER BOARD

The daughter board inserted into Connector J1, Connector J4, and Connector J9 (available at the top right corner of the EVAL-AD5791SDZ evaluation board) includes a voltage reference. The voltage supplied by the voltage reference is gained up and inverted to provide the positive and negative reference voltages required by the [AD5791](#), which are routed to the EVAL-AD5791SDZ board via the J4 connector.

ADR445 Reference Board

The EVAL-AD5791SDZ evaluation kit provides the [EV-ADR445-REFZ](#) reference board to complete the hardware required to evaluate the [AD5791](#).

The [ADR445](#) is a 5 V low noise reference with $3\text{ ppm}/^{\circ}\text{C}$ maximum temperature drift and $2.25\text{ }\mu\text{V}$ p-p noise specifications across the operating temperature range. Figure 3 shows the typical integral nonlinearity (INL) performance.

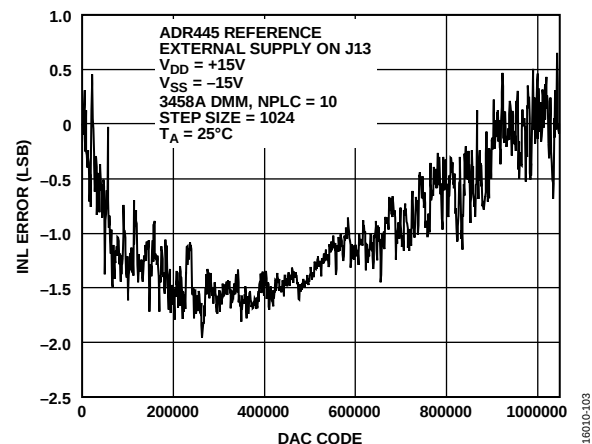


Figure 3. [AD5791](#) with [ADR445](#) INL Performance

Link JP1 selects the source of the reference voltage between the [ADR445](#) and an external 5 V reference voltage applied at the VR_EXT connector. Refer to Table 2 for the link details.

Table 2. JP1 Link Reference Voltage Selection

JP1 Link Position	Reference Voltage Selection
A	ADR445
B	5 V external reference voltage applied at VR_EXT connector

LTZ1000 and LTC6655 Reference Boards

The EV-LTZ1000-REFZ and EV-LTC6655-REFZ reference boards, including the LTZ1000 and LTC6655 voltage references respectively, are also available to evaluate the AD5791.

The LTZ1000 reference board components maintain the 1 ppm accuracy of the AD5791. The LTZ1000 is a 7.2 V ultraprecision reference specified with 0.05 ppm/°C temperature drift and ultra-low 1.2 μ V p-p noise. The voltage reference is used in conjunction with low drift amplifiers (ADA4077-2) and a low drift, thermally matched resistor for the scaling and gain circuits. Place a cover over the reference board to reduce thermal errors due to air currents flowing over the reference board. Figure 4 shows the typical INL performance using the LTZ1000 reference.

The LTC6655 reference board offers improved noise and temperature drift performance over the ADR445 solution. The LTC6655 is a low noise, low drift precision reference with 2 ppm/°C temperature drift and 1.25 μ V p-p noise. Figure 5 shows the typical INL performance of the AD5791 using the LTC6655 reference.

A minimum external unipolar supply of 3.3 V is required to supply the EVAL-AD5791SDZ with the EV-LTZ1000-REFZ board or with the EV-LTC6655-REFZ board combination. Alternatively, external dual supplies can supply the motherboard and daughter board.

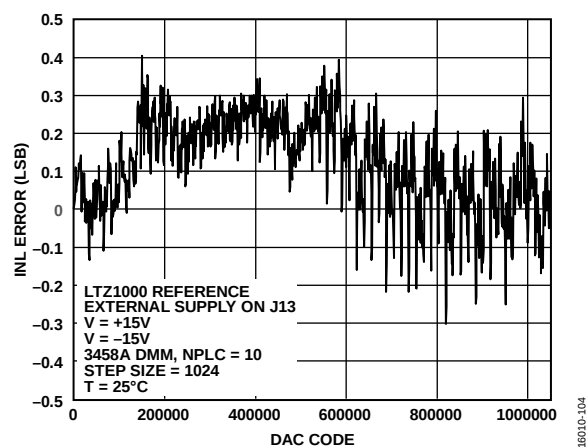


Figure 4. AD5791 with LTZ1000 INL Performance

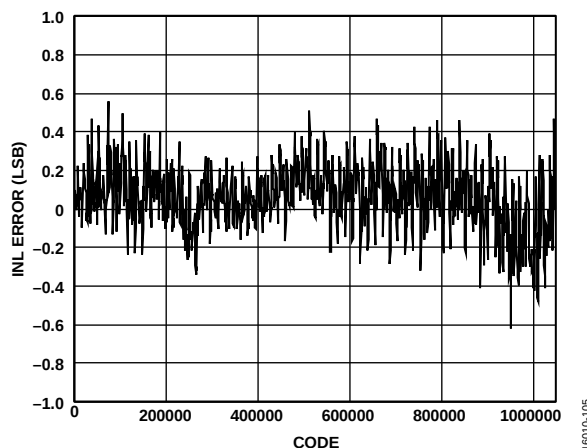


Figure 5. AD5791 with LTC6655 INL Performance

Table 3. Link Options

Link No.	Description
LK1	This link selects the source of the digital power supply from Connector J11. Position A must be selected at all times. Position A selects the source from the SDP board. Position B selects the source from Connector J12.
LK2	This link selects whether or not the power solution on the board is used to supply the AD5791. When this link is inserted, the ADP5070 dc-to-dc switch is used to supply the AD5791 in single supply. When this link is removed, the ADP5070 dc-to-dc switch is bypassed.
LK3	This link selects the state of the $\overline{\text{LDAC}}$ pin. When this link is inserted, $\overline{\text{LDAC}}$ is at logic low. When this link is removed, $\overline{\text{LDAC}}$ is at logic high.
LK4	This link selects the state of the $\overline{\text{RESET}}$ pin. When this link is inserted, $\overline{\text{RESET}}$ is at logic low. When this link is removed, $\overline{\text{RESET}}$ is at logic high.
LK5	This link selects the voltage source for the digital supply V_{CC} pin. When this link is inserted, the digital supply is sourced from an external 3.3 V single supply (Connector J11) with Link LK1 on position A. Note that the J11 connector can be supplied with a range of 3.3 V to 5.5 V when Link LK5 is inserted. When this link is removed, the digital supply is sourced from the adjusted voltage generated by the ADP5070 and regulated by the ADP7118. Note that the J11 connector can be supplied with a range of 3.3 V to 18 V when Link LK5 is removed.
LK6	This link selects whether the ADP7118 regulator is included in the V_{DD} source circuit. When this link is inserted, the ADP7118 regulator is bypassed. When this link is removed, the ADP7118 regulator adjusts the positive analog supply generated by the ADP5070 power solution.
LK7	This link selects whether the ADP7182 regulator is included in the V_{SS} source circuit. When this link is inserted, the ADP7182 regulator is bypassed. When this link is removed, the ADP7182 regulator adjusts the negative analog supply generated by the ADP5070 power solution.
LK8	This link selects the voltage source for the IOV_{CC} pin. Position A selects an externally applied voltage at Pin 10 of Connector J12. Position B selects the source from the SDP board. This position must be used when V_{CC} is larger than 3.3V. Position C connects IOV_{CC} to V_{CC} .
LK9	This link selects the voltage source for the negative analog supply V_{SS} . Position A selects the source from the voltage externally applied at V_{SS} of Connector J13. Position B selects the source from the negative voltage generated by the ADP5070 and adjusted by an ADP7182 regulator, depending on the position of Link LK7.
LK10	This link selects the voltage source for the positive analog supply V_{DD} . Position A selects the source from the voltage externally applied at V_{DD} of Connector J13. Position B selects the source from the positive voltage generated by the ADP5070 and adjusted by an ADP7118 regulator, depending on the position of Link LK6.
LK11	This link selects the state of the $\overline{\text{CLR}}$ pin. When this link is inserted, $\overline{\text{CLR}}$ is at logic low. When this link is removed, $\overline{\text{CLR}}$ is at logic high.

ON-BOARD CONNECTORS

Table 4 shows the connectors on the EVAL-AD5791SDZ.

Table 4. On-Board Connectors

Connector	Function
J1 to J9	Voltage reference daughter board connectors
J11	Digital power supply connector
J12	Digital interface pin header connector
J13	Analog power supply connector
J14	SDP board connector
VO	DAC output connector
VO_BUF	Buffered DAC output connector
VR_EXT	5 V voltage reference input connector

Connector J12 Pin Descriptions

Figure 6 and Table 5 show the Connector J12 pins.

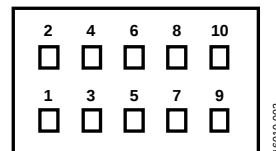


Figure 6. Connector J12 Pin Configuration

Table 5. Connector J12 Pin Descriptions

Pin No.	Description
1	CLR
2	$\overline{\text{LDAC}}$
3	$\overline{\text{RESET}}$
4	SCLK
5	SDIN
6	SDO
7	$\overline{\text{SYNC}}$
8	DGND
9	DGND
10	IOVCC

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The AD5791 evaluation kit includes self installing software on a CD. The software is compatible with Windows XP or later Windows-based PCs. If the setup file does not run automatically, you can run **setup.exe** from the CD.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

After installation from the CD is complete, power up the AD5791 evaluation board as described in the Power Supplies and Default Link Options section. Connect the SDP board to the AD5791 evaluation board and then to the USB port of your PC using the supplied cable.

When the evaluation system is detected, proceed through any dialog boxes that appear. This completes the installation.

SOFTWARE OPERATION

To launch the software, complete the following steps:

1. From the **Start** menu, select **Analog Devices – AD5791 > AD5791 Evaluation Software**. The main window of the software displays (see Figure 8).
2. If the evaluation system is not connected to the USB port when the software is launched, a connectivity error dialog displays (see Figure 7). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

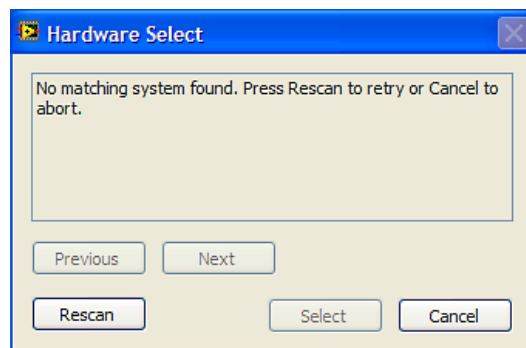


Figure 7. Connectivity Error Alert

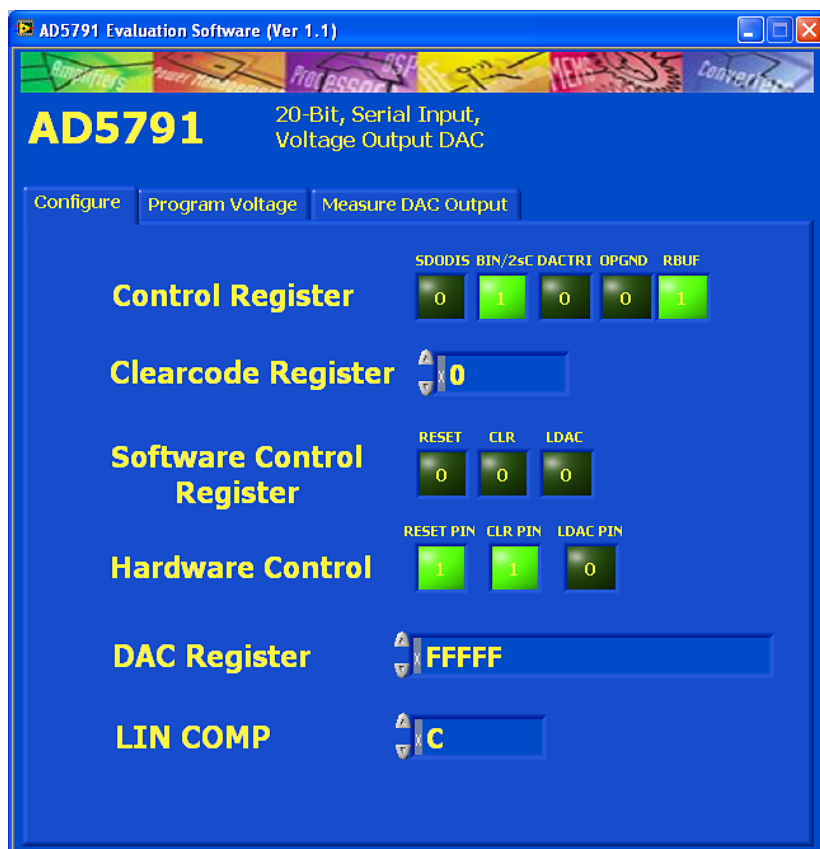


Figure 8. Main Window

MAIN WINDOW

The main window is divided into three tabs: **Configure**, **Program Voltage**, and **Measure DAC Output**.

Configure

The **Configure** tab allows access to the control register, clear code register, software control register, and DAC register, and also allows control of the **RESET**, **CLR**, and **LDAC** pins, as shown in Figure 8.

Program Voltage

The **Program Voltage** tab programs the DAC register with a value calculated from the three entered values: the positive voltage reference (**VREFP**), the negative voltage reference (**VREFN**), and the desired output voltage input to the **Program Voltage** field, as shown in Figure 9.



Figure 9. Program Output Voltage Window

Measure DAC Output

The **Measure DAC Output** section allows the PC to control an Agilent 3458A multimeter to measure and log the DAC output voltage.

The multimeter is controlled over a general-purpose interface bus (GPIB). Once connected to the PC, the multimeter must first be configured via its front panel before taking a measurement. Figure 11 shows the measurement options. The software runs through a sequence of steps, programming the DAC register and measuring the DAC output voltage. The sequence begins with the software programming the DAC with the **Start Code** value, incrementing the programmed value at each step by the **Code Step** value, and finishing when the programmed value reaches the **Stop Code** value. A delay between measurements can be inserted, if required. The GPIB address of the multimeter must be specified.

To begin the measurement, click **START**. Halt the measurement at any time by clicking **STOP**. When the measurement is completed, a dialog box appears to allow the data to be saved as a spreadsheet file with three columns of data. The first column is the DAC code, the second column is the DAC voltage in volts, and the third column is the INL error in least significant bits (LSBs), as shown in Figure 10. A graph of both DAC output voltage vs. DAC code and INL error vs. DAC code displays on screen. In the measurement example shown in Figure 11, measurements are taken in 1024 code steps beginning at Code 0 and finishing at Code 1,047,552, in total 1023 measurements. With the number of power line cycles (NPLC) setting on the multimeter set to 1, the measurement takes ~75 sec to complete. To complete an all codes measurement, requiring 1,048,576 measurement points, the measurement takes ~21 hours to complete.

	A	B	C
	0	-10.0002	0
	1024	-9.98066	0.120122
	2048	-9.96113	0.086736
	3072	-9.9416	0.13781
	4096	-9.92206	0.150508
	5120	-9.90253	0.109467
	6144	-9.883	0.183557
	7168	-9.86347	0.157878
	8192	-9.84394	0.201298
0	9216	-9.8244	0.252373
1	10240	-9.80487	0.242002
2	11264	-9.78534	0.085883
3	12288	-9.76581	0.090874
4	13312	-9.74628	-0.03458

Figure 10. Saved Data Format

If an Agilent 3458A multimeter is not connected to the PC, the software steps through the codes without taking any measurements.

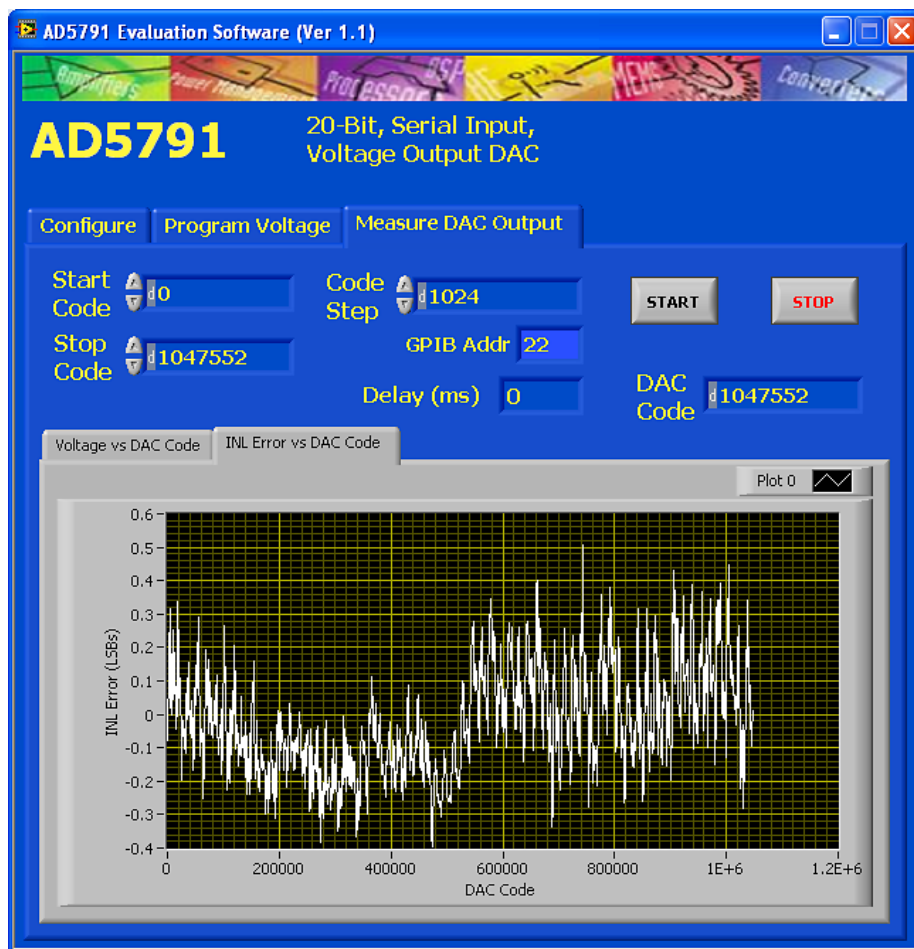


Figure 11. Measure DAC Output Window

EVALUATION BOARD SCHEMATICS AND ARTWORK

AD5791 CARRIER BOARD

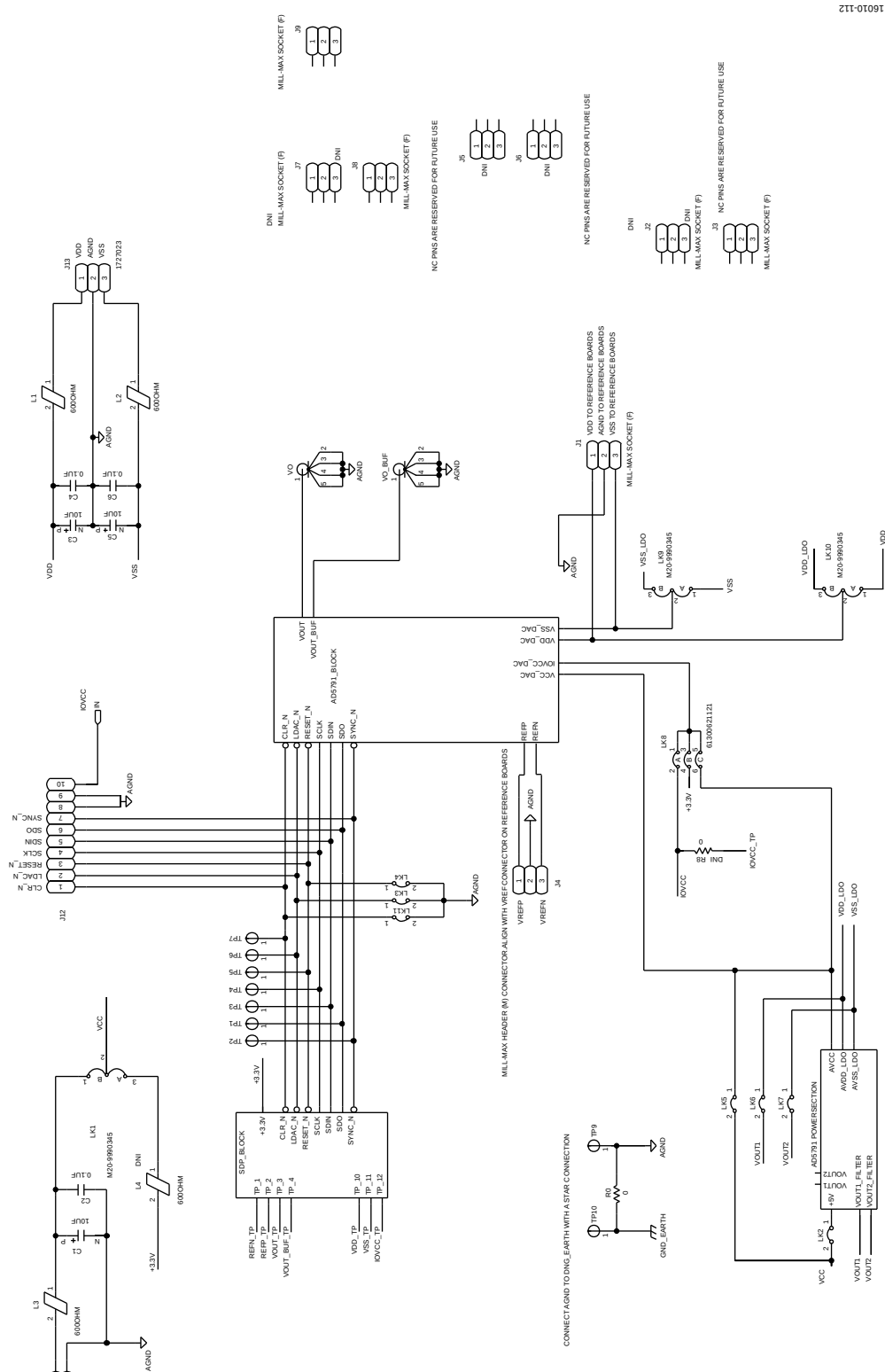


Figure 12. Schematic of the Main AD5791 Circuitry

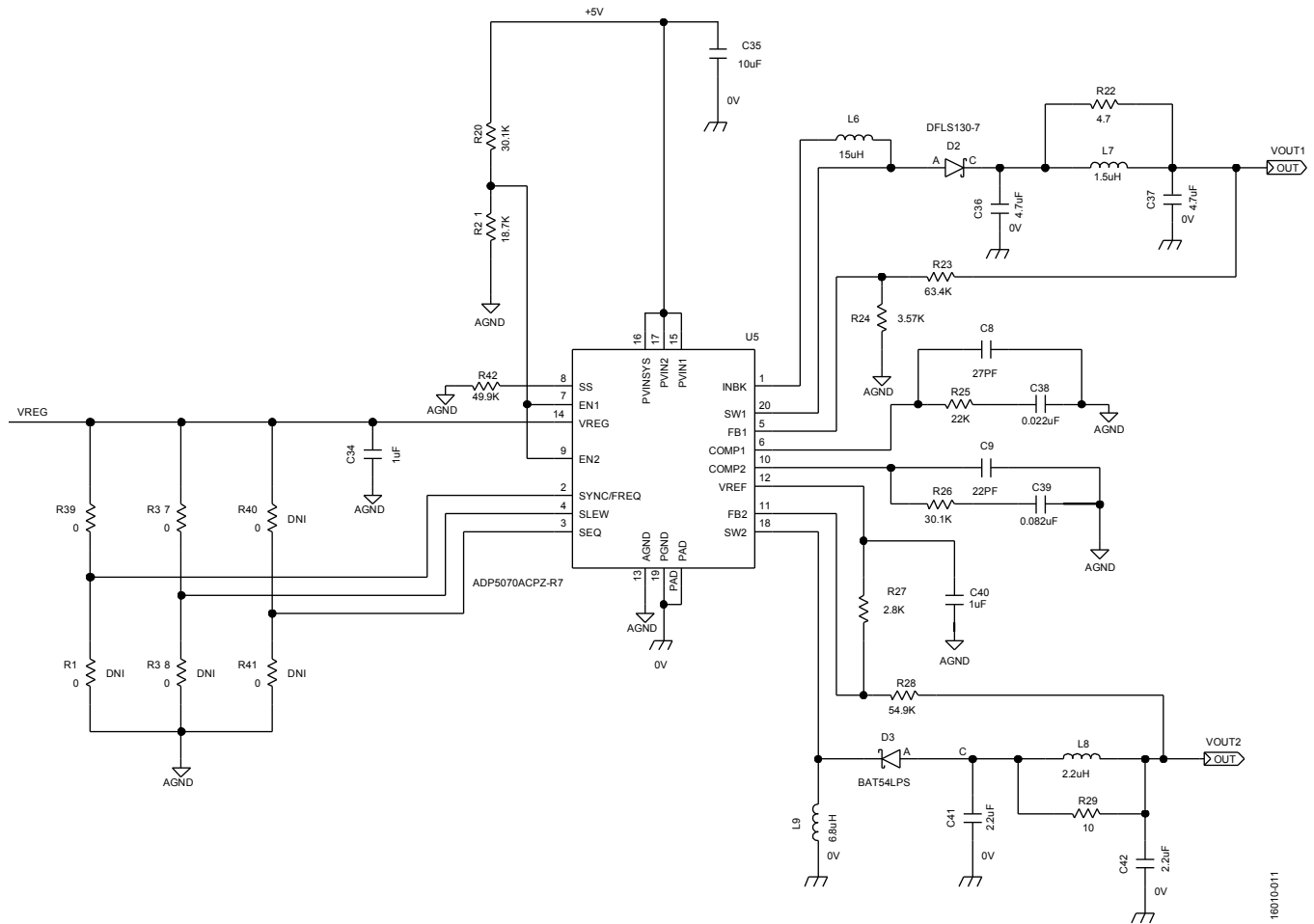


Figure 13. Schematic of the ADP5070 DC-to-DC Switch Circuitry

18010-011

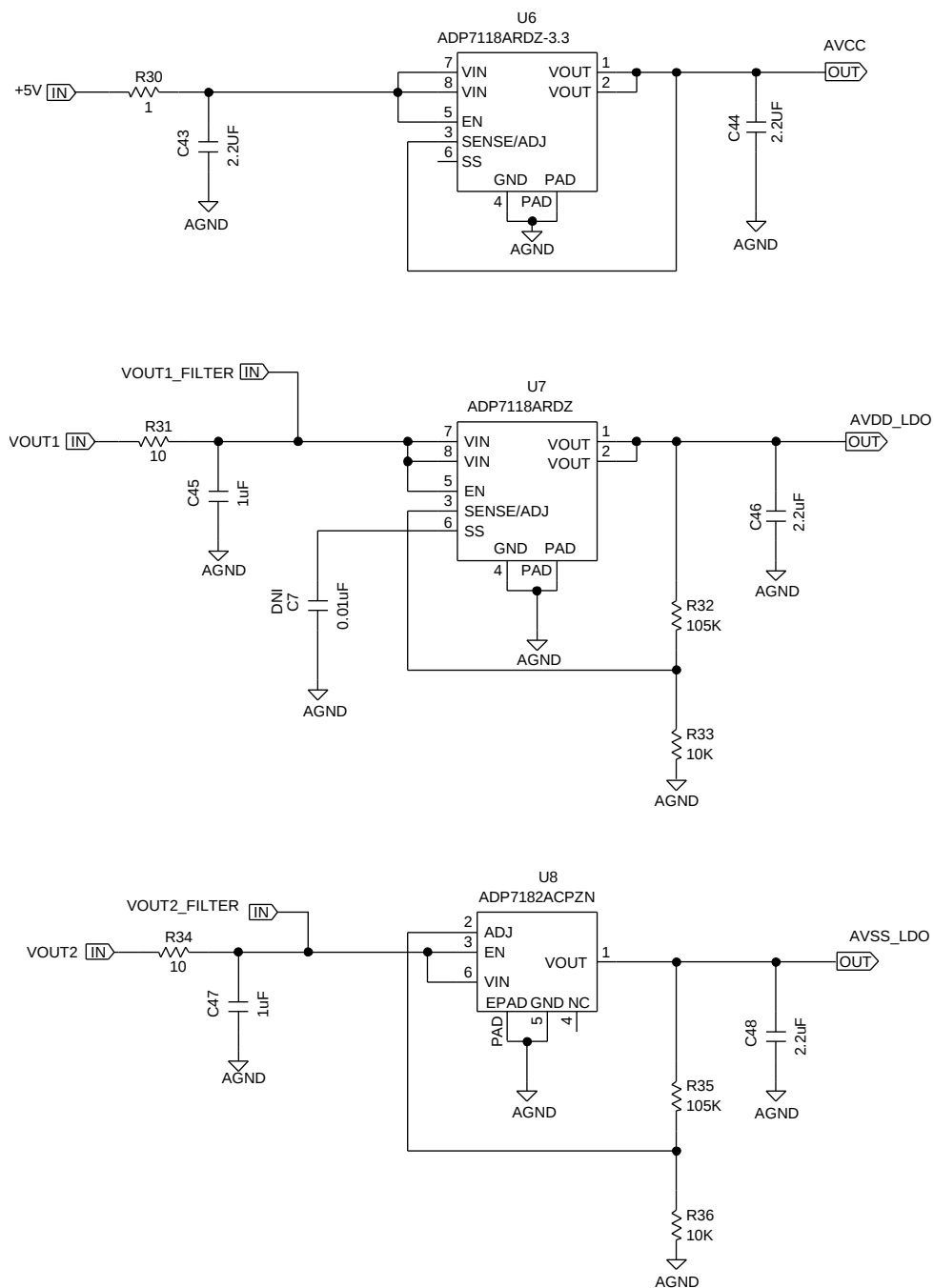


Figure 14. Schematic of the LDOs (ADP7118 and ADP7182) from the Power Solution Circuitry

16010-012

16010-115

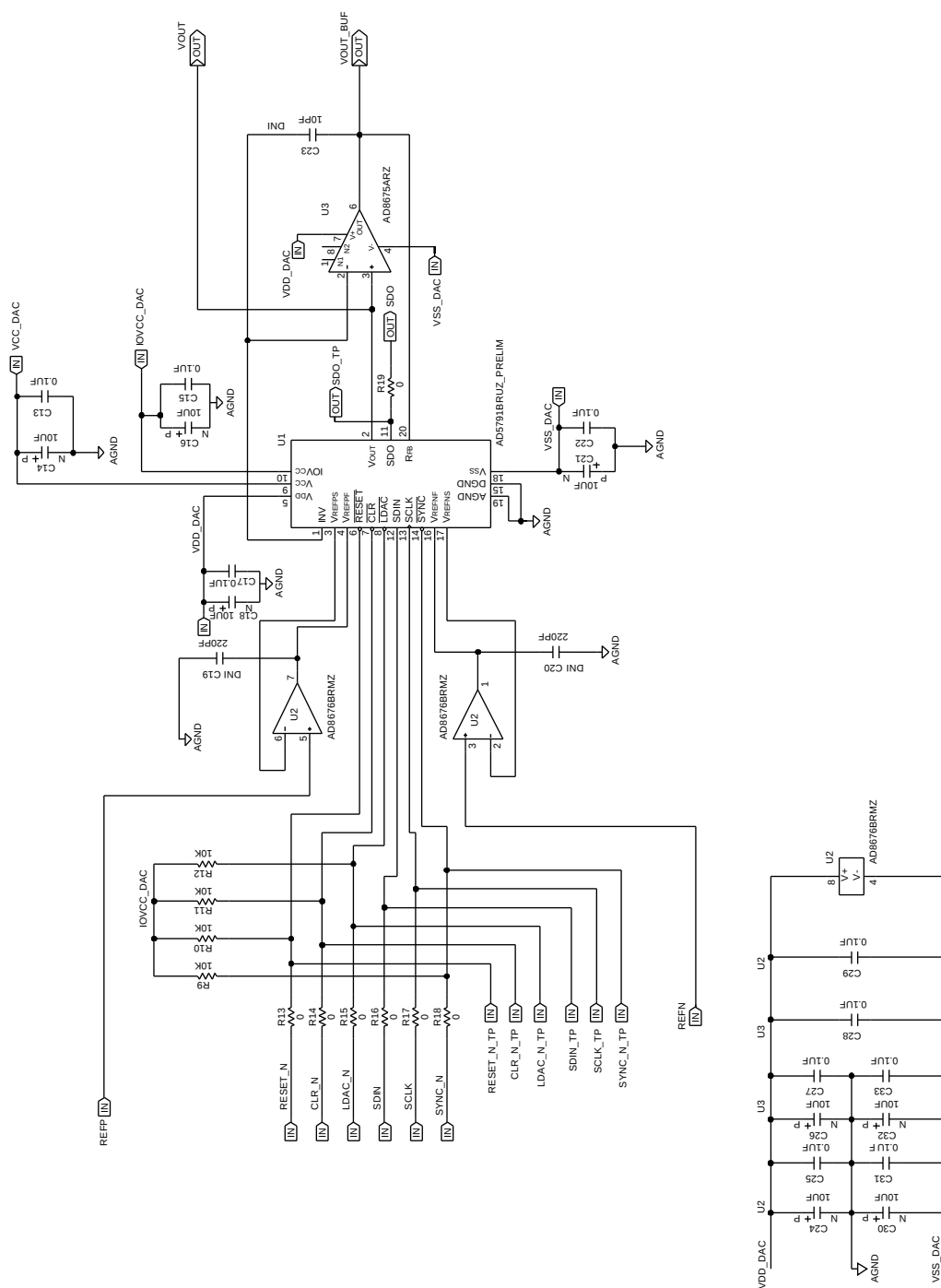


Figure 15. Schematic of the AD5791 Circuitry

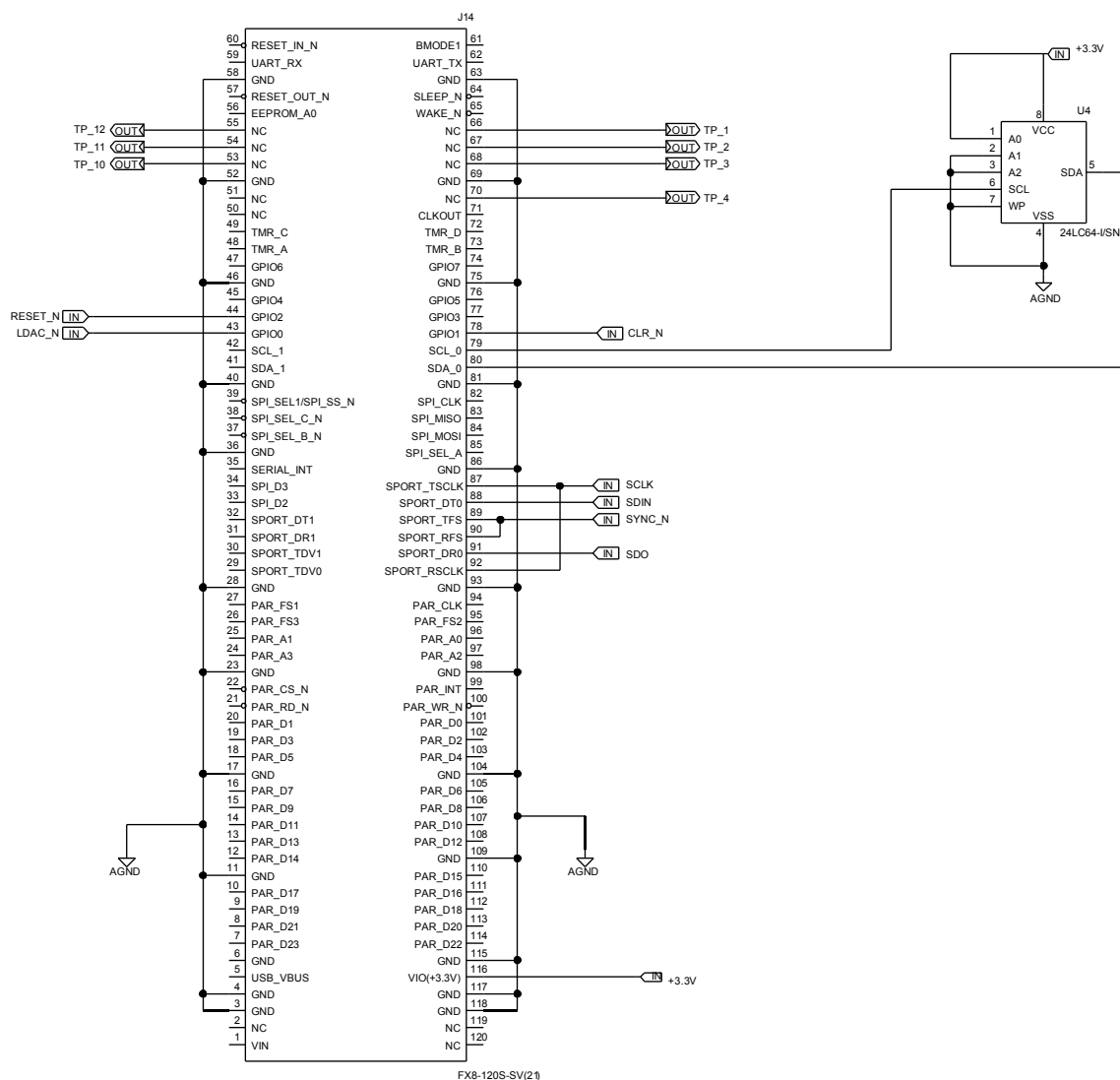


Figure 16. Schematic of the SDP Board Connector

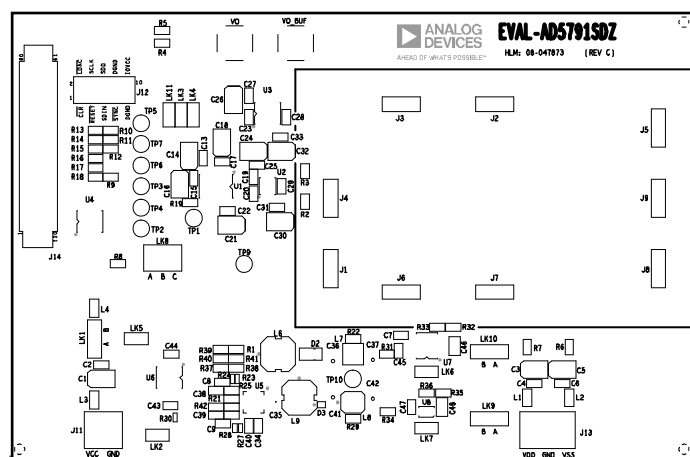


Figure 17. Component Placement Schematic

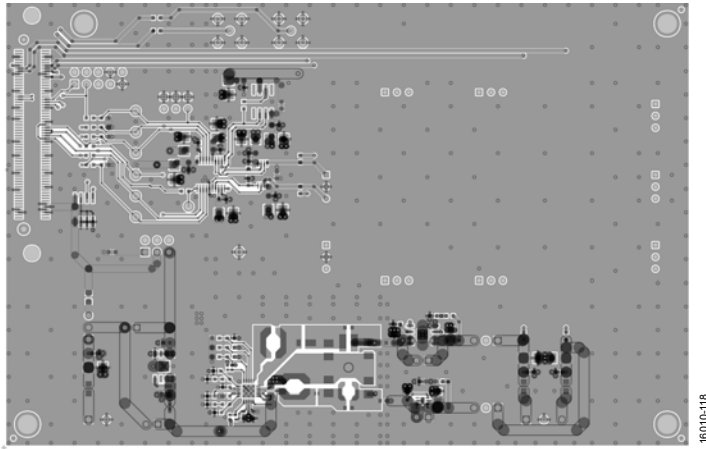


Figure 18. Top Printed Circuit Board (PCB) Layer Schematic

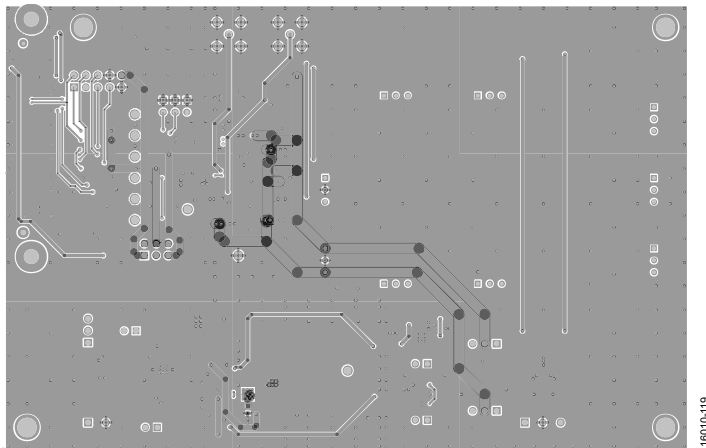


Figure 19. Bottom PCB Layer Schematic

ADR445 REFERENCE VOLTAGE DAUGHTER BOARD

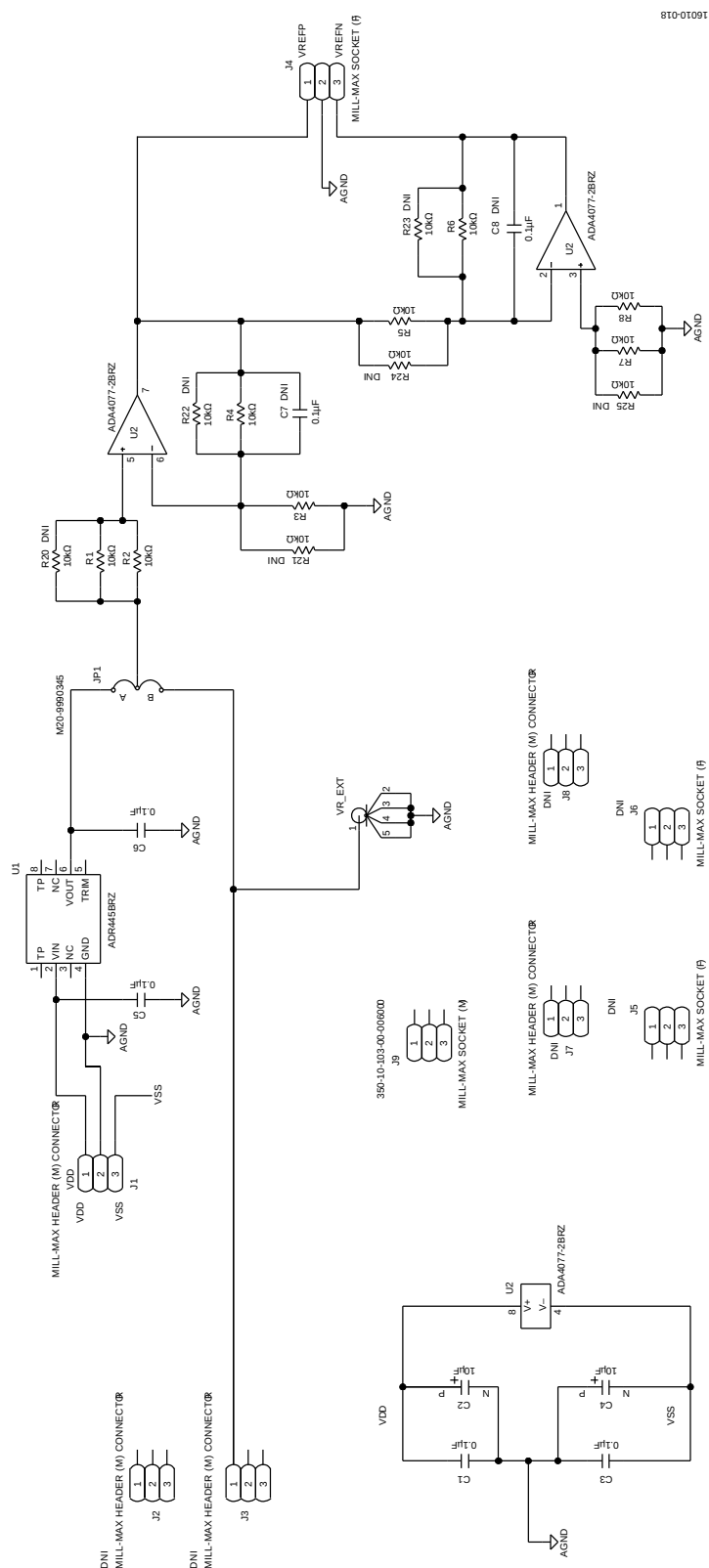


Figure 20. Schematic of the EV-ADR445-REFZ

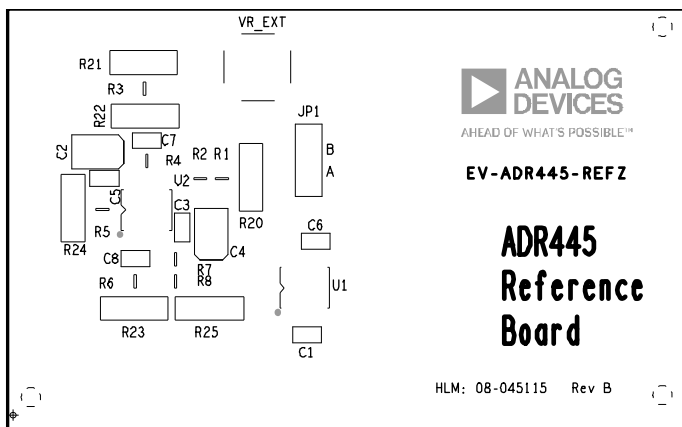


Figure 21. EV-ADR445-REFZ Component Placement Schematic

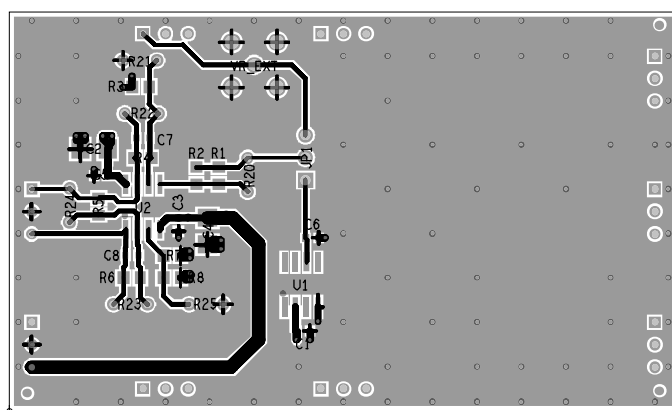


Figure 22. EV-ADR445-REFZ Top PCB Layer Schematic

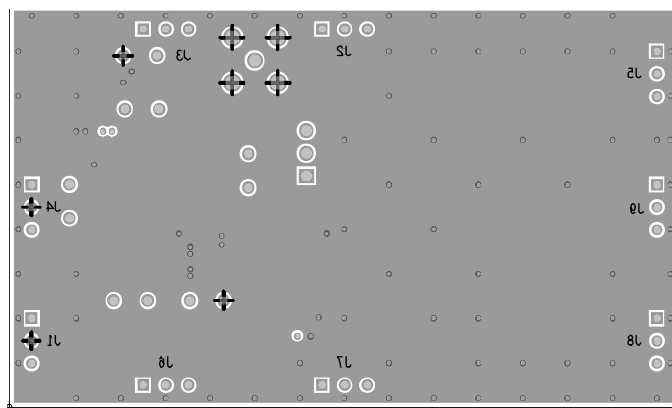


Figure 23. EV-ADR445-REFZ Bottom PCB Layer Schematic

LTZ1000 REFERENCE VOLTAGE DAUGHTER BOARD

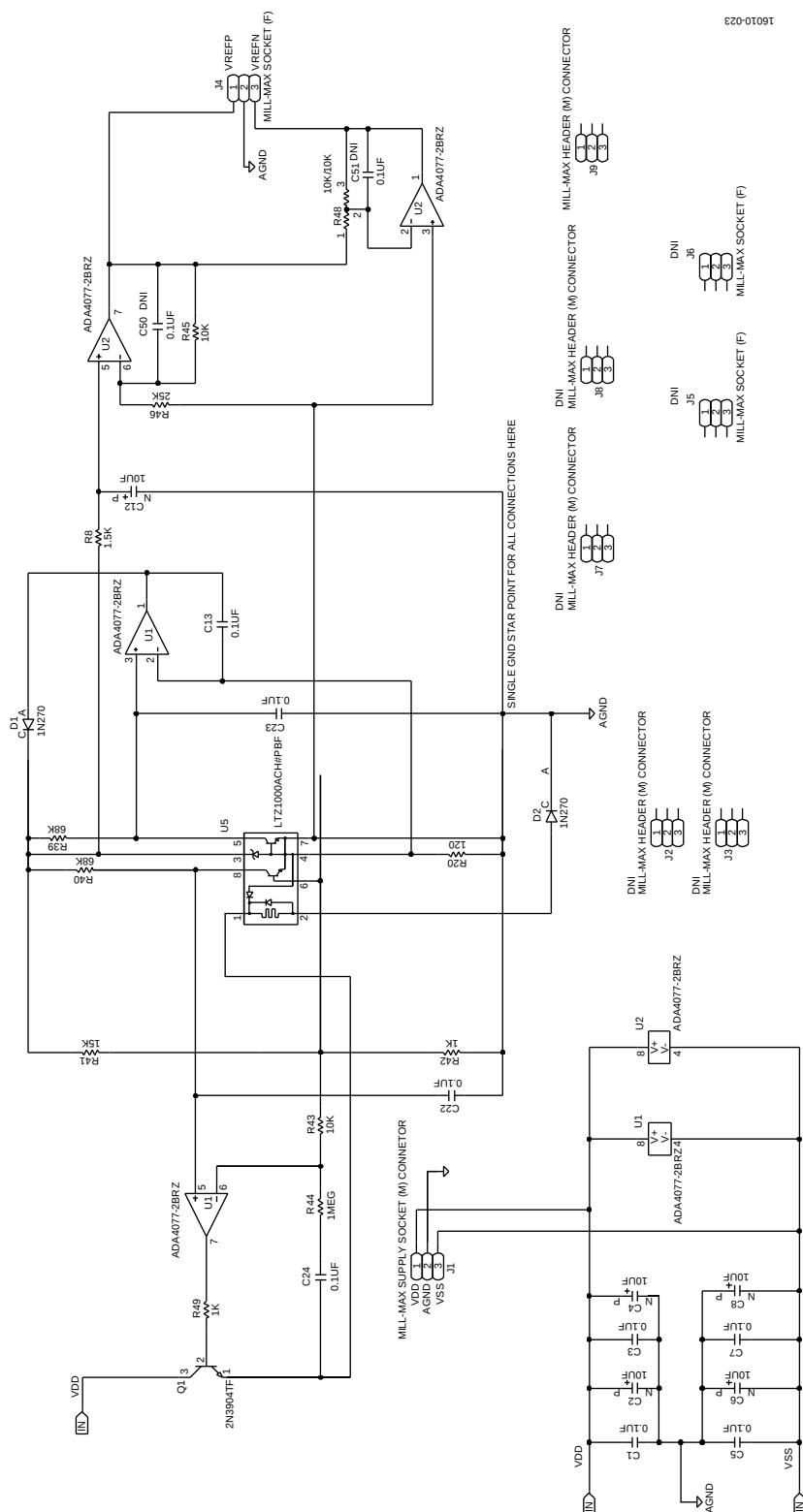


Figure 24. Schematic of the EV-LTZ1000-REFZ

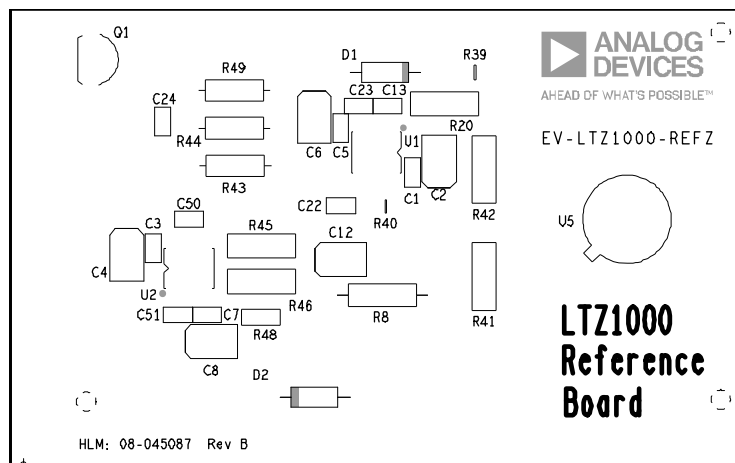


Figure 25. EV-LTZ1000-REFZ Component Placement Schematic

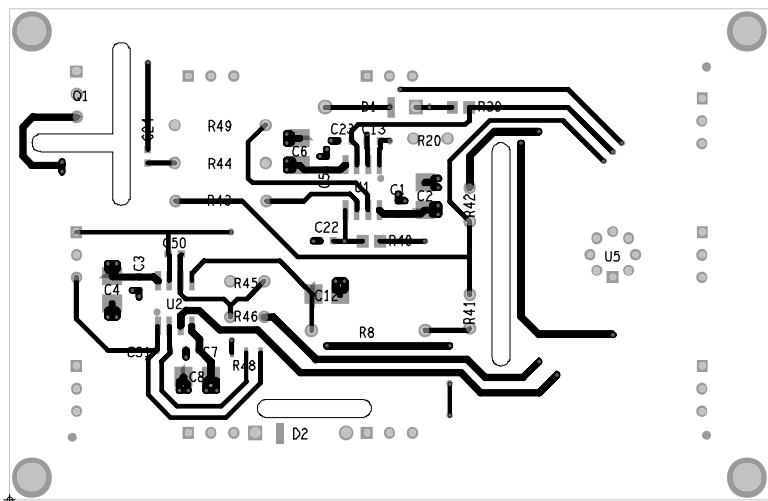


Figure 26. EV-LTZ1000-REFZ Top PCB Layer Schematic

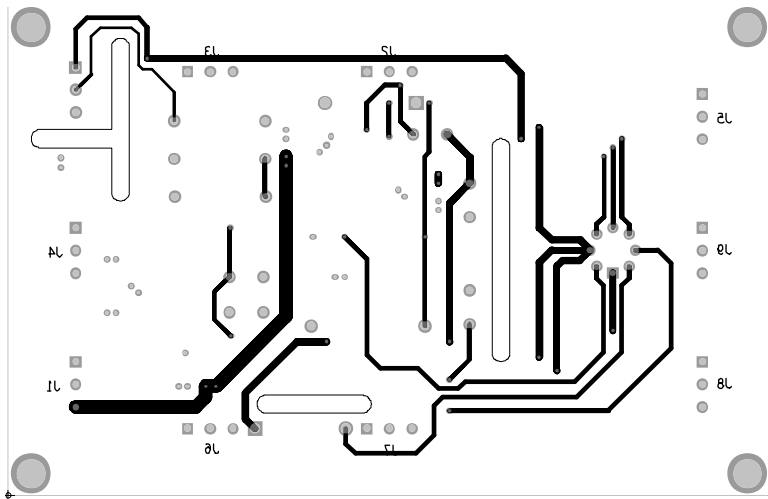


Figure 27. EV-LTZ1000-REFZ Bottom PCB Layer Schematic

LTC6655 REFERENCE VOLTAGE DAUGHTER BOARD

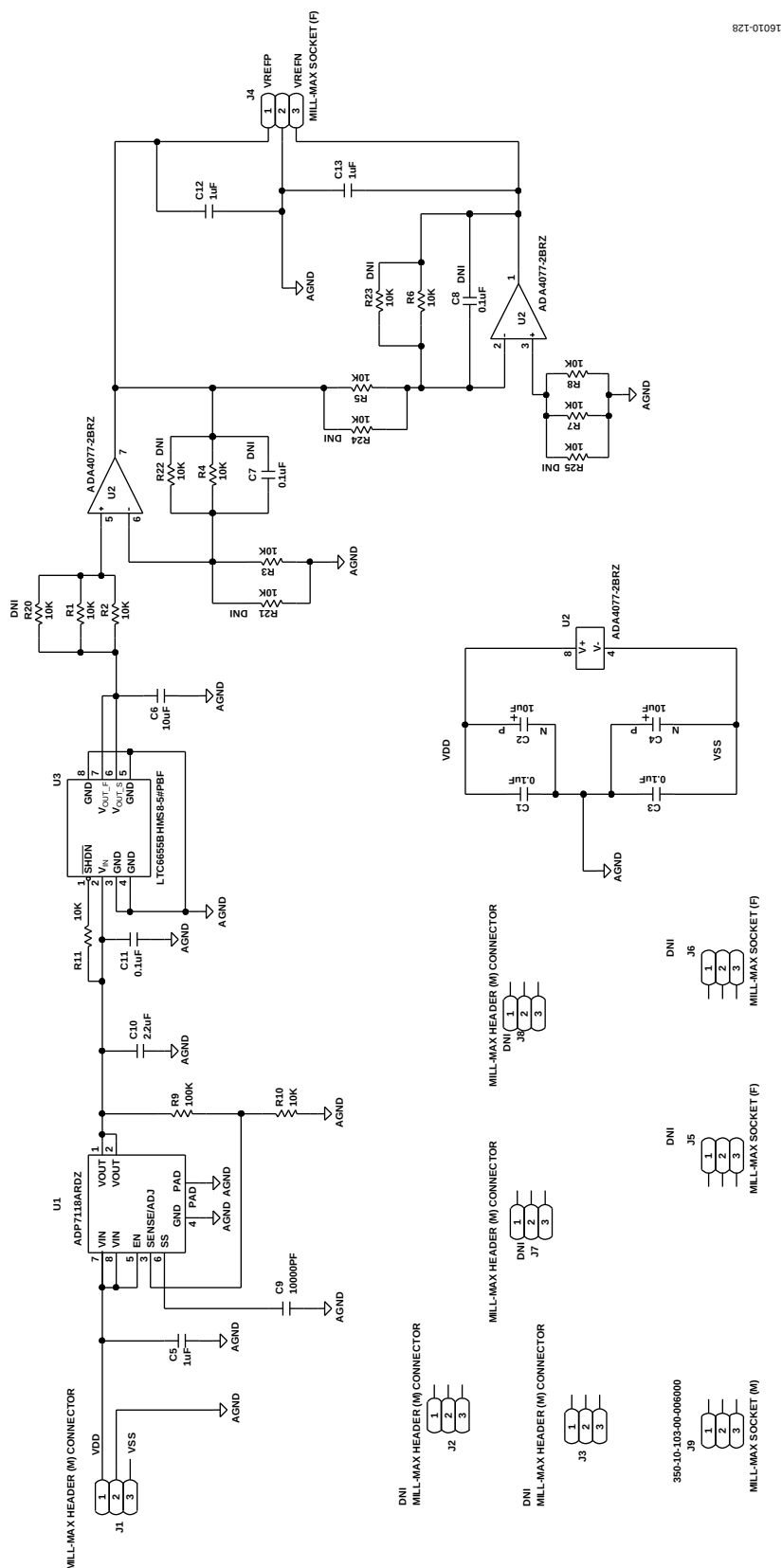


Figure 28. Schematic of the [EV-LTC6655-REFZ](#)

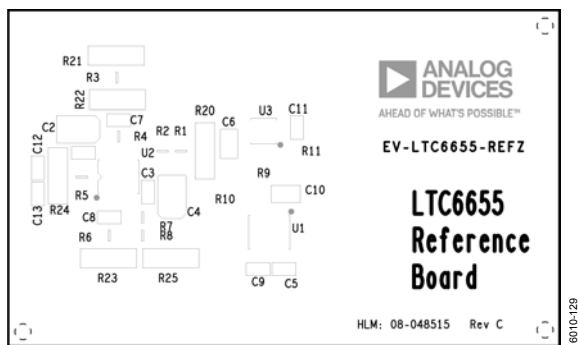


Figure 29. EV-LTC6655-REFZ Component Placement Schematic

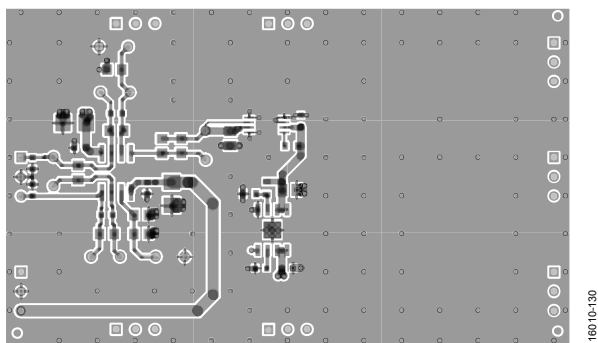


Figure 30. EV-LTC6655-REFZ Top PCB Layer Schematic

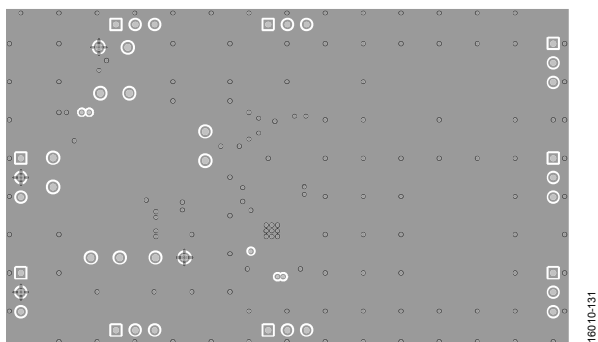


Figure 31. EV-LTC6655-REFZ Bottom PCB Layer Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 6. AD5791 Carrier Board

Reference Designator	Part Description	Part Number
C1, C3, C5, C14, C16, C18, C21, C24, C26, C30, C32	Capacitors, 3528, 10 μ F	TAJB106K016RNJ
C2, C4, C6, C13, C15, C17, C22, C25, C27 to C29, C31, C33	Capacitors, 0603, 25 V, 0.1 μ F, $\pm$ 10%	C1608X8R1E104K
C34, C40	Capacitors, 0603, 6.3 V, 1 μ F, $\pm$ 20%	JMK107B7105MA
C35	Capacitor, 0805, 10 V, 10 μ F, $\pm$ 20%	TACH106M010XTA
C36, C37	Capacitors, 1206, 50 V, 4.7 μ F, $\pm$ 20%	C3216X7R1H475M160AC
C38	Capacitor, 0603, 16 V, 0.022 μ F, $\pm$ 10%	0603YC223KAT2A
C39	Capacitor, 0603, 16 V, 0.082 μ F, $\pm$ 10%	CL10B823K08NNNC
C41, C42	Capacitors, 1206, 25 V, 2.2 μ F, $\pm$ 10%	C3216X7R1E225K
C43, C44	Capacitors, 0603, 10 V, 2.2 μ F, $\pm$ 10%	GRM188R71A225KE15D
C45, C47	Capacitors, 0603, 16 V, 1 μ F, $\pm$ 10%	CGA3E1X7R1C105K080AC
C46, C48	Capacitors, 0805, 25 V, 2.2 μ F, $\pm$ 10%	GRM21BR71E225KA73L
C8	Capacitor, 0603, 50 V, 27 pF, $\pm$ 5%	2238 867 15279
C9	Capacitor, 0603, 50 V, 22 pF, $\pm$ 5%	CC0603JRNPO9BN220
D2	Schottky diode	DFLS130-7
D3	Schottky diode	BAT54LPS
J1 to J9	3-position female headers, single-row connectors, 2.54 mm pitch	310-13-103-41-001000
J11	2-position terminal block (3.81 mm pitch)	1727010
J12	10-position male header connector (3.81 mm pitch)	M20-9980546
J13	3-pin terminal block (3.81 mm pitch)	1727023
J14	120-way connector, 0.6 mm pitch	FX8-120S-SV(21)
J4	3-position male header single row connector, 2.54 mm pitch	350-10-103-00-006000
L1, L2, L3	Surface-mount power inductors	7427920415
L6	Surface-mount power inductor	LPS6235-153MRB
L7	Surface-mount power inductor	XFL4020-152MEB
L8	Surface-mount power inductor	LPS4018-222MRB
L9	Surface-mount power inductor	LPS6235-682MRB
LK1, LK9, LK10	3-pin single-inline (SIL) header	M20-9990345
LK2 to LK7, LK11	2-contact headers, two rows, through hole	69157-102
LK8	6-pin header	61300621121
R0, R13 to R19, R37, R39	Resistors, 0 Ω , 0.0625 W, 1%, 0603	MC0603WG00000T5E-TC
R9 to R12	Resistors, 10 k Ω , 0.0625 W, 1%, 0603	MC0063W0603110K
R20, R26	Resistors, 30.1 k Ω , 0.1 W, 1%, 0603	ERJ-3EKF3012V
R21	Resistor, 18.7 k Ω , 0.1 W, 1%, 0603	ERJ-3EKF1872V
R22	Resistor, 4.7 Ω , 0.1 W, 1%, 0603	ERJ-3RQF4R7V
R23	Resistor, 63.4 k Ω , 0.0625 W, 1%, 0402	ERJ-2RK6342X
R24	Resistor, 3.57 k Ω , 0.1 W, 1%, 0402	ERJ-2RK63571X
R25	Resistor, 22 k Ω , 0.1 W, 1%, 0603	CRCW060322K0FKEA
R27	Resistor, 2.8 k Ω , 0.1 W, 1%, 0402	ERJ-2RK62801X
R28	Resistor, 54.9 k Ω , 0.1 W, 1%, 0402	ERJ-2RK65492X
R29, R31, R34	Resistors, 10 Ω , 0.1 W, 1%, 0603	ERJ-3EKF10R0V
R30	Resistor, 1 Ω , 0.0625 W, 5%, 0402	CRCW04021R00JNED
R32, R35	Resistors, 105 k Ω , 0.1 W, 1%, 0603	ERJ-3EKF1053V
R33, R36	Resistors, 10 k Ω , 0.1 W, 1%, 0603	ERJ-3EKF1002V
R42	Resistor, 49.9 k Ω , 0.1 W, 1%, 0603	ERJ-3EKF4992V
TP1 to TP7, TP9, TP10	Red test points	TP-104-01-02
U1	1 ppm 20-bit, $\pm$ 1 LSB INL, voltage output DAC	AD5791BRUZ
U2	Ultraprecision, 36 V, 2.8 nV/ $\sqrt$ Hz dual rail-to-rail output op amp	AD8676BRMZ

Reference Designator	Part Description	Part Number
U3	36 V precision, 2.8 nV/ $\sqrt{\text{Hz}}$ rail-to-rail output op amp	AD8675ARZ
U4	64 kb I ² C serial electrically erasable programmable read only memory (EEPROM)	24LC64-I/SN
U5	1 A/0.6 A dc to dc switching regulator with independent positive and negative outputs	ADP5070ACPZ-R7
U6	20 V, 200 mA, low noise, complementary metal-oxide-semiconductor (CMOS) LDO linear regulator, 3.3 V fixed output voltage	ADP7118ARDZ-3.3
U7	20 V, 200 mA, low noise, CMOS LDO linear regulator	ADP7118ARDZ
U8	–200 mA, low noise linear regulator	ADP7182ACPZN
VO, VO_BUF	Straight PCB mount Subminiature Version B (SMB) jacks, 50 Ω	1-1337482-0
Not Applicable	Shorting links on LK1, LK9, and LK10, 2.54mm pitch, contact center	QPC02SXGN-RC

Table 7. [ADR445](#) Daughter Board

Reference Designator	Part Description	Part Number
C1, C3, C5, C6	Capacitors, 0603, X8R, 25 V, 0.1 μF , $\pm 10\%$	C1608X8R1E104K
C2, C4	Capacitors, 3528, 16 V, 10 μF , $\pm 10\%$	TAJB106K016RNJ
J1 to J9	3-position male header, single-row connectors, 2.54 mm pitch	350-10-103-00-006000
J4	3-position female header, single-row connector, 2.54 mm pitch	310-13-103-41-001000
JP1	3-position header connector	M20-9990345 + M7567-05
R1 to R8	Resistors, 10 k Ω , 0.125 W, 0.01%, 0805	ERA-6AEB103V
U1	Ultralow noise 5 V voltage reference	ADR445BRZ
U2	High precision dual amplifier	ADA4077-2BRZ
VR_EXT	Straight PCB mount SMB jack, 50 Ω	1-1337482-0

Table 8. [LTZ1000](#) Daughter Board

Reference Designator	Part Description	Part Number
C1, C3, C5, C7, C13, C22, C23, C24	Capacitors, 0603, 25 V, 0 μF , $\pm 10\%$	C1608X8R1E104K
C2, C4, C6, C8, C12	Capacitors, 3528, 16 V, 1 μF , $\pm 10\%$	TAJB106K016RNJ
D1, D2	Radio frequency (RF)/pin diodes	1N270
J1 to J9	3-position male header single row connectors, 2.54 mm pitch	350-10-103-00-006000
J4	3-position female header single row connector, 2.54 mm pitch	310-13-103-41-001000
Q1	Single bipolar junction transistor	2N3904TF
R20	Resistor, 120 Ω , 0.6 W, 0.01%, through hole	Y1453120R000T9
R39, R40	Resistors, 68 k Ω , 0.1 W, 0.1%, 0805	PCF0805-13-68K-B-T1
R41	Resistor, 15 k Ω , 0.6 W, 0.01%, through hole	Y145315K0000T9
R42	Resistor, 1 k Ω , 0.6 W, 0.01%, through hole	Y14531K00000T9
R43	Resistor, 10 k Ω , 0.6 W, 1%, through hole	MRS25000C1002FRP00
R44	Resistor, 1 M Ω , 0.6 W, 1%, through hole	MRS25000C1004FCT00
R45	Resistor, 10 k Ω , 0.6 W, 0.005%, through hole	Y145310K0000V9L
R46	Resistor, 25 k Ω , 0.6 W, 0.01%, through hole	Y145325K0000T9
R48	Resistor, 10 k Ω /10 k Ω , 0.1 W, 0.01%, 1505	Y1685V0001TT9
R49	Resistor, 1 k Ω , 0.6 W, 1%, through hole	MRS25000C1001FRP00
R8	Resistor, 1.5 k Ω , 0.25 W, 1%, through hole	CMF-551501FT-1
U1, U2	High precision dual amplifiers	ADA4077-2BRZ
U5	Ultraprecision reference	LTZ1000ACH#PBF

Table 9. LTC6655 Daughter Board

Reference Designator	Part Description	Part Number
C1, C3, C11	Capacitors, 0603, 25 V, 0.1 μ F, $\pm$ 10%	C1608X8R1E104K080AA
C2, C4	Capacitors, 3528, 16 V, 10 μ F, $\pm$ 10%	TAJB106K016RNJ
C5	Capacitor, 0603, 16 V, 1 μ F, $\pm$ 10%	GRM188R61C105KA93D
C6	Capacitor, 0805, 10 V, 1 μ F, $\pm$ 10%	CL21B106KPQNNNE
C9	Capacitor, 0603, 25 V, 1 nF, $\pm$ 10%	C1608X7R1E103K
C10	Capacitor, 0805, 25 V, 2.2 μ F, $\pm$ 10%	GRM21BR71E225KA73L
C12, C13	Capacitors, 0603, 10 V, 1 μ F, $\pm$ 10%	GRM188R71A105KA61D
J1 to J9	3-position male headers, single-row connectors, 2.54 mm pitch	350-10-103-00-006000
J4	3-position female header, single-row connector, 2.54 mm pitch	310-13-103-41-001000
R1, R2, R3, R4, R5, R6, R7, R8	Resistors, 0805, 10 k Ω , 0.125 W, 0.1%	ERA-6AEB103V
R10, R11	Resistors, 0603, 10 k Ω , 0.1 W, 1%	ERJ-3EKF1002V
R9	Resistor, 0603, 100 k Ω , 0.1 W, 1%	ERJ-3EKF1003V
U1	Low dropout regulator	ADP7118ARDZ
U2	High precision dual amplifiers	ADA4077-2BRZ
U3	Low noise, low drift precision reference	LTC6655BHMS8-5#PBF

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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