ON Semiconductor

Test Procedure for the NCN8026AMNGEVB Evaluation Board

TEST EQUIPMENT

The following equipment listed in Table 1 is suggested for the evaluation.

Table 1. Test Equipment

Description	Main Features	Example of Equipment (Note 1)	Qty.
Regulated Power Supply	200 mA DC current capability	Tektronix PS2520G	2
Multimeter		Keithley 2000 or 2001	2
Sourcemeter		Keithley 2400	1
Oscilloscope	500 MHz bandwidth, four channel scope, minimum 1MB memory per channel (Note 2)	Tektronix TDS744, 754 or 784 / TDS5054 series or LeCroy WR5060 TDS5104B, 1 GHz, 5GS/s	1
Voltage probe	4 probes, 500MHz bandwidth	Tektronix or LeCroy	4
Waveform generator	Pattern generator	Agilent 81104A 80 MHz or HP8110A 150MHz 2 outputs	1
SMB Cable			1

1. Equipment used in the context of this Application Note Manual
2. Greater Scope memory per channel offers better resolution

TEST PROCEDURE

Refer to Figure 1 on page 4 for an overview of the main features of the evaluation board.

Initial Setup

The initial setup given here is recommended before starting measurements on the board.

- Set the CMDVCC/ in the OFF position (High).
- Set CS/ in the ON position: Chip selected, position Low.
- Set CLKDIV1 and CLKDIV2 into low position (lowest frequency F_{CLKIN})
- VESL0 and VSEL1 are used to change the output CVCC (card power supply) or the smart card interface mode which can be 1.8V, 3.0V or 5.0V. Change VSEL0 and VSEL1 using the switches (see Figure 2) according to Table 2 below. When VSEL0 = 0 then VSEL1 is in the mode 5V/3V*bar*, when VSEL0=1 then VSEL1 is in the mode 1.8V / 3V*bar*. The initial setup can be VSEL0 = 0 and VSEL1 = 1 for selecting the 5V mode. The CVCC output voltage can be changed on the fly when the smart card interface is active (/CMDVCC = Low). Nevertheless, it is recommended to change CVCC after having deactivated the device then reconfiguring CVCC by setting the appropriate VSEL0 and VSEL1 and reactivating the smart card interface.

Table 2: CVCC programming

VSEL0	VSEL1	CVCC
1	1	3.0 V
1	0	5.0 V
0	1	3.0 V
0	0	1.8 V

- As a precaution, if using the built-in resistive load, turn the 1 kΩ potentiometer to obtain a resistor output value of 1 kΩ, and then connect the jumper.

DC Power Supplies

Two power supplies are used to bias the demo board. VDDP is the input voltage of LDO Regulator. VDD is the "digital" power supply which biases the input stages of the NCN8026A device (control and signal inputs).
VDD and VDDP must be connected to the board to ensure correct operation. Connect the VDD and VDDP power supplies using the 2 pin male connectors J4 and J3 respectively. Refer to the recommended operating ranges for VDD and VDDP in the datasheet. Use VDD = VDDP = 5 V to get started.

Clock Frequency

CLKDIV1 and CLKDIV2 select the frequency divider for the card clock CCLK according to Table 3 given below.

Table 3: Clock division ratio programming

CLKDIV1	CLKDIV2	CCLK Frequency
0	1	f_{CLKIN} / 1
0	0	f_{CLKIN} / 2
1	0	f_{CLKIN} / 4
1	1	f_{CLKIN} / 8

The Clock

The clock is applied externally (SMB connector). Refer to the datasheet for the recommended frequency and voltage levels that can be applied at CLKIN.

Card presence

The typical socket is normally open, so PRES/ has been chosen; nevertheless the PRES and PRES/ test points can also be used for signaling the presence of a card and starting up the circuit. If not using a smart card, connect PRES/ to ground.

Start the measurement

To start the measurments, set the board as it follows:

1. Set CLKDIV1 and CLKDIV2 to select the correct frequency.
2. Set VSEL0 and VSEL1 to select the correct output voltage.
3. Check that the 1 kΩ potentiometer jumper is turned to 1 kΩ.
4. Set /CS low.
5. Set CMDVCC/ high.
6. Check that VDD and VDDP are set to 5 V, and set the current limit to 100mA. Turn on the power supplies VDD and VDDP.
7. Toggle /CMDVCC from High to Low to start the device (activation sequence run).
8. Change the CVCC output voltage with the VSEL0 and VSEL1 switches. Check that all CVCC voltages are output correctly according to Table 2.
9. Apply a clock to CLKIN and observe the card clock at CCLK. Use CLKDIV1 and CLKDIV2 to change the clock frequency. Check that all clock divisions are output correctly according to Table 3.

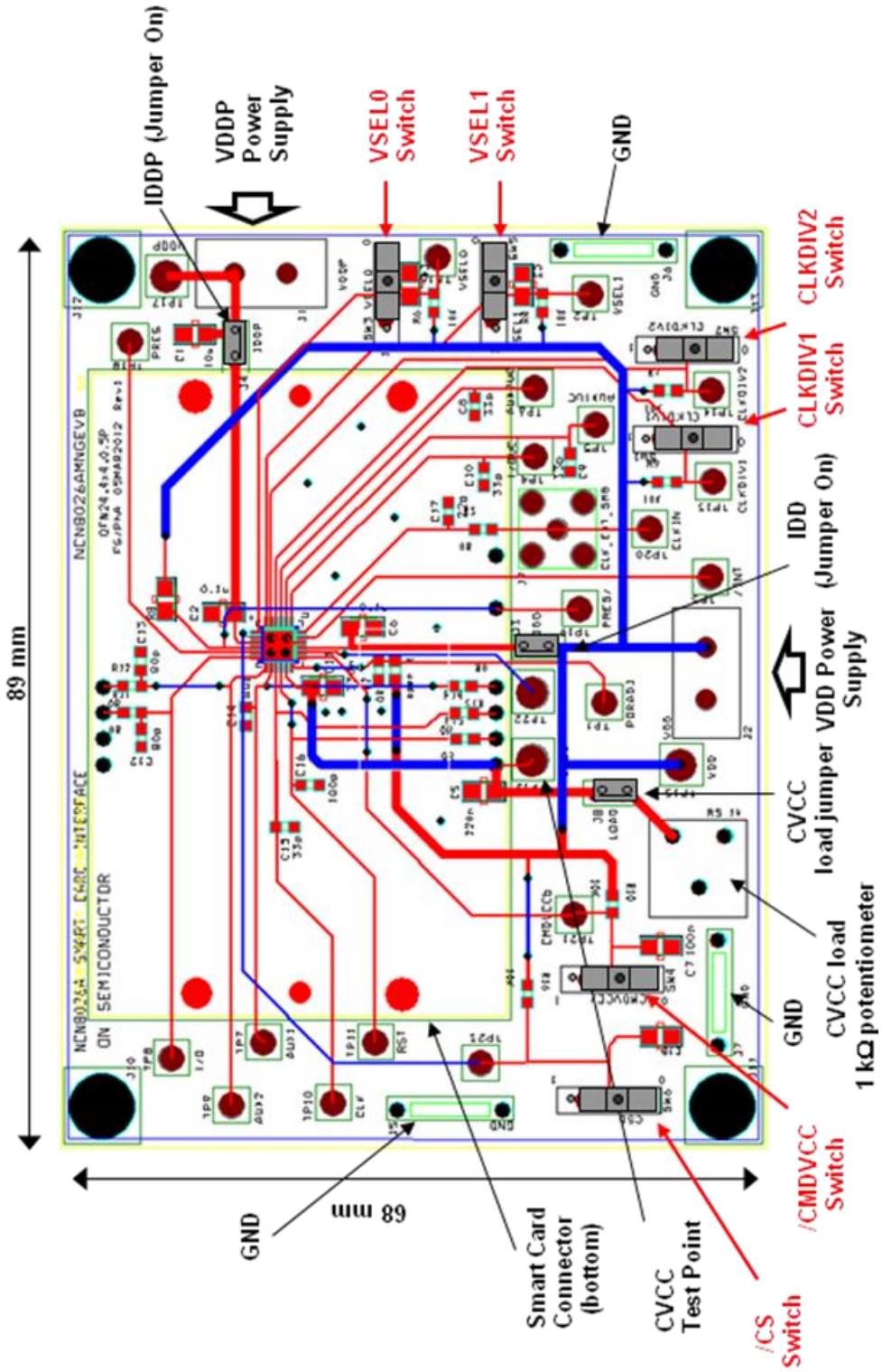


Figure 2: Board Description