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APPLICATION NOTE 6628

HOW A SIMO PMIC ENHANCES POWER EFFICIENCY FOR WEARABLE IOT DESIGNS

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Abstract: Small form factor and minimal power loss are key criteria for internet of things (IoT) hardware, particularly wearables. Meeting these criteria typically involves some tradeoffs. For example, to meet a specific power consumption goal, a designer usually would have to compromise with an increase in design size. This application note explains how an integrated power management IC (PMIC) operating three independent switching regulator outputs while using a single inductor enables compact IoT hardware powered by a Li+ cell.

Introduction

The internet of things (IoT) across all sectors is driving exponential growth in data acquisition across all sectors. From appliances to automobiles and beyond, autonomous “smart” things are processing data and collectively forming the network commonly known as the IoT. In this IoT world, a “smart” thing is loosely defined as a node that generates information of substantial value; however, implementing the hardware responsible for data acquisition calls for meticulous design planning. Consider a wearable device. To enable wearables to operate for long periods of time, they must be designed for efficient power management and with a compact form-factor. This includes maximizing the available battery capacity and designing for ultralow power while maintaining a small solution footprint.

Extending Battery Capacity

Batteries provide a temporary, unregulated power source for portable electronics. Primary batteries are a one-time use power source; secondary batteries generally provide half the energy density while allowing recharging. Among the most common rechargeable cell chemistries are lithium-ion (Li+) with a nominal voltage of near 3.7V, $LiMn_2O_4$, $LiCoO_2$, $LiNiO_2$, Lithium Nickel Manganese Cobalt Oxide (NCM), and Lithium Nickel Cobalt Aluminum Oxide (NCA). One rechargeable cell chemistry, $LiFePO_4$, has a nominal voltage of approximately 3.3V. While powering a device, the battery, which has finite source resistance, becomes loaded. As a result of the current consumption of the load, while in use, the available battery voltage decreases.

The more the load consumes power, the more significant the decrease in battery voltage and effective capacity. When effective capacity decreases, there’s less available time for the same current supplied to the downstream circuitry. The battery’s effective capacity is also negatively impacted by ambient temperature and charge/discharge cycles. For these reasons, the battery requires a form of regulated distribution with the following features:

- Provides power conversion for several voltage rails as efficiently as possible
- Steps down a fully charged battery and step up a discharged battery to maintain a constant voltage across the load
- Prevents exceeding the minimum cut-off voltage
- Prevents exceeding the maximum discharge current

The highest minimum input voltage required in a power management system is the lowest battery voltage the system can operate on. To maximize the available battery capacity, a power tree using the lowest battery voltage possible is required. Note that batteries come specified with a minimum cut-off voltage before the battery becomes stressed and lifespan starts to decrease considerably. As a result, the power tree should be designed to operate down to the battery's minimum cut-off voltage and should enter undervoltage lockout (UVLO) shortly afterward.

Maximizing System Efficiency

Wearable IoT devices with lightweight and compact form factors generally call for tiny batteries with reduced runtime. When the voltage rail is not in use, the power management system should shut down. To efficiently manage voltage rails in wearable IoT designs, a power management integrated circuit (PMIC) can provide flexibility by enabling/disabling power blocks when required. A PMIC can essentially enable a wearable IoT device to operate for a longer period of time between charges.

A PMIC that integrates the power tree provides design flexibility by administering power sequencing and switching, protection, monitoring, and control. Using an integrated power tree brings the advantage of maximum system efficiency versus the same power tree solution designed using discrete components, i.e., the regulators exist in a separate package apart from the PMIC. When access to all circuitry is internal to an integrated power tree, power loss is reduced because charging/discharging pin capacitance does not exist between power circuit blocks.

A power management system performs DC-DC power conversion in three distinct forms, with differences in physical size, flexibility, and efficiency.

- Linear regulators—can be fully integrated and have voltage scalability, but are not efficient
- Capacitor-based switching regulators—can be fully integrated and efficient, but do not have voltage scalability
- Inductor-based switching regulators—can be highly efficient and have voltage scalability, but tend not to be fully integrated

In general, capacitor-based switching regulators—also called charge pumps—aren't standard because of their limited output voltage scalability. For example, charge pumps are considered a suitable choice for gate drivers; however, for the circuit blocks in wearables, charge pumps aren't equipped to output the required current needed at specific voltages. That's why for these devices, linear and inductor-based switching regulators provide the most flexible power management.

To maximize efficiency, a buck regulator provides a constant input voltage to a linear regulator. **Figure 1** depicts a common single-inductor power tree in a wearable IoT device for these circuit blocks: haptic feedback, display, wireless communication, and the microprocessor core. In this typical implementation, the branch that starts from the Li+ cell goes to the buck regulator and ends at the 1.85V LDO linear regulator, resulting in a total efficiency of 81.2%. If the 1.85V LDO linear regulator were to have been connected directly to the Li+ battery, efficiency would equal to 48.7%—a 10x increase in power loss. This additionally demonstrates the value of a buck regulator in a battery-powered system.

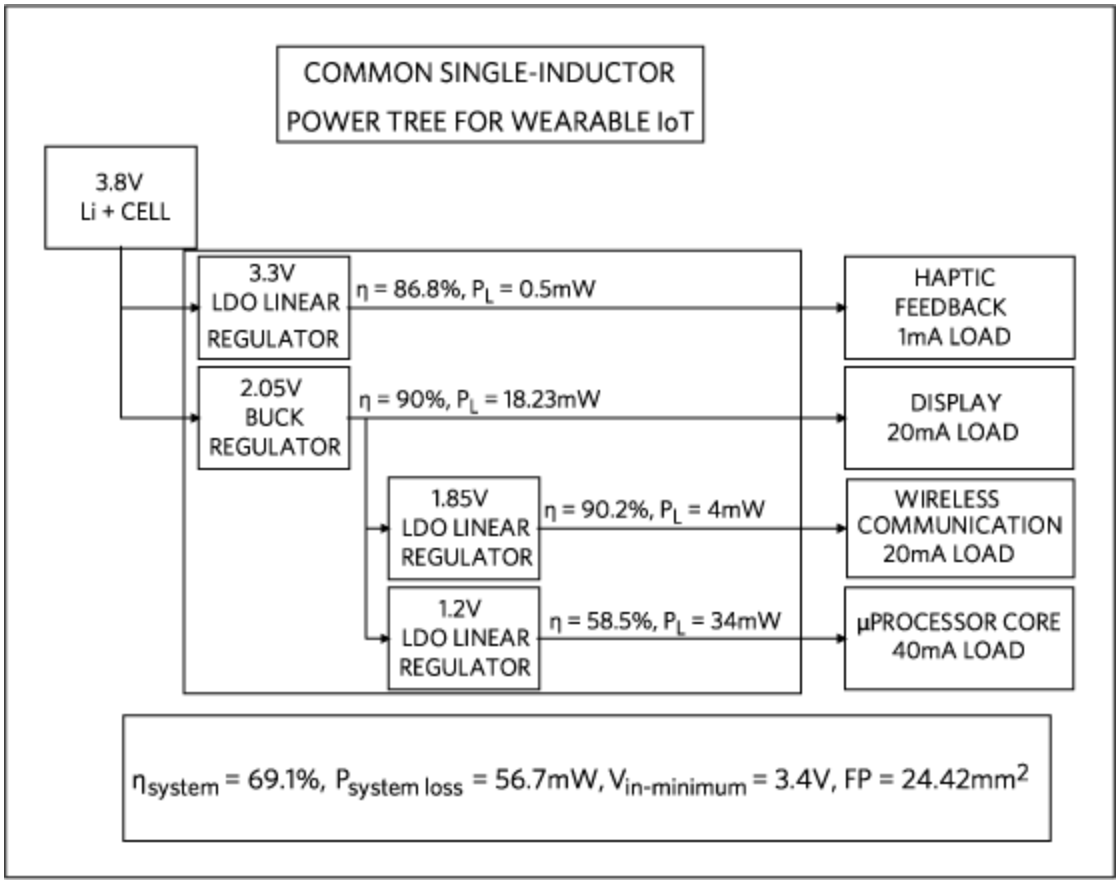

Figure 1. Common single-inductor power tree using a typical PMIC.

The following two equations calculate the power loss PL and efficiency η for linear regulators only.

Power Loss: $PL = (V_{IN} – V_{OUT}) \times IL$

Efficiency: $\eta = V_{OUT} / V_{IN}$

The following two equations calculate the same parameters but are applicable to all linear and switching regulators.

Power Loss: $PL = PO \times (1 – \eta) / \eta$

Efficiency: η = PO / PI(4)

In Figure 1, the total product of each power block efficiency defines the system efficiency ηsystem = 69.1%. The sum of each power block power loss defines the system power loss Psystem loss at 56.7mW. The 3.3V LDO with a maximum dropout voltage of 100mV dictates the minimum input voltage required by the system, which is 3.4V. The actual system footprint FP is determined by the wafer-level package (WLP) size (2.72mm x 2.47mm), the 0402 capacitors (in imperial units), and the 2.2µH 0805 inductor as depicted in **Figure 2**.

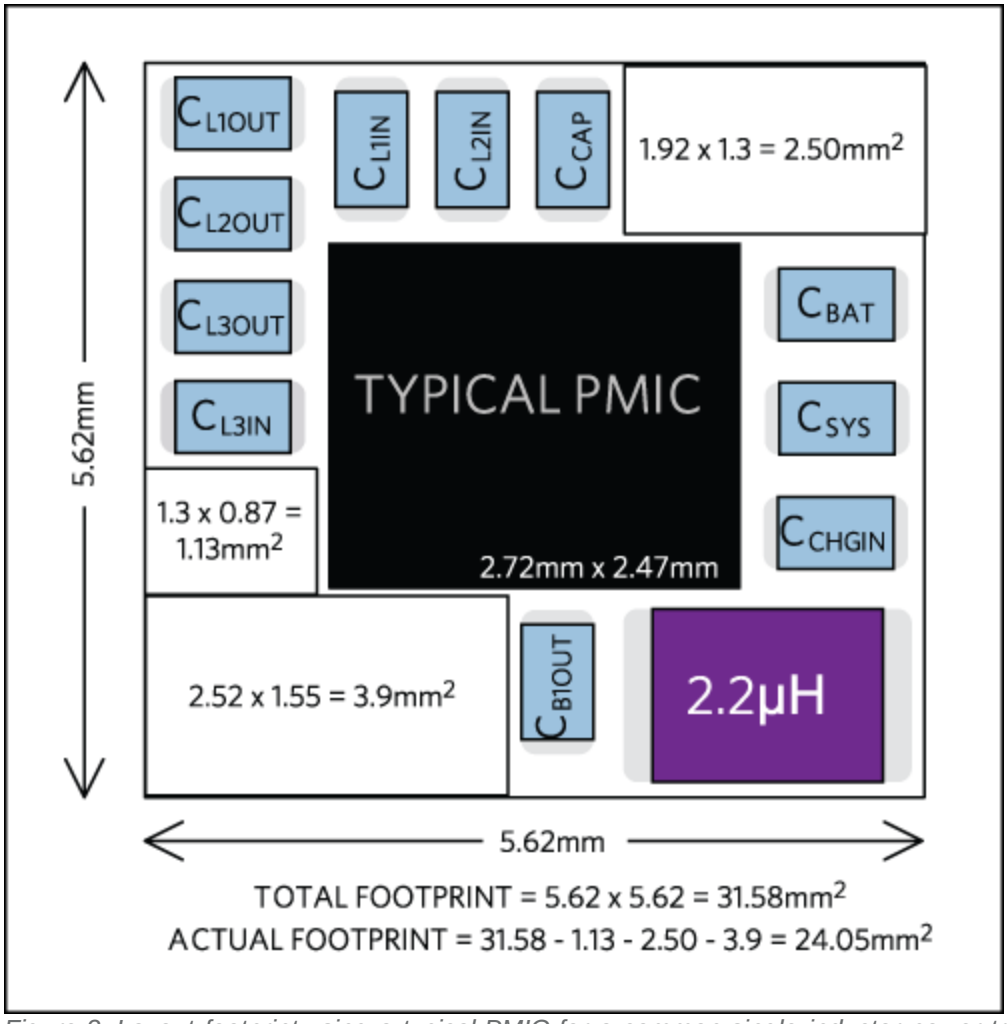

Figure 2. Layout footprint using a typical PMIC for a common single-inductor power tree. Footprint sizes for external components are given in imperial units.

Table 1 provides the physical dimensions of 0402 and 0805 surface-mount component packages.

Table 1. 0402/0805 Package Surface-Mount Component Size and Dimensions

Package (Imperial Units)	Dimensions (Width × Length)
0402	5mm x 1mm
0805	1.25mm x 2.0mm

Power Tree Figure of Merit

In a power tree, minimum size and maximum efficiency tend to be mutually exclusive, causing a trade-off between the two. To compare power loss and footprint size for different power tree implementations, consider a figure of merit (FoM), defined as:

Figure of Merit: FoM = FP x PL

where PL defines power loss in W, and FP defines the footprint size of the power tree solution in m2. A power tree with the lowest FoM is the implementation with the lowest power loss PL in the smallest footprint size FP combined. An ideal power tree would have a FoM equal to zero; however, in practical applications, there's typically a finite PCB area and power loss due to power conversion. The FoM for the common single-inductor power tree solution in Figure 1 is 1.39 x 10-3. Therefore, a power tree solution with both a decrease in power loss and a smaller footprint size would achieve a smaller FoM value.

In the power tree shown in Figure 1, there's room to enhance system efficiency, power loss, and thermal performance; however, there are trade-offs. The 1.2V LDO linear regulator can be replaced with a second on-board buck regulator, reducing power loss considerably but also bringing the following disadvantages:

- Requires an additional inductor with a height equivalent to a stack of five printer papers
- Adds more than 1mg of weight to the wearable IoT device
- Requires 8.3% more layout area (larger footprint)
- Creates an additional switching loop that can harm overall system performance
- The minimum-input voltage required by the power tree remains the same

If one does not lower the minimum-input voltage required by the power tree results, then access to the available battery capacity in the wearable IoT device is not maximized. The common single-inductor power tree in Figure 1, with a minimum input voltage of 3.3V plus the dropout voltage of the LDO linear regulator, does not use all the available battery capacity of a LiFePO4 battery with a nominal open-circuit voltage slightly below 3.5V. In cases of short bursts of high power demanded by downstream circuitry, the common single-power tree can experience UVLO because there is not enough voltage margin between the loaded voltage of a LiFePO4 and the minimum input voltage required by the power tree for operation. This common dilemma can be solved by using a single-inductor, multiple-output (SIMO) topology to lower as much as possible the FoM and the minimum input voltage required.

Reducing Power Loss and Footprint Through SIMO PMIC with Low FoM

There might be a temptation, in order to achieve high efficiency and thermal performance, to avoid linear regulators because of the always-on series-pass transistor in the control loop. But then, one must consider the space constraints on the PCB for a wearable device. Given this, a linear regulator might be the better option, providing the added benefit of a clean voltage supply required by noise-sensitive electronics such as pulse oximeters, hearables, and biopotential AFEs. These design trade-offs are unavoidable. System performance should not suffer because of a compromise—in fact, this situation opens the opportunity to design an efficient system power tree with a low FoM.

A power tree that operates from the battery's maximum nominal voltage down to the minimum cut-off voltage requires a DC-DC regulator that outputs a constant voltage without regard to the input voltage level. A non-inverting buck-or-boost regulator provides this functionality. With this type of regulator, we can efficiently step down the voltage of a new/recharged battery while it steps up a low battery voltage. As such, the battery powers the device across its full voltage range, maximizing operating time based on the current consumed.

Using a buck-boost topology as a pre-regulator enhances a cascaded linear regulator. This way, if the battery voltage nears the minimum cut-off, the linear regulator sees a constant voltage supply from the buck-boost. A buck-boost pre-regulator allows for configuration of an input voltage for the linear regulator just above the dropout voltage for minimum power loss and maximum efficiency. With a safety margin above the dropout voltage of a few percent, we can weather a future large load transient and maintain the input voltage of the linear regulator above the required minimum UVLO.

A power tree with the lowest FoM possible includes these features:

- Highly integrated PMIC with controls, protective, and topology-specific functions in one IC package.
- Single inductor shared between independent multiple buck-boost outputs, as well as a switching control algorithm that can maintain the multiple outputs within regulation while sharing the same magnetic component.
- Pulse frequency modulation (PFM) provides each output rail service before the voltage begins to fall out of regulation.
- Low quiescent current, Iq.

A SIMO PMIC reduces power loss as well as footprint. **Figure 3** shows a fully integrated SIMO implementation.

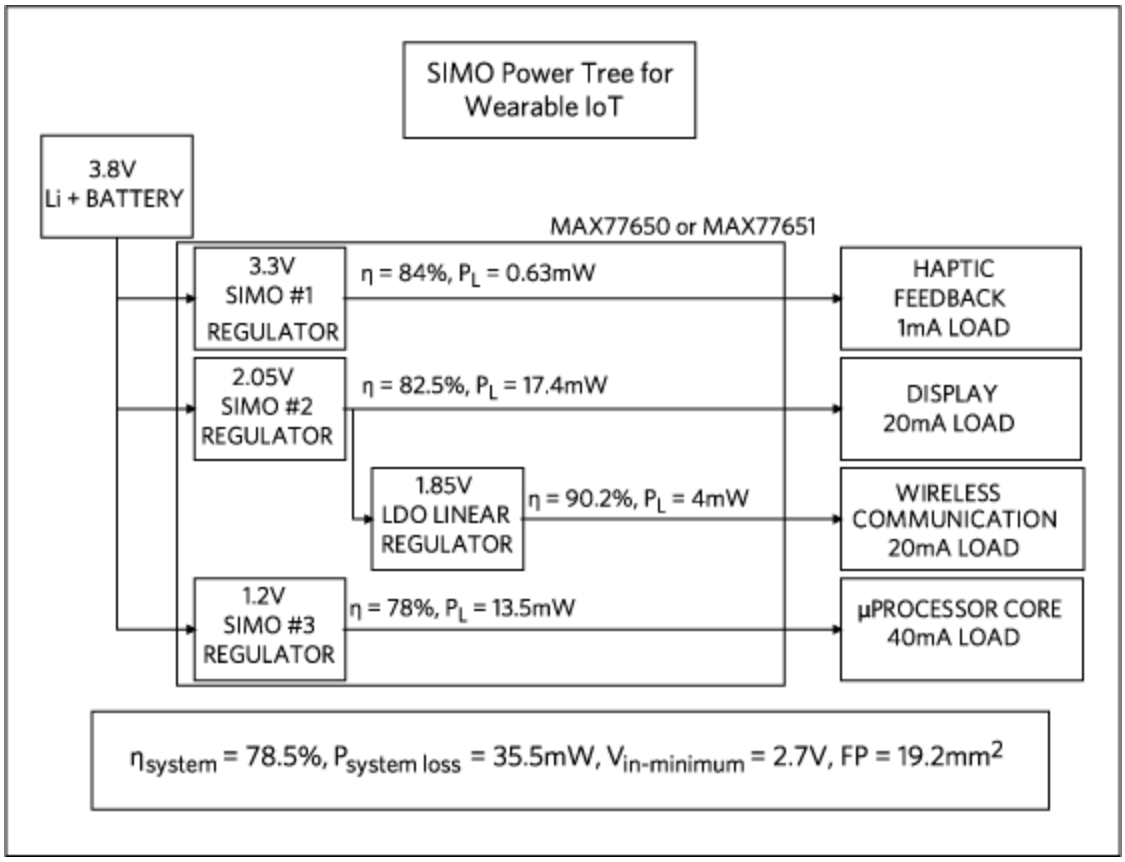

Figure 3. A SIMO power tree using the MAX77650/1 PMIC.

In Figure 3, the total product of each power block efficiency defines the system efficiency ηsystem = 78.5%. The sum of each power block power loss defines the system power loss Psystem loss = 35.5mW. The MAX77650/1 internal control logic dictates the minimum input voltage required by the system, which is 2.7V. The actual system footprint FP is determined by the MAX77650/1 wafer-level package (WLP) size (2.75mm x 2.15mm), the 0201 CBST capacitor, the 0402 capacitors, and the 2.2µH 0805 inductor as shown in **Figure 4**.

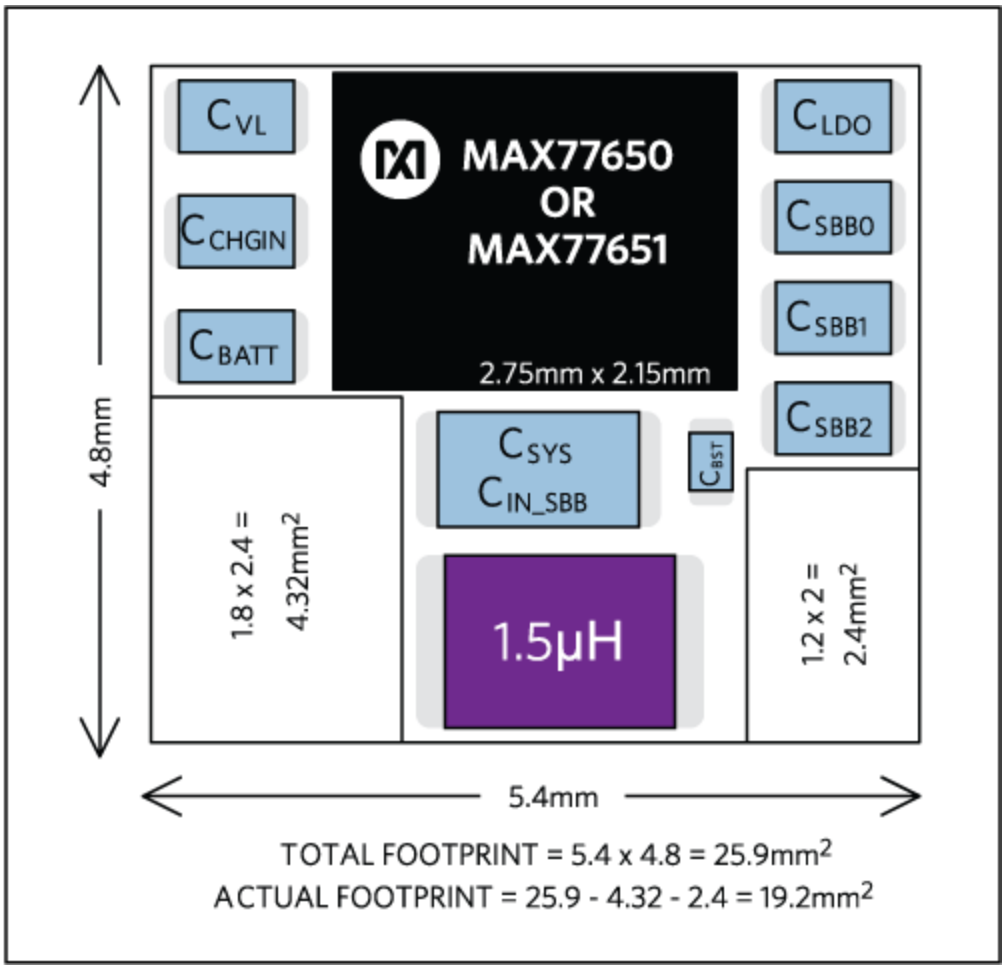

Figure 4. Layout footprint using the MAX77650/1 for a SIMO power tree. Footprint sizes for external components are given in imperial units.

Table 2 provides the physical dimensions of the 0201 surface-mount component package for CBST.

Table 2. 0201 Package Surface-Mount Component Size and Dimensions

Package (Imperial Units)	Dimensions (Width × Length)
0201	0.3mm x 0.6mm

A SIMO solves the footprint size problem by sharing a single inductor between the multiple independent buck-boost outputs. With a footprint roughly equal to 10x the area of a pinhead, the MAX77650/1 achieves a simple layout and minimizes pin capacitance that would otherwise waste power during discharge.

An integrated power tree solution also allows sharing of bypass capacitors due to pin outputs being next to each other on the IC package. The MAX77650/1 allows:

- Pin SYS and pin IN_SBB to share the same bypass capacitor
- Pin IN_LDO and pin SBBO to share the same bypass capacitor

Sharing bypass capacitors when possible and reducing the value of bypass capacitors for voltage rails placed in low-power and shutdown modes often makes more power available for the device's standard functions. Due to its integration of three independent outputs from a single inductor, the MAX77650/1 H-bridge buck-boost topology results in a SIMO power tree in Figure 3 with a FoM of 0.682 x 10-3—nearly half of the common single-inductor power tree FoM.

Also, by entering PFM mode under light loads, the SIMO provides power to the output only when necessary to maintain efficiency. When circuit blocks in a device often enter a low-power or sleep mode, then PFM becomes a requirement. With this approach, outputs that need service are given a charging cycle while the others are skipped. PFM lowers power dissipation by reducing switching losses as the load decreases.

Conclusion

Table 3 shows how with a FoM of half the value compared to the common power tree, the SIMO power tree provides the best combination of footprint size and power loss for the same system-load requirements. With a minimum input voltage of 2.7V, the SIMO power tree maximizes access to the available battery capacity.

Table 3. FoM and Minimum Input Voltage for Common Single-Inductor and SIMO Power Trees

	Common	SIMO
Figure of Merit	1.39×10^{3}	0.682×10^{3}
Minimum Operating Voltage	LDO Voltage + 3.3V	2.7V

Common SIMO Figure of Merit 1.39 x 10-3 0.682 x 10-3 Minimum Operating Voltage LDO Voltage + 3.3V 2.7V
Along with a low FoM and minimum operating voltage, the MAX77650/1 provides an integrated smart power selector, Li+/Li-Poly charger, protective functions configurable through I^2C, three LED current sinks, an analog multiplexer, and several power-monitor AFEs. With a minimum input voltage of 2.7V, the MAX77650/1 maximizes available battery capacity of LiFePO4 cells with a minimum cut-off voltage of 2.8V.

With a low FoM, an extended battery life reduces the cost of replacing/recharging batteries in wearable IoT designs. A low FoM ensures that the device can maximize the use of a low-capacity battery, reducing battery cost and allowing IoT devices to be smaller. A SIMO power tree solution configured for the application's usage profile extends operating time for the wearable IoT device.

This might or might not be applicable.

A similar version of this App Note appeared in *EDN* on February 6, 2018.

Related Parts		
MAX77650	Ultra-Low Power PMIC with 3-Output SIMO and Power Path Charger for Small Li+	Free Samples
MAX77651	Ultra-Low Power PMIC with 3-Output SIMO and Power Path Charger for Small Li+	Free Samples

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