

ADC12J2700EVM and ADC12J1600EVM User's Guide

User's Guide



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Introduction

The ADC12J2700EVM and ADC12J1600EVM is an evaluation board used to evaluate the ADC12J2700 and ADC12J1600 analog-to-digital converter (ADC) from Texas Instruments. The ADC12J2700 and ADC12J1600 device is a single-channel, 12-bit ADC capable of operating at sampling rates up to 4 Giga-samples per second (GSPS). The ADC12J2700 and ADC12J1600 device output data is transmitted over a standard JESD204B high-speed serial interface.

This evaluation board also includes the following important features:

- Transformer-coupled signal input network allowing a single-ended signal source from 400 MHz to 3 GHz
- The LMX2581 device generates the ADC sampling clock
- The LMK04828 system clock generator that generates FPGA reference clocks for the high-speed serial interface and may be used to generate the ADC sampling clock
- Transformer-coupled clock input network to test the ADC performance with a very low-noise clock source
- LM95233 temperature sensor
- High-speed serial data output over a standard FMC interface connector
- Device register programming through USB connector and FTDI USB-to-SPI bus translator

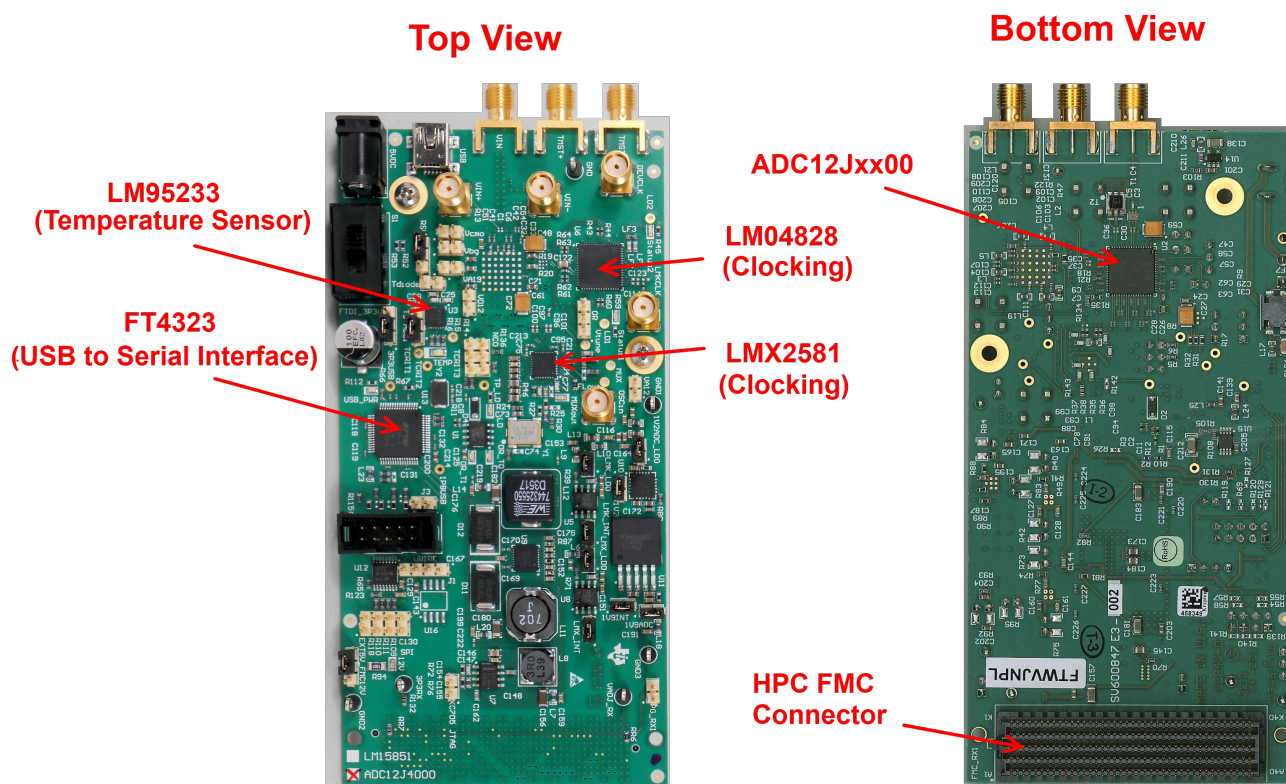


Figure 1-1. EVM Orientation

The digital data from the ADC12J2700EVM and ADC12J1600EVM board is quickly and easily captured with the TSW14J56EVM data capture board. The TSW14J56EVM captures the high-speed serial data, decodes the data, stores the data in memory, and then uploads it to a connected PC through a USB interface for analysis. The High-Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

With proper hardware selection in the HSDC Pro software, the TSW14J56 device is automatically configured to support a wide range of operating speeds of the ADC12J2700EVM and ADC12J1600EVM, but the device may not cover the full operating range of the ADC device. Serial data rates (and corresponding sampling rates) of 10 Gb/s (4 GSPS) down to 1 Gb/s (1 GSPS) are supported.

In the following sections of this document, the ADC12J2700EVM and ADC12J1600EVM evaluation board is referred to as the *EVM* and the ADC12J2700 and ADC12J1600 device is referred to as the *ADC* device.

Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the ADC device.

2.1 Evaluation Board Feature Identification Summary

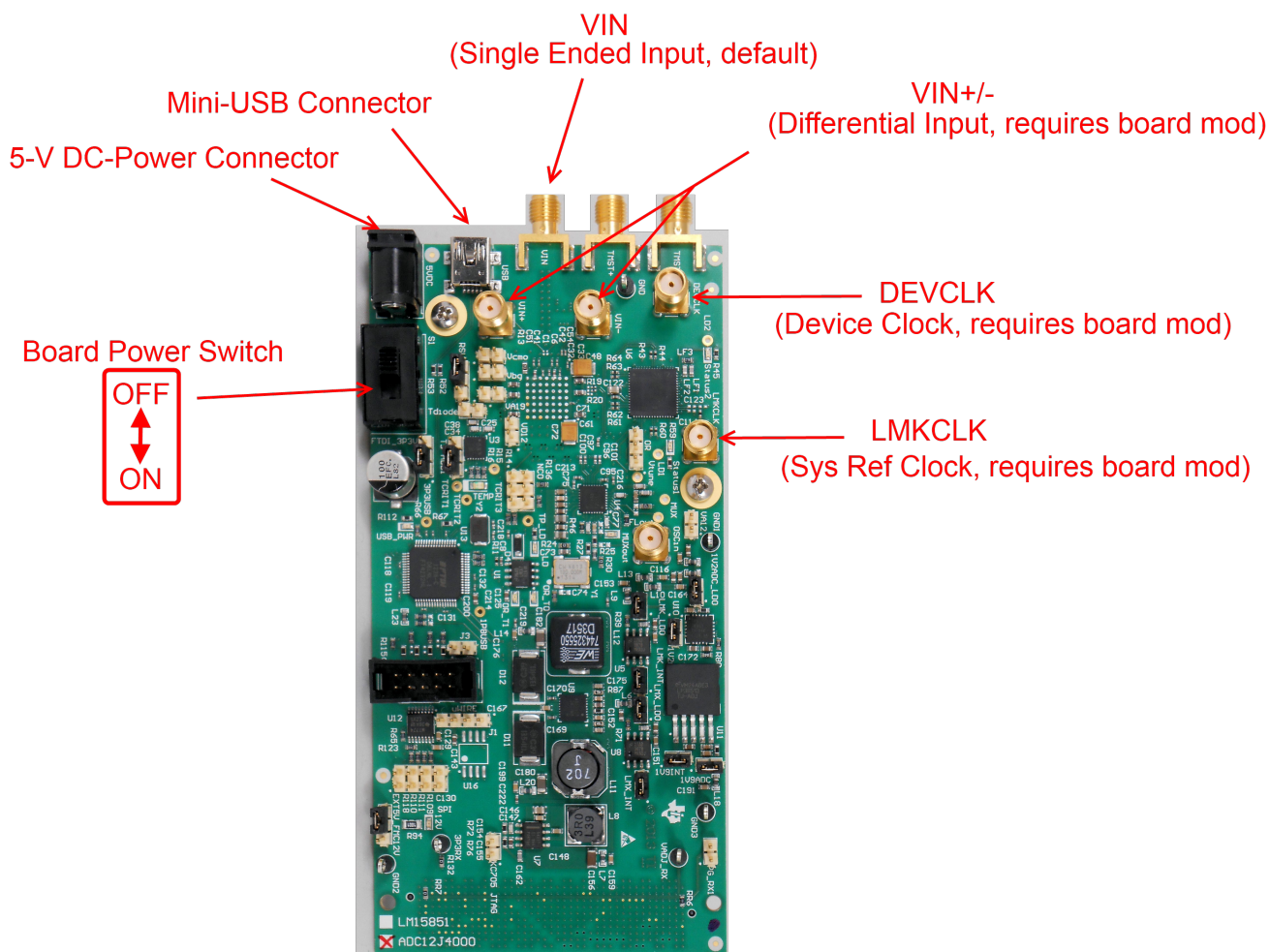


Figure 2-1. EVM Feature Locations

2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- Mini-USB cable
- 110 V to 240 V AC to 5-V DC-Power Adapter

The following equipment is not included in the EVM evaluation kit, but is required for evaluation of this product:

- TSW14J56EVM data capture board plus 5-V power supply and mini-USB cable
- High-Speed Data Converter Pro software
- PC computer running Windows XP, 7, or 8
- One low-noise signal generator for analog input. TI recommends the following generators:
 - HP HP8644B
 - Rohde & Schwarz™ SMA100A
- Bandpass filter for analog input signal (500 MHz or desired frequency). The following filters are recommended:
 - Bandpass filter, greater than or equal to 60 dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5 dB insertion loss
 - Trilithic™ 5VH-series tunable BPF
 - K&L Microwave™ BT-series tunable BPF
 - TTE KC6 or KC7-series fixed BPF
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the ADC12J2700EVM and ADC12J1600EVM have an onboard clocking solution. A few small board modifications enable external clocking. If external clocking is used, the following equipment is recommended.

- Two low-noise signal generators. TI recommends similar models to the an analog input source.
- Two bandpass filters for clock inputs. TI recommends filters similar to the analog-input path filter.

NOTE: For frequencies at 3100 MHz and below, the two clock sources must be set to the same value. For frequencies above 3100 MHz, the clock source that is used to drive the LMK04828 (labeled LMKCLK) must be half of the frequency used to drive the ADC12J2700 and ADC12J1600 sampling clock (labeled DEVCLK)

Setup Procedure

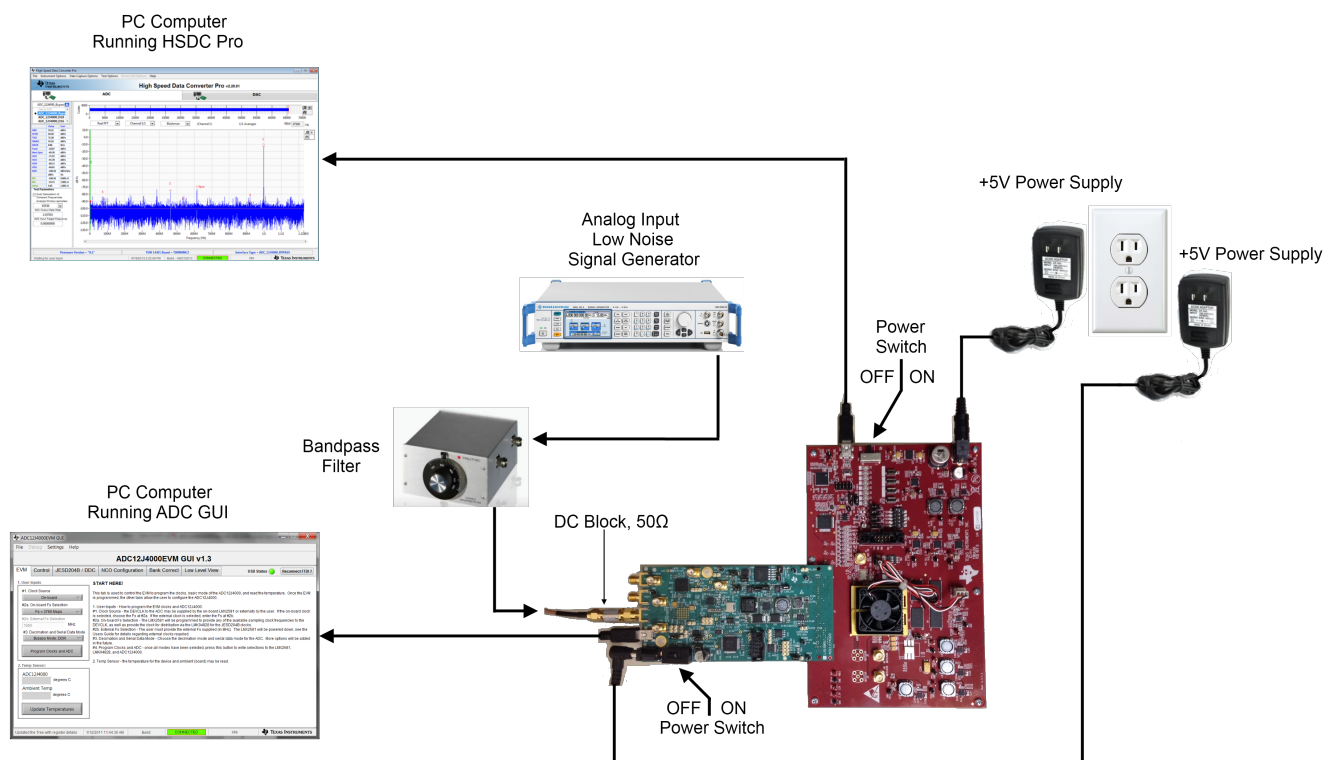


Figure 3-1. EVM Test Setup

NOTE: The HSDC Pro software must be installed before connecting the TSW14J56EVM to the PC for the first time.

3.1 Install the High Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

3.2 Install the Configuration GUI Software

1. Download the Configuration GUI software from the EVM tool folders at <http://www.ti.com/tool/ADC12J2700EVM> and <http://www.ti.com/tool/ADC12J1600EVM>.
2. Extract files from the .zip file.
3. Run the setup.exe executable file and follow the instructions.

3.3 Connect the EVM and TSW14J56EVM

With the power off, connect the ADC12J2700EVM and ADC12J1600EVM to the TSW14J56EVM through the FMC connector as shown in [Figure 3-1](#). Ensure that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm that the power switch on the TSW14J56EVM is in the off position. Connect the 5-V power supply adapter to the TSW14J56EVM.
2. Confirm that the 5-V power supply for the ADC12J2700EVM and ADC12J1600EVM is turned off. Connect the 5-V power supply to the power connector (the power connector that is the closest to the USB connector).

CAUTION

Do not turn on the power to any board. Powering up the boards in the incorrect order could potentially cause damage to one of the boards.

3.5 Connect the Signal Generators to the EVM (RF Signal Off)

1. Connect a signal generator to the VIN input of the ADC12J2700EVM and ADC12J1600EVM through a bandpass filter and attenuator at the SMA connector. This must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal from the generator. Configure the signal generator for 497.97MHz, 0 dBm.

If external Clocking is Used (Optional)

2. Connect a signal generator to the DEVCLK input of the EVM through a bandpass filter. This signal generator must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal coming from the generator. Configure the signal generator for 4 GHz. For best performance when using an RF signal generator, the power input to the CLK SMA connector must be 11 dBm (2.2 Vpp into 50 Ω) must be at least 4 dBm to function. Therefore, the signal generator must increase above 11 dB by an amount equal to any additional attenuation in the clock signal path, such as the insertion loss of the bandpass filter. For example, if the filter insertion loss is 2 dB, the signal generator must be set to 11 dBm + 2 dB = 13 dBm.
3. Connect a signal generator to the LMKCLK input of the EVM through a bandpass filter. Configure the signal generator to 2 GHz.

NOTE:

1. At sampling frequencies less than 3100 MHz, the LMKCLK must be set to the same frequency as the DEVCLK. For sampling frequencies above 3100 MHz, LMKCLK must be set to half the frequency of the DEVCLK.
2. Frequency locking the input signal generators using the 10-MHz reference can also be done if coherent sampling is desired. This is not required as HSDC Pro offers windowing options for FFT analysis. Ensure that both clocking sources are locked together with a 10-MHz reference to ensure functionality.
3. Do not turn on the RF output of any signal generator at this time.

3.6 Turn On the TSW14J56EVM Power and Connect to the PC

1. Turn on the power switch of the TSW14J56EVM.
2. Connect a mini-USB cable from the PC to the TSW14J56EVM.
3. If this is the first time connecting the TSW14J56EVM to the PC, then follow the on-screen instructions to automatically install the device drivers. See the TSW14J56EVM user's guide ([SLWU086](#)) for specific instructions.

3.7 Turn On the ADC12J2700EVM and ADC12J1600EVM Power Supplies and Connect to the PC

1. Turn on the 5-V power supply to power up the EVM.
2. Connect the EVM to the PC with the mini-USB cable.

3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to VIN. If external clocking is used, turn on the RF signal outputs connected to DEVCLK and LMKCLK.

3.9 Open the ADC12J2700EVM and ADC12J1600EVM GUI and Program the ADC and Clocks

The Device Configuration GUI must be installed separately from the HSDC Pro installation and as a stand-alone GUI.

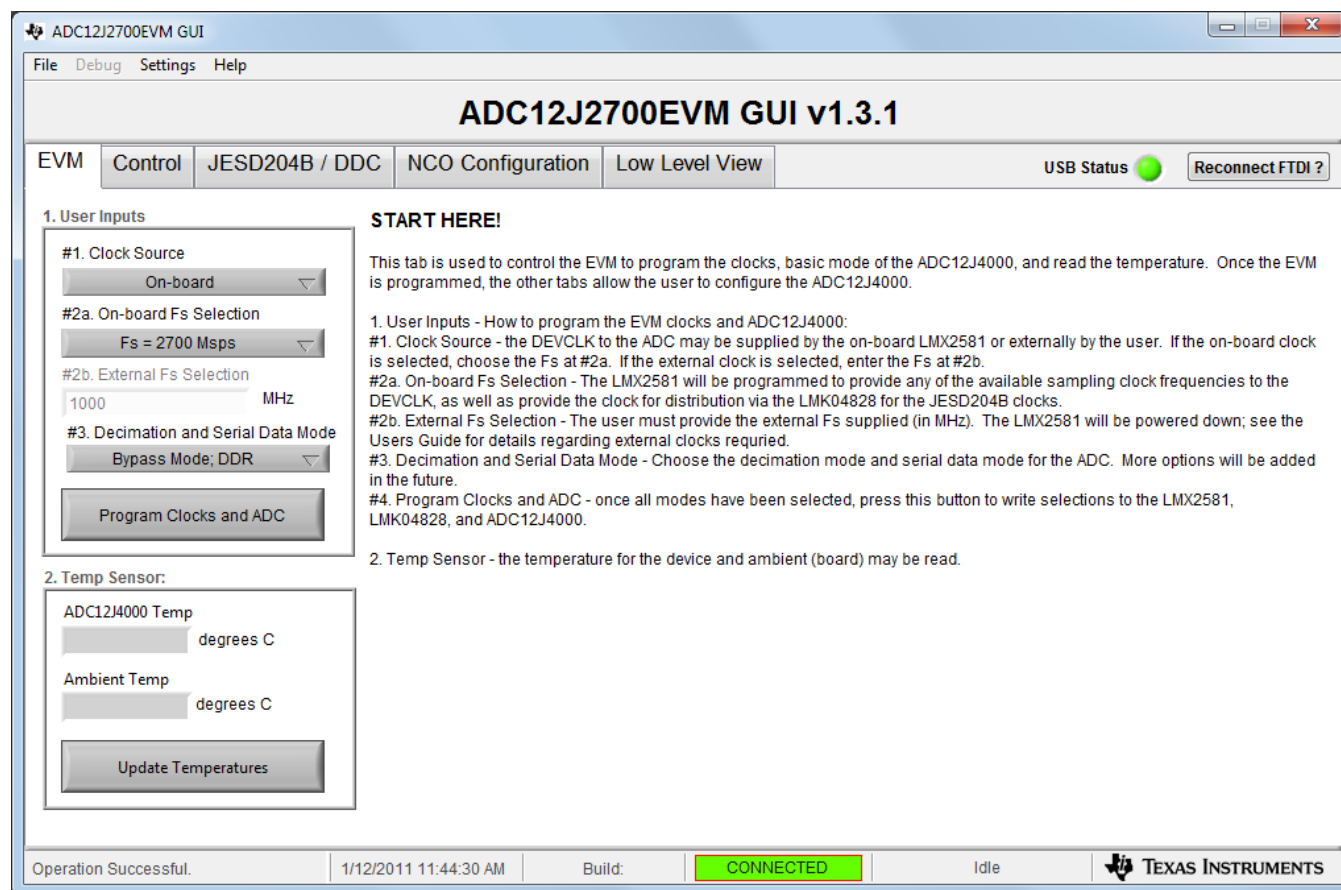


Figure 3-2. Configuration GUI EVM Tab

Figure 3-2 and Figure 3-4 show the GUI open to the *EVM* tab and *Control* tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices, namely the ADC12J2700, ADC12J1600, LMK04828, and LMX2581. The register map for each device is provided in the device data sheet ([SLAS990](#), [SNAS605](#), and [SNAS601](#), respectively).

1. Open the ADC12J2700EVM and ADC12J1600EVM GUI
2. Select the onboard clock as the clock source
3. Select Fs = 2700 or 1600 Msps as the onboard Fs selection
4.
 - a. If raw output data is desired, select Bypass Mode; DDR for the decimation and serial data mode.
 - b. If decimation is desired, select one of the decimate options. Decimate-by-16; DDR for example.

5. Click Program Clocks and ADC

3.10 Configure NCO Tab (if Decimation is Selected)

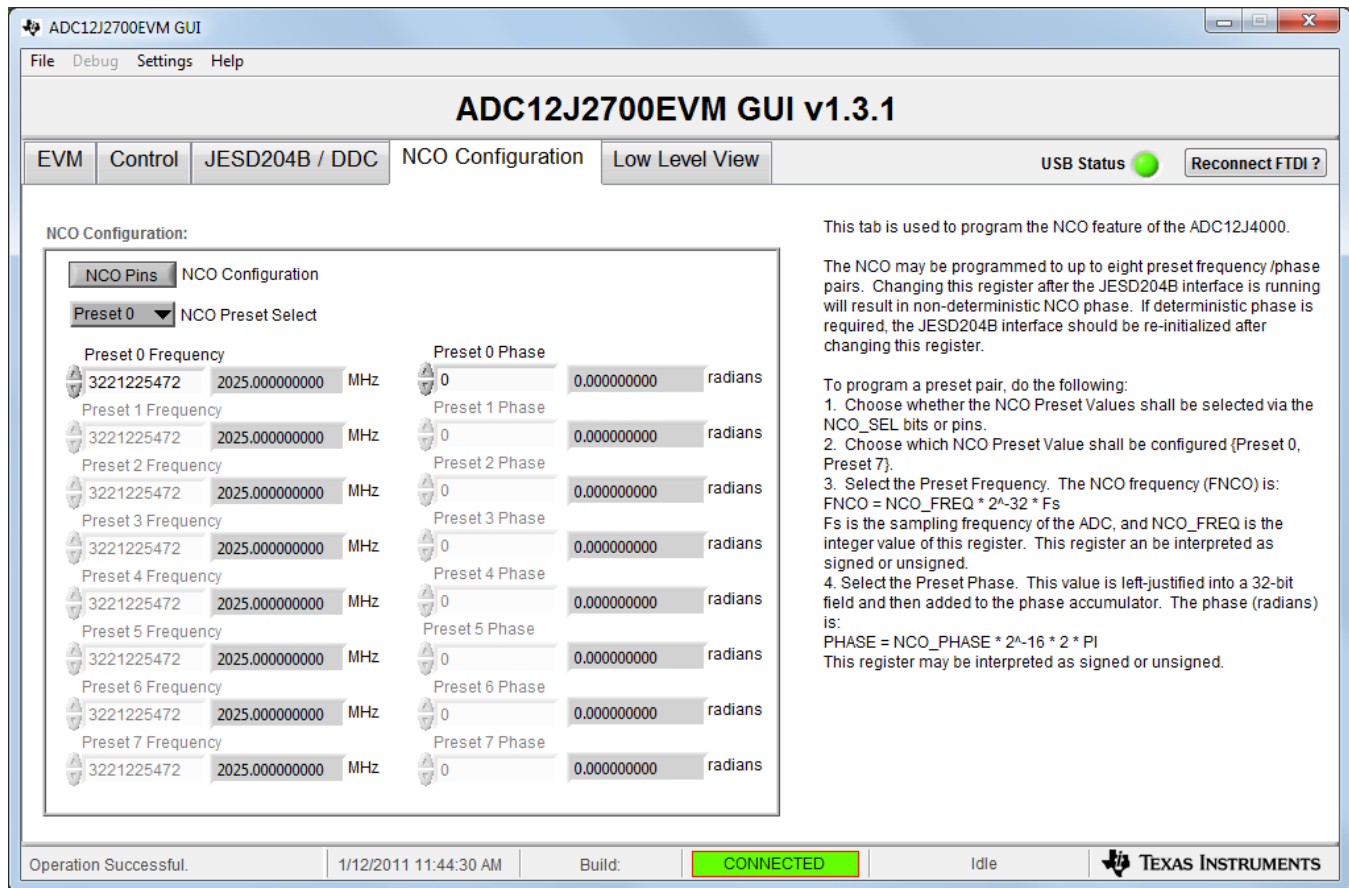


Figure 3-3. Configure NCO Tab

1. Select *Register Bits* as NCO Configuration
2. Select *Preset 0* for NCO Preset Select
3. Change *Preset 0* Frequency to 865113990 if $f_{(\text{SAMPLE})} = 2700$ Msps or 1272325993 if $f_{(\text{SAMPLE})} = 1600$ Msps, which corresponds to an NCO frequency of 543.847627239 MHz or 473.978367820 MHz respectively.

3.11 Calibrate the ADC Device on the EVM

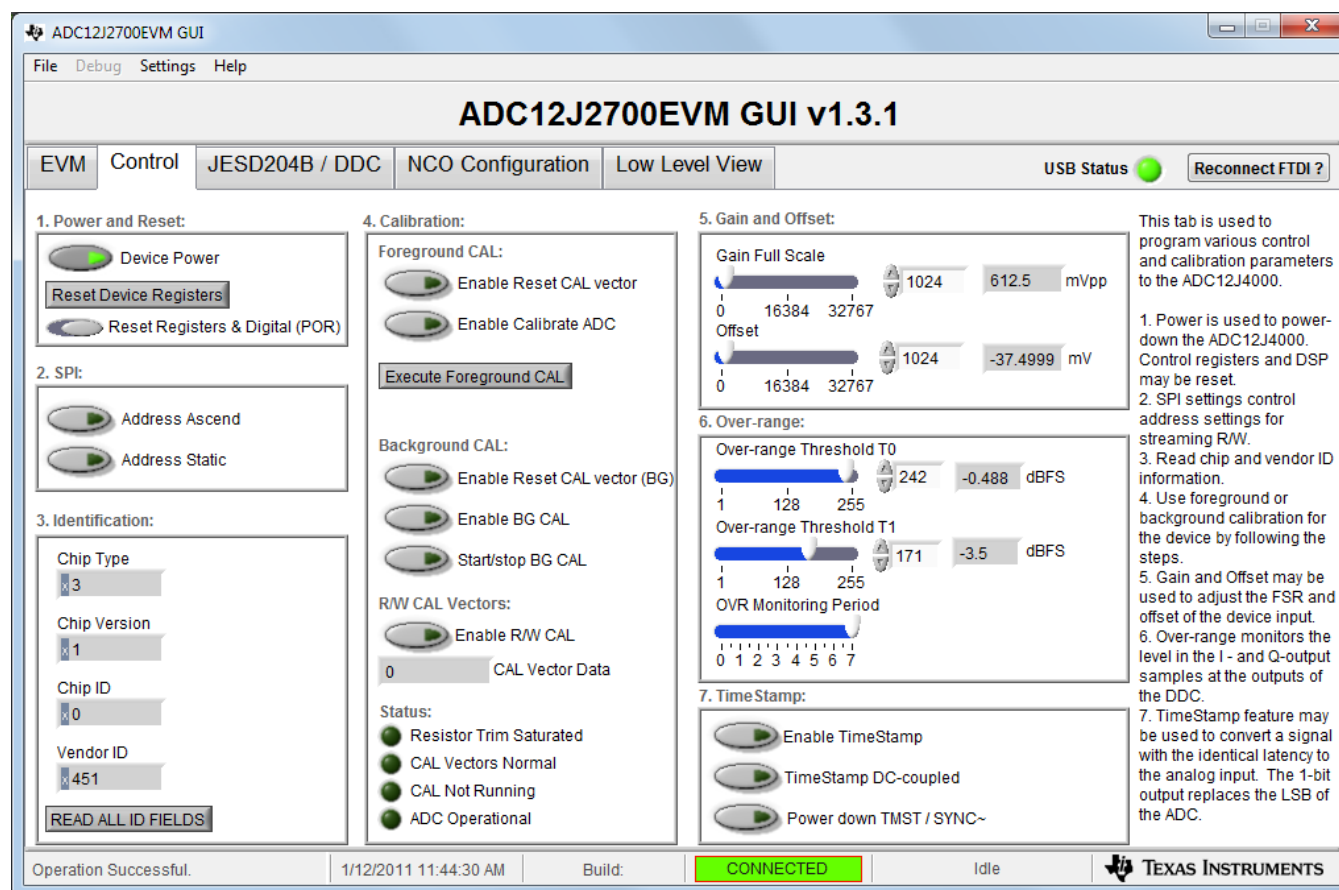


Figure 3-4. Configuration GUI ADC Control

1. With the EVM GUI open on the PC, navigate to the *Control* tab.
2. Click *Execute Foreground CAL* to calibrate the ADC.

NOTE: This calibrate button executes a calibration sequence that is required for full performance. This calibration is performed automatically during the [Section 3.9](#) step but must be performed again, any time the sampling rate changes, after significant temperature change of the ADC, or after exiting the power-down mode. See the ADC12J2700 and ADC12J1600 device data sheet, [SLAS969](#), for details regarding the necessary calibration sequence.

3.12 Open the HSDC Software and Load the FPGA Image to the TSW14J56EVM

1. Open the HSDC Pro software.
2. Click **OK** to confirm the serial number of the TSW14J56EVM device.
3. Select the *ADC12J4000_BYPASS* or *ADC12JXX00_BYPASS* device from the ADC select drop-down in the top left corner and click **Yes** to update the firmware.

NOTE: If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See [Appendix C](#) for more details.

4. Enter the ADC Output Data Rate (f_{SAMPLE}) as 2700M or 1600M or the desired output sample rate. This number must be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.13 Verify the TSW14J56EVM Switch Settings, Initialize the JESD204B Link (CPU_RESET), and Verify TSW14J56EVM Status LEDs

1. Observe the switches and jumpers on the TSW14J56EVM and verify that they are in the correct position. The required switch settings are shown in [Table 4-2](#).
2. Click the *CPU_RESET* button (SW7) on the TSW14J56EVM. This button is used to reset the JESD204B receiver core in the receiving FPGA and must be pressed after power-up, after changing the test setup, or after changing particular device configuration registers.
3. Verify the status of the D1 to D8 LEDs on the TSW14J56EVM. See [Appendix B](#) for more information regarding the status LEDs.

Table 3-1. Default State of LEDs on the TSW14J56EVM During Typical Operation

LED	STATUS
D1	Blinking
D2	On
D3	Blinking
D4	On
D5	On
D6	Off
D7	Off
D8	On
FPGA_DONE	On

3.14 Capture Data Using the HSDC Pro Software

1. Select the test to perform.
2. Select the data view.
3. Select the channel to view.
4. Click the capture button to capture new data.

Additional tips:

- Use the *Notch Frequency Bins* from the *Test Options* file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the *Capture Option* dialog from the *Data Capture Options* file menu to change the capture depth or to enable FFT averaging.
- For analyzing only a portion of the spectrum, use the *Single Tone* test with the *Bandwidth Integration Markers* from the *Test Options* file menu. The *Channel Power* test is also useful.
- For analyzing only a subset of the captured data, set the *Analysis Window (samples)* setting to a value

less than the number total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.

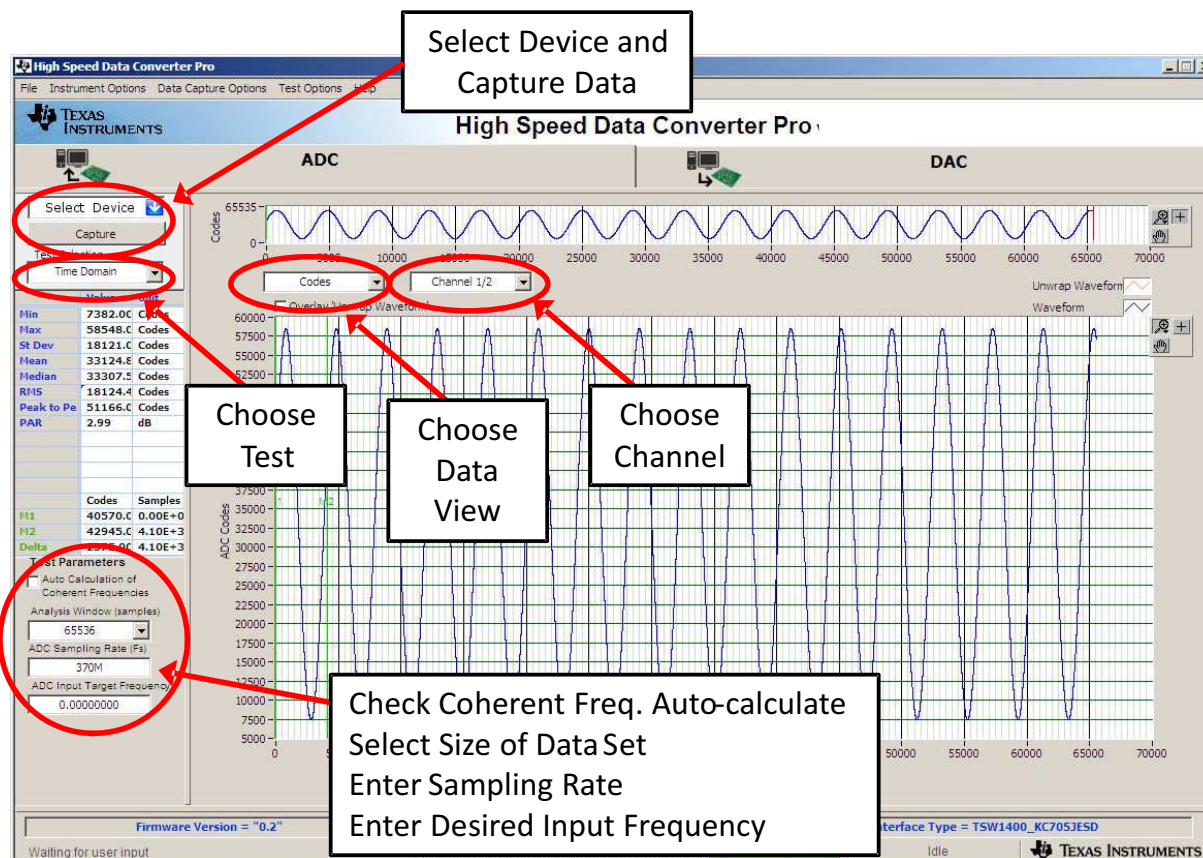


Figure 3-5. High Speed Data Converter Pro (HSDC) GUI

3.15 Re-Verify TSW14J56EVM Status LEDs

Verify the status of the D1 to D8 LEDs on the TSW14J56EVM. See [Appendix B](#) for more information regarding the status LEDs.

NOTE: D4 has changed to indicate that the JESD204B link is established.

Table 3-2. Default State of LEDs on the TSW14J56EVM during Typical Operation

LED	STATUS
D1	Blinking
D2	On
D3	Blinking
D4	Off
D5	On
D6	Off
D7	Off
D8	On
FPGA_DONE	On

Device Configuration

The ADC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

For more information about the registers in the ADC device, see the ADC12J2700 and ADC12J1600 data sheet ([SLAS969](#)) .

4.1 Supported JESD204B Device Features

The ADC device supports some configuration of the JESD204B interface. Due to limitations in the TSW14J56EVM firmware, all JESD204B link features of the ADC device are not supported. [Table 4-1](#) lists the supported and non-supported features.

Table 4-1. Supported and Non-Supported Features of the JESD204B Device

JESD204B FEATURE	SUPPORTED BY ADC DEVICE	SUPPORTED BY TSW14J56EVM
Number of lanes per channel (L)	L = 1, 2, 3, 4, 5, 8 ⁽¹⁾	L = 1,2,4,8 supported L = 3 and 5 not currently supported
Number of frames per multiframe (K)	$K_{min} = 2-12$ ⁽¹⁾ $K_{max} = 32$	Most values of K supported, constrained by requirement that $K \times F = 4^n$
Scrambling	Supported	Supported
Test patterns	PBR7, PBR11, PBR15, Ramp, D21.5, K28.5, Repeat ILA, Modified RPAT, Long/Short Transport, Serial Out 0, Serial Out 1, Bypass Lane ID, Bypass ADC Data ⁽¹⁾	ILA, Ramp, Long/Short Transport and Bypass ADC Data supported. Other patterns not supported at this time.
Speed	Lane rates from 1 to 10 Gbps ⁽¹⁾	Lane rates from 2 to 10 Gbps currently supported. $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.

⁽¹⁾ Dependent on bypass or decimation mode and output rate selection

4.2 Tab Organization

Control of the ADC device features are available in the EVM, JESD204B/DDC, NCO Configuration, Bank Correct, and Low-Level View tabs.

4.3 Low-Level Control

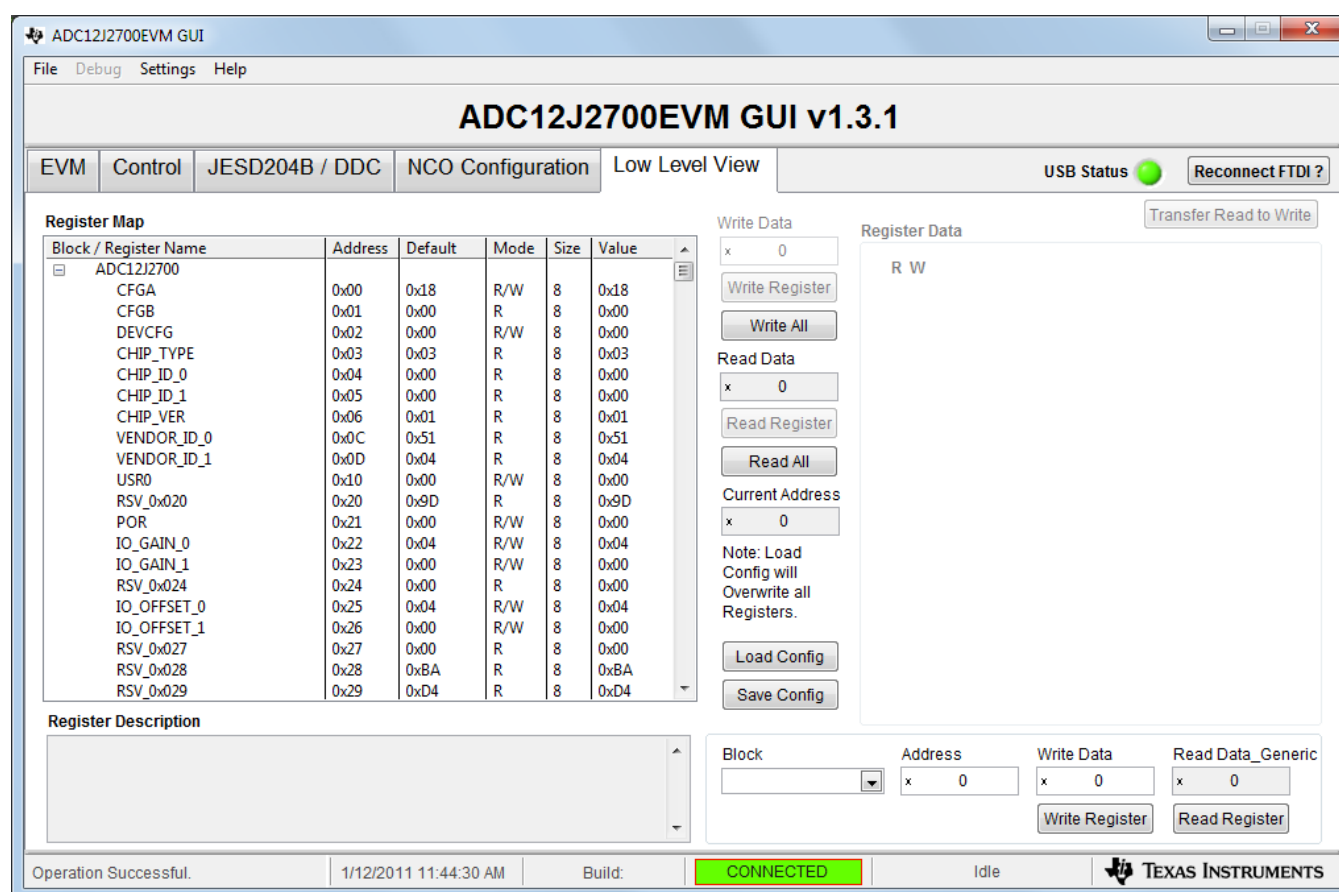
The Low-Level tab, listed in [Figure 4-1](#), allows configuration of the devices at the bit-field level. At any time, the following controls can be used to configure or read from the device.

Table 4-2. Low-Level Controls

CONTROL	DESCRIPTION
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers - Clicking on a register field allows individual bit manipulation in the register data cluster - The value column shows the value of the register at the time the GUI was last updated - The LR column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the Write Data field

Table 4-2. Low-Level Controls (continued)

CONTROL	DESCRIPTION
Write all button	Update all registers shown in the register map summary with the values shown in the Register Map Summary Can be used to re-synchronize the GUI with the state of the hardware
Read register button	Read from the register highlighted in the register map summary and display the results in the Read Data field
Read-all button	Read from all register in the register map summary and display current state of hardware
Load configuration button	Load a configuration file from disk and execute the commands in the file
Save configuration button	Save a configuration file to disk that contains the current state of configuration
Register data cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the <i>Block</i> drop-down box using the address and write data information


Figure 4-1. Low-Level Register Control Tab

Evaluation Troubleshooting

Table 5-1. Troubleshooting

ISSUE	TROUBLESHOOT
General problems	• Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J56EVM. Verify that the power switches are in the on position. • Check signal and clock connections to EVM. • Visually check the top and bottom layers of the board to verify that nothing looks discolored or damaged. • Check the connection of all boards together. • Try pressing the CPU_RESET button on the TSW14J56EVM. Also try clicking <i>Instrument Options</i> → <i>Reset Board</i> after changing the ADC configuration. • Try power-cycling the external power supply to the EVM, and reprogram the LMK and ADC devices.
TSW14J56 LEDs are not correct	• Verify the settings of the configuration switches on the TSW14J56EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the ADC device internal registers are configured properly. • If LEDs are not blinking, reprogram the ADC EVM devices. • Try pressing the CPU_RESET button on the TSW14J56EVM. • Try capturing data in HSDC Pro to force an LED status update
Configuration GUI is not working properly	• Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a <i>USB serial device</i> is recognized when the EVM is connected to the PC. • Verify that the green <i>USB Status</i> LED light in the top right corner of the GUI is lit. If it is not lit, click the <i>Reconnect FTDI</i> button. • Try restarting the configuration GUI.
Configuration GUI is not able to connect to the EVM	• Use the free FT_PROG software from FTDI chip and verify that the on-board FTDI chip is programmed with the product description <i>ADC12J2700EVM</i> and <i>ADC12J1600EVM</i>.
HSDC Pro software is not capturing good data or analysis results are incorrect.	• Verify that the TSW14J56EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDC software. • Check that the proper ADC device is selected. This should match in both HSDC Pro and the ADC GUI. • Check that the analysis parameters are properly configured.
HSDC Pro software gives a time-out error when capturing data	• Try to reprogram the LMK device and reset the JESD204 link. • Verify that the ADC sampling rate is correctly set in the HSDC software.
Sub-optimal measured performance	• Try clicking <i>Execute Foreground CAL</i> on the <i>Control</i> tab of the configuration GUI to recalibrate the ADC. • Check that the spectral analysis parameters are properly configured. • Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.

References

- ADC12J2700 and ADC12J1600 data sheet, [SLAS969](#)
- TSW14J56EVM user's guide, [SLWU086](#)
- User's guide for the High Speed Data Converter Pro Software, also available in the help menu of the software, [SLWU087](#)
- LMK04828 data sheet, [SNAS605](#)
- LMX2581 data sheet, [SNAS601](#)
- FTD245 Driver Installation Manual, www.ftdichip.com/Support/Documents/InstallGuides.htm

LED Configuration

B.1 TSW14J56EVM LED Bank and Switch Configuration

The LEDs on the TSW14J56EVM indicate the status of the capture board and the status of the JESD204B link. [Table B-1](#) list the LEDs and the LED indications.

Table B-1. Meaning of LEDs on the TSW14J56EVM

COLUMN HEAD 1	COLUMN HEAD 2
FPGA_DONE	FPGA Programming On: FPGA has been programmed Off: FPGA has not been programmed, or is being programmed
D1	TX SYNC~ On: Synchronization being requested (code group synchronization phase of link initialization) Off: Synchronization not request (code group synchronization complete) Note: The status of this LED is only valid after attempting a data capture in HSDC Pro
D2	TX Device Clock Blinking: Device clock is being received from the LMK device on the EVM Not blinking: Device clock not received
D3	SYNC~ On: Synchronization being requested (code group synchronization phase of link initialization) Off: Synchronization not request (code group synchronization complete) The status of this LED is only valid after attempting a data capture in HSDC Pro
D4	RX Device Clock Blinking: Device clock is being received from the LMK device on the EVM Not blinking: Device clock not received.
D5	No Function
D6	DDR3 Memory Calibration Done On: Calibration not done Off: Calibration done, typical operation
D7	DDR3 Memory Calibration Success On: Calibration not successful Off: Calibration successful, typical operation
D8	DDR3 Memory Calibration Fail On: Calibration not failed, typical operation Off: Calibration failed

**Table B-2. Required State of Switches on the
TSW14J56EVM**

SWITCH	STATUS
SW1[1]	Off
SW1[2]	Off
SW1[3]	Off
SW1[4]	Off
SW4[1]	Off
SW4[2]	Off
SW4[3]	Off
SW4[4]	Off
SW8, MSEL0-MSEL4	All on
TDI, TDO, TCK, TMS jumpers	All must be shorting pins 1 to 2
JP1 (Y1 PWR)	Short pins 1 to 2 (HI setting)
J8 (USB PWR)	Short pins 1 to 2
JP9 (U8 ENB)	Short pins 2 to 3

HSDC Pro Settings for Optional ADC Device Configuration

C.1 Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitter (ADC device) is configured using the K parameter on the JESD204B tab in the Configuration GUI. This parameter must be matched by the receiving device, but configuration of the K parameter of the receiver is not supported at this time.

C.2 Customizing the EVM for Optional Clocking Support

By default, the LMX2581 is configured to generate the device clock with an onboard crystal oscillator and the LMK04828 is used as a clock distribution and provides the system reference clock for the FPGA. The EVM can be configured to use an external clock with the following steps (see [Figure C-1](#)):

1. Modify the Hardware:
 - (a) Remove C32 and C33. Populate C30 and C36.
 - (b) Remove C112 and C113. Populate C114 and C123.
2. Connect the Signal Generators:
 - (a) Connect the 10-MHz references between signal generators.
 - (b) Sig Gen 1 connects to DEVCLK. Set to $F_{clk} = F_{DEVCLK}$.
 - (c) Sig Gen 2 connects to LMKCLK.
For $F_{DEVCLK} > 3100$ MHz
 $FLMKCLK = F_{DEVCLK} / 2$ connects
For $F_{DEVCLK} < 3100$ MHz, $FLMKCLK = F_{DEVCLK}$
3. Program the GUI:
 - (a) In the EVM tab, set the Clock Source to *External*.
 - (b) Enter the Sampling Frequency (DEVCLK) in step 2(b).

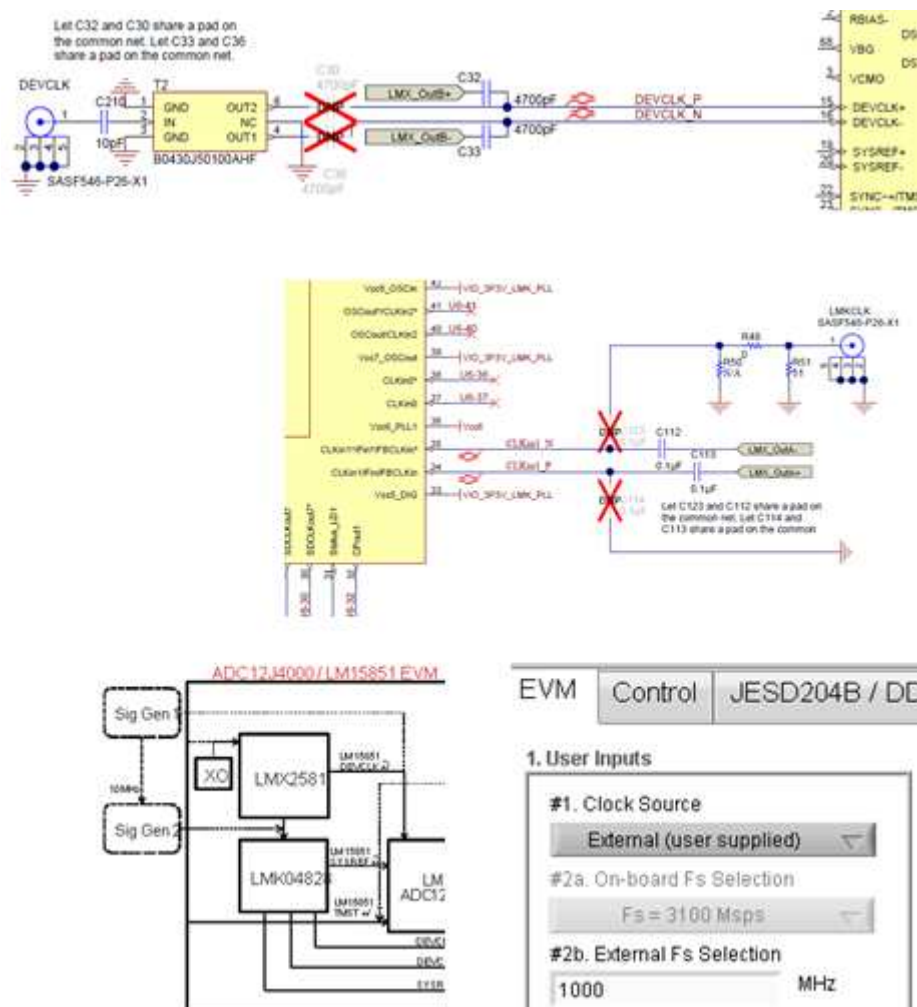


Figure C-1. Configuration for Optional Clocking Support

The LMX2581 and LMK04828 may be reconfigured to exercise more features, but this EVM is not intended to be a full evaluation platform for these devices. For a full evaluation platform see the LMK04828 tool folder: www.ti.com/tool/lmk04828bevm and the LMX2581 tool folder: <http://www.ti.com/tool/lmx2581evm>.

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U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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