

N-channel 650 V, 1.6 Ω typ., 2.3 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 3.3x3.3 HV package

Datasheet - production data

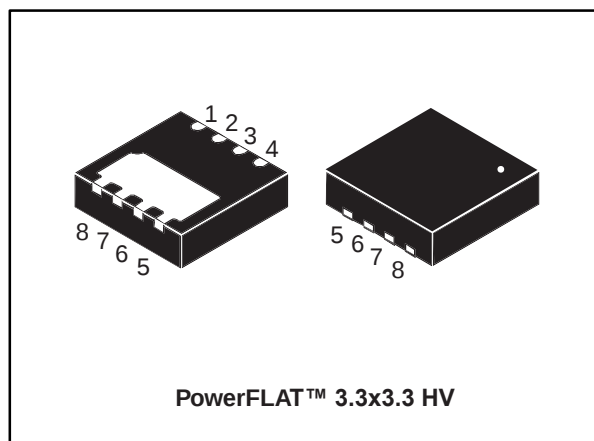
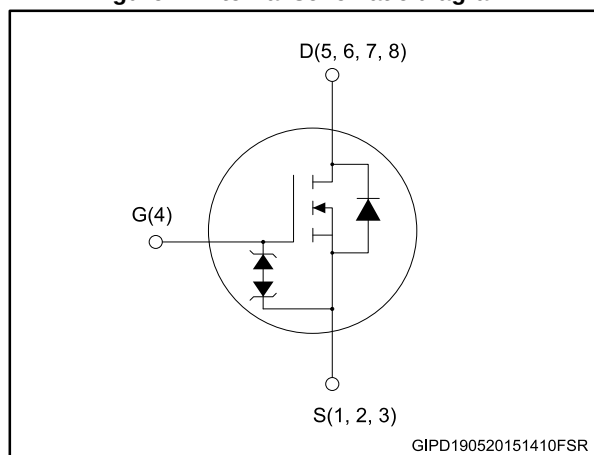


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL3N65M2	650 V	1.8 Ω	2.3 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Application

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL3N65M2	3N65M2	PowerFLAT™ 3.3x3.3 HV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.3	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.45	A
$I_D^{(2)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	0.7	A
$I_D^{(2)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	0.43	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	2.8	A
$P_{TOT}^{(2)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	22	W
I_{AS}	Avalanche current, repetitive or not-repetitive ⁽³⁾	0.3	A
E_{AS}	Single pulse avalanche energy ⁽⁴⁾	70	mJ
$dv/dt^{(5)}$	Peak diode recovery voltage slope	15	V/ns
T_J	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

⁽¹⁾The value is rated according $R_{thj-case}$.

⁽²⁾When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10\text{ s}$.

⁽³⁾Pulse width limited by T_{jmax} .

⁽⁴⁾Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$.

⁽⁵⁾ $I_{SD} \leq 2.3\text{ A}$, $dv/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3: Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	5.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max.	62.5	$^\circ\text{C}/\text{W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0 V)	I _D = 1 mA	650			V
I _{DSS}	Zero-gate voltage drain current (V _{GS} = 0 V)	V _{DS} = 650 V			1	μA
I _{GSS}	Gate body leakage current (V _{DS} = 0 V)	V _{GS} = ± 25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 1 A		1.6	1.8	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	155	-	pF
C _{oss}	Output capacitance		-	8	-	pF
C _{rss}	Reverse transfer capacitance		-	0.2	-	pF
C _{oss eq.} (1)	Output equivalent capacitance	V _{GS} = 0, V _{DS} = 0 V to 520 V	-	18	-	pF
R _g	Gate input resistance	f = 1 MHz gate DC bias = 0 test signal level = 20 mV open drain	-	8.5	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 2.3 A	-	5	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	1	-	nC
Q _{gd}	Gate-drain charge	(see Figure 15: "Test circuit for gate charge behavior")	-	1.7	-	nC

Notes:

(1)C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 1.15 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Test circuit for resistive load switching times")	-	6	-	ns
t _r	Rise time		-	3.4	-	ns
t _{d(off)}	Turn-off delay time		-	17	-	ns
t _f	Fall time		-	21.5	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		2.3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		9.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.3 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	184		ns
Q_{rr}	Reverse recovery charge		-	0.7		μC
I_{RRM}	Reverse recovery current		-	7.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 2.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	300		ns
Q_{rr}	Reverse recovery charge		-	1.1		μC
I_{RRM}	Reverse recovery current		-	7.4		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

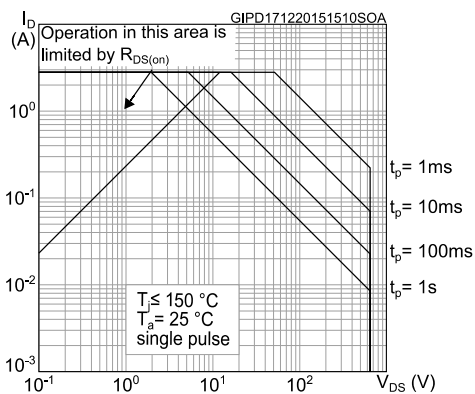


Figure 3: Thermal impedance

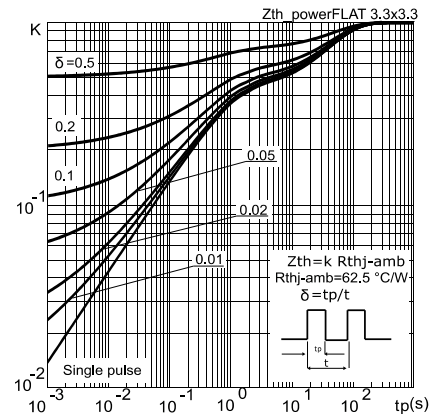


Figure 4: Output characteristics

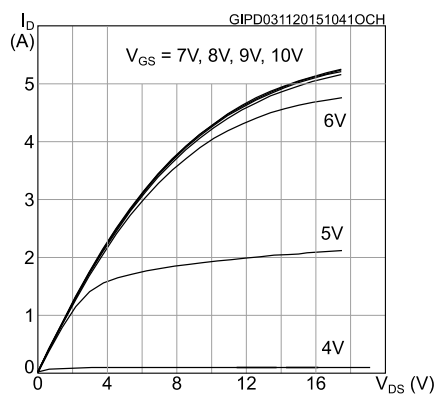


Figure 5: Transfer characteristics

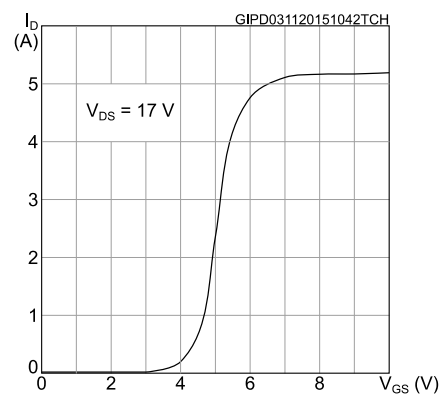


Figure 6: Gate charge vs gate-source voltage

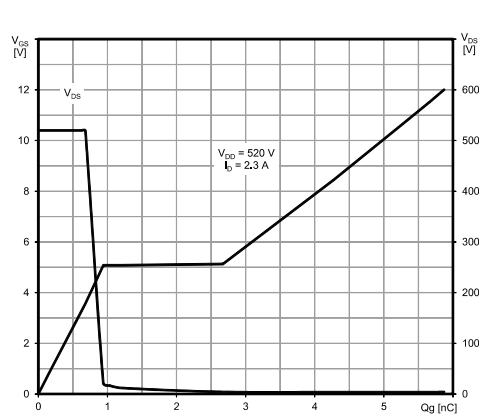


Figure 7: Static drain-source on-resistance

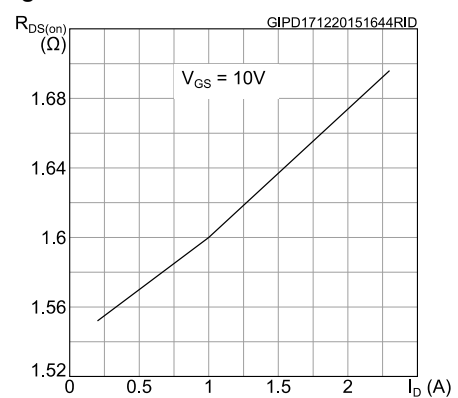


Figure 8: Capacitance variations

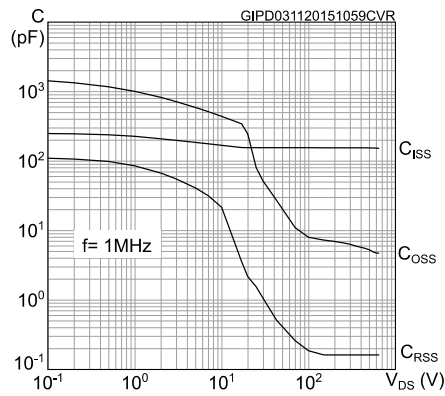


Figure 9: Normalized gate threshold voltage vs temperature

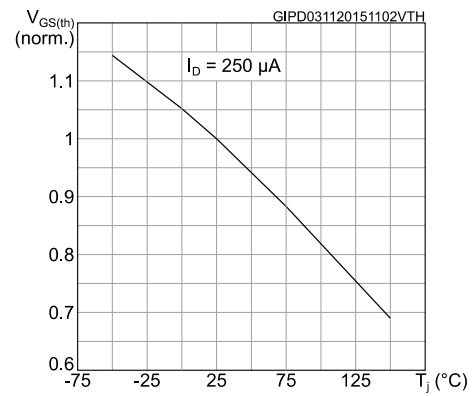


Figure 10: Normalized on-resistance vs temperature

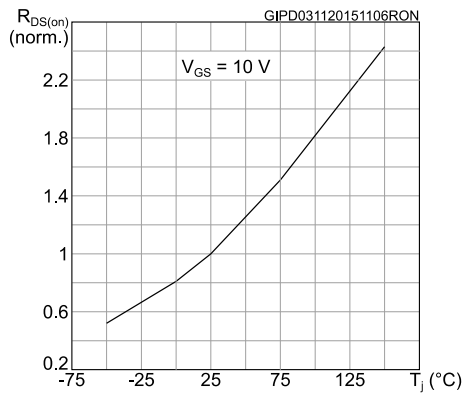
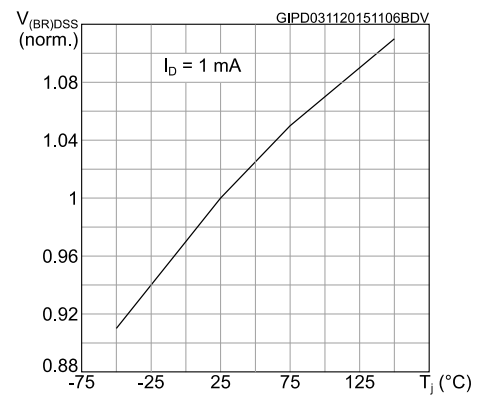
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics

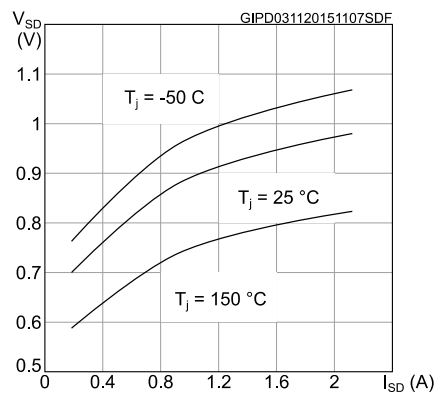
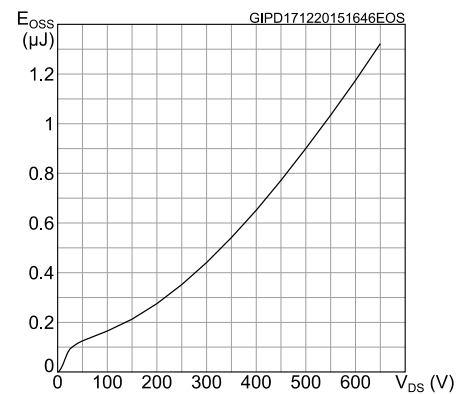


Figure 13: Output capacitance stored energy



3 Test circuits

Figure 14: Test circuit for resistive load switching times



Figure 15: Test circuit for gate charge behavior



Figure 16: Test circuit for inductive load switching and diode recovery times



Figure 17: Unclamped inductive load test circuit



Figure 18: Unclamped inductive waveform



Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 Power FLAT™ 3.3x3.3 HV package information

Figure 20: PowerFLAT™ 3.3x3.3 HV package outline

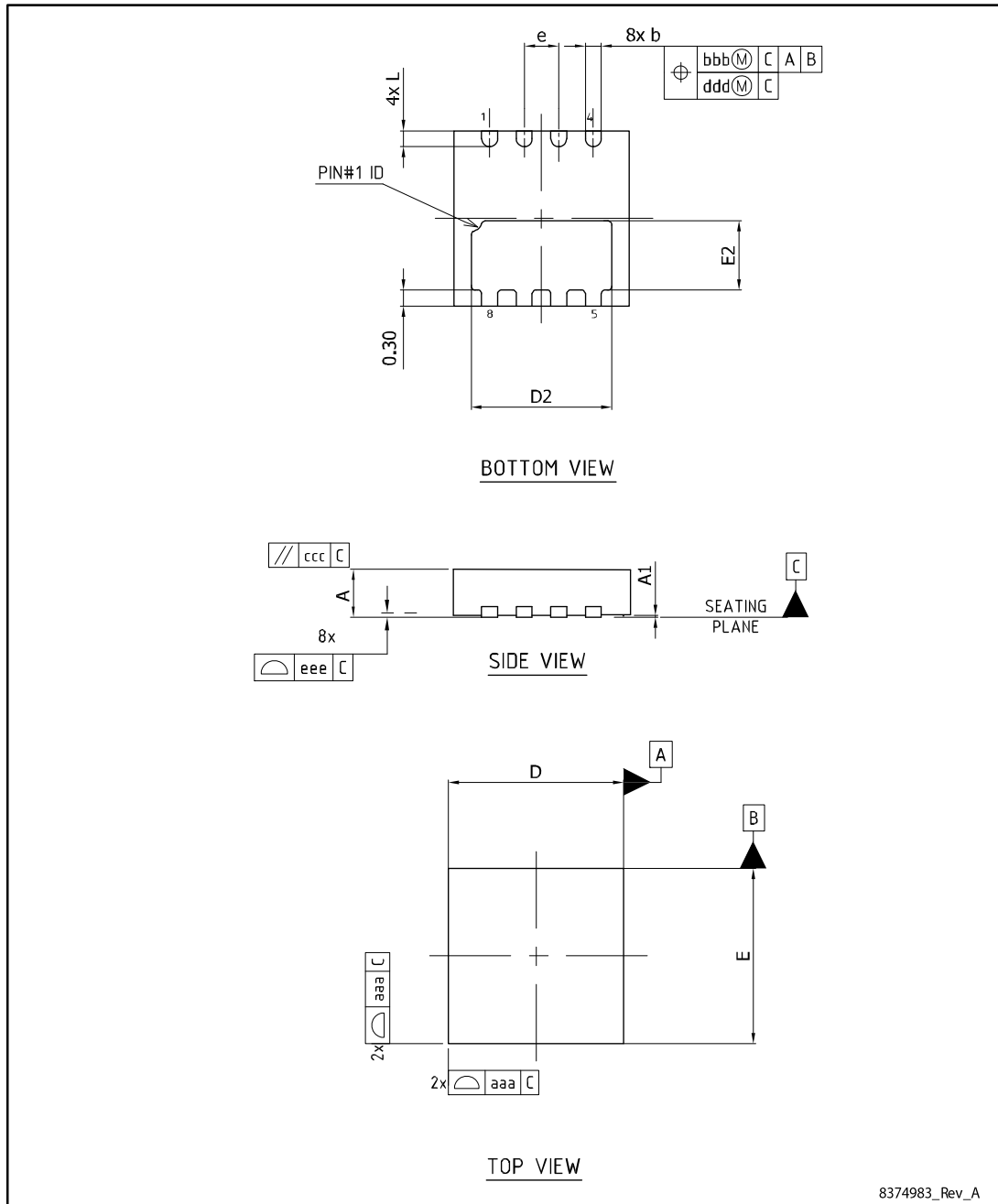
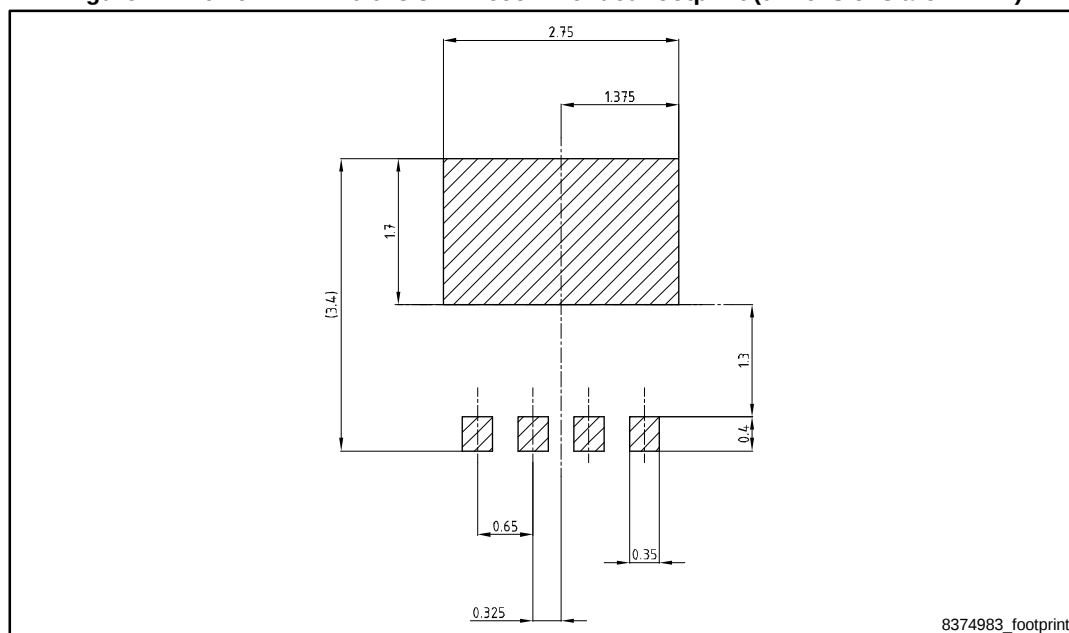


Table 8: PowerFLAT™ 3.3x3.3 HV package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
b	0.25	0.30	0.40
D		3.30	
D2	2.50	2.65	2.75
e		0.65	
E		3.30	
E2	1.15	1.30	1.40
L	0.20	0.30	0.40
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 21: PowerFLAT™ 3.3x3.3 HV recommended footprint (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
19-May-2015	1	First release.
17-Dec-2015	2	Updated title in cover page. Updated electrical characteristic section. Added electrical characteristic curves. Minor text changes.
12-Apr-2016	3	Updated Section "Features" . Updated Table 2: "Absolute maximum ratings" and Table 5: "Dynamic" . Changed Figure 6: "Gate charge vs gate-source voltage" . Document status promoted from preliminary to production data.

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