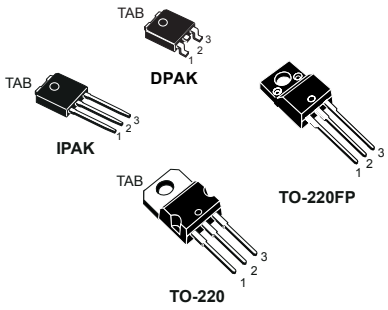
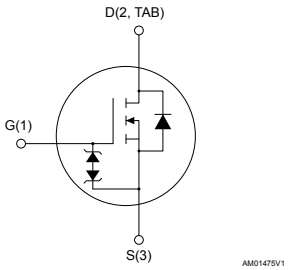
STD9N65M2, STF9N65M2
STP9N65M2, STU9N65M2

Datasheet

N-channel 650 V, 0.79 Ω typ., 5 A MDmesh M2 Power MOSFETs in DPAK, TO-220FP, TO-220 and IPAK packages





Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STD9N65M2	650 V	0.90 Ω	5 A	DPAK
STF9N65M2				TO-220FP
STP9N65M2				TO-220
STU9N65M2				IPAK

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the MDmesh M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.

STPOWER

Product status link
STD9N65M2
STF9N65M2
STP9N65M2
STU9N65M2

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	TO-220FP	
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	5	5(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	3.2	3.2(1)	A
I_{DM} (2)	Drain current (pulsed)	20		A
P_{TOT}	Total power dissipation at T_C = 25 °C	60	20	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)		2.5	kV
dv/dt(3)	Peak diode recovery voltage slope	15		V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50		V/ns
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range	-55 to 150		°C

1. *Current limited by package.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 5 A, di/dt = 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} ≤ 520 V.*

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	TO-220	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.08	6.25	2.08		°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb	50				°C/W
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-ambient		62.5		100	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max)	1	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	105	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.79	0.90	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	310	-	pF
C_{oss}	Output capacitance		-	18	-	pF
C_{rss}	Reverse transfer capacitance		-	0.9	-	pF
$C_{oss\ eq.}$ (1)	Equivalent capacitance energy related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	109	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	6.6	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 5 A	-	10.3	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	2.4	-	nC
Q_{gd}	Gate-drain charge	(see Figure 18. Test circuit for gate charge behavior)	-	4.8	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 2.5 A,	-	7.5	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	6.6	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 17. Test circuit for resistive load switching times and Figure 22. Switching time waveform)	-	22.5	-	ns
t_f	Fall time		-	18	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	276		ns
Q_{rr}	Reverse recovery charge		-	1.7		µC
I_{RRM}	Reverse recovery current		-	12.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	312		ns
Q_{rr}	Reverse recovery charge		-	1.9		µC
I_{RRM}	Reverse recovery current		-	12.4		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for DPAK and IPAK

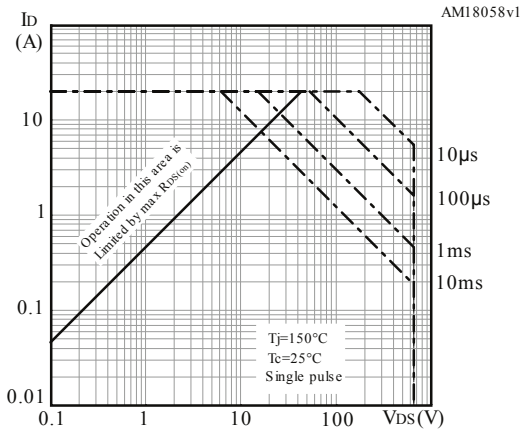


Figure 2. Thermal impedance for DPAK and IPAK

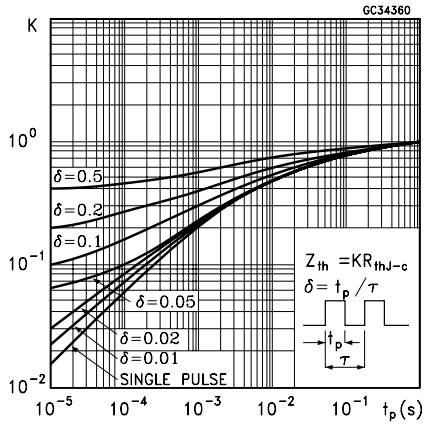


Figure 3. Safe operating area for TO-220FP

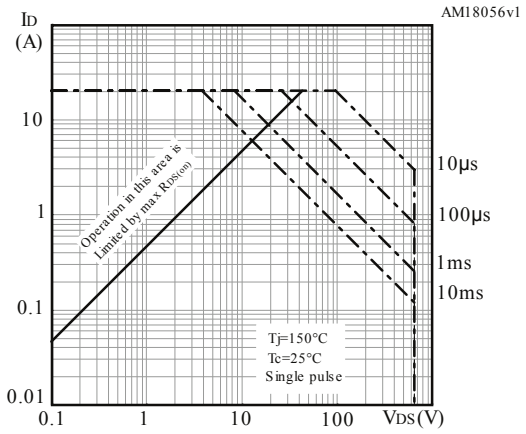


Figure 4. Thermal impedance for TO-220FP

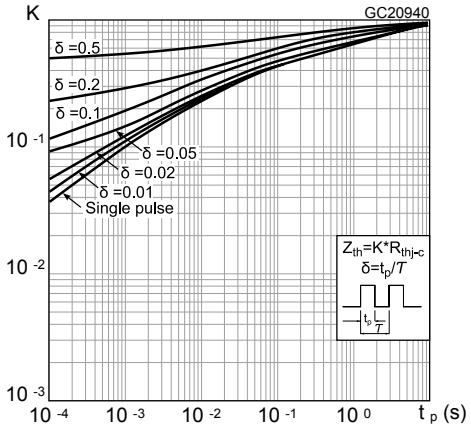


Figure 5. Safe operating area for TO-220

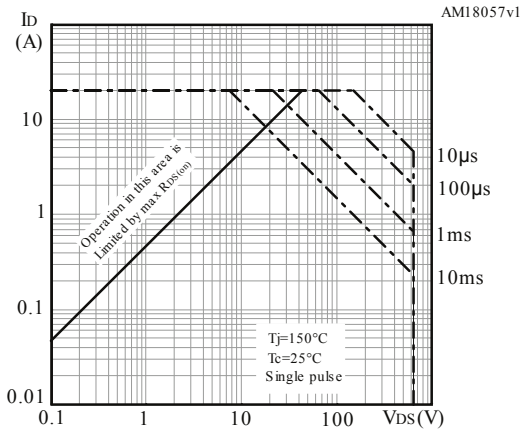


Figure 6. Thermal impedance for TO-220

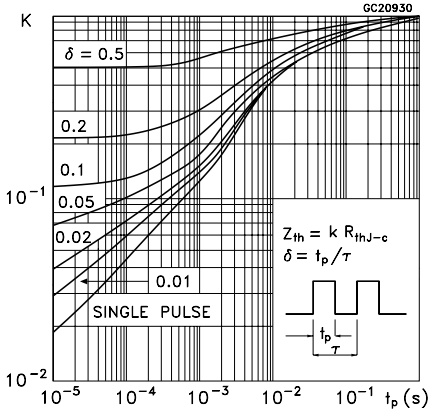


Figure 7. Output characteristics

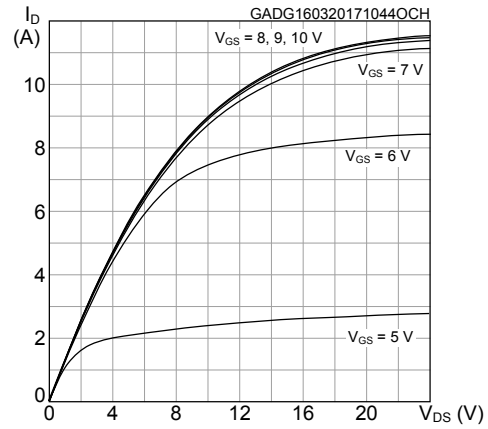


Figure 8. Transfer characteristics

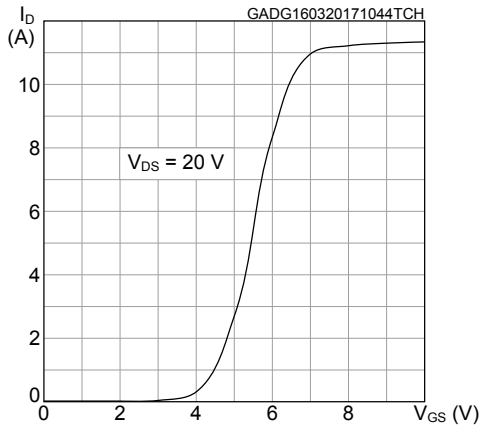


Figure 9. Gate charge vs gate-source voltage

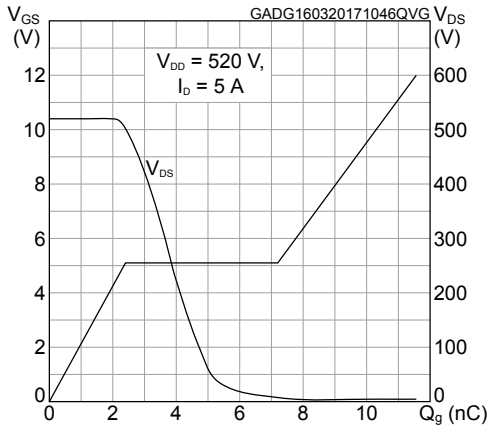


Figure 10. Static drain-source on-resistance

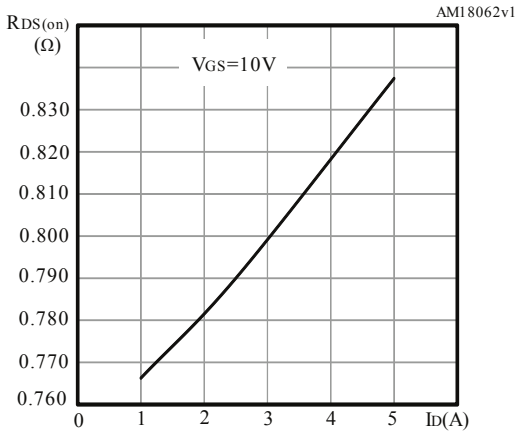


Figure 11. Capacitance variations

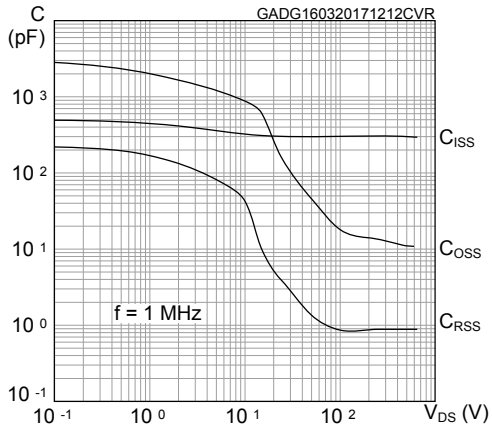


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

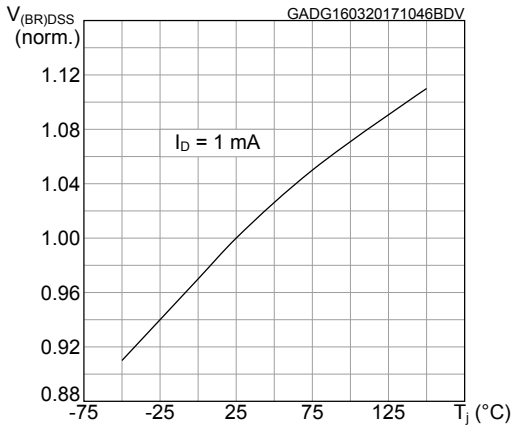


Figure 13. Normalized gate threshold voltage vs temperature

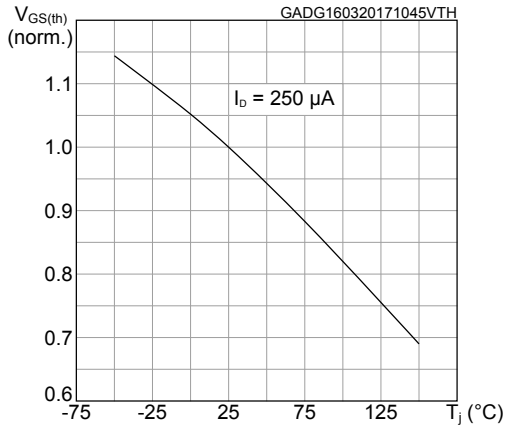


Figure 14. Normalized on-resistance vs temperature

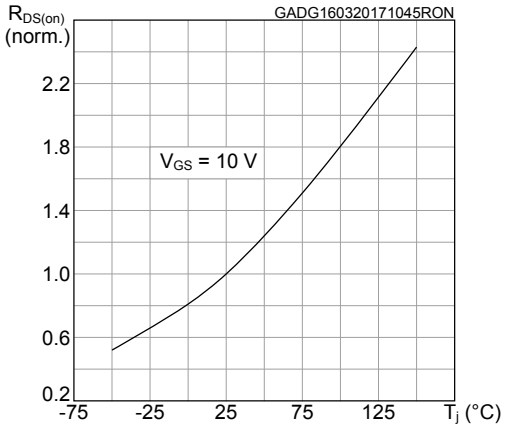


Figure 15. Source-drain diode forward characteristics

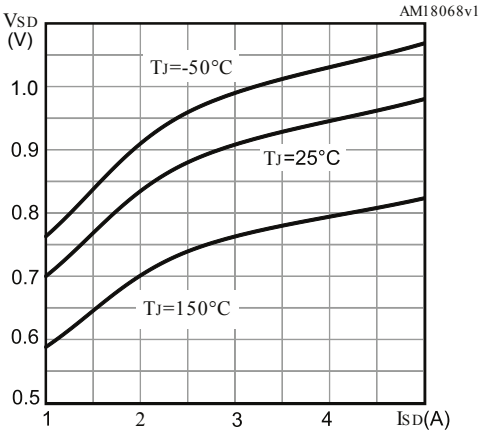
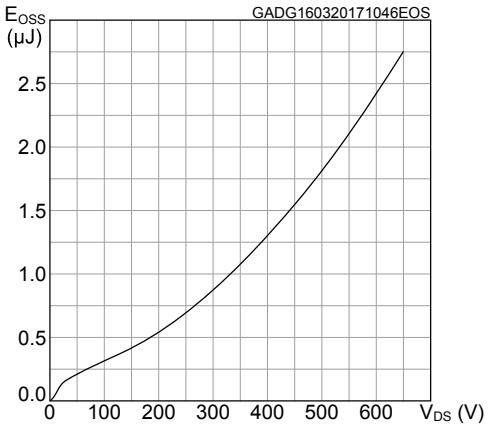


Figure 16. Output capacitance stored energy



3 Test circuits

Figure 17. Test circuit for resistive load switching times

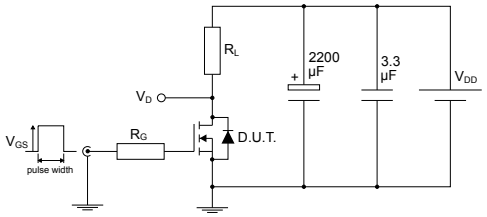


Figure 18. Test circuit for gate charge behavior

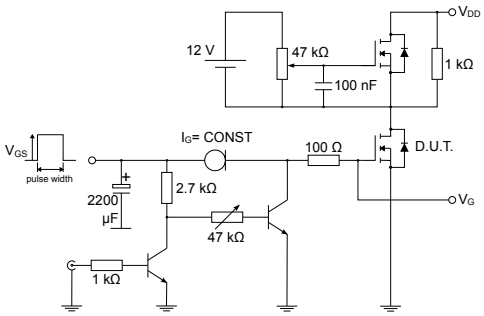


Figure 19. Test circuit for inductive load switching and diode recovery times

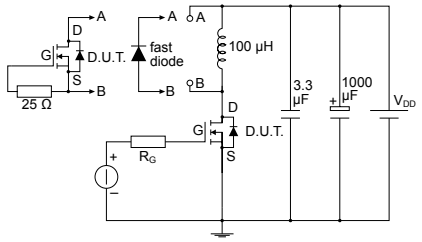


Figure 20. Unclamped inductive load test circuit

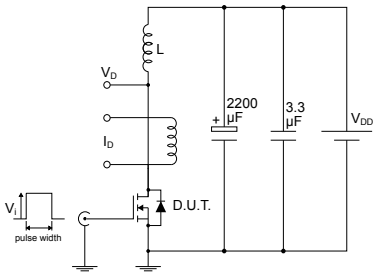


Figure 21. Unclamped inductive waveform

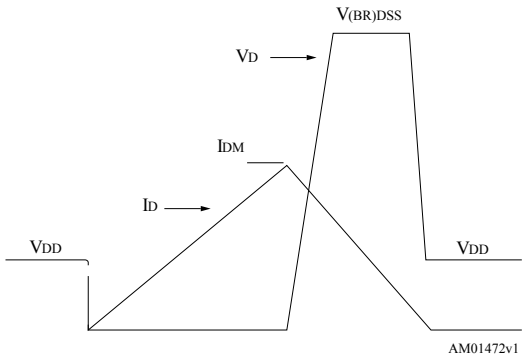
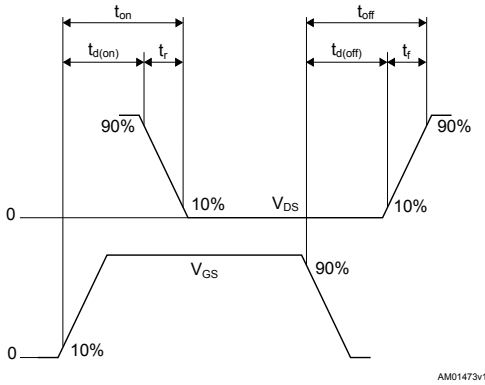


Figure 22. Switching time waveform

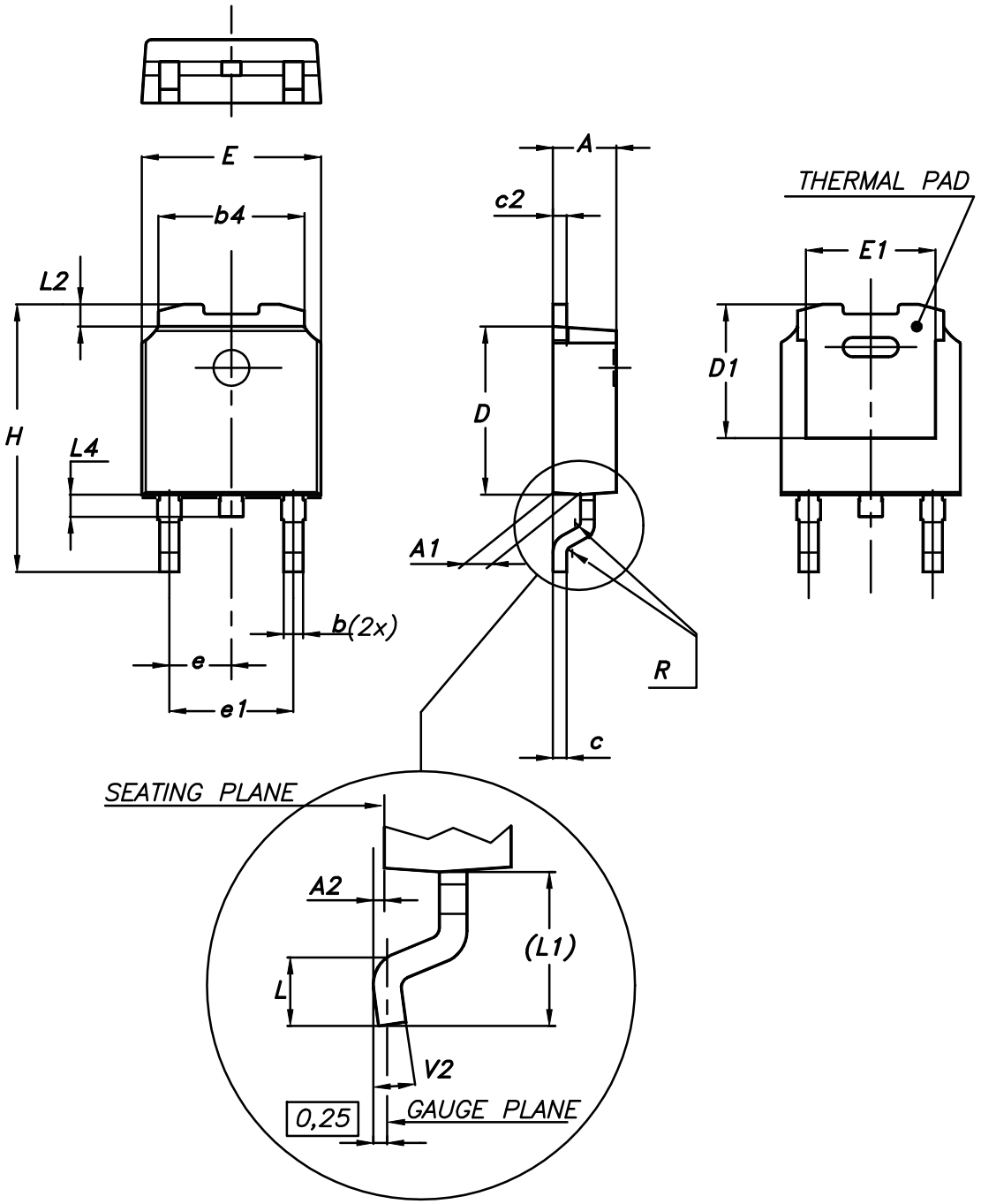


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 23. **DPAK (TO-252) type A package outline**



0068772_A_26

Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 24. **DPAK (TO-252) type C package outline**

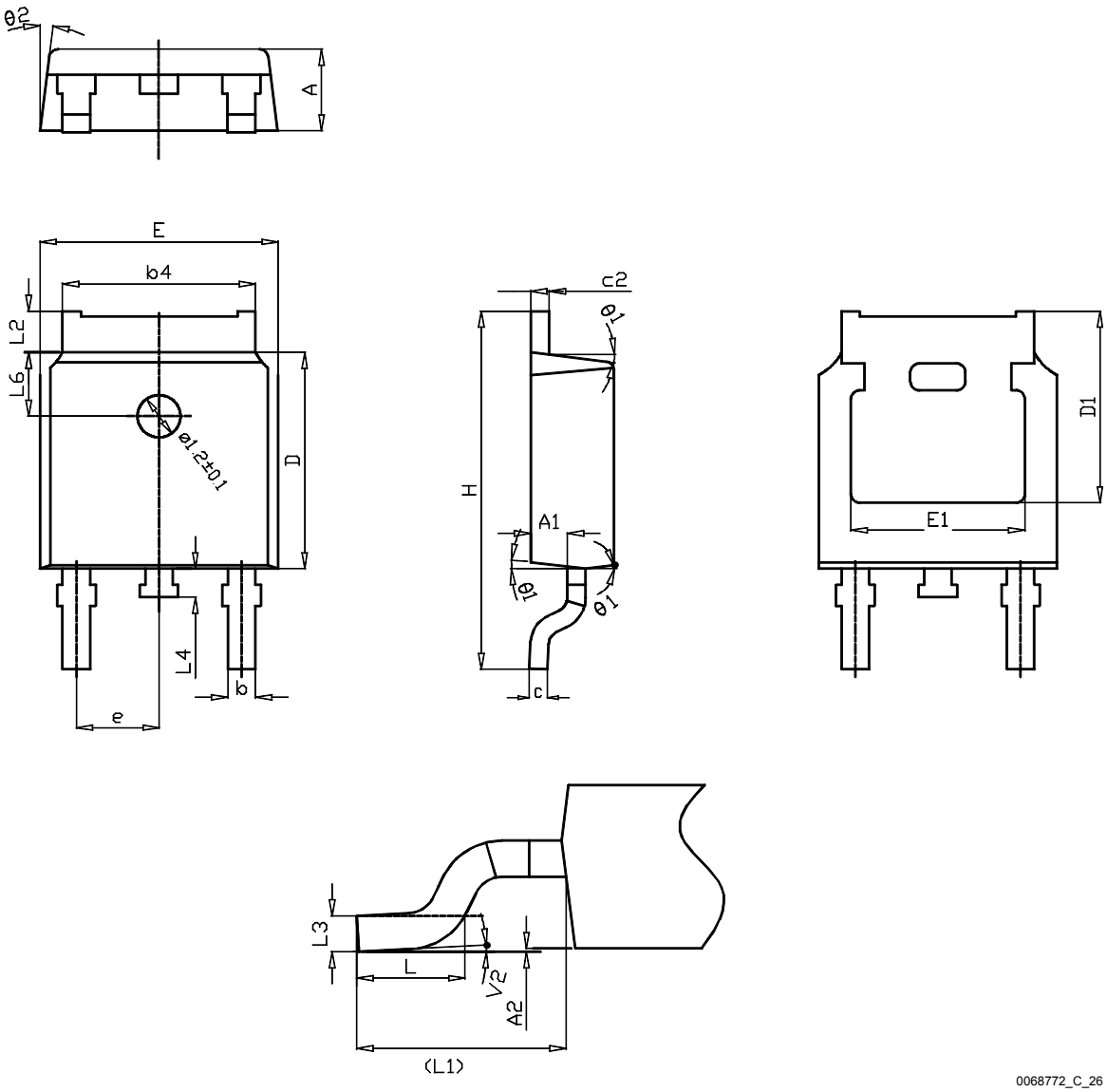
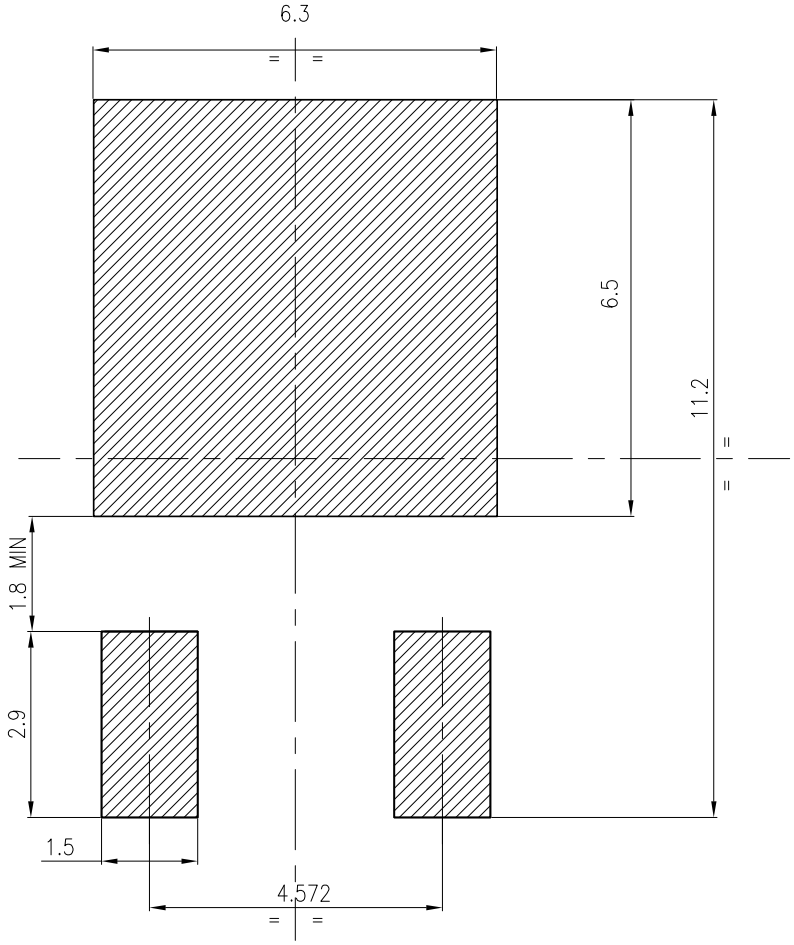


Table 9. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 25. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



FP_0068772_26

4.3 DPAK (TO-252) packing information

Figure 26. **DPAK (TO-252) tape outline**

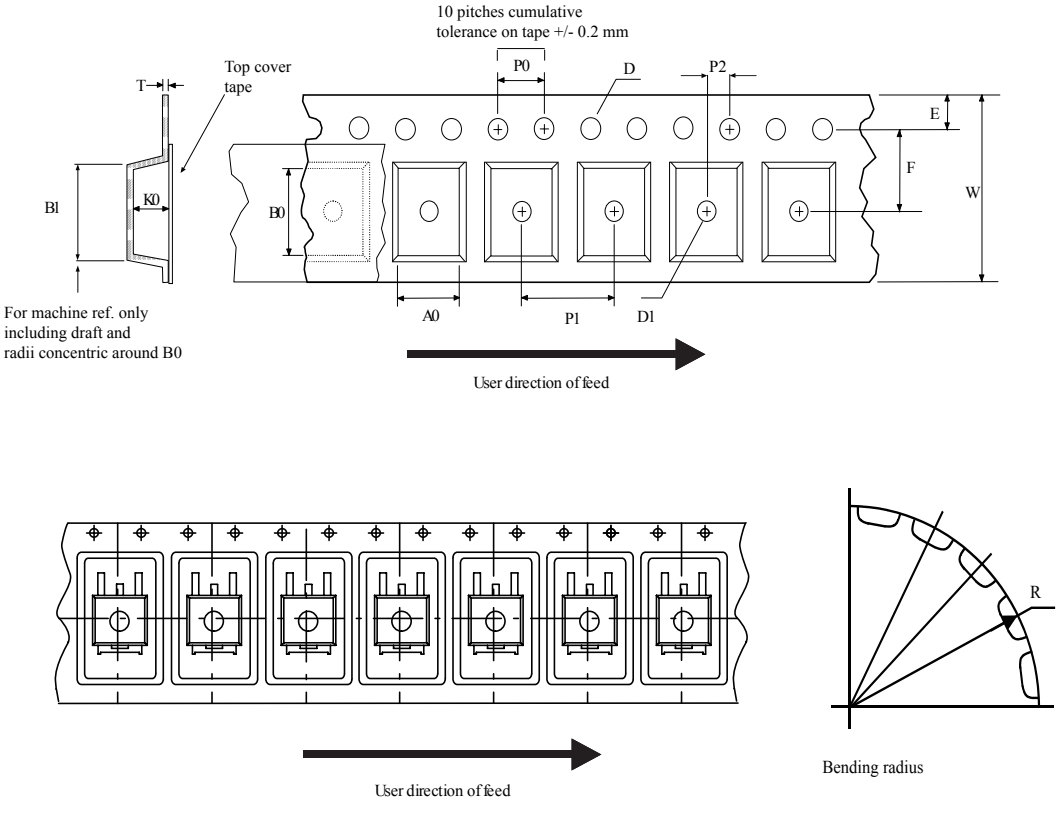
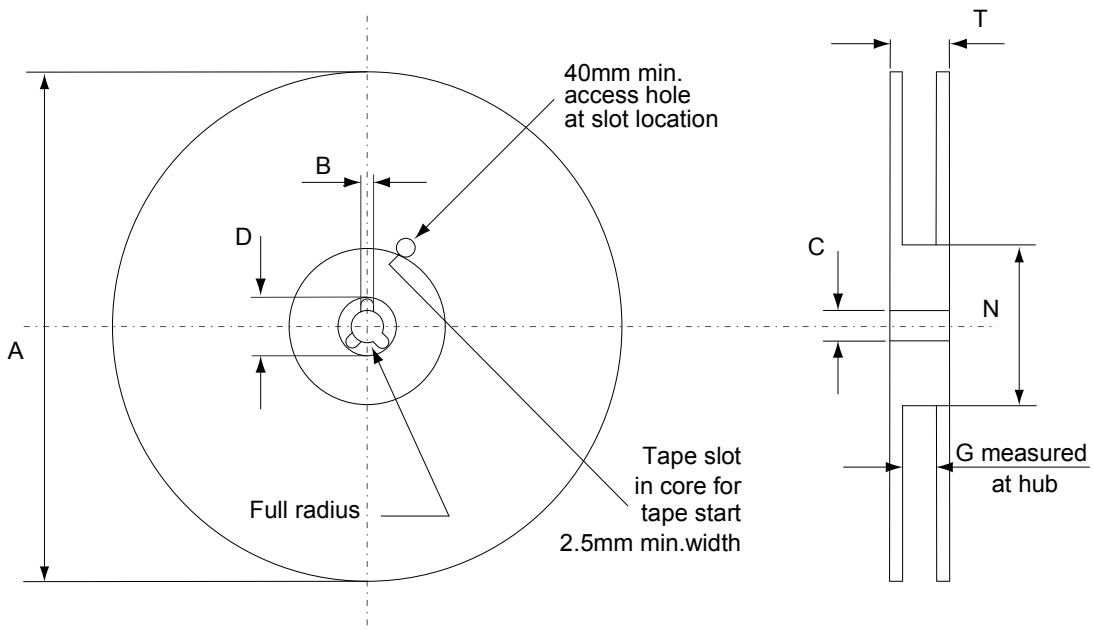


Figure 27. **DPAK (TO-252) reel outline**



AM06038v1

Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220FP package information

Figure 28. **TO-220FP package outline**

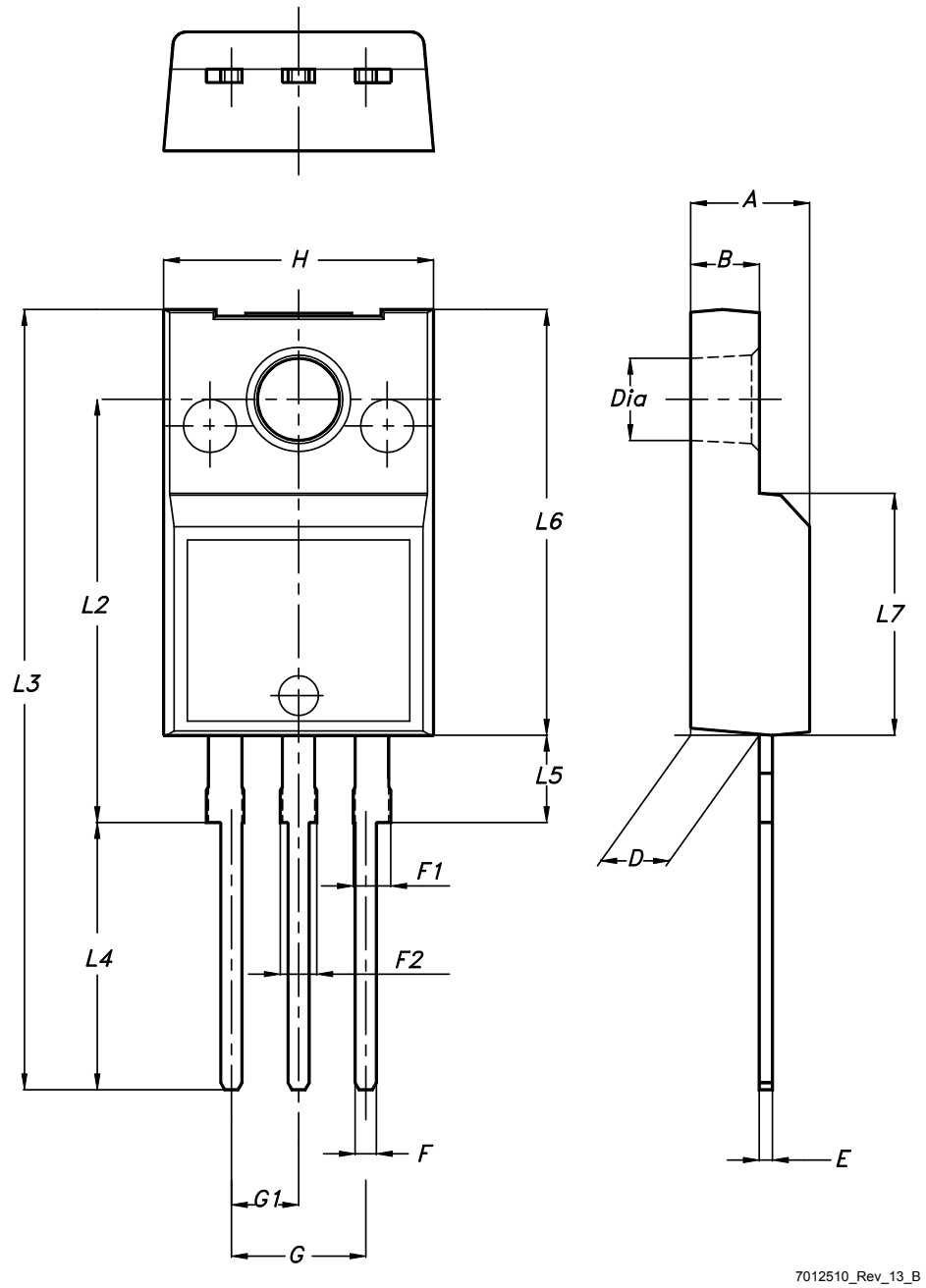
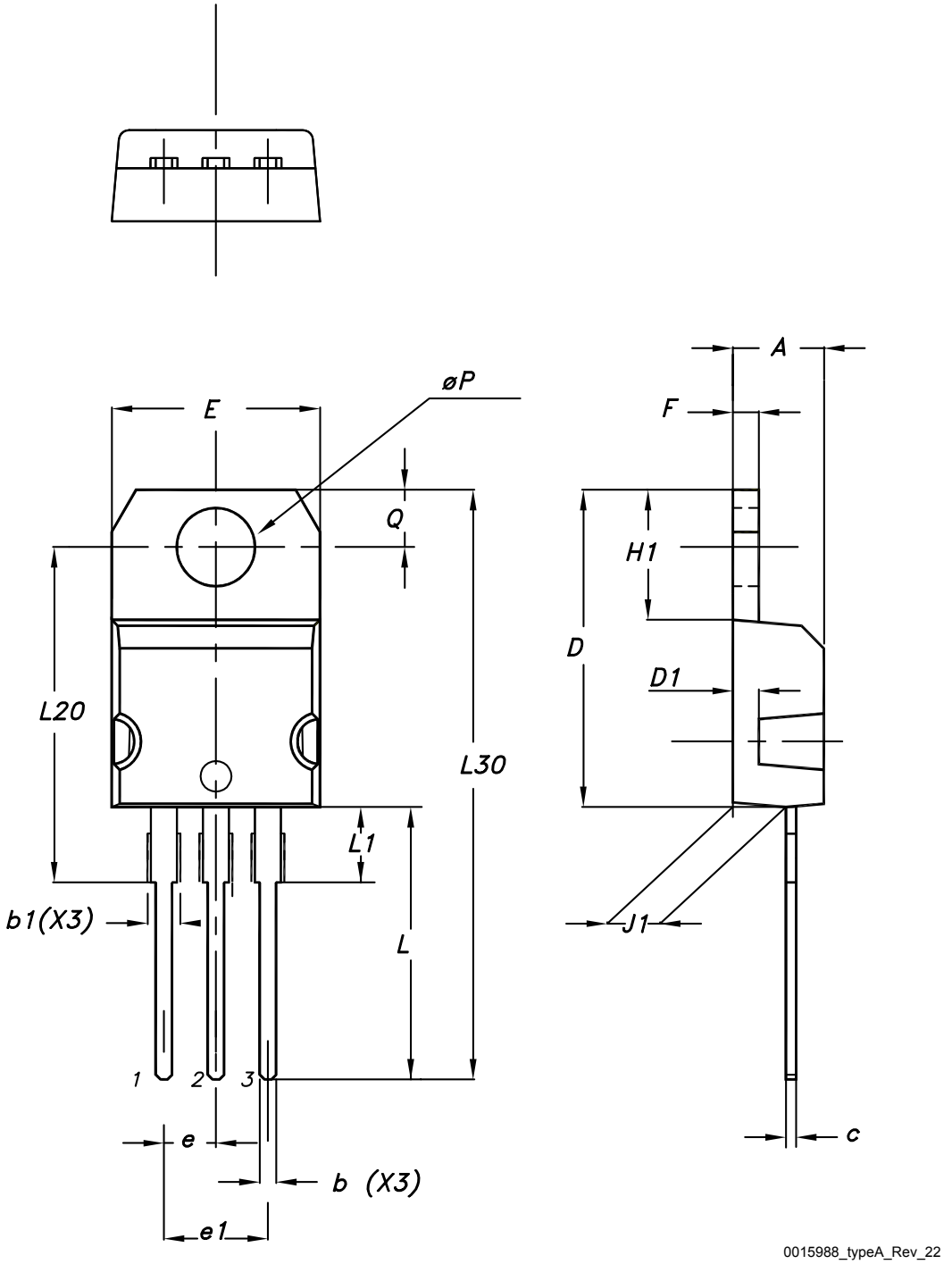


Table 11. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.5 TO-220 type A package information

Figure 29. **TO-220 type A package outline**



0015988_typeA_Rev_22

Table 12. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.6 IPAK (TO-251) type A package information

Figure 30. **IPAK (TO-251) type A package outline**

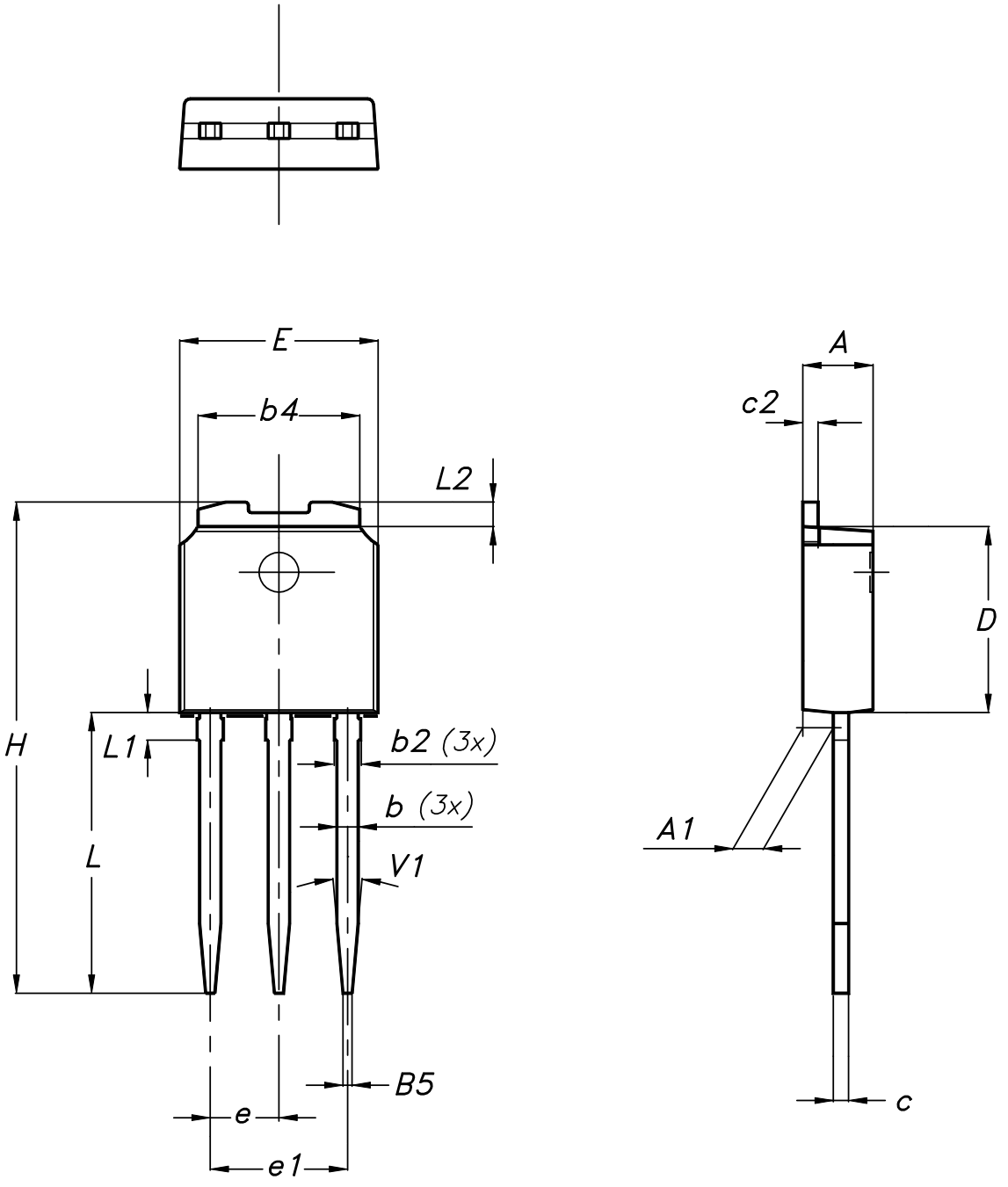
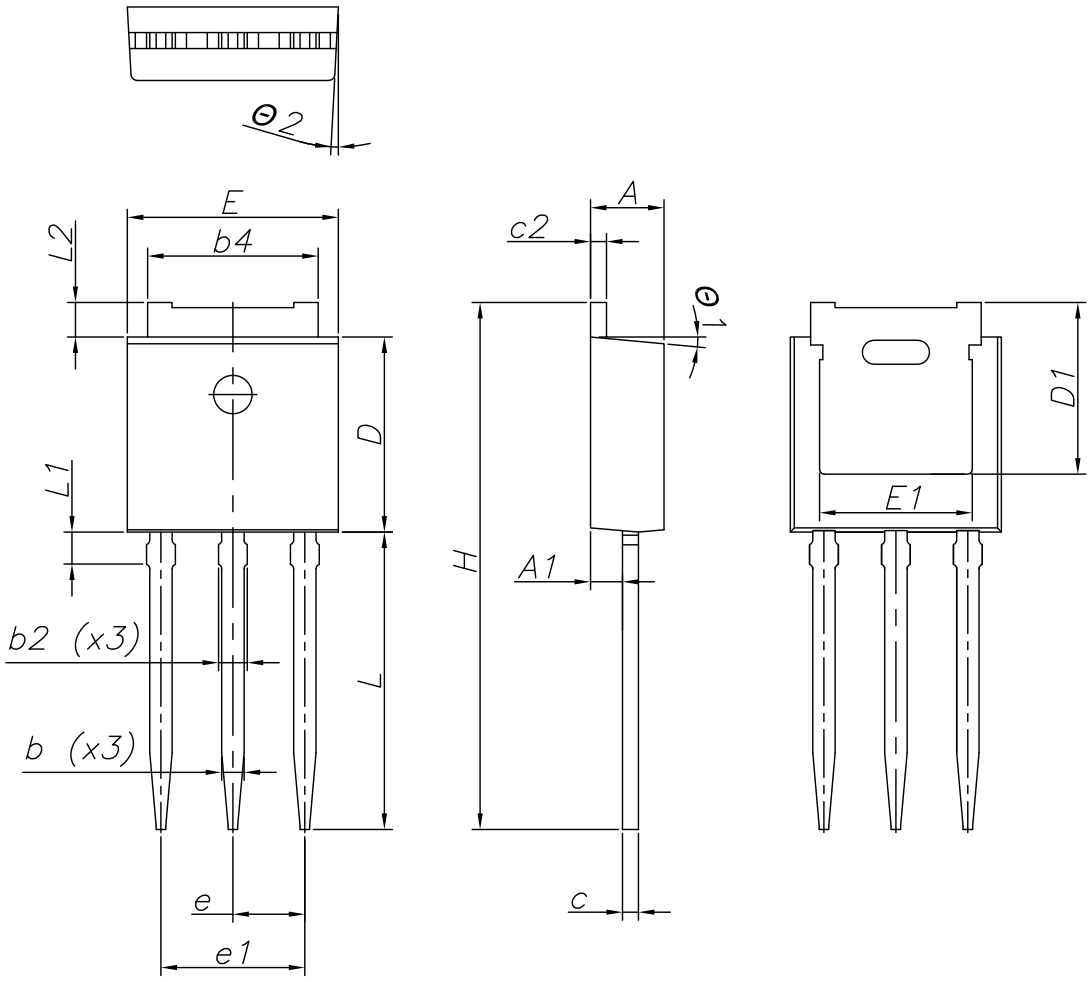


Table 13. **IPAK (TO-251) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.7 IPAK (TO-251) type C package information

Figure 31. **IPAK (TO-251) type C package outline**



0068771_IK_typeC_rev14

Table 14. **IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Ordering information

Table 15. **Order codes**

Order code	Marking	Package	Packing
STD9N65M2	9N65M2	DPAK	Tape and reel
STF9N65M2		TO-220FP	Tube
STP9N65M2		TO-220	
STU9N65M2		IPAK	

Revision history

Table 16. **Document revision history**

Date	Version	Changes
24-Feb-2014	1	First release.
15-Jul-2014	2	– Modified: title, *Features* and *Description* – Modified: *Figure 5* and *15* – Updated: *Figure 28* and *Table 12* – Minor text changes.
19-Jun-2019	3	Removed maturity status indication from cover page. The document status is production data. Updated Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 2.1 Electrical characteristics (curves) Minor text changes.

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