TLE4275-Q1 5-V Low-Dropout Voltage Regulator

1 Features

- Qualified for Automotive Applications
- Output Voltage 5 V ± 2%
- Very Low Current Consumption
- Power-On and Undervoltage Reset
- Reset Low-Level Output Voltage < 1 V
- Very Low Dropout Voltage
- Short-Circuit Proof
- Reverse-Polarity Proof

2 Applications

- Qualified for Automotive Applications
- Cluster
- Body Control Modules
- Heating Ventilation and Air Conditioning (HVAC)

3 Description

The TLE4275-Q1 is a monolithic integrated low-dropout voltage regulator offered in a 5-pin TO package. The device regulates an input voltage up to 45 V to V_{OUT} = 5 V (typical). The device can drive loads up to 450 mA and is short-circuit proof. At overtemperature, the incorporated temperature protection turns off the TLE4275-Q1. The device generates a reset signal for an output voltage, $V_{OUT,rt}$, of 4.65 V (typical). By the use of an external delay capacitor, one can program the reset delay time.

The input capacitor, C_{IN}, compensates for line fluctuation. Using a resistor of approximately 1 Ω in series with C_{IN} dampens the oscillation of input inductance and input capacitance. The output capacitor, C_{OUT}, stabilizes the regulation circuit. The specification for stability is at C_{OUT} ≥ 22 µF and ESR ≤ 5 Ω, within the operating temperature range. Stability for electrolytic capacitors specifically is at C_{OUT} ≥ 68 µF within the operating temperature range. See the application report on low-temperature stability, SLVA501, for further details.

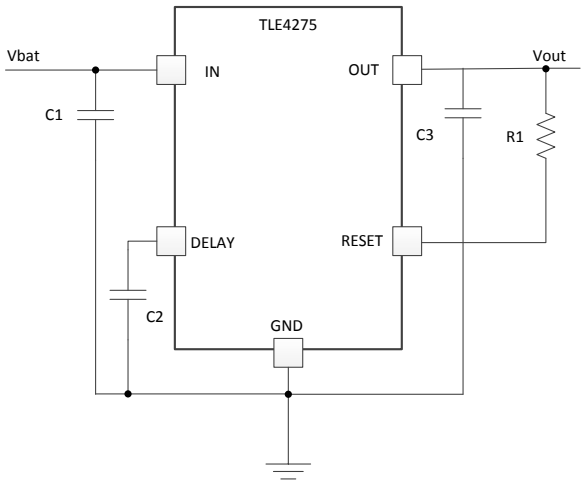
The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor through a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The device also incorporates a number of internal circuits for protection against: *overload*, *overtemperature*, and *reverse polarity*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLE4275-Q1	DDPAK/TO-263 (5)	10.16 mm × 8.42 mm
	TO-252 (5)	6.10 mm × 6.60 mm
	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application



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5 Revision History

Changes from Revision H (March 2013) to Revision I **Page**

- Added *Applications, Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed KTT values in *Thermal Information* table ... 4

Changes from Revision G (January 2013) to Revision H **Page**

- Deleted row for θ_{JA} from *Absolute Maximum Ratings* table ... 4

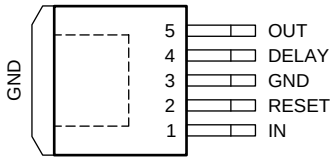
Changes from Revision F (May 2011) to Revision G **Page**

- Updated *Pin Functions* table with PWP package pin information. ... 3

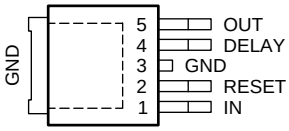
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6 Pin Configuration and Functions

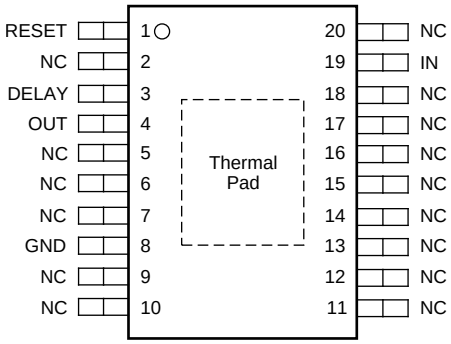
KTT Package
5-Pin DDPAK/TO-263
Top View



KVU Package
5-Pin TO-252
Top View



PWP Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	NO.				
	KTT	KVU	PWP		
DELAY	4	4	3	O	Reset delay. Connect to ground with a capacitor to set delay time.
GND	3	3	8	O	Ground. Internally connected to heatsink
IN	1	1	19	I	Input. Connect to ground as close to device as possible, through a ceramic capacitor.
NC	—	—	2, 5–7, 9–18, 20	—	Not connected
OUT	5	5	4	O	Output. Connect to ground with ≥ 22-µF capacitor, ESR < 5 Ω at 10 kHz.
RESET	2	2	1	I	Reset output. Open-collector output

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range(2)	IN	–42	45	V
		DELAY	–0.3	7	
V_O	Output voltage range	OUT	–1	16	V
		RESET	–0.3	25	
I_I	Input current	DELAY		±2	mA
I_O	Output current	RESET		±5	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	6000	V
		Machine model (MM)(2)	400	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) MM ESD rating tested per JESD22-A115.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage	5.5	42	V
T_J	Junction temperature	–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLE4275-Q1			UNIT
		KTT	KVU	PWP	
		5 PINS	5 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.8	40.3	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.0	31.8	22.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	17.2	19.1	
ψ_{JT}	Junction-to-top characterization parameter	6.3	2.8	0.6	
ψ_{JB}	Junction-to-board characterization parameter	5.4	17.1	18.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	0.7	1.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953) .

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7.5 Electrical Characteristics

over recommended operating free-air temperature range, V_I = 13.5 V, T_J = −40°C to 150°C (unless otherwise noted) (see Figure 18)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	I_O = 5 mA to 400 mA, V_I = 6 V to 28 V		4.9	5	5.1	V
		I_O = 5 mA to 200 mA, V_I = 6 V to 40 V		4.9	5	5.1	
I_O	Output current limit			450	700	950	mA
I_q	Current consumption, $I_q = I_I - I_O$	I_O = 1 mA	T_J = 25°C		150	200	µA
			$T_J \le$ 85°C		150	220	
		I_O = 250 mA			5	10	mA
		I_O = 400 mA			12	22	
V_{DO}	Dropout voltage(1)	I_O = 300 mA, $V_{do} = V_I - V_O$			250	500	mV
	Load regulation	I_O = 5 mA to 400 mA			15	30	mV
	Line regulation	ΔV_I = 8 V to 32 V, I_O = 5 mA		–15	5	15	mV
PSRR	Power-supply ripple rejection	f_r = 100 Hz, V_r = 0.5 V_{pp}			60		dB
$\frac{\Delta V_O}{\Delta T}$	Temperature output-voltage drift				0.5		mV/K
$V_{O,rt}$	RESET switching threshold			4.5	4.65	4.8	V
V_{ROL}	RESET output low voltage	$R_{ext} \ge$ 5 kΩ, V_O > 1 V			0.2	0.4	V
I_{ROH}	RESET output leakage current	V_{ROH} = 5 V			0	10	µA
$I_{D,c}$	RESET charging current	V_D = 1 V		3	5.5	9	µA
V_{DU}	RESET upper timing threshold			1.5	1.8	2.2	V
V_{DRL}	RESET lower timing threshold			0.2	0.4	0.7	V

(1) Measured when the output voltage V_O has dropped 100 mV from the nominal value obtained at V_I = 13.5 V

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rd}	RESET delay time	C_D = 47 nF	10	16	22	ms
t_{rr}	RESET reaction time	C_D = 47 nF		0.5	2	µs

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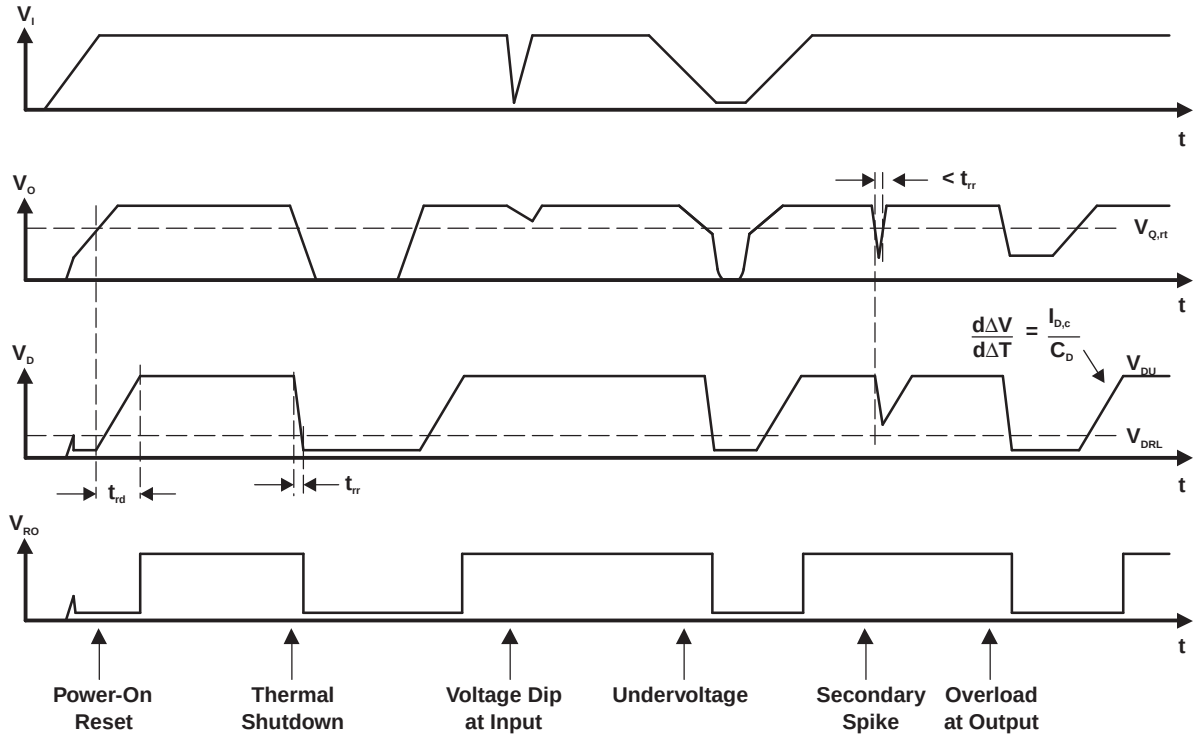
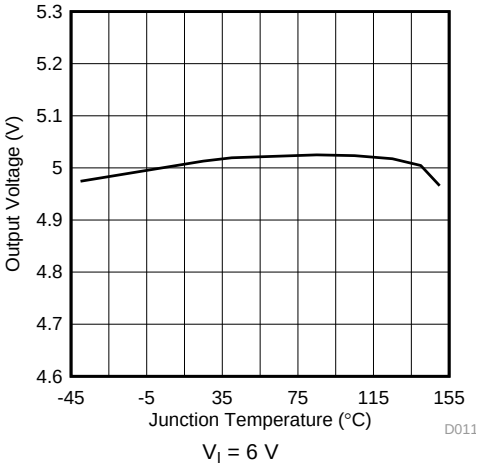


Figure 1. Reset Timing Diagram

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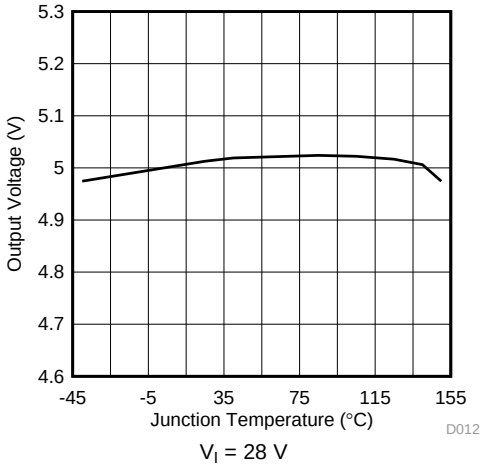
7.7 Typical Characteristics

At T_A = 25ºC



V_I = 6 V

Figure 2. Output Voltage vs Junction Temperature



V_I = 28 V

Figure 3. Output Voltage vs Junction Temperature

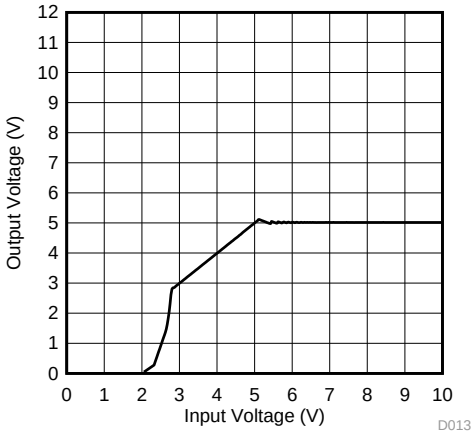


Figure 4. Output Voltage vs Input Voltage

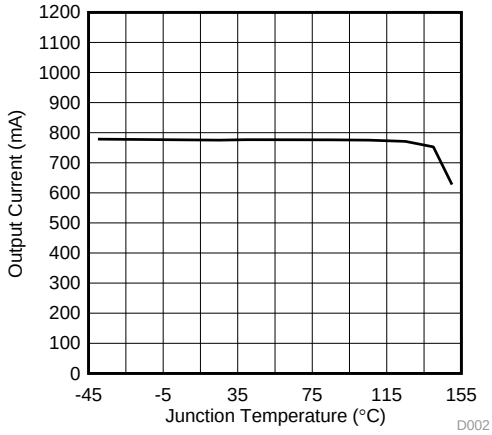
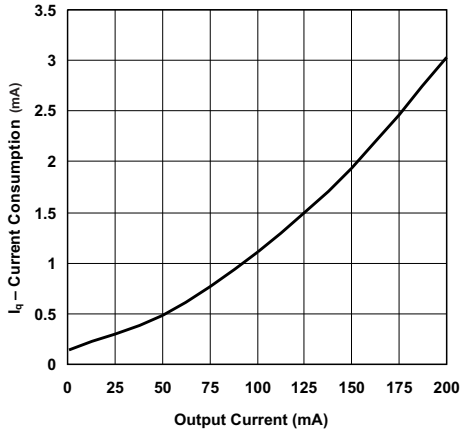
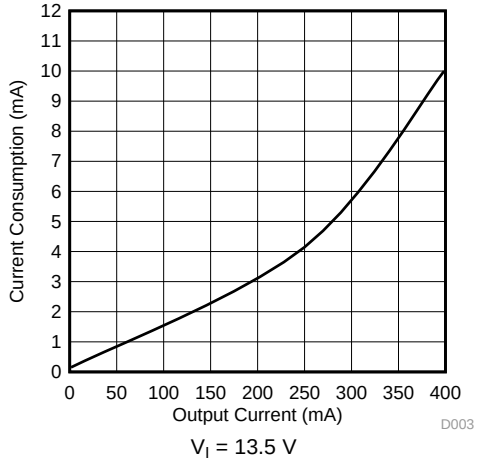


Figure 5. Output Current vs Junction Temperature



V_I = 13.5 V

Figure 6. Current Consumption vs Output Current



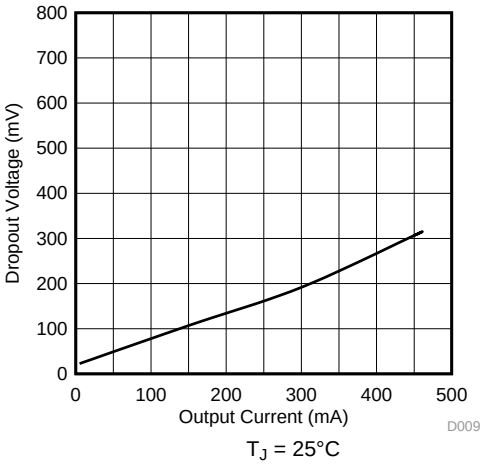
V_I = 13.5 V

Figure 7. Current Consumption vs Output Current

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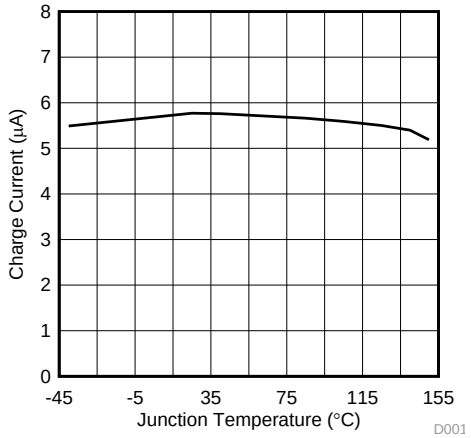
Typical Characteristics (continued)

At T_A = 25ºC



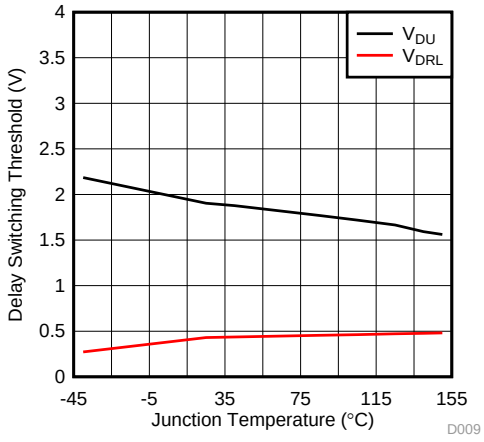
T_J = 25°C

Figure 8. Dropout Voltage (V_{do}) vs Output Current



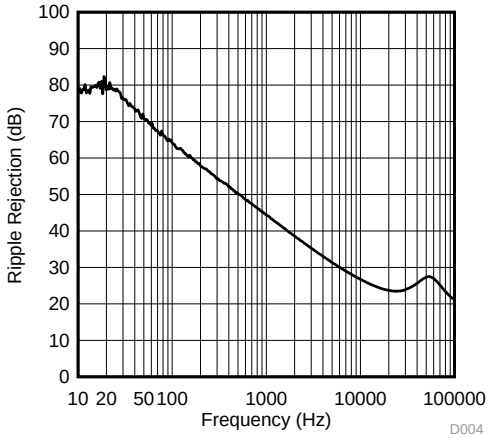
V_I = 13.5 V V_D = 1 V

Figure 9. Charge Current ($I_{D,C}$) vs Junction Temperature



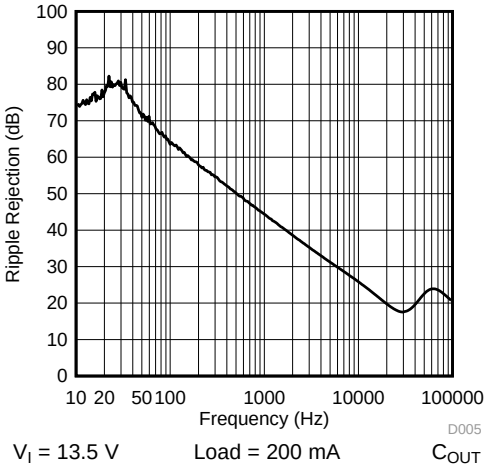
V_I = 13.5 V

Figure 10. Delay Switching Threshold vs Junction Temperature



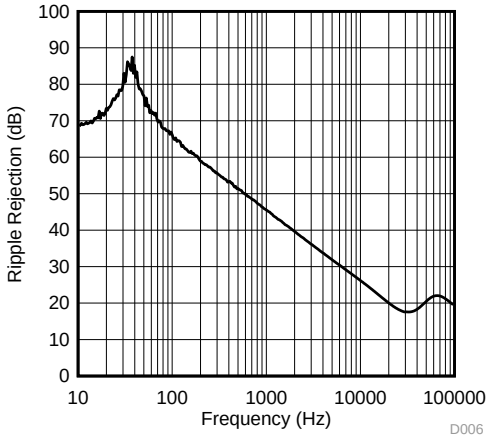
V_I = 13.5 V Load = 1 mA C_{OUT} = 22 µF

Figure 11. Power-Supply Ripple Rejection vs Frequency



V_I = 13.5 V Load = 200 mA C_{OUT} = 22 µF

Figure 12. Power-Supply Ripple Rejection vs Frequency



V_I = 13.5 V Load = 400 mA C_{OUT} = 22 µF

Figure 13. Power-Supply Ripple Rejection vs Frequency

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Typical Characteristics (continued)

At T_A = 25ºC

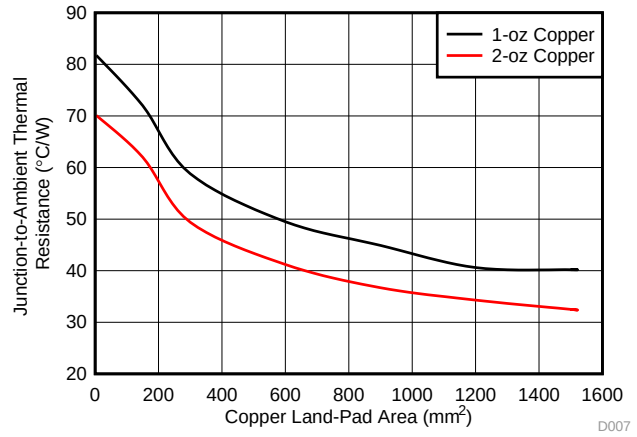


Figure 14. Thermal Resistance vs Copper Land Pad Area (JEDEC 51-3 Low-K Board)

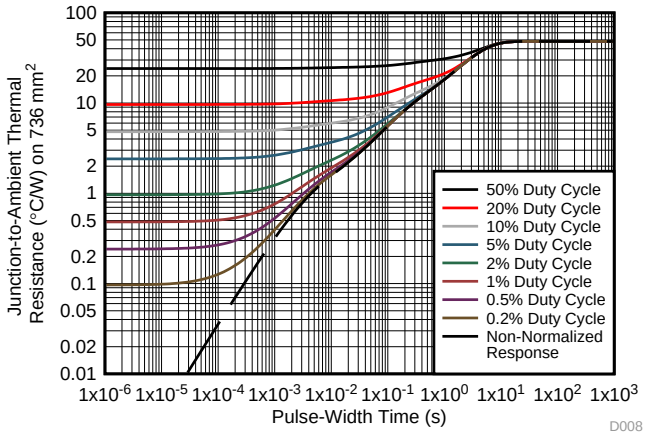


Figure 15. Thermal Resistance vs Pulse Width Time for Various Duty Cycles

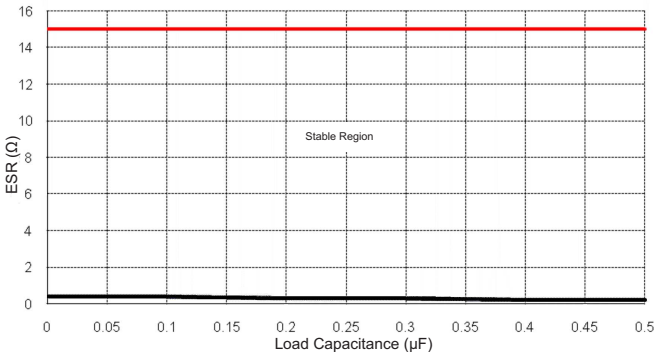


Figure 16. ESR Stability vs Load Current

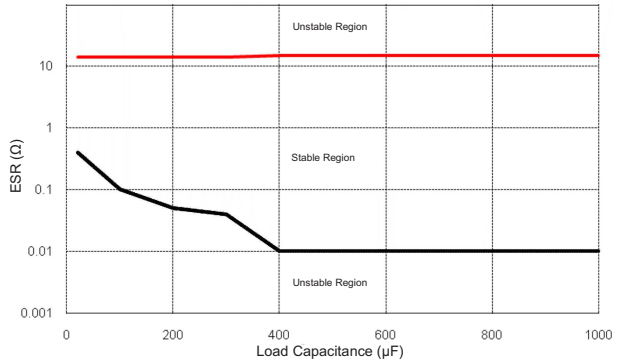


Figure 17. ESR Stability vs Load Capacitance

8 Parameter Measurement Information

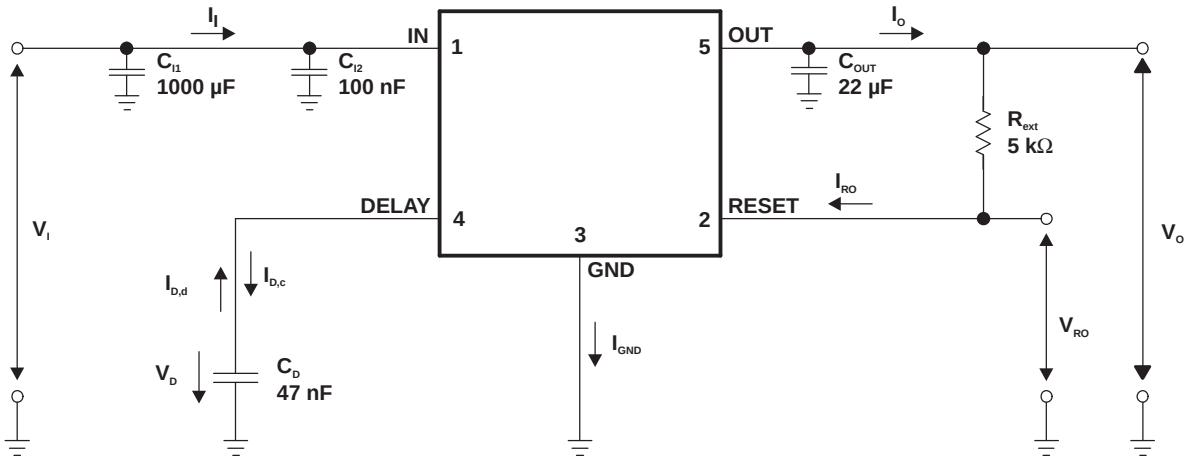


Figure 18. Test Circuit

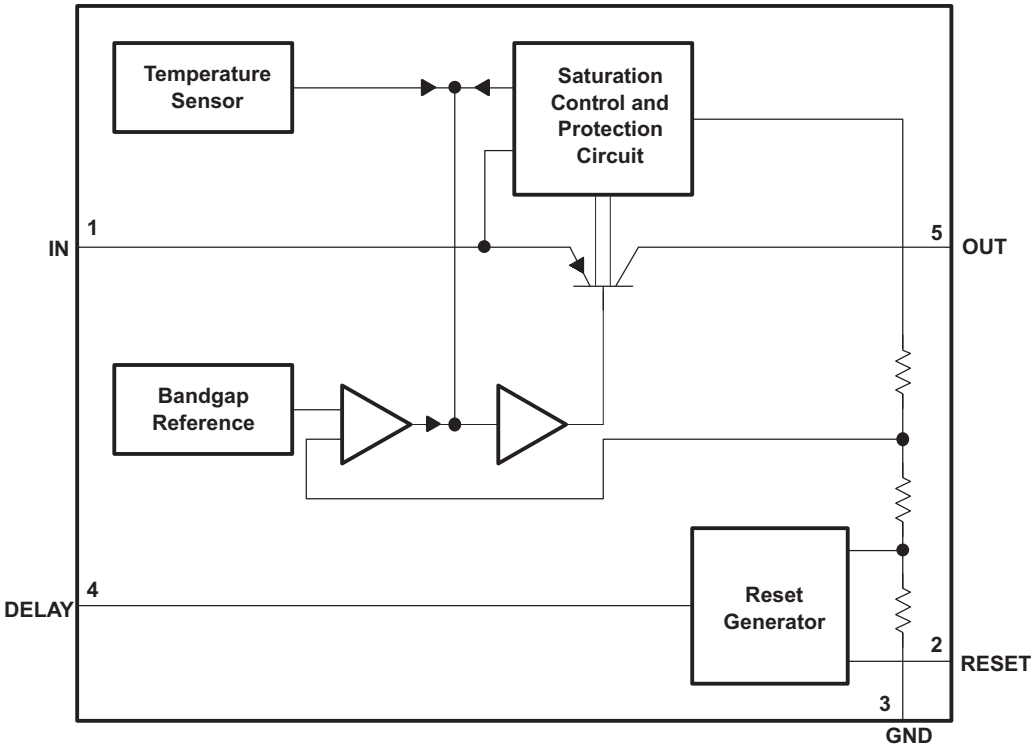
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9 Detailed Description

9.1 Overview

The TLE4275-Q1 device is a monolithic integrated low-dropout voltage regulator offered in a 5-pin TO package. The device regulates an input voltage up to 45 V to V_{OUT} = 5 V (typical). The device can drive loads up to 450 mA and is short circuit proof. At over temperature, the incorporated temperature protection turns off the TLE4275-Q1 device. The device generates a reset signal for an output voltage, $V_{OUT,rt}$, of 4.65 V (typical). By the use of an external delay capacitor, one can program the reset delay time.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Regulated Output (OUT)

The OUT terminal is the regulated 5-V output. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current.

9.3.2 Power-On-Reset (RESET)

The power-on-reset is an output with an external pull up resistor to the regulated supply. The reset output remains low until the regulated V_O exceeds approximately 4.65 V and the power-on-reset delay has expired.

9.3.3 Reset Delay Timer (DELAY)

An external capacitor on this terminal sets the timer delay before the reset terminal is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. The reset pulse delay time t_d, is defined with the charge time of an external capacitor DELAY.

$$t_d = \frac{C_{delay} \times V_{DU}}{I_{D,c}} \quad (1)$$

9.4 Device Functional Modes

9.4.1 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_O) and switch resistance ($R_{(SW)}$). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Figure 19 shows typical application circuits for the TLE4275-Q1. Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps in order to prevent a reset from occurring. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

10.2 Typical Application

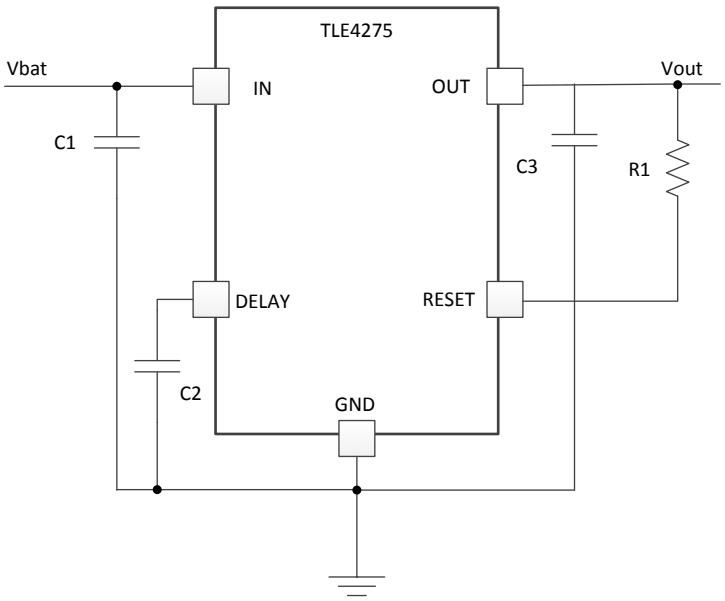


Figure 19. Typical Application Diagram

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 to 40 V
Output voltage	5 V
Output current rating	400 mA
Output capacitor range	10 to 500 µF
Output capacitor ESR range	1 mΩ to 20 Ω
DELAY capacitor range	100 pF to 500 nF

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Output capacitor
- Power-up reset delay time

10.2.2.1 Power-Up Reset Capacitance

To calculate the power-up reset capacitance, use Equation 2.

$$t_d = \frac{C_{delay} \times V_{DU}}{I_{D,c}}$$

$$C_{delay} t_d = \frac{t_d \times I_{D,c}}{V_{DU}} = \frac{t_d \times 5.5 \times 10^{-6}}{1.8} \quad (2)$$

10.2.2.2 Thermal Consideration

Calculate the power dissipated by the device according to Equation 3.

$$P_T = I_O \times (V_I - V_O) + V_I \times I_Q$$

where

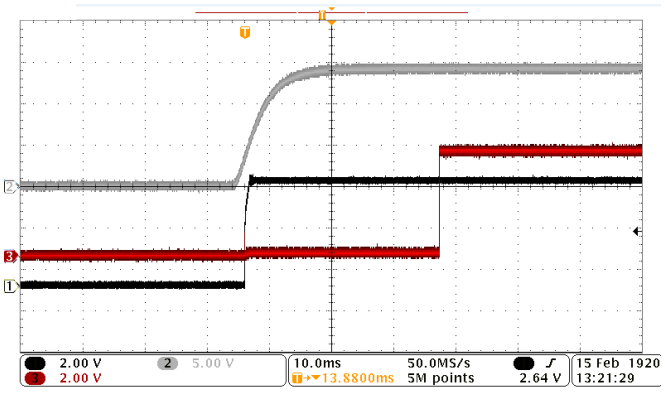
- P_T = Total power dissipation of the device.
- I_O = output current
- V_I = input voltage
- V_O = output voltage (3)

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (4)$$

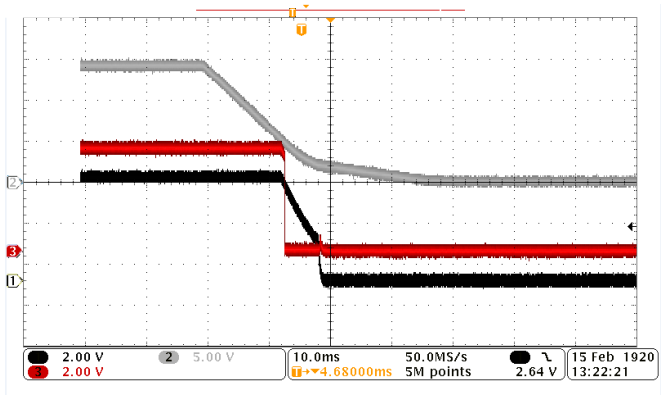
10.2.3 Application Curves

Load = 200 mA, C_{in} = 22 µF, C_{out} = 10 µF



CH1 : V_{out}, CH2: V_{in}, CH3: V_{reset}.

Figure 20. Power Up Waveform



CH1 : V_{out}, CH2: V_{in}, CH3: V_{reset}.

Figure 21. Power Down Waveform

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11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TLE4275-Q1 device, an electrolytic capacitor with a value of 47 µF and a ceramic bypass capacitor are recommended to add at the input.

12 Layout

12.1 Layout Guidelines

- Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.
- Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close to the device as possible and on the same side of the PCB as the regulator.

12.2 Layout Example

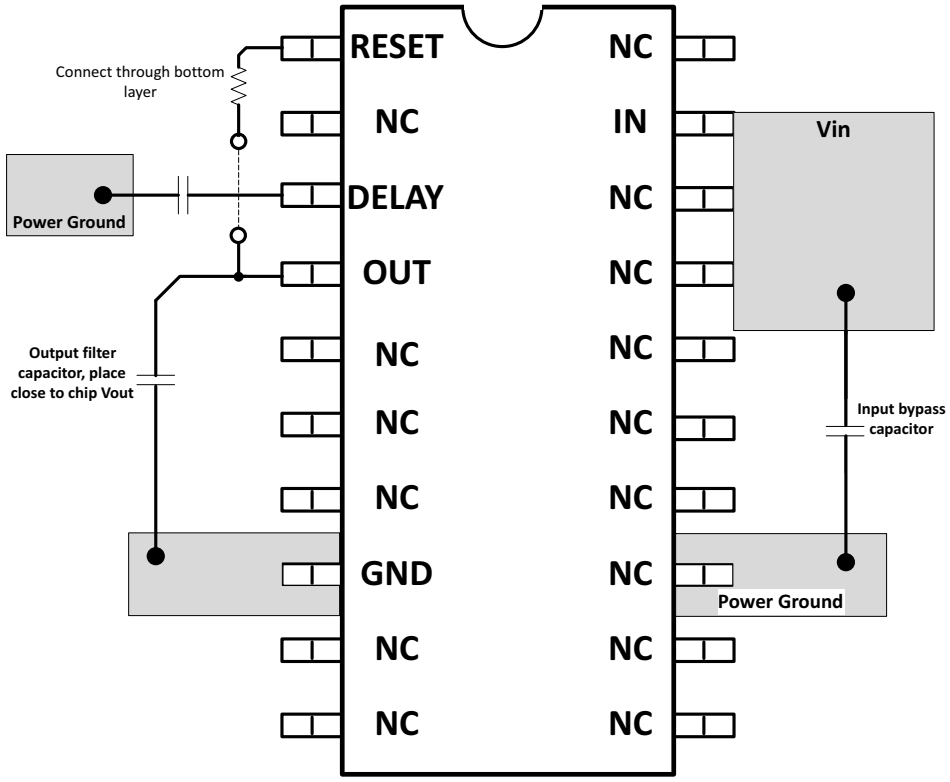


Figure 22. TLE4275-Q1 HTSSOP Layout Design Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

TLE4275-Q1 Low Temperature Stability, SLVA501

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE4275QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	TLE4275Q	Samples
TLE4275QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	TLE4275Q	Samples
TLE4275QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLE4275Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

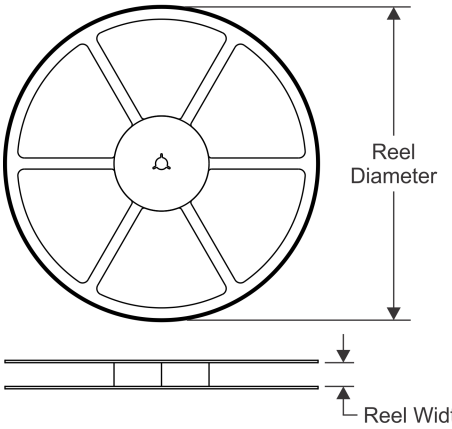
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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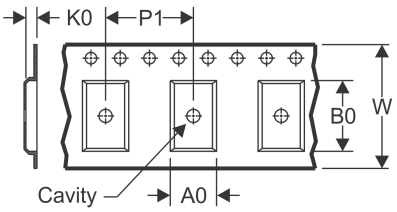
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

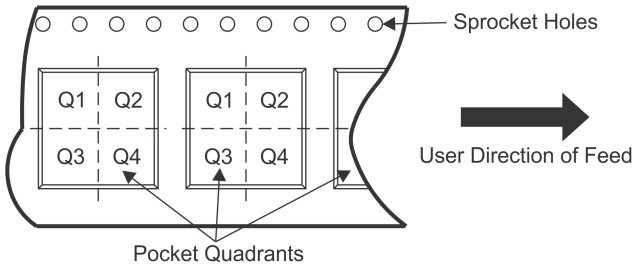


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

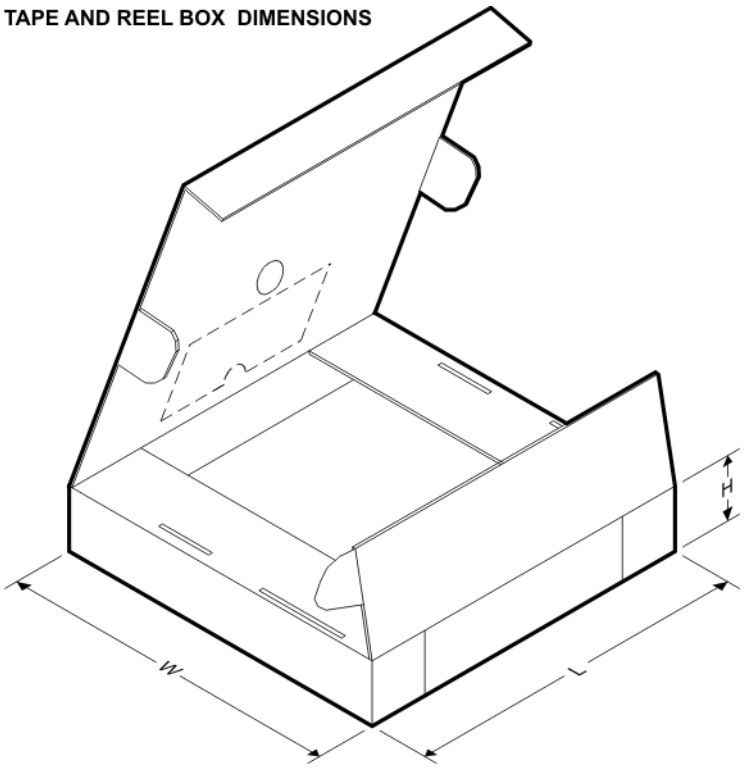
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE4275QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TLE4275QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLE4275QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

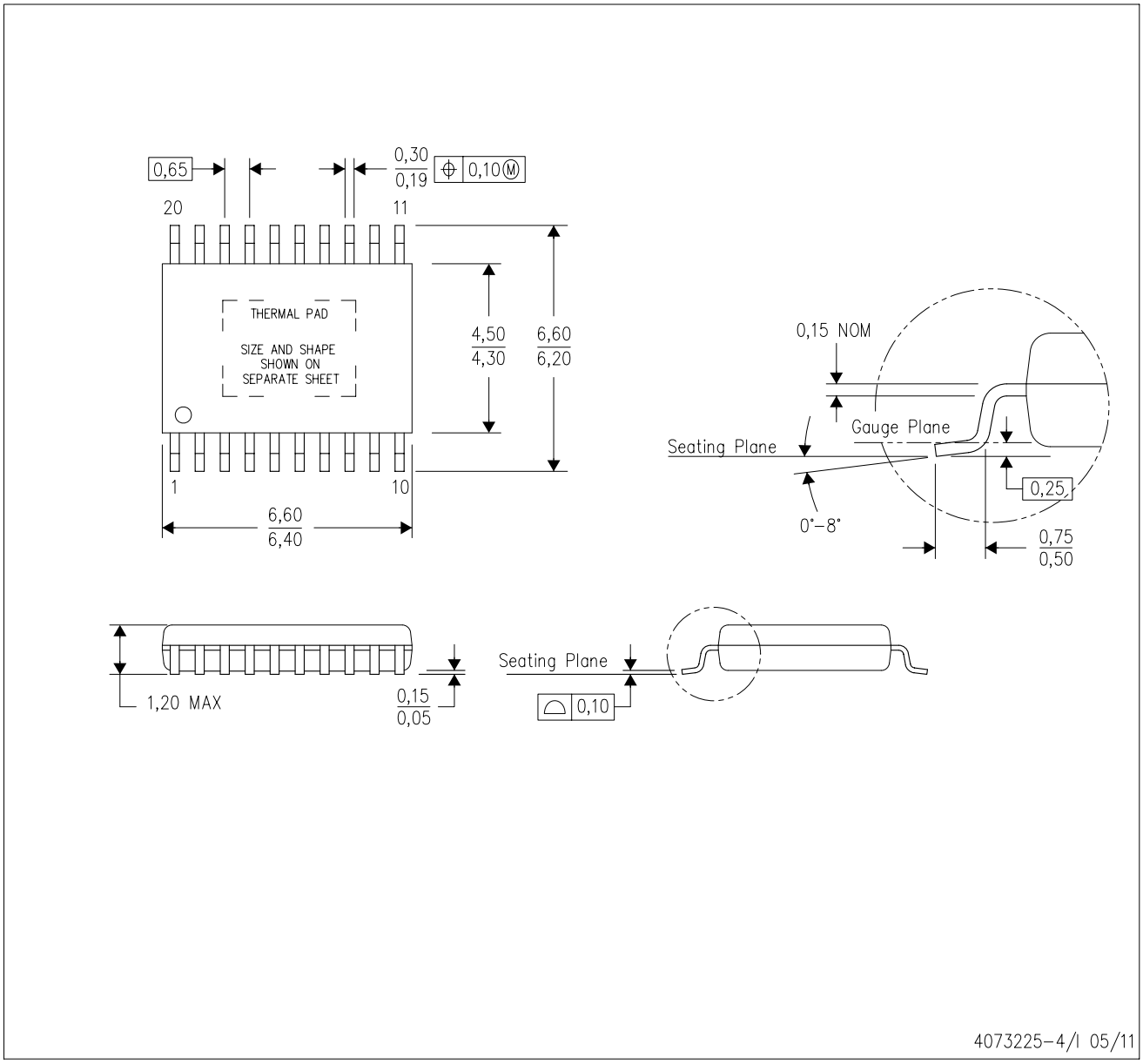
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE4275QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TLE4275QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TLE4275QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

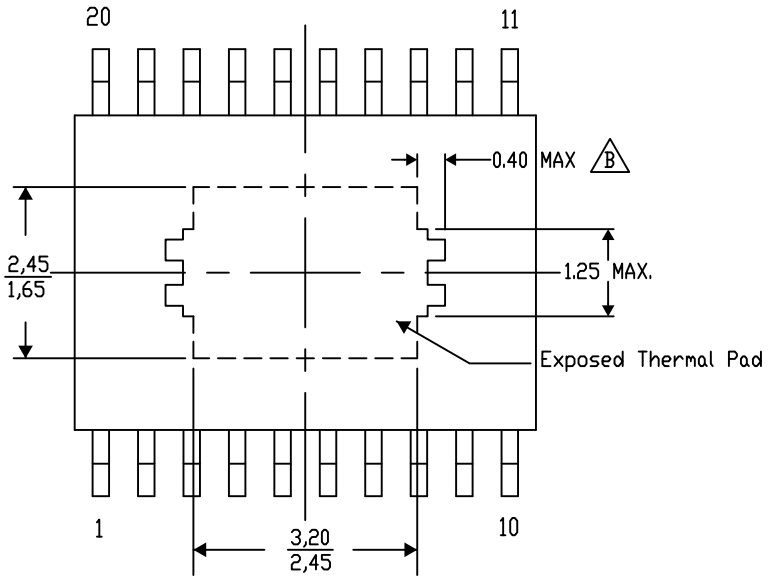
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

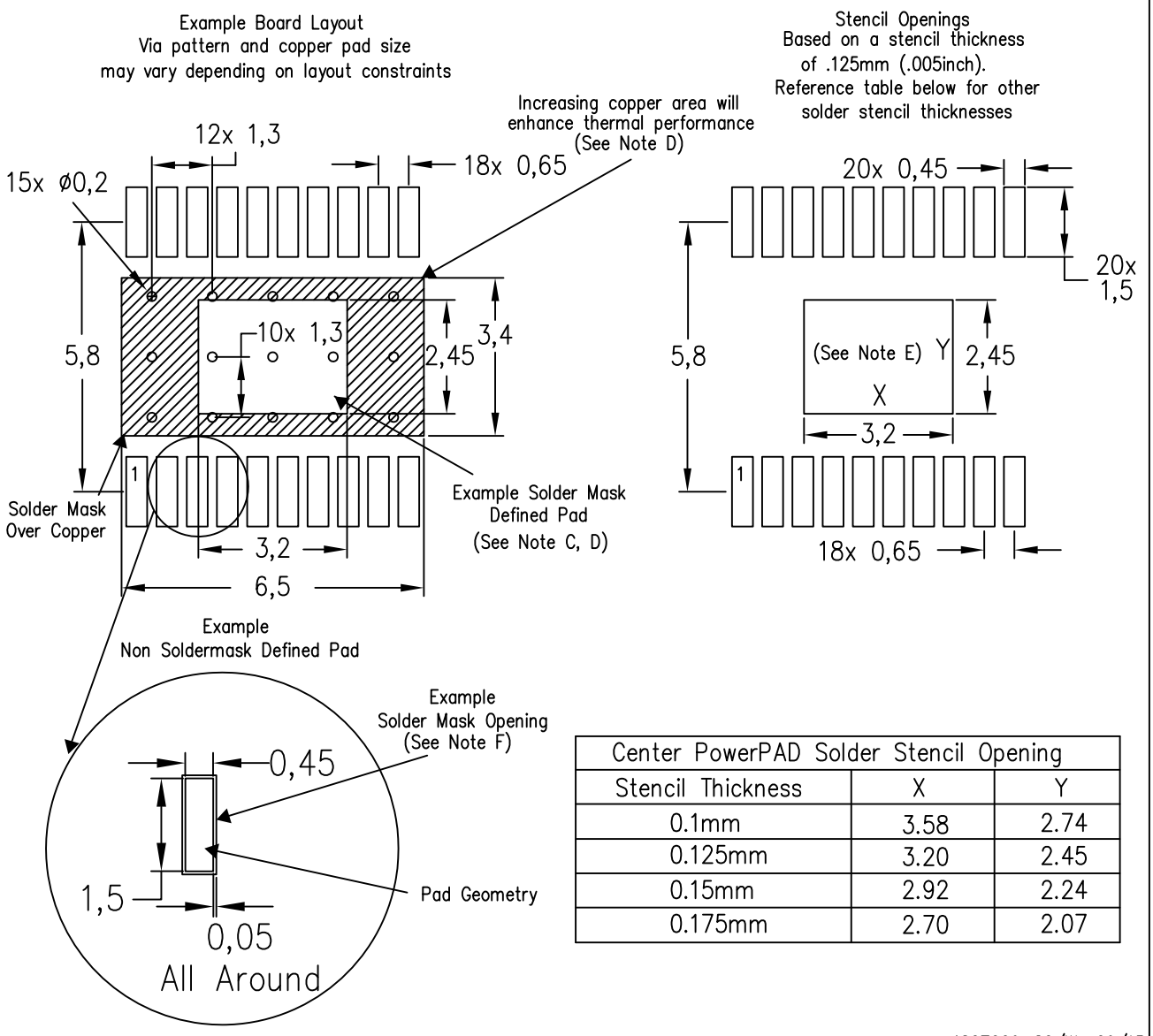
4206332–18/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

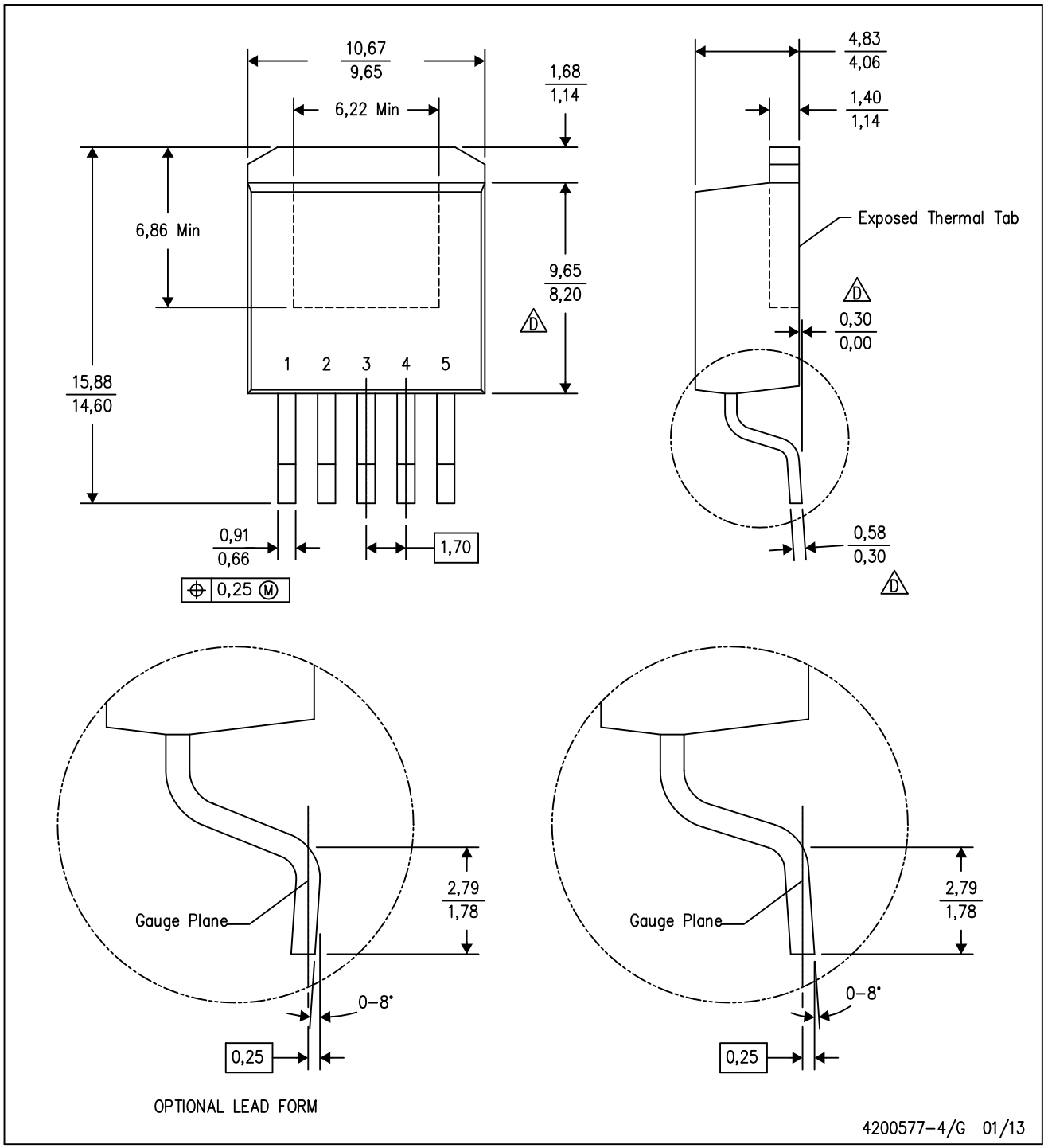


Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.58	2.74
0.125mm	3.20	2.45
0.15mm	2.92	2.24
0.175mm	2.70	2.07

4207609–26/W 09/15

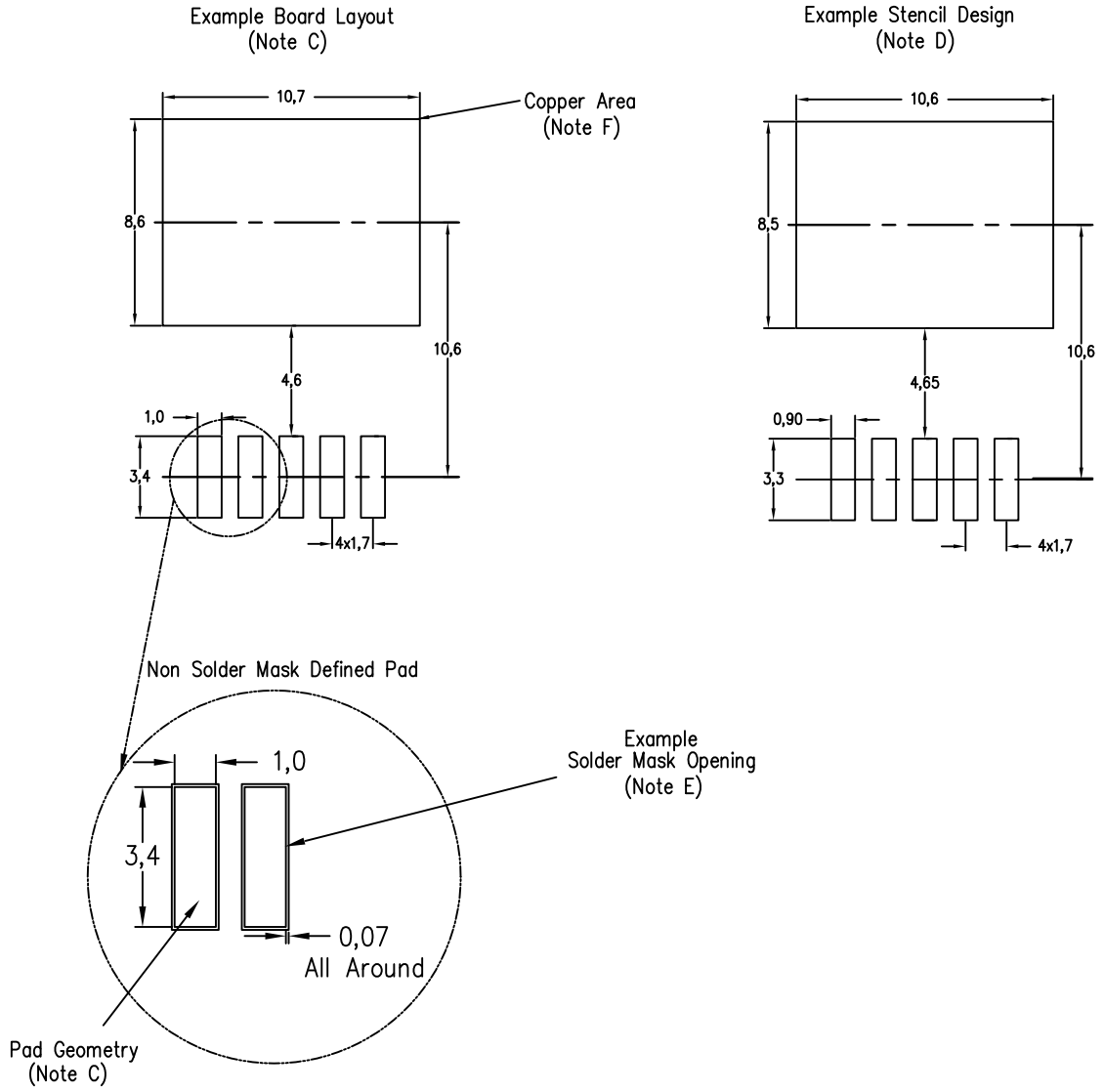
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



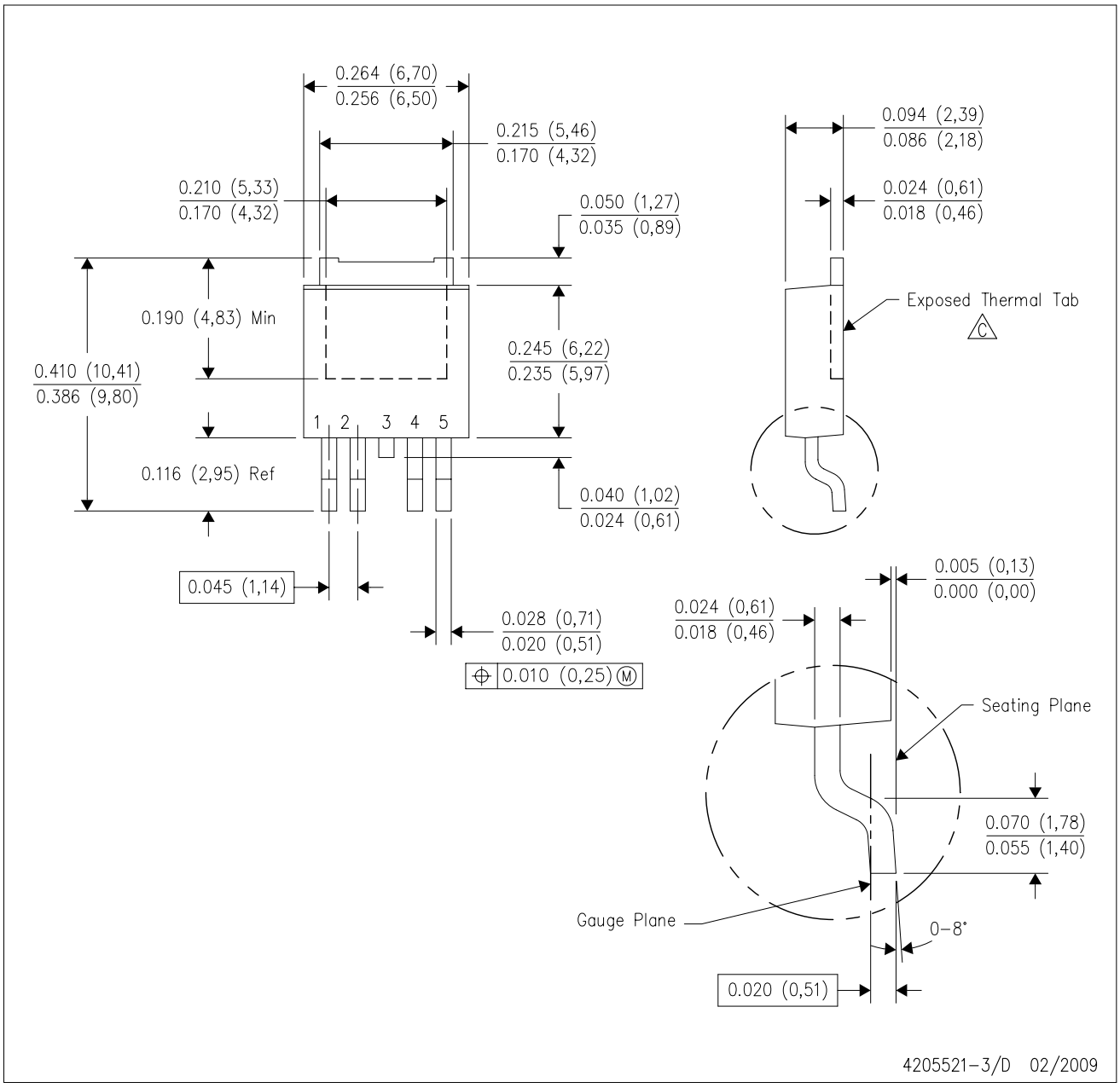
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

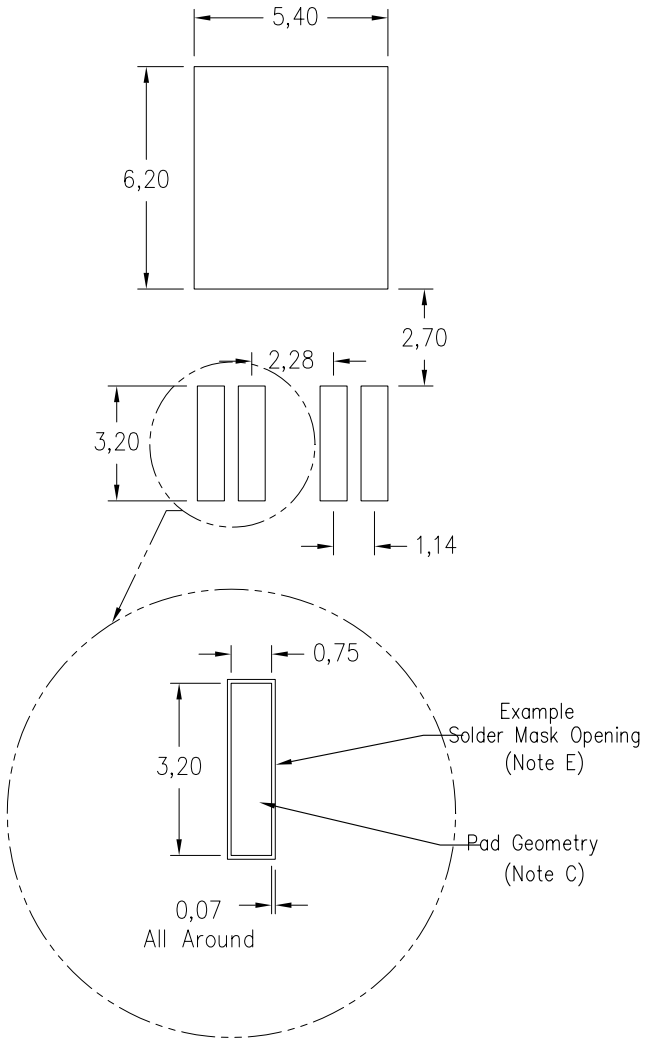
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



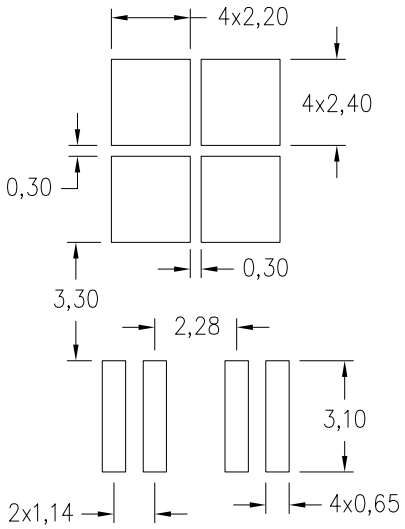
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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