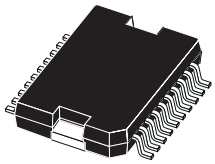
L9949

DOOR ACTUATOR DRIVER

- ONE FULL BRIDGE FOR 6A LOAD (r_{on} = 150mΩ)
- THREE HALF BRIDGES FOR 1.6A LOAD (r_{on} = 800mΩ)
- ONE HIGHSIDE DRIVER FOR 6A LOAD (r_{on} = 100mΩ)
- VERY LOW CURRENT CONSUMPTION IN STANDBY MODE (I_S < 6µA, typ. Tj ≤ 85°C)
- SERIAL PERIPHERAL INTERFACE (SPI) TO MICROCONTROLLER
- ALL OUTPUTS SHORT CIRCUIT PROTECTED
- CURRENT MONITOR OUTPUT FOR FULL BRIDGE AND HIGHSIDE DRIVER
- ALL OUTPUTS OVER TEMPERATURE PROTECTED
- OPEN LOAD DIAGNOSTIC FOR ALL OUTPUTS
- OVERLOAD DIAGNOSTIC FOR ALL OUTPUTS

MULTIPOWER BCD60III TECHNOLOGY



PowerSO20
ORDERING NUMBER: L9949

FULL BRIDGE FOR DOOR LATCH OR MIRROR RETRACT, HALF BRIDGES FOR MIRROR AXIS CONTROL AND HIGH-SIDE DRIVER FOR MIRROR DEFROSTER

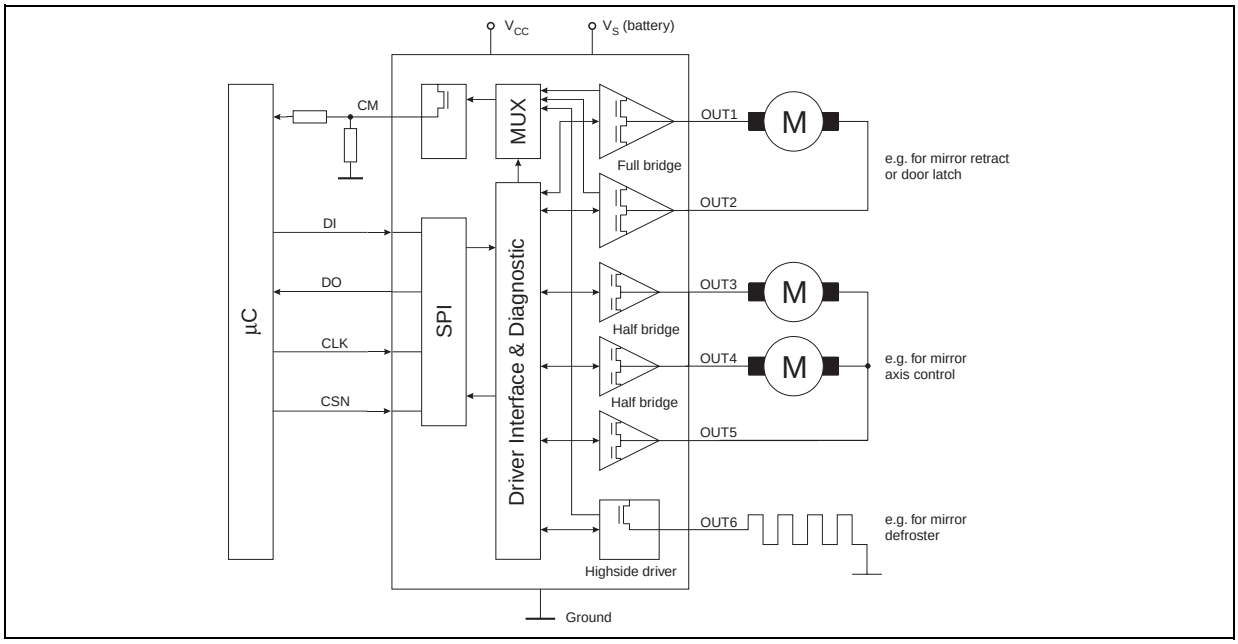
APPLICATIONS

- FOR AUTOMOTIVE APPLICATIONS, E.G.

DESCRIPTION

The L9949 is a microprocessor controlled power interface for automotive applications. It is realized in multipower BCD60III technology. Up to three DC mo-

BLOCK DIAGRAM



DESCRIPTION (continued)

tors and one grounded resistive load can be driven with its three half bridges, one full bridge and one highside driver power outputs. The integrated standard serial peripheral interface (SPI) controls all operation modes (forward, reverse, brake and high impedance). All diagnostic informations are available via the SPI.

Dual Power Supply: V_S and V_{CC}

The power supply voltage V_S supplies the full bridge, the half bridges and the highside driver. An internal charge-pump are used to drive the highside switches. The logic supply voltage V_{CC} (stabilized 5V) is used for the logic part and the SPI of the device. Due to the independent logic supply voltage the control and status information will not be lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on (V_{CC} increases from undervoltage to $V_{VCC\ OFF}$ = 4.2V) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{VCC\ ON}$ = 3.4V), the outputs are switched to tristate (high impedance) and the status registers are cleared.

Standby-Mode

The standby mode of the L9949 is activated by setting the bits 12 and 13 of the Input Data Register to zero. All latched data will be cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at V_S (V_{CC}) is less than typ. 6µA (40µA) for CSN = high (DO in tristate). By switching the V_{CC} voltage a very low quiescent current can be achieved. If one of the bits 12 and 13 are set to high, the device will be switched to active mode.

Inductive Loads

Each half bridge is built by internally connected highside and a lowside power DMOS transistor. Due to the built-in reverse diodes of the output transistors inductive loads can be driven at the outputs OUT1 to OUT5 without external free-wheeling diodes. The highside driver OUT6 is intended to drive resistive loads only hence only a limited energie (E<1mJ) can be dissipated by the internal ESD-diode in freewheeling condition. For inductive loads (L>100µH) an external free-wheeling diode connected to GND and OUT6 is needed.

Diagnostic Functions

All diagnostic functions (over/open load, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered and the condition has to be valid for at least 10µs (0.5ms, respectively) before the corresponding status bit in the status registers will be set. The filters are used to improve the noise immunity of the device. The open load and temperature warning function are intended for information purpose and will not change the state of the output drivers. In contrast, the overload and thermal shutdown condition will disable the corresponding driver (overload) or all drivers (thermal shutdown), respectively. The microcontroller has to clear the status bits to reactivate the corresponding drivers. This is to avoid an uncontrolled switching behaviour of the device which may result in a heavy noise on the GND and V_S lines in case of an fault condition (e.g. short to GND or V_S).

Overvoltage and Undervoltage Detection

If the power supply voltage V_S rises above the overvoltage threshold $V_{SOV\ OFF}$ (max. 22V), the outputs OUT1 to OUT6 are switched to high impedance state to protect the load. If the supply voltage recovers to normal operating voltage, the device will return to the programmed state (lockout bit 14 = 0). When the voltage V_S drops below the undervoltage threshold $V_{SUV\ OFF}$ (min. 6V), the output stages are switched to high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage V_S and the internal charge-pump recovers to normal operating voltage the system returns to the programmed state (lockout bit 14 = 0). If the lockout bit 14 is set, the automatic turn-on of the drivers is deactivated. The microcontroller needs to clear the status bits to reactivate the drivers.

Temperature Warning and Thermal Shutdown

When the junction temperature rises above $T_{j\,TW}$ a temperature warning flag is set and is available via the SPI. If the junction temperature increases above the second threshold $T_{j\,SD}$, the thermal shutdown bit will be set and the power DMOS transistors of the output stages are switched off to protect the device. In order to reactivate the output stages the junction temperature must decrease below $T_{j\,SD}$ - $T_{j\,SD\,HYS}$ and the thermal shutdown bit has to be cleared by the microcontroller.

Open Load Detection

The open load detection monitors the voltage drop of current sense resistors in each highside and lowside driver of the output stage. The output signal of an open load comparator has to be valid for at least 0.5 ms (t_{dOL}) to set the open load bit (bit 1-11) in the status register 1.

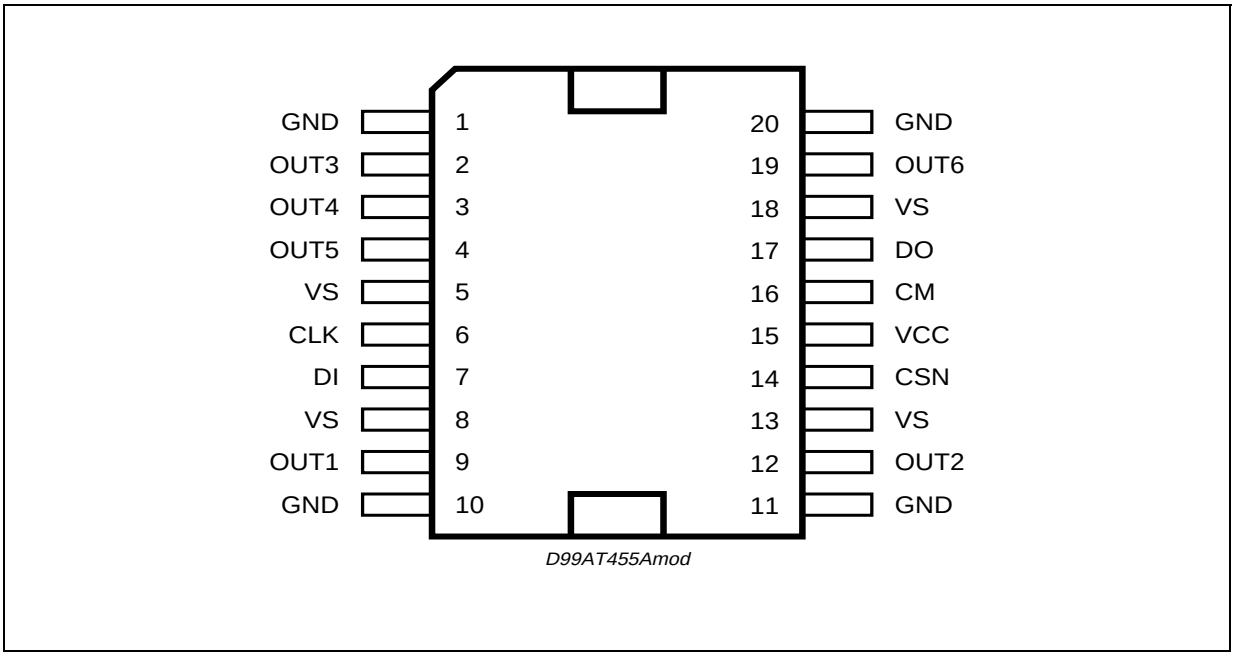
Over Load Detection

In the case of an overcurrent condition an overcurrent flag (bit 1-11) is set in the status register 0 in the same way as open load detection. If the overcurrent signal is valid for at least t_{ISC} = 10µs, the overcurrent flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. The microcontroller has to clear the status bits to reactivate the corresponding driver.

Current monitor

The current monitor output sources a current image at the current monitor output which has a fixed ratio (1/ 10000) of the instantaneous current of the selected highside driver. The bits 12 and 13 of the Input Data register controls which of the outputs OUT1, OUT2 and OUT6 will be multiplexed to the current monitor output. The current monitor output allows a more precise analyse of the actual state of the load rather than the detection of an open- or overload condition. For example this can be used to detect the motor state (free-running, loaded or blocked) or the temperature of the heating element.

Figure 1. Pin Connection (Top view)



PIN FUNCTION

N°	Pin	Description
1, 10, 11, 20	GND	**Ground:** Reference potential ***Important**:* For the capability of driving the full current at the outputs all pins of GND must be externally connected !
5, 8, 13, 18	V_S	**Power supply voltage (battery):** For this input a ceramic capacitor as close as possible to GND is recommended. ***Important**:* For the capability of driving the full current at the outputs all pins of V_S must be externally connected !
15	V_{CC}	**Logic supply voltage:** For this input a ceramic capacitors as close as possible to GND are recommended.
14	CSN	**Chip Select Not input:** This input is low active and requires CMOS logic levels. The serial data transfer between L9949 and micro controller is enabled by pulling the input CSN to low level. If an input voltage of more than 9.6V above VCC is applied to CSN pin the L9949 will be switched into a test mode.
6	CLK	**Serial clock input:** This input controls the internal shift register of the SPI and requires CMOS logic levels.
7	Data In	**Serial data input:** The input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 16bit control word and the least significant bit (LSB, bit 0) is transferred first.
17	Data Out	**Serial data output:** The diagnosis data is available via the SPI and this tristate-output. The output will remain in tristate, if the chip is not selected by the input CSN (CSN = high)
16	CM	**Current monitor output:** Depending on the multiplexer bits 12 and 13 of the Input Data register this output sources an image of the instant current through the corresponding highside driver with a ratio of 1/10000
9	OUT1	**Halfbridge-output 1:** The output is built by a highside and a lowside switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode, highside driver from OUT1 to V_S, lowside driver from GND to OUT1). This output is overcurrent and open load protected.
12	OUT2	**Halfbridge-output 2:** $\longrightarrow$ see OUT1 (pin 9)
2	OUT3	**Halfbridge-output 3:** The output is built by a highside and a lowside switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode, highside driver from OUT3 to VS, lowside driver from GND to OUT3). This output is overcurrent and open load protected.
3	OUT4	**Halfbridge-output 4:** $\longrightarrow$ see OUT3 (pin 2)
4	OUT5	**Halfbridge-output 5:** $\longrightarrow$ see OUT3 (pin 2)
19	OUT6	**Highside-driver-output 6:** The output is built by a highside switch and can be used only for a resistive load, because the internal reverse diode from GND to OUT6 is missing. This highside switch is a power DMOS transistor with an internal parasitic reverse diode from OUT6 to V_S (bulk-drain-diode). The output is overcurrent and open load protected.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3...28	V
	single pulse t_{max} < 400 ms	40	V
V_{CC}	stabilized supply voltage, logic supply	-0.3 to 6	V
V_{DI} V_{DO} V_{CLK} , V_{CSN}	digital input / output voltage	-0.3 to V_{CC} + 0.3	V
V_{CM}	current monitor output	-0.3 to V_{CC} + 0.3	V
$I_{OUT1,OUT2,OUT6}$	output current	±10	A
$I_{OUT3,OUT5}$	output current	±5	A

Note: All maximum ratings are absolute ratings. Leaving the limitation of anyone of these values may cause an irreversible damage of the integrated circuit!

ESD PROTECTION

Parameter	Value	
All pins	±2(1)	kV
output pins: OUT1 – OUT6	±4(2)	kV

(1) HBM according to MIL 883C, Methode 3015.7 or EIA/JESD22-A114-A
(2) HBM with all unzapped pins grounded

THERMAL DATA

Symbol	Parameter	Value	Unit

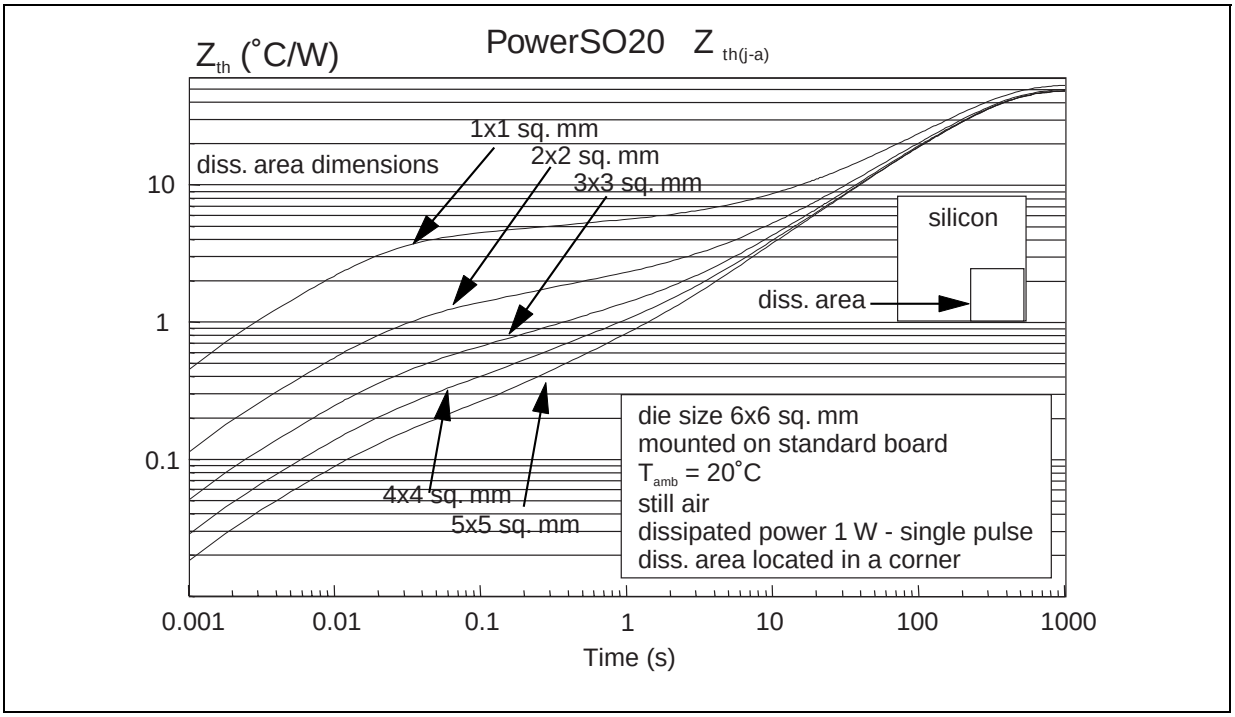
Operating junction temperature:

T_j	Operating Junction Temperature	-40 to 150	°C

Temperature warning and thermal shutdown:

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature Warning Threshold Junction Temperature	T_j increasing			150	°C
$T_{jTW\ OFF}$	Temperature Warning Threshold Junction Temperature	T_j decreasing	120			°C
$T_{jTW\ HYS}$	Temperature Warning Hysteresis			10		K
$T_{jSD\ ON}$	Thermal Shutdown Threshold Junction Temperature	T_j increasing			180	°C
$T_{jSD\ OFF}$	Thermal Shutdown Threshold Junction Temperature	T_j decreasing	150			°C
$T_{jSD\ HYS}$	Thermal Shutdown Hysteresis			10		K

Figure 2. Thermal Data of Package



ELECTRICAL CHARACTERISTCS

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = -40 to 150 °C, unless otherwise specified. The voltages are refered to GND and currents are assumed positive, when the current flows into the pin.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply						
V_S	Operating Supply Voltage Range		7		28	V
I_S	DC Supply Current	active mode, V_S = 16 V, V_{CC} = 5.3 V, OUT1 - OUT6 floating		7	20	mA
	Quiescent Supply Current	standby mode, V_S = 16 V, V_{CC} = 0 V, T_j < 85 °C(1) OUT1 - OUT6 floating		6	12	µA
I_{CC}	DC Supply Current	active mode, CSN = V_{CC}, V_S = 16 V; V_{CC} = 5.3 V		1	2	mA
	Quiescent Supply Current	standby mode, CSN = V_{CC}, V_S = 16V, V_{CC} = 5.3V, T_j < 85 °C(1) OUT1 - OUT6 floating		40	75	µA
$I_S + I_{CC}$	Sum Supply Quiescent Current	standby mode, CSN = V_{CC}, V_S = 16 V, V_{CC} = 5.3 V, T_j < 85 °C OUT1 - OUT6 floating		50	90	µA

ELECTRICAL CHARACTERISTCS (continued)

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = -40 to 150 °C, unless otherwise specified. The voltages are refered to GND and currents are assumed positive, when the current flows into the pin.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit

(1) Parameter is measured at -40°C and 25°C. Value for 85°C is guaranteed by design

Over- and undervoltage detection

$V_{SUV\ ON}$	V_S UV-Threshold Voltage	V_S increasing			7.6	V
$V_{SUV\ OFF}$	V_S UV-Threshold Voltage	V_S decreasing	6			V
$V_{SUV\ hyst}$	V_S UV-hysteresis	$V_{SUV\ ON} - V_{SUV\ OFF}$		0.6		V
$V_{SOV\ OFF}$	V_S OV-threshold voltage	V_S increasing			22	V
$V_{SOV\ ON}$	V_S OV-threshold voltage	V_S decreasing	18			V
$V_{SOV\ hyst}$	V_S OV-hysteresis	$V_{SOV\ OFF} - V_{SOV\ ON}$		1		V
$V_{VCC\ OFF}$	Power-on-reset Threshold	V_{CC} increasing			4.2	V
$V_{VCC\ ON}$	Power-on-reset Threshold	V_{CC} decreasing	3.4		4	V
$V_{VCC\ hyst}$	Power-on-reset Hysteresis	$V_{VCC\ OFF} - V_{VCC\ ON}$		0.3		V

Current Monitor Output

V_{CM}	Functional Voltage Range	V_{CC} = 5 V	0		4	V
$I_{CM,r}$	Current Monitor Output Ratio: I_{CM} / $I_{OUT1,2,6}$	0 V ≤ V_{CM} ≤ 4 V		$\frac{1}{10000}$		-
$I_{CM\ acc}$	Current Monitor Accuracy	0V ≤ VCM ≤ 4V, I_{CM} =50µA, 600 µA (FS=full scale=600µA)		4% + 1%FS	8% + 2%FS	

Outputs: OUT1 - OUT6

$R_{ON\ OUT1}$	On-resistance to Supply or GND	V_S = 13.5 V, T_j = 25 °C, I_{OUT1} = ± 3.0 A			150	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT1} = ± 3.0 A			225	mΩ
		V_S = 8.0 V, T_j = 25 °C, I_{OUT1} = ± 3.0 A			180	mΩ
$R_{ON\ OUT2}$	On-resistance to Supply or GND	V_S = 13.5 V, T_j = 25 °C, I_{OUT2} = ± 3.0 A			150	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT2} = ± 3.0 A			225	mΩ
		V_S = 8.0 V, T_j = 25 °C, I_{OUT2} = ± 3.0 A			180	mΩ

ELECTRICAL CHARACTERISTCS (continued)

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = -40 to 150 °C, unless otherwise specified. The voltages are refered to GND and currents are assumed positive, when the current flows into the pin.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{ON\ OUT3}$	On-resistance to Supply or GND	V_S = 13.5 V, T_j = 25 °C, I_{OUT3} = ± 0.8 A			800	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT3} = ± 0.8 A			1250	mΩ
		V_S = 8.0 V, T_j = 25 °C, I_{OUT3} = ± 0.8 A			980	mΩ
$R_{ON\ OUT4}$	On-resistance to Supply or GND	V_S = 13.5 V, T_j = 25 °C, I_{OUT4} = ± 0.8 A			800	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT4} = ± 0.8 A			1250	mΩ
		V_S = 8.0 V, T_j = 25 °C, I_{OUT4} = ± 0.8 A			980	mΩ
$R_{ON\ OUT5}$	On-resistance to Supply or GND	V_S = 13.5 V, T_j = 25 °C, I_{OUT5} = ± 0.8 A			800	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT5} = ± 0.8 A			1250	mΩ
		V_S = 8.0 V, T_j = 25 °C, I_{OUT5} = ± 0.8 A			980	mΩ
$R_{ON\ OUT6}$	On-resistance to Supply	V_S = 13.5 V, T_j = 25 °C, I_{OUT6} = - 2.5 A			100	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT6} = - 2.5 A			150	mΩ
		V_S = 8.0 V, T_j = 25 °C, I_{OUT6} = - 2.5 A			120	mΩ
$\lvert I_{OUT1}\rvert$	Output Current Limitation to Supply or GND	sink and source, current ramp	6		10	A
$\lvert I_{OUT2}\rvert$	Output Current Limitation to Supply or GND	sink and source, current ramp	6		10	A
$\lvert I_{OUT3}\rvert$	Output Current Limitation to Supply or GND	sink and source, current ramp	1.6		2.5	A
$\lvert I_{OUT4}\rvert$	Output Current Limitation to Supply or GND	sink and source, current ramp	1.6		2.5	A
$\lvert I_{OUT5}\rvert$	output current limitation to Supply or GND	sink and source, current ramp	1.6		2.5	A
$\lvert I_{OUT6}\rvert$	Output Current Limitation to GND	source, current ramp	6.3		11	A
$\lvert I_{OUT6/res}\rvert$	Output Current Limitation to GND switching into resistive load	source, switching into resistive load, go-nogo test	5.1		11	A

For details of the on-resistance (R_{on} over temperature) see the figures „Typical r_{on} characteristics“ for the differential output stages (FIGURE 3, FIGURE 4, FIGURE 5)

Figure 3. TYPICAL R_{ON} CHARACTERISTICS OUT1,2

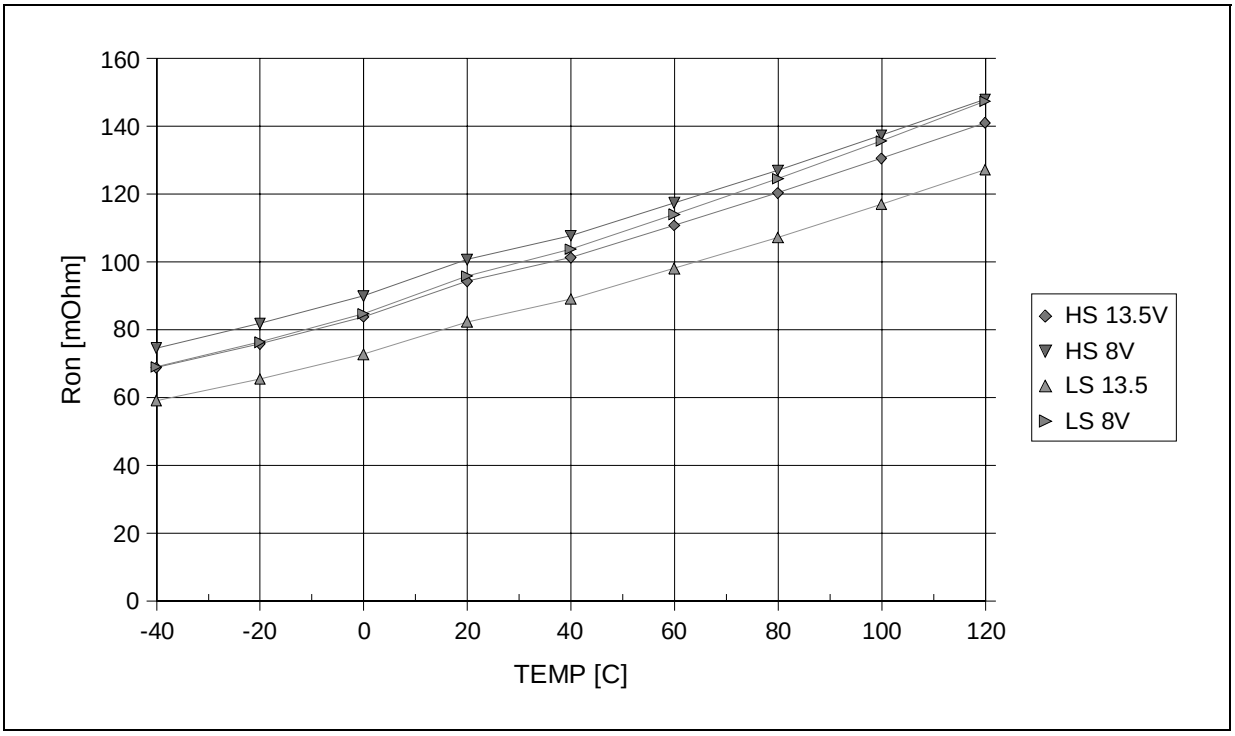


Figure 4. TYPICAL R_{ON} CHARACTERISTICS OUT3,4,5

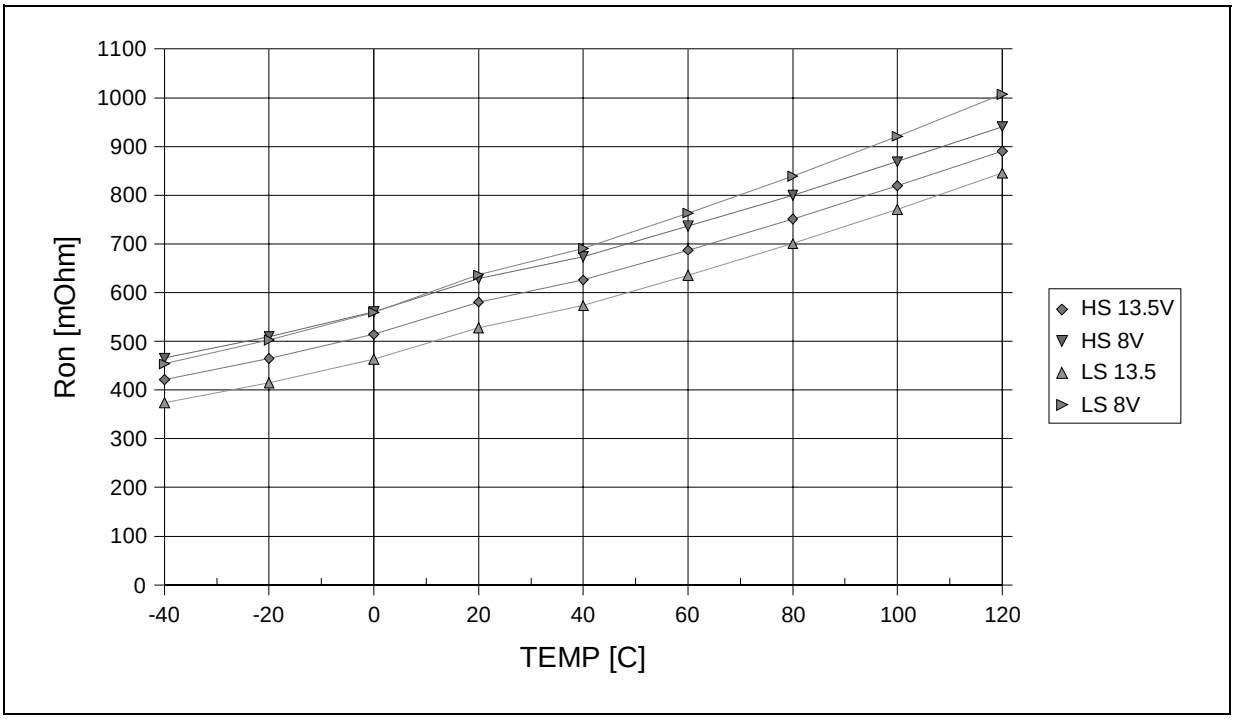
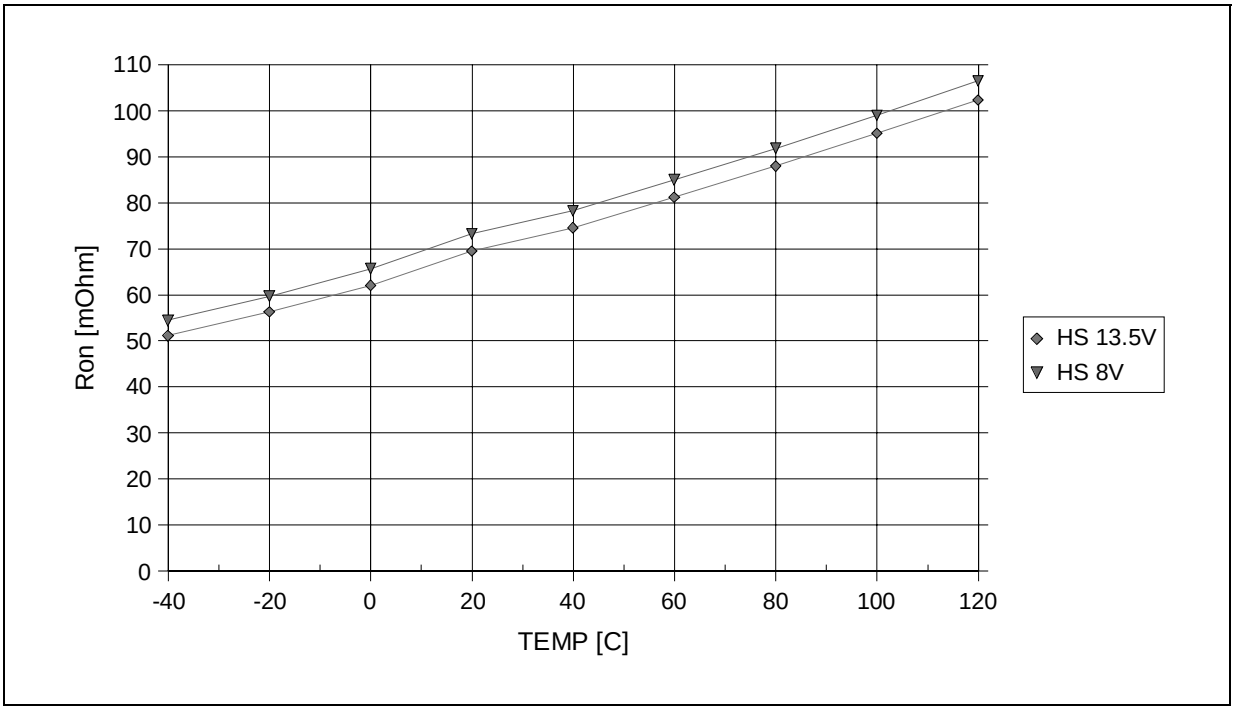


Figure 5. TYPICAL R_{ON} CHARACTERISTICS OUT6



ELECTRICAL CHARACTERISTCS

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = -40 to 150 °C, unless otherwise specified. The voltages are refered to GND and currents are assumed positive, when the current flows into the pin.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUTS: OUT1 - OUT6						
$t_{d\ ON\ H}$	Output Delay Time, Highside Driver On	V_S = 13,5 V corresponding low side driver is not active	20	40	80	µs
$t_{d\ OFF\ H}$	Output Delay Time, Highside Driver Off	V_S = 13,5 V	80	150	300	µs
$t_{d\ ON\ L}$	Output Delay Time, Lowside Driver On	V_S = 13,5 V corresponding highside driver is not active	20	40	80	µs
$t_{d\ OFF\ L}$	Output Delay Time, Lowside Driver Off	V_S = 13.5 V	80	150	300	µs
$t_{D\ HL}$	Dead Time, Source to Sink	$t_{d\ ON\ L}$ (HS was on) - $t_{d\ OFF\ H}$	5		200	µs
$t_{D\ LH}$	Dead Time, Sink to Source	$t_{d\ ON\ H}$ (LS was on) - $t_{d\ OFF\ L}$	5		200	µs
I_{QLH}	Leakage Current Highside Drivers of OUT1-6	V_{OUT1-6} = 0 V, standby mode	0	2	5	µA
		V_{OUT1-6} = 0 V, active mode	-40	-15	0	µA
I_{QLL}	Leakage Current Lowside Drivers of OUT1-5	V_{OUT1-5} = V_S, standby mode	0	7	20	µA
		V_{OUT1-5} = V_S, active mode	-40	-15	0	µA

ELECTRICAL CHARACTERISTCS (continued)

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = -40 to 150 °C, unless otherwise specified. The voltages are refered to GND and currents are assumed positive, when the current flows into the pin.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUTS: OUT1 - OUT6						
I_{OLD12}	Open Load Detection Current of OUT1 and OUT2		80	160	320	mA
I_{OLD345}	Open load detection current of OUT3, OUT4 and OUT5		20	40	60	mA
I_{OLD6}	open load detection current of OUT6		60	160	320	mA
t_{dOL}	minimum duration of open load condition to set the status bit		500		3000	µs
t_{ISC}	minimum duration of overcurrent condition to switch off the driver		10		100	µs
dV_{OUT12}/dt	slew rate of OUT1 and OUT2	V_S = 13.5 V, for highside driver: I_{load} = -3A, for lowside driver: I_{load} = 3A	0.1	0.2	0.4	V/µs
dV_{OUT345}/dt	slew rate of OUT3, OUT4 and OUT5	V_S = 13.5 V, for highside driver: I_{load} = -0.8A, for lowside driver: I_{load} = 0.8A	0.09	0.2	0.4	V/µs
dV_{OUT6}/dt	slew rate of OUT6	V_S = 13.5 V, I_{load} = -2.5A	0.1	0.2	0.4	V/µs

Figure 6. Application Circuit Diagram

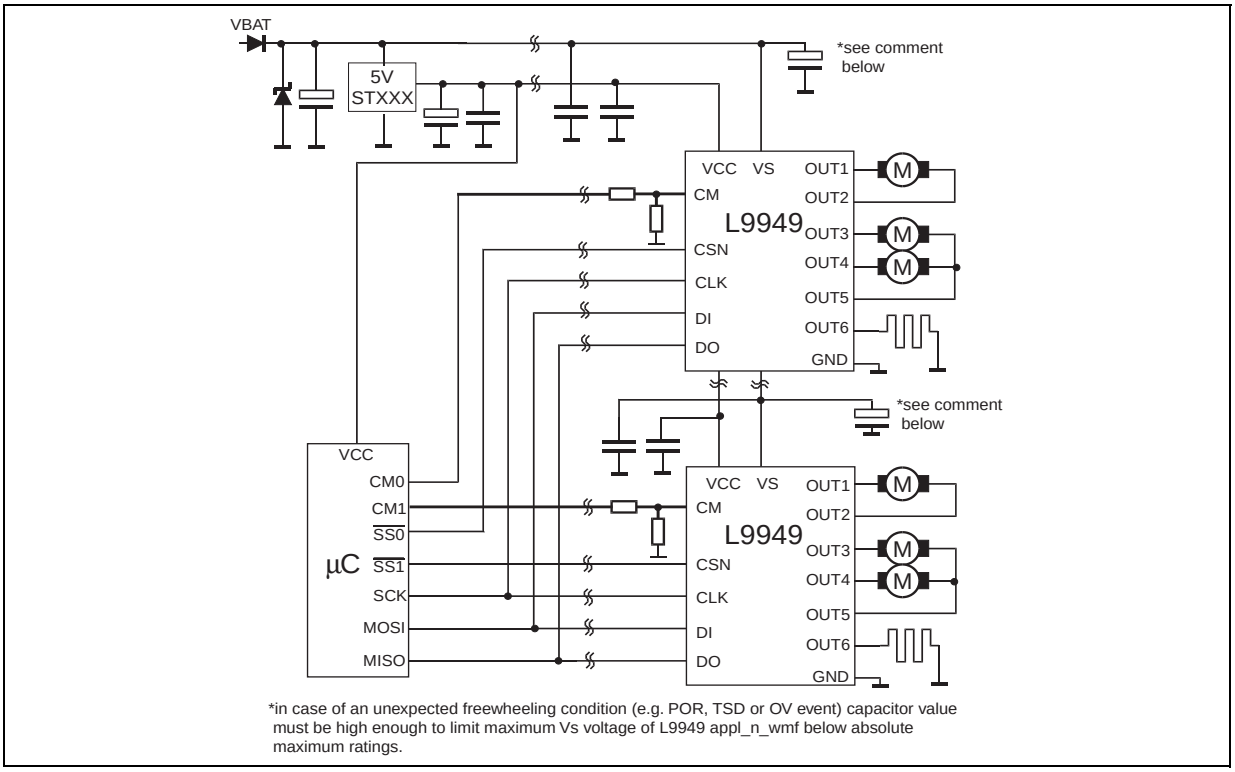
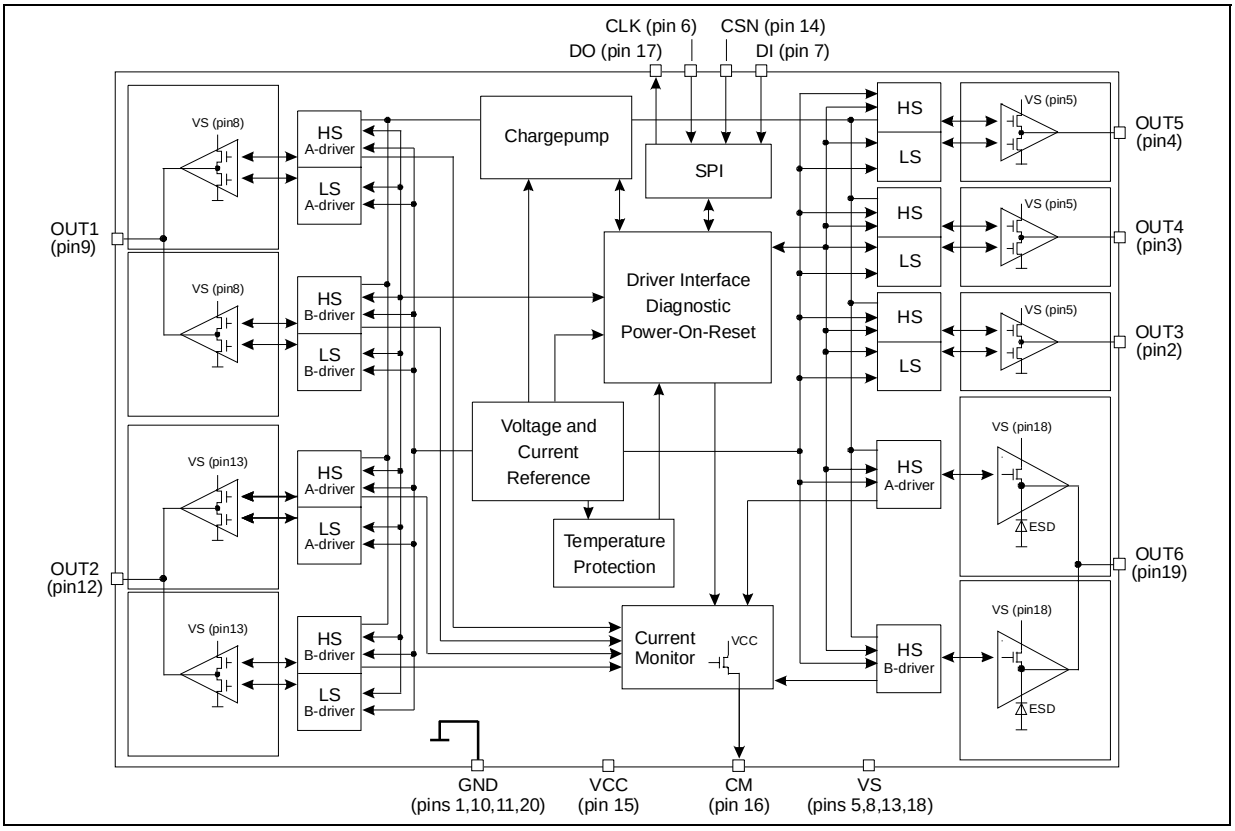


Figure 7. Functional Block Diagram



FUNCTIONAL DESCRIPTION OF THE SPI

Serial Peripheral Interface (SPI)

This device uses a standard SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: CPOL = CPHA = 0 or CPOL = CPHA = 1.

For these two modes, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

The difference of these two modes is the standby polarity of the CLK. For CPOL = 0 the CLK remains low and for CPOL = 1 the CLK remains high.

This device is not limited to microcontrollers with a build-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect the status bit 0 (fault condition) of the device which is a logical-or of all bits in the status registers 0 and 1. The microcontroller can poll the status of the device without the need of a full SPI-communication cycle.

Note: In contrast to the SPI-standard the least significant bit (LSB) will be transfered first (see. FIGURE 8).

Chip Select not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal will activate the output driver and a serial communication can be started.

Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the

rising edge of the CLK signal and shifted into an internal 16 bit shift register. At the rising edge of the CSN signal the contents of the shift register will be transfered to Data Input Register (see FIGURE 8).

The SPI uses an internal 16 bit counter which will be reset at the rising edge of the CSN signal. Only the first 16 bits of the data input DI will be relevant. If more than 16 bits are transfered the trailing bits will be ignored.

Serial Data Out (DO)

The output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal (see FIGURE 8).

Input Data Register

After the rising edge of CSN the contents of the input shift register will be written to the input data register. Depending on bit 0 the contents of the selected status register will be transfered to DO during the current communication cycle. Bit 1-11 controls the behaviour of the corresponding driver. If bit 12 and bit 13 are zero, the device will go into the standby-mode. If at least one of both bits are one these bits will be used to control the current monitor multiplexer. Bit 14 selects the V_S lockout mode. If this bit is set, an over- or undervoltage condition at the power supply V_S will disable all driver stages until the status bit will be cleared by the microcontroller. Bit 15 is used to reset all status bits in both status registers. The bits in the status registers will be cleared after the current communication cycle (rising edge of CSN).

Status Register

This devices uses two status registers to store and to monitor the state of the device. Bit 0 is used as a fault bit and is a logical-NOR combination of all other bits in both status registers. The state of this bit can be polled by the microcontroller without the need of a full SPI-communication cycle (see FIGURE 13). If one of the overcurrent bits is set, the corresponding driver will be disabled. The microcontroller has to clear the overcurrent bit to enable the driver. If the thermal shutdown bit is set, all drivers will go into a high impedance state. Again the microcontroller has to clear the bit to enable the drivers. The behaviour of the device in case of an over- or undervoltage condition will depend on the V_S lockout bit (bit 14) in the input data register. If bit 14 is cleared, the device will reactivate the drivers if the power supply V_S returns to normal operating range. In this case no interaction from the microcontroller is needed.

Test Mode

Due to the current limitations of a single bond wire the output stages OUT1, 2 and 6 need two bond wires in parallel. For the full output current driving capability it is necessary to check that both bond wires are connected correctly to the lead frame. Therefore the drivers and DMOS-transistors of the outputs OUT1, 2 and 6 are splitted into two independet stages, one for each bond wire (see FIGURE 6.4). In normal operating mode the splitted outputs are connected in parallel. In the test mode bit 5 and 6 of the input data register select the A-driver, bit 7 and 8 the B-driver. If all four bits (5 - 8) are switched to high level, no driver will be activated. For all combinations beside both high of bit 5 and 6 or bit 7 and 8 the output stages OUT3 and OUT4 are controlled like in normal operating mode. In any case the output stages are protected against shoot through current. Furthermore the inputs CLK and DI are connected by an OR to the output DO for testing the threshold voltages and the hysteresis. The input CLK can be tested by clamping the input DI to low level and vice versa.

SPI Interface – Input Data and Status Register

Input Data Register			
BIT	**Function**		
15	High level reset all bits in selected status register		
14	V_S under- / overvoltage lockout bit		
13 12	Control bits for standby mode and Current monitor multiplexer		
	bit13	bit12	function
	0	0	standby mode
	0	1	OUT1
	1	0	OUT2
	1	1	OUT6
11	OUT6 – HS driver on/off (1)		
10	OUT5 – HS driver on/off (1)		
9	OUT5 – LS driver on/off (1)		
8	OUT4 – HS driver on/off 5(1)	test mode bit 8 | bit 7 1 | 1 B-driver is active	
7	OUT4 – LS driver on/off 5(1)		
6	OUT3 – HS driver on/off 5(1)	test mode bit 6 | bit 5 1 | 1 A-driver is active	
5	OUT3 – LS driver on/off 5(1)		
4	OUT2 – HS driver on/off 5[1]		
3	OUT2 – LS driver on/off [1]		
2	OUT1 – HS driver on/off [1]		
1	OUT1 – LS driver on/off [1]		
0	Status register select bit L: status register 0; H: status register 1		

Status Register		
BIT	**Function**	
	Register 0	**Register 1**
15	always H	always H
14	V_S overvoltage	not used – set to L
13	V_S undervoltage	chargepump off
12	Temperature shutdown	Temperature warning
11	OUT6 – HS driver overcurrent	OUT6 – HS driver open load
10	OUT5 – HS driver overcurrent	OUT5 – HS driver open load
9	OUT5 – LS driver overcurrent	OUT5 – LS driver open load
8	OUT4 – HS driver overcurrent	OUT4 – HS driver open load
7	OUT4 – LS driver overcurrent	OUT4 – LS driver open load
6	OUT3 – HS driver overcurrent	OUT3 – HS driver open load
5	OUT3 – LS driver overcurrent	OUT3 – LS driver open load
4	OUT2 – HS driver overcurrent	OUT2 – HS driver open load
3	OUT2 – LS driver overcurrent	OUT2 – LS driver open load
2	OUT1 – HS driver overcurrent	OUT1 – HS driver open load
1	OUT1 – LS driver overcurrent	OUT1 – LS driver open load
0	no fault condition (2)	

H = on; L = off; HS = highside; LS = lowside

(1) If the bits of HS- and LS-driver of the same output stage are high, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from V_S to GND.

(2) A logical NOR-combination of all bits 1 to 14 in both status registers. This bit can be polled by the micro-controller without the need of the full SPI communication (see Figure 13). A broken VCC-connection of the L9949 can be detected by the microcontroller, because all 15 bits low or high is not a valid frame.

SPI INTERFACE ELECTRICAL CHARACTERISTCS

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = -40 to 150 °C, unless otherwise specified. The voltages are refered to GND and currents are assumed positive, when the current flows into the pin.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Delay time from standby to active mode						
t_{set}	Delay Time	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.			200	µs
Inputs: CSN, CLK and DI						
V_{INL}	Input Low Level	V_{CC} = 5 V			1.5	V
V_{INH}	Input High Level	V_{CC} = 5 V	3.5			V
V_{INHyst}	Input Hystersis	V_{CC} = 5 V	0.5			V
I_{CSNin}	Pull Up Current at input CSN	V_{CSN} = 3.5 V	-50	-25	-10	µA
$I_{CLK\ in}$	Pull Down Current at input CLK	V_{CLK} = 1.5 V	10	25	50	µA
$I_{DI\ in}$	Pull Down Current at input DI	V_{DI} = 1.5 V	10	25	50	µA
C_{in} (1)	Input Capacitance at input CSN or CLK	0 V < V_{CC} < 5.5 V		10	15	pF
DI timing (see Fig. 9)(2)						
t_{CLK}	Clock Period	V_{CC} = 5 V	1000			ns
t_{CLKH}	Clock High Time	V_{CC} = 5 V	400			ns
t_{CLKL}	Clock Low Time	V_{CC} = 5 V	400			ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_{CC} = 5 V	400			ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_{CC} = 5 V	400			ns
$t_{set\ DI}$	DI setup time	V_{CC} = 5 V	200			ns
$t_{hold\ DI}$	DI hold time	V_{CC} = 5 V	200			ns
$t_{r\text{-}in}$	Rise Time of Input Signal DI, CLK, CSN	V_{CC} = 5 V			100	ns
$t_{f\text{-}in}$	Fall Time of Input Signal DI, CLK, CSN	V_{CC} = 5 V			100	ns
DO						
V_{DOL}	Output Low Level	V_{CC} = 5 V, I_D = -4 mA		0.2	0.4	V
V_{DOH}	Output High Level	V_{CC} = 5 V, I_D = -4 mA	V_{CC} -1.3	V_{CC} -1.0		V
		V_{CC} = 5 V, I_D = -200 µA; T_j = 25°C	V_{CC} -0.8			V

SPI INTERFACE ELECTRICAL CHARACTERISTCS (continued)

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = -40 to 150 °C, unless otherwise specified. The voltages are refered to GND and currents are assumed positive, when the current flows into the pin.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{DOLK}	Tristate Leakage Current	$V_{CSN} = V_{CC}$, 0 V < V_{DO} < V_{CC}	-10		10	µA
C_{DO}	Tristate Input Capacitance	$V_{CSN} = V_{CC}$, 0 V < V_{CC} < 5.5 V		10	15	pF
DO timing (see Figg. 10 & 11)						
$t_{r\ DO}$	DO Rise Time	C_L = 100 pF, I_{load} = -1mA		50	100	ns
$t_{f\ DO}$	Data Out Fall Time	C_L = 100 pF, I_{load} = 1mA		50	100	ns
$t_{en\ DO\ tri\ L}$	DO Enable Time from tristate to low level	C_L = 100 pF, I_{load} = 1mA pull-up load to V_{CC}		80	250	ns
$t_{en\ DO\ L\ tri}$	DO Disable Time from low level totristate	C_L = 100 pF, I_{load} = 4mA pull-up load to V_{CC}		200	400	ns
$t_{en\ DO\ tri\ H}$	DO Enable Time from tristate to high level	C_L = 100 pF, I_{load} = -1mA pull-down load to GND		80	250	ns
$t_{en\ DO\ H\ tri}$	DO Disable Time from high level totristate	C_L = 100 pF, I_{load} = -4mA ppull-down load to GND		200	400	ns
$t_{d\ DO}$	DO Delay Time	V_{DO} < 0.3 V_{CC}, V_{DO} > 0.7 V_{CC}, C_L = 100 pF		50	250	ns

(1) Value of input capacity is not measured in production test. Parameter guarenteed by design.
(2) DI timing parameters tested in production by a passed/failed test:
Tj=-40°C/+25°C: SPI communication @2MHz
Tj=+125°C: SPI communication @1.25MHz

Figure 8. SPI-Interface - Transfer Timing Diagram

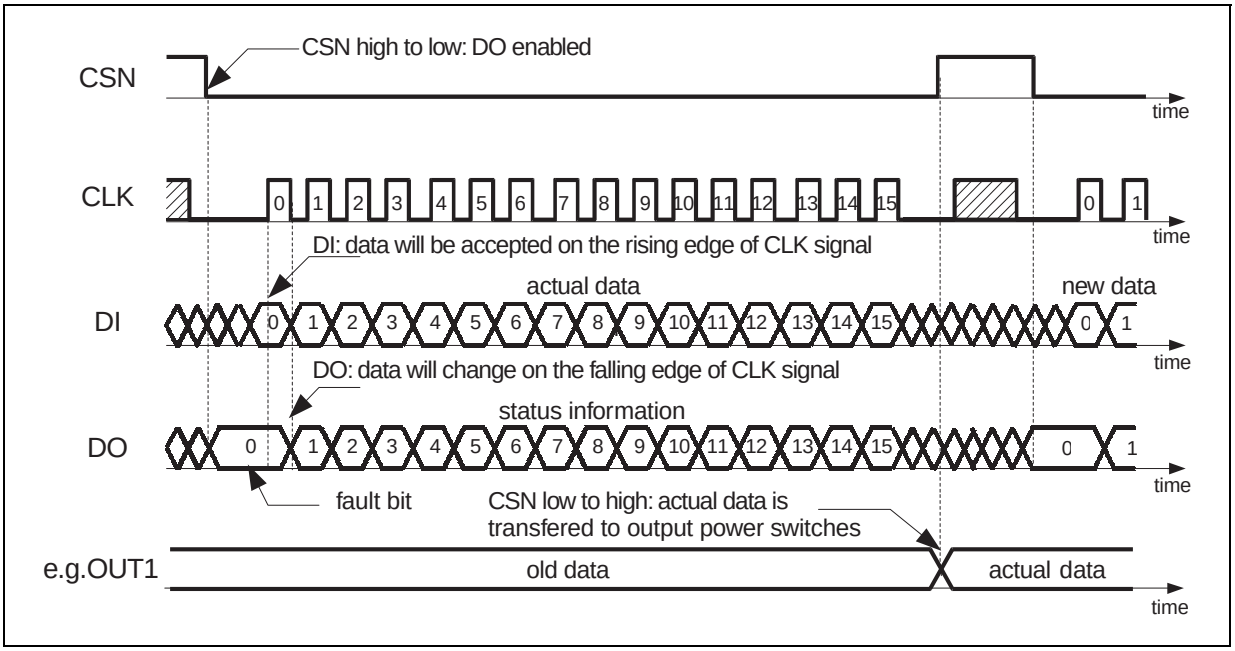


Figure 9. SPI-interface - Input Timing

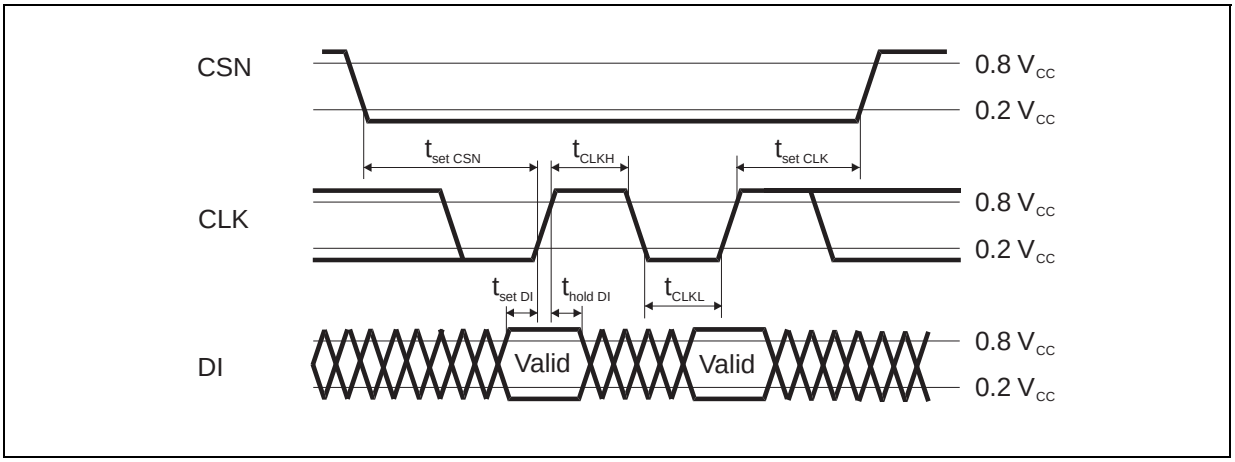


Figure 10. Data Out Valid Data Delay Time and Valid Time

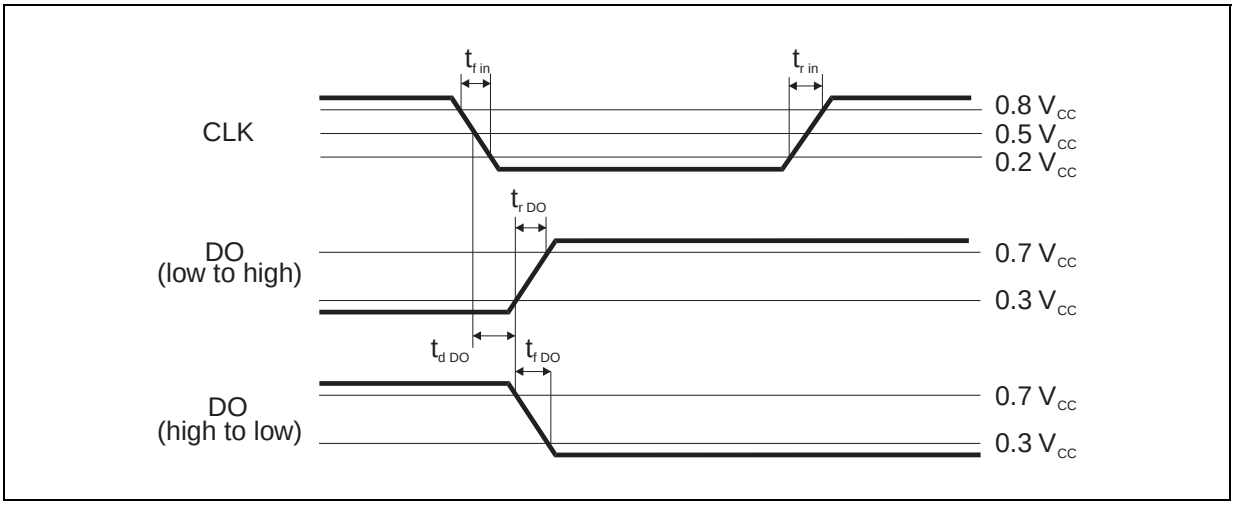


Figure 11. SPI-Interface - Data Out Enable and Disable Time

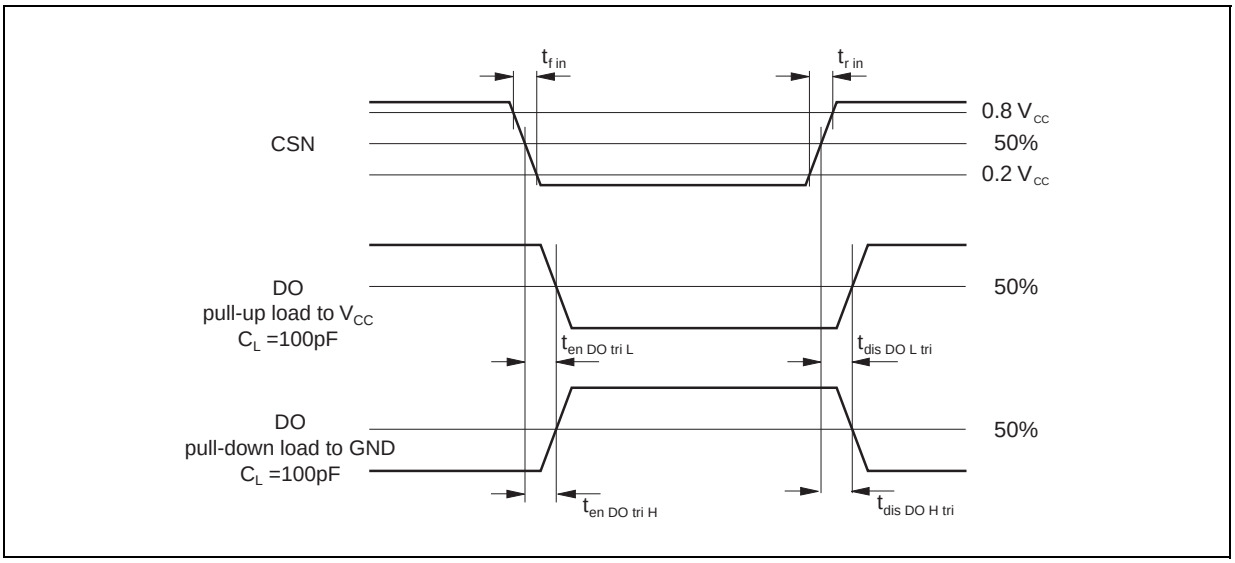


Figure 12. SPI-Interface - Driver Turn On/Off Timing

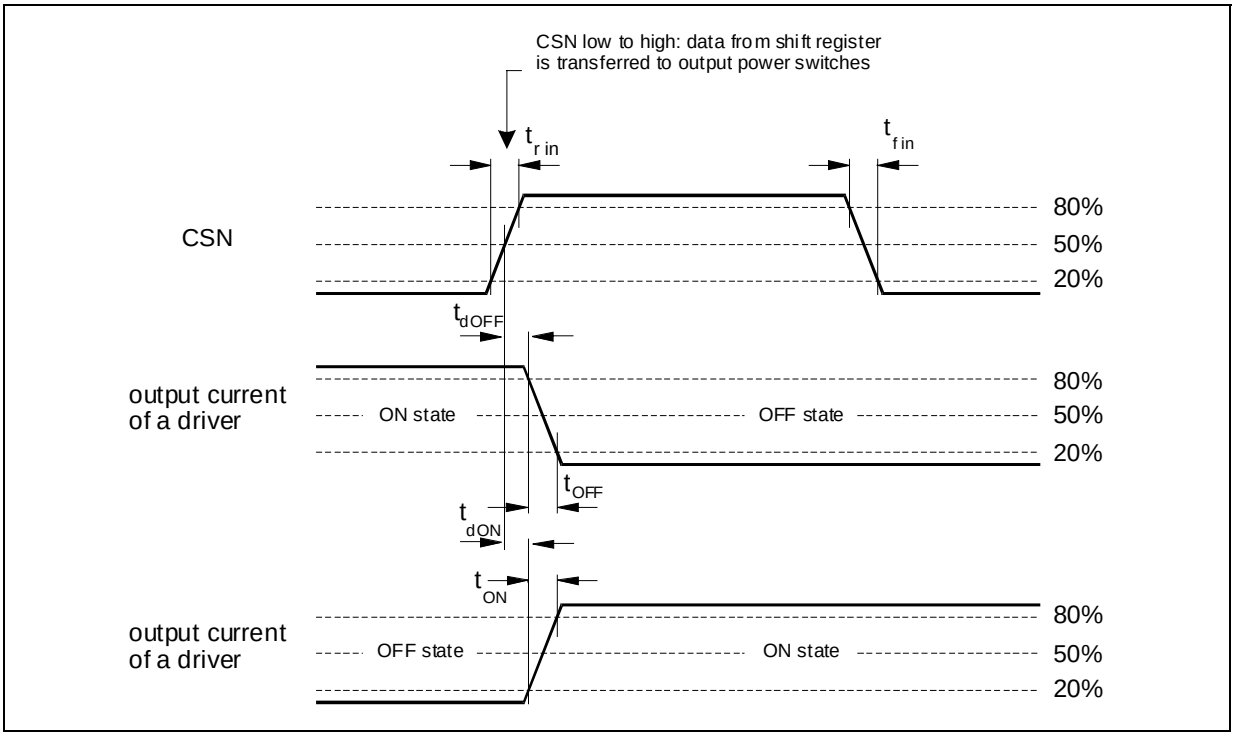
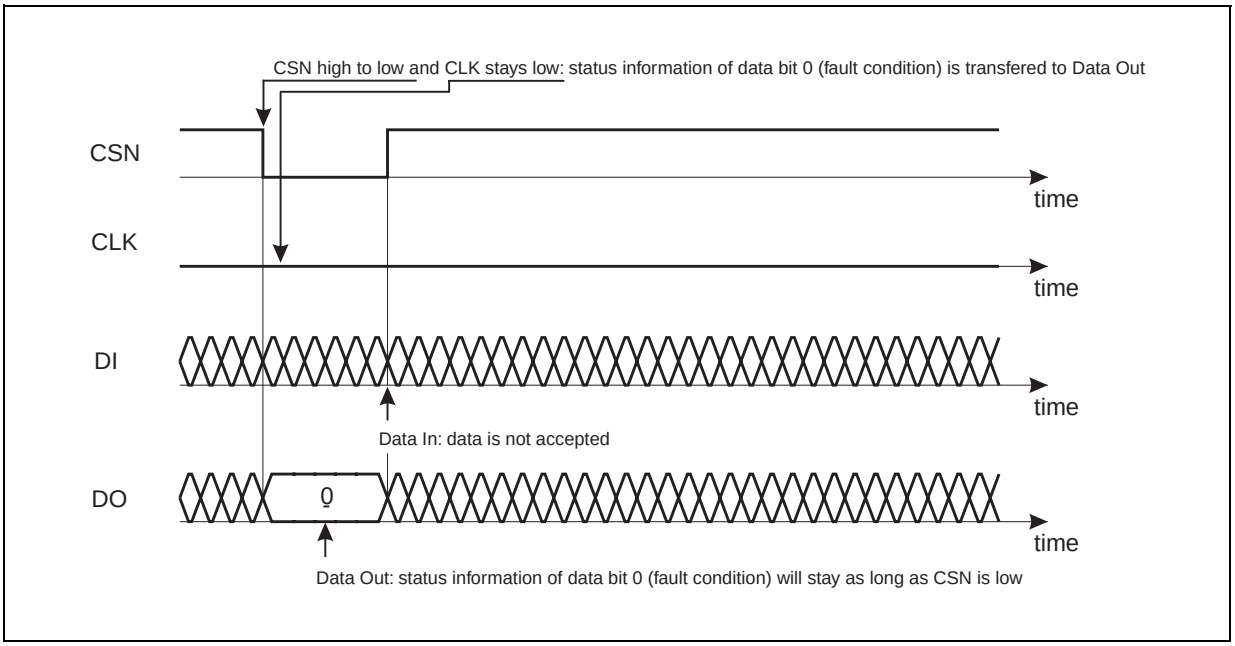


Figure 13. SPI-Interface - Timing of Status Bit 0 (Fault Condition)

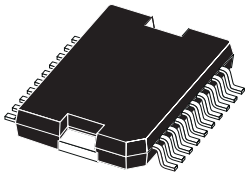


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max.)					
T		10			0.394	

(1) “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions: “E”, “G” and “a3”.

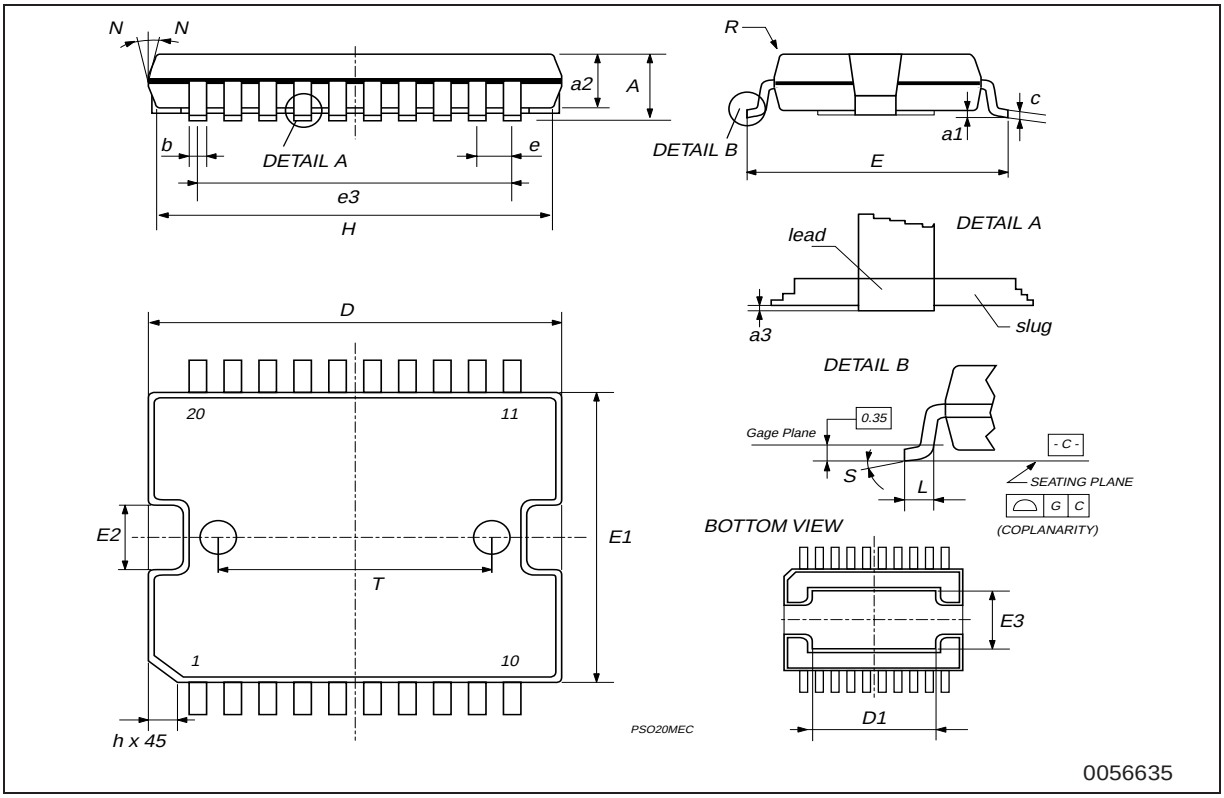
OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



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