DESCRIPTION

Demonstration circuit 1150A 1150A is a featuring the LTC5554 IC, a 7-bit programmable gain amplifier. It incorporates a variety of passive components to support configurations for varied applications.

The LT5554 is a differential input and output precision programmable gain amplifier with 16dB gain range and 0.125dB gain step.

The seven LT5554 gain control inputs (PGx, x=0,2,..6) and the STROBE input can be coupled to TTL (DC-coupling type) or ECL and (low-voltage) CMOS drivers (AC-coupling type) without external components. The 3-state MODE pin allows the selection of the coupling type. The LT5554 gain state can be updated asynchronously when STROBE is HIGH or synchronously using the STROBE input positive transition. In the latter STROBED-MODE, the external control logic time skew is eliminated and synchronization with the ADC clock is possible.

With 0.125dB step resolution and 5ns settling time, the LT5554 may be suited in quasi-continuous gain control applications.

The LT5554 power and voltage gain for Maximum Gain is 18dB when application R_{out}=50•. Application gain can be changed with different R_{out} selections.

The LT5554 amplifier is unconditionally stable. Consequently, LC-filters or SAW filters can be connected to the LT5554 I/O pins without padding.

Lacking global feed-back, the LT5554 has -80dB reverse isolation @ 400MHz (package limited).

Design files for this circuit board are available. Call the LTC factory.

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Table 1. Typical DEMO BOARD Performance Summary [T_A = 25°C, V_{CC} = 5V, VccO = 5V, ENB = 3V, MODE = 5v, STROBE = 2.2V, H_{IH} = 2.2V, MAXIMUM GAIN, P_{OUT} = 4dBm/Tone ($2V_{P-P}$ into 50Ω), Δf = 200KHz]

SYMBOL	PARAMETER	CONDITIONS	TYPICAL PERFORMANCE		UNIT
V_{CC}	Supply Voltage		4.75 to 5.25		V
$V_{CC}O$	OUT± Output Pin DC Common Mode Voltage	(For more detail, Please see Note 4 of data sheet)	3.5 to 6		V
I_{CC}	V_{CC} Supply Current	V_{CC} = 5V	100		mA
I_{ODC}	OUT± Quiescent Current	OUT± Voltages = 5V	96		mA
R_{IN}	Input Resistance	F_{IN}=100MHz	45		Ω
C_{IN}	Input Capacitance	F_{IN}=100MHz	2.8		pF
R_O	Output Resistance	F_{IN}=100MHz	400		Ω
C_O	Output Capacitance	F_{IN}=100MHz	1.9		pF
HD2	Second Harmonic Distortion	Pout=10dBm (Single Tone), F_{IN}=100MHz, R_{OUT} = 50Ω	**-76**		**dBc**
HD3	Third Harmonic Distortion	Pout=10dBm (Single Tone), F_{IN}=100MHz, R_{OUT} = 50Ω	**-62**		**dBc**
			R_{OUT}		
			50Ω	**100Ω**	
G_{VMAX}	Maximum Voltage Gain	F_{IN}=200MHz	13.7	19.6	dB
G_{PMAX}	Maximum Power Gain	F_{IN}=200MHz	13.6	16.6	dB
IIP3	Input Third Order Intercept Point	F_{IN}=200MHz	27.8	27	dBm
OIP3	Output Third Order Intercept Point	F_{IN}=200MHz	41.5	44	dBm
IMD3	Intermodulation Product	F_{IN}=200MHz	-84	-88	dBc
V_{ONOISE}	Output Noise Noise Spectral Density	F_{IN}=200MHz	10.7	21.4	nV/√Hz
NF	Noise Figure	F_{IN}=200MHz	10	10	dB
RTI	Input Referred Noise Spectral Density	F_{IN}=200MHz	1.34	1.34	nV/√Hz
SFDR	Spurious Free Dynamic Range	F_{IN}=200MHz	128	128	dBm/Hz

Table 2. DC1150A Board I/O Description

CONNECTOR	FUNCTION	COMMENTS
J1	Singe-Ended Input	50Ω Signal source, no external termination necessary
J3	Singe-Ended Output	50Ω matched, can drive network/spectrum analyzer input
VCC	LT5554 VCC pin.	Connect to power supply 5V.
VCCO	Output bias voltage	Connect to power supply 5V.
VPG	Bias STROBE and all PGx via 10KΩ resistors.	Connect to power supply in 3 to 5V range for Maximum Gain state. Connect to GROUND for Minimum Gain state.
ENABLE	Enable/Shut-down	Connect to 5V to enable LT5554, or connect to GND for shut-down.

MODE	Selects STROBE and PGx input type	Connect to 5V for gain control inputs DC-coupled TTL levels. (consult tables 1 and 2 on page 19 of datasheet for other settings)
STROBE	VGA gain update mode	STROBE=H : gain is asynchronously set by PGx transitions. STROBE=L : gain is not changed by PGx transitions. STROBE=signal : gain is synchronously set by the PGx state strobed by the STROBE pin positive transitions.
PG0 … PG6	VGA control inputs	Biased by default from VPG via 10kΩ resistors when left open. Apply the desired level to corresponding PGx Turret or J5 connector pin to change the gain state.
VDEC	Input common-mode voltage test point	Self-biasing within LT5554, normally open. When voltage is applied, the internal bias buffer source and sink currents can be measured.

Table 3. DC1150A Board I/O Optional Features

CONNECTOR	FUNCTION	COMMENTS
J5	External LT5554 state control	Board Edge Connector can be used instead of board mounted turrets to control the LT5554 state.
J2	PG1/PG2	Timing evaluation. 50Ω matched SMA connector
J4	PG3/PG4	Timing evaluation. 50Ω matched SMA connector
J6	PG5/PG6	Timing evaluation. 50Ω matched SMA connector
J7	STROBE	Timing and full speed up to 200MHz evaluation. 50Ω matched SMA connector

Table 4. DC1150A Board I/O Optional circuits

INPUT PORT	OUTPUT PORT	COMMENTS
Single-Ended with transformer coupled to differential source	Differential outputs converted to Single-Ended with transformer	Single-Ended Input and Output with transformers. (Standard Demo Board is shipped with this configuration.) Simplified Input and Output circuits is shown on page 4.
Differential Inputs with Capacitively-Coupled to a Differential Source	Differential outputs converted to Single-Ended with transformer	Differential Capacitively-Coupled input and Output with transformer. Circuit modification is shown on page 5.
Single-Ended with transformer coupled to differential source	Differential wide band Decoupling capacitors Outputs	Single-Ended transformer Input and differential 100 decoupling capacitors outputs. Circuit modification is shown on page 6.
Single-Ended with transformer coupled to differential source	Differential 50 Outputs with transformer	Single-Ended transformer Input and Differential 50 outputs with transformer. Circuit modification is shown on page 7.

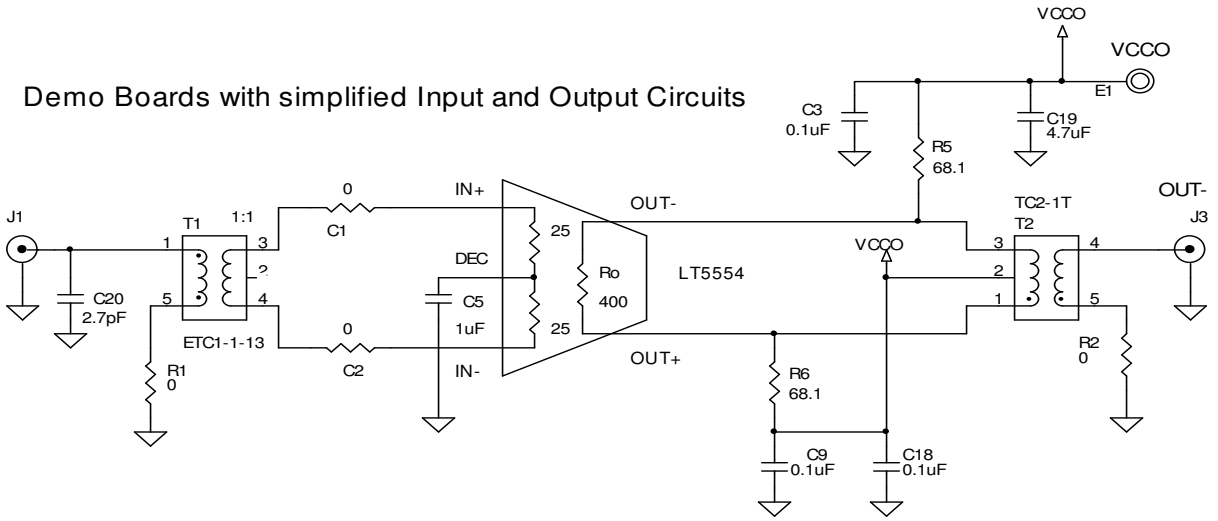
Table 5. DC1150A Board different Rout Impedance

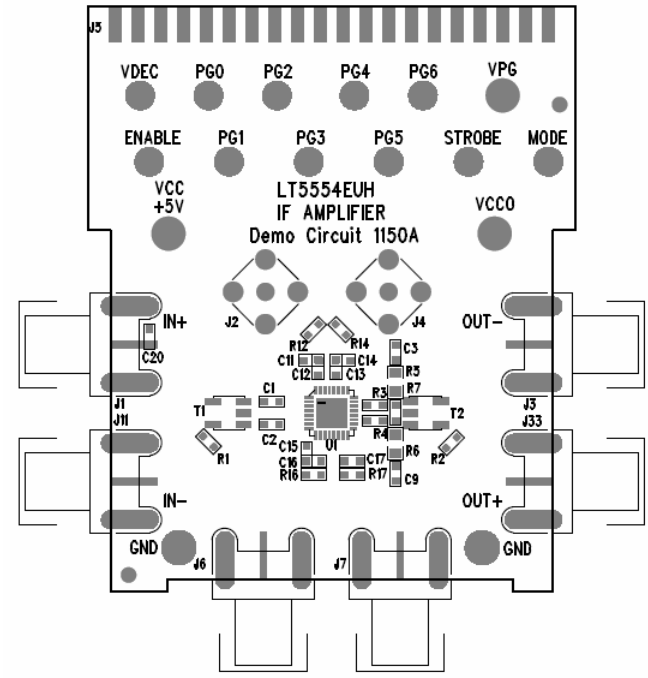
ROUT ***	FUNCTION	COMMENTS
Rout=50•	50• Single-ended output(J3)	R5 and R6 = 68.1•. T2 =TC2-1T. (Standard Demo Board installed with these components values)
Rout=75•	50• Single-ended output(J3)	Replace R5 and R6 from 68.1• to 124•. T2(TC2-1T) replace with TC3-1T(Mini-Circuit)
Rout=100•	50• Single-ended output(J3)	Replace R5 and R6 from 68.1• to 205•. T2(TC2-1T) replace with TC4-1W(Mini-Circuit)

NOTE: *** Consult Tables 3, 4 page 23, 24 respectively of datasheet for others Rout Options.

LT5554 STANDARD DEMO BOARD WITH SINGLE-ENDED INPUT AND OUTPUT TRANSFORMERS

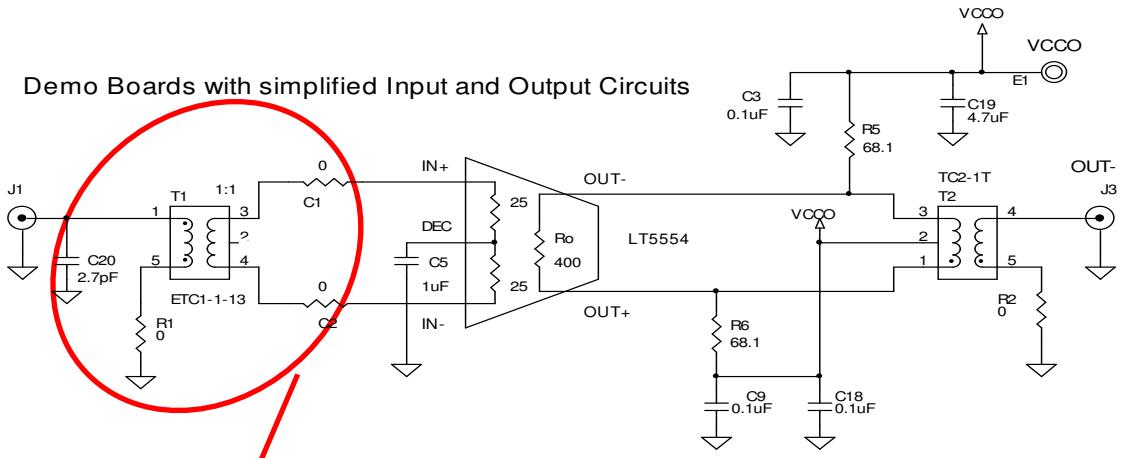
Demo Boards with simplified Input and Output Circuits



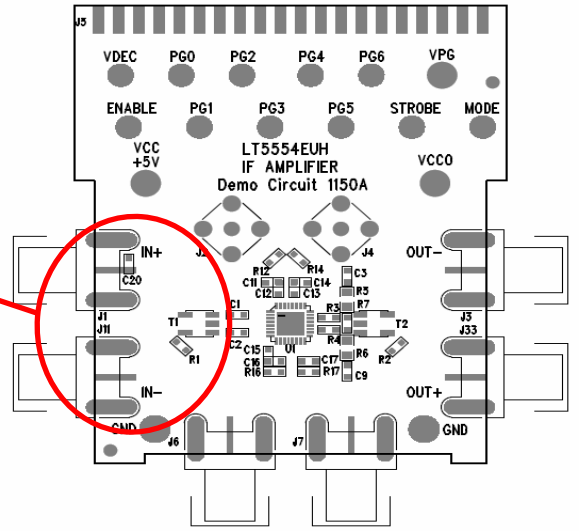


Demo Board's Silk Screen

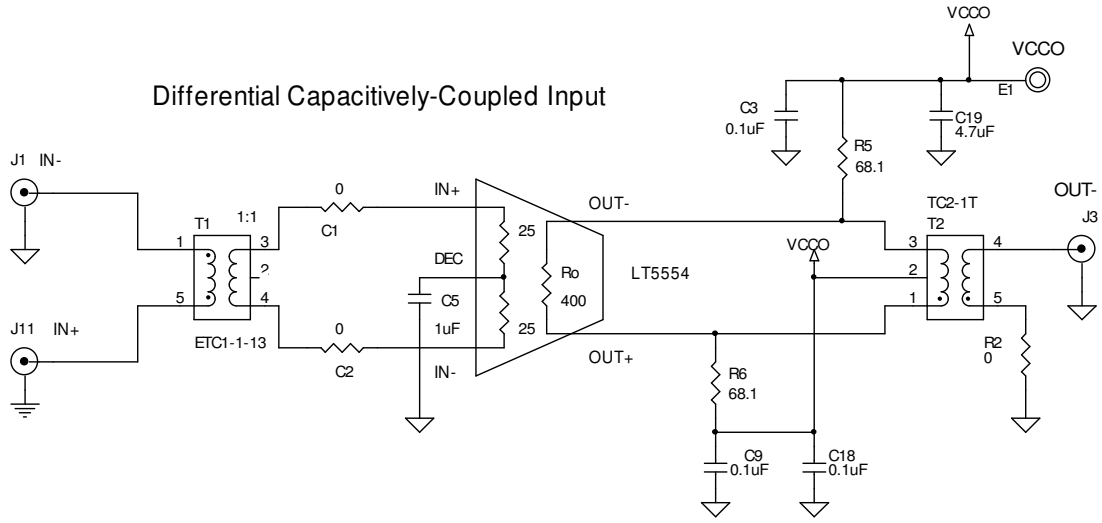
MODIFICATION FOR 50 SINGLE-ENDED TRANSFORMER INPUT TO DIFFERENTIAL INPUT



1) Remove T1 and bypass with 0 resistors. (Connecting transformer footprint 1 to 3 and pin 5 to 4)
2) Install decoupling capacitors C1 and C2.
3) Install J11 connector.
4) Remove C20 and R1.

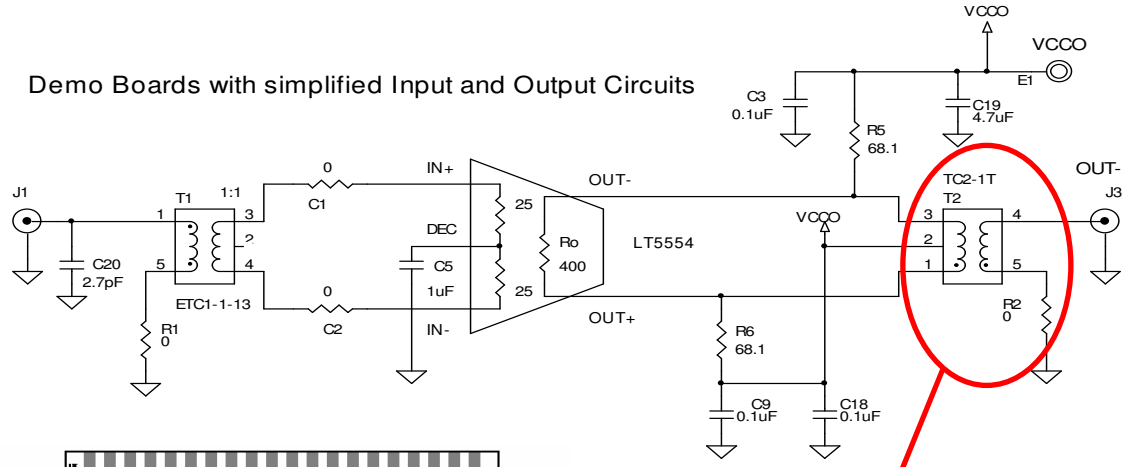


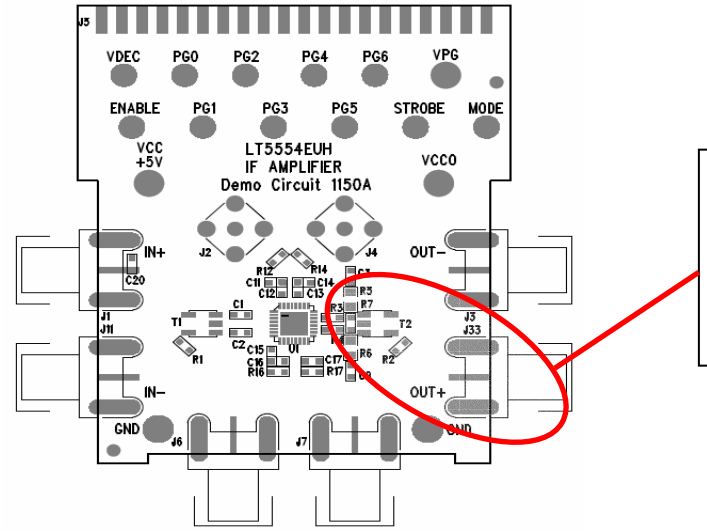
MODIFIED INPUT CIRCUIT



MODIFICATION FOR 50 SINGLE-ENDED TRANSFORMER OUTPUT TO DIFFERENTIAL 100 WIDE BAND OUTPUT

Demo Boards with simplified Input and Output Circuits

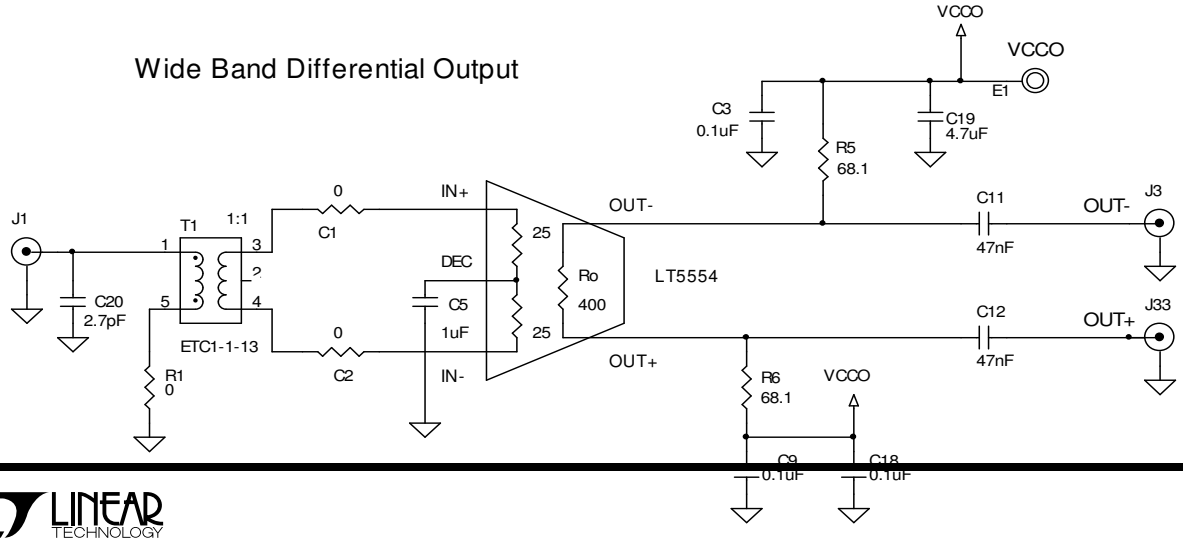




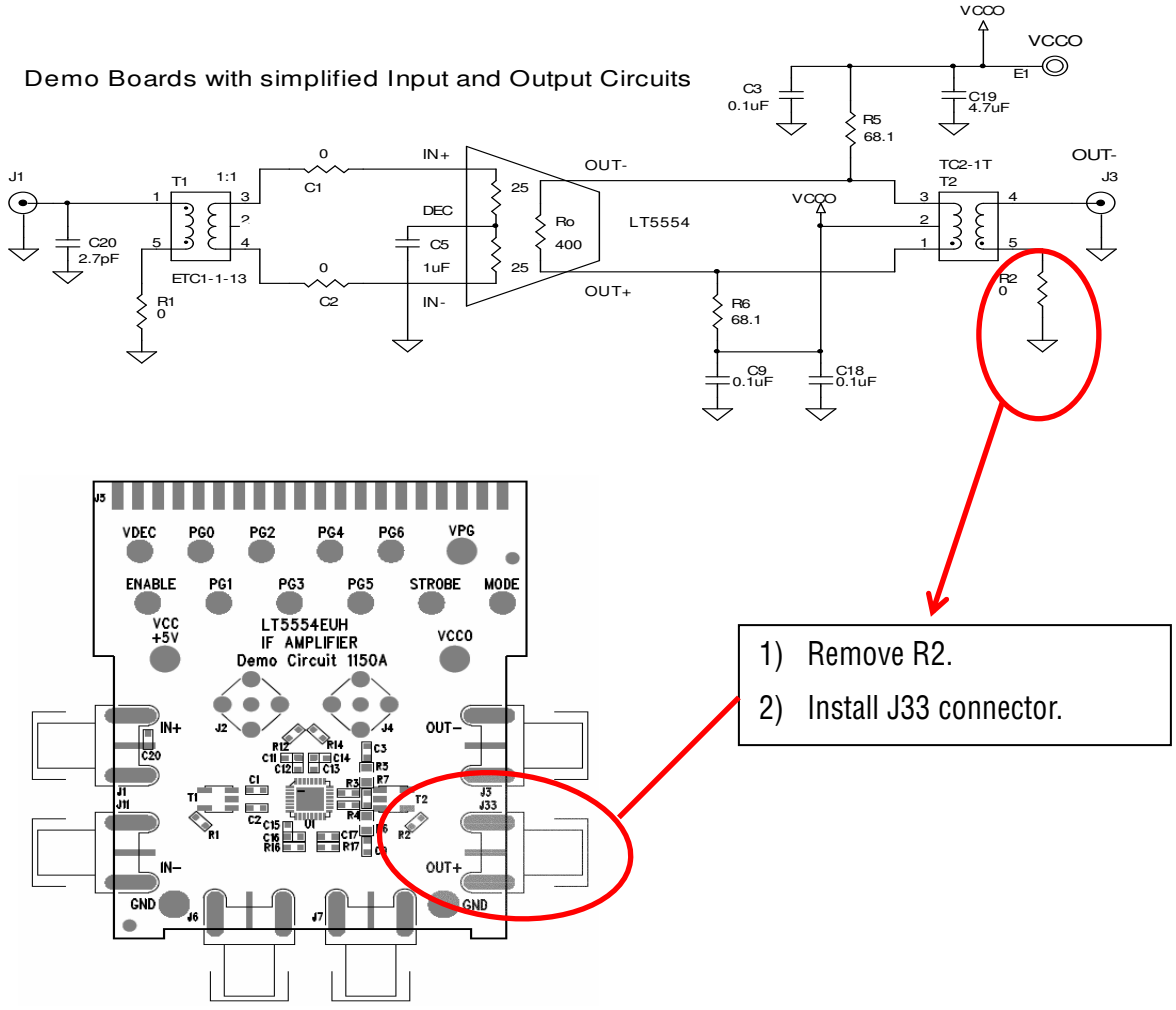
1) Remove R2 and T2.
2) Install decoupling capacitors C11 and C12 (using T2 footprint).
3) Install J33 connector.

Modified Output circuit

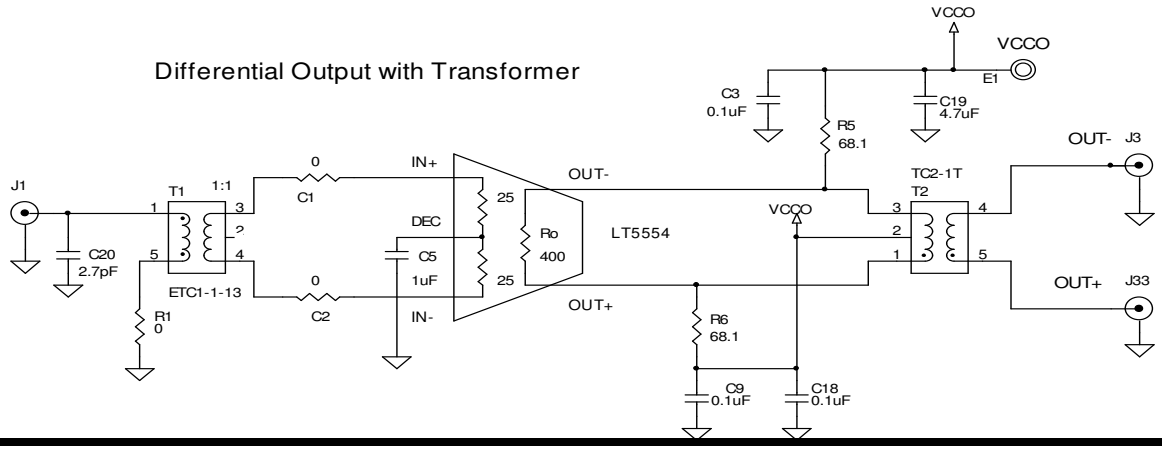
Wide Band Differential Output



MODIFICATION FOR 50 SINGLE-ENDED TO 50 DIFFERENTIAL OUTPUT WITH TRANSFORMER



Modified Output circuit



ADDITIONAL INFORMATION

INTERMODULATION AND HARMONIC DISTORTION MEASUREMENTS

The LT5554 performance is better than most signal generators and spectrum analyzers can provide. The available instrumentation performance test consists in connecting the signal source to the spectrum analyzer (bypass the DC1150A board). If the measured performance is worse than LT5554 datasheet figure, please refer to the Application Note 97 (published for the related LT5514 part) for signal source conditioning and spectrum analyzer setup.

OUTPUT POWER MATCHING RELATED OIP3 AND GAIN -3DB DISCREPANCY

The R_{OUT} stands for the total output impedance as seen by the LT5554 open-collector outputs with equates to R_0 || (R5+R6) || R(T2). (where R_0 =400Ω is the LT5554 internal resistor and R(T2) is the T2 transformer secondary impedance).

Then, the LT5554 power gain is:

$G_P=10\log(R_{IN} * G_M^2 * R_{OUT})$ in dB

The DC1150A board output power matching loss on [R_0 || (R5+R6)] accounts for a DC1150A measured Board-Gain and OIP3 -3dB lower than the LT5554 datasheet performance stated for driving an on-board load, without output power matching (like in the ADC interface application case).

HIGHER OIP3 AND R_{out} MEASUREMENTS

By default, the DC1150A board has R_{OUT} = 50Ω which provides best SFDF, not necessarily best OIP3.

Higher OIP3 can be obtained reconfiguring the DC1150A board for R_{OUT} > 50Ω.

For DC1150A board output modifications, please refer to Table 5 above or figure 16 and table 3 on page 23 of the LT5554 datasheet.

If the application bandwidth is greater than the T2 output transformer bandwidth, the DC1150A board can be reconfigured according to the LT5554 datasheet figure 17 and table 4.

TIMING MEASUREMENTS

The DC1150A timing measurements require the J2, J4, J6 (PGx), J7 (STROBE) connectors to be mounted. The function of each connector is outlined in table 2 above and the circuit is depicted in the datasheet (page 26) figure 20 to be implemented according to datasheet instructions. This setup can evaluate only three PGx at a time.

The LT5554 part can be seen as a multiplier with an analog port (IN+, IN-) and a 7-bit logarithmic DAC port and opens the signal synthesizer and conditioning applications. The DC1150A board can be used to test the LT5554 in such applications if PGx 7-bit data is supplied via the J5 edge connector.

DRIVING THE INPUTS DC-COUPLED

It is possible to drive the LT5554 inputs differentially with DC coupling. Transformer T1 should be replaced with 0Ω resistors and connector J11 reconfigured as for differential input as illustrated on page 5.

The LT5554 internal input common-mode bias reference available at DEC pin is used for the external DC level shifter circuit used to drive the LT5554 IN+, IN- inputs in DC-coupling applications. The DC current flowing into LT5554 IN+, IN- inputs can be monitored and maintained within +/- 200µA limits for best operation. The external drive circuit must have a DC 100Ω differential output

impedance to retain the specified LT5554 gain step accuracy.

AC-COUPLED DIFFERENTIAL OUTPUTS

The LT5554 outputs can drive differentially a 3V ADC like LTC2254/5 LTC2208/9 with AC coupling. Transformer T2 should be replaced with 0Ω resistors and connector J33 reconfigured as described in Table 4 and illustrated on page 6 for differential output. Resistors R5 and R6=28.7Ω should be mounted to provide a differential 50Ω source impedance for the ADC inputs. The circuit is shown in figure 1 below.

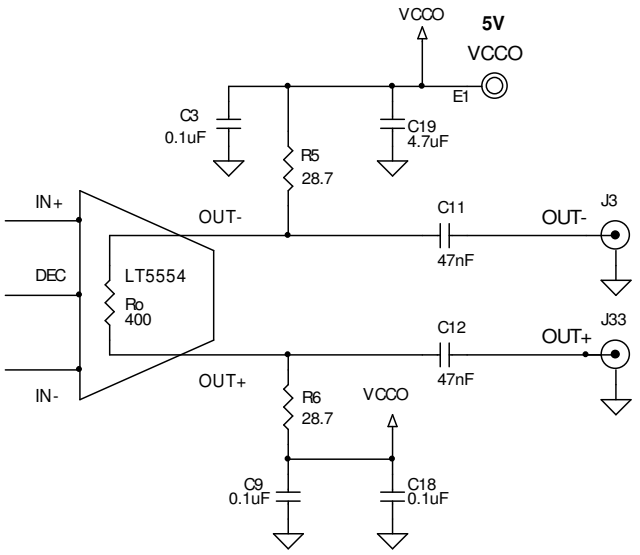


Figure 1. Differential 50 Ohm source impedance for ADC

The LT5554 IODC=45mA output bias current (fairly constant throughout VGA range and temperature) will produce a 1.3V drop across (each) R5, R6 connected to VccO=5V. The DC1150A board common mode voltage at J3, J33 connectors is 3.7V. The VccO=5V specified OIP3=46dBm changes to OIP3=44.5dBm for 3.7V output common mode voltage.

The ADC part will have Vcc=5V and GROUND DC level shifted with 2V and appropriately decoupled to the board ground plane. Then the common mode voltage of both parts will be fairly aligned.

A further refinement user may consider is to use external (high impedance) DC-current sources either open-loop or in a DC-loop controlled by the ADC V_{CM} internal reference. This allows the setting of the LT5554 DC output common mode voltage independent of R5, R6 values.

When high OP1dB are desired, the VccO can be increased but must not exceed the absolute maximum rating of 7V for OUT+ and OUT- (in shut-down full VccO voltage is applied to OUT+, OUT-).

ADC INPUT OVERDRIVE PROTECTION

Unlike LTC ADC parts, some ADC parts from other vendors may exhibit long recovery time when ADC inputs are driven beyond supply rail. With 5ns recovery time, the LT5554 part can provide the power limiting function when driving such ADC parts. The DC1150A board required modifications to test the power limiting function are based on one of the following two methods:

Low R_{OUT} values (current limiting)

Lower the VccO supply voltage (voltage limiting)

This is possible because LT5554 linearity close to compression is still good as depicted in the LT5554 datasheet typical characteristic section.

SCHEMATIC NOTES

The following schematic components may not be required in user application:

- C6, the MODE decoupling capacitor
- C5, the DEC decoupling capacitor. C5 improves with a few dB the input common mode performance only for frequencies below 100MHz.
- C4, C8 the VCC decoupling capacitors. The LT5554 has VCC internal voltage regulators and HF decoupling.

QUICK START PROCEDURE

Table 2 shows the function of each connector and turret and figure 4 is showed a Full Schematic version of DC1150A board.

Refer to figure 2 for the connection diagram and figure 3 for the standard DC1150A board schematic and follow the procedure below for evaluation with a single 5V power supply:

- Connect the VCC and VCCO to the 5V power supply.
- Connect the ENABLE and MODE to the 5V power supply to enable the LT5554.
- Connect the VPG to the 5V power supply to set the LT5554 VGA in Maximum Gain state. Alternatively, VPG connected to GROUND will set the Minimum Gain state.
- The LT5554 gain can be changed from Gmax or Gmin according to a binary code by connecting any PGx (x=0,2, .. 6) to 5V respectively 0V. PG0 controls the LSB 0.125dB gain step while PG6 change the MSB 8dB gain step.
- Apply an input signal to J1. The input is impedance-matched to 50Ω.
- Observe the output via J3. The output is impedance-matched to 50Ω, suitable for the input of a network or a spectrum analyzer.

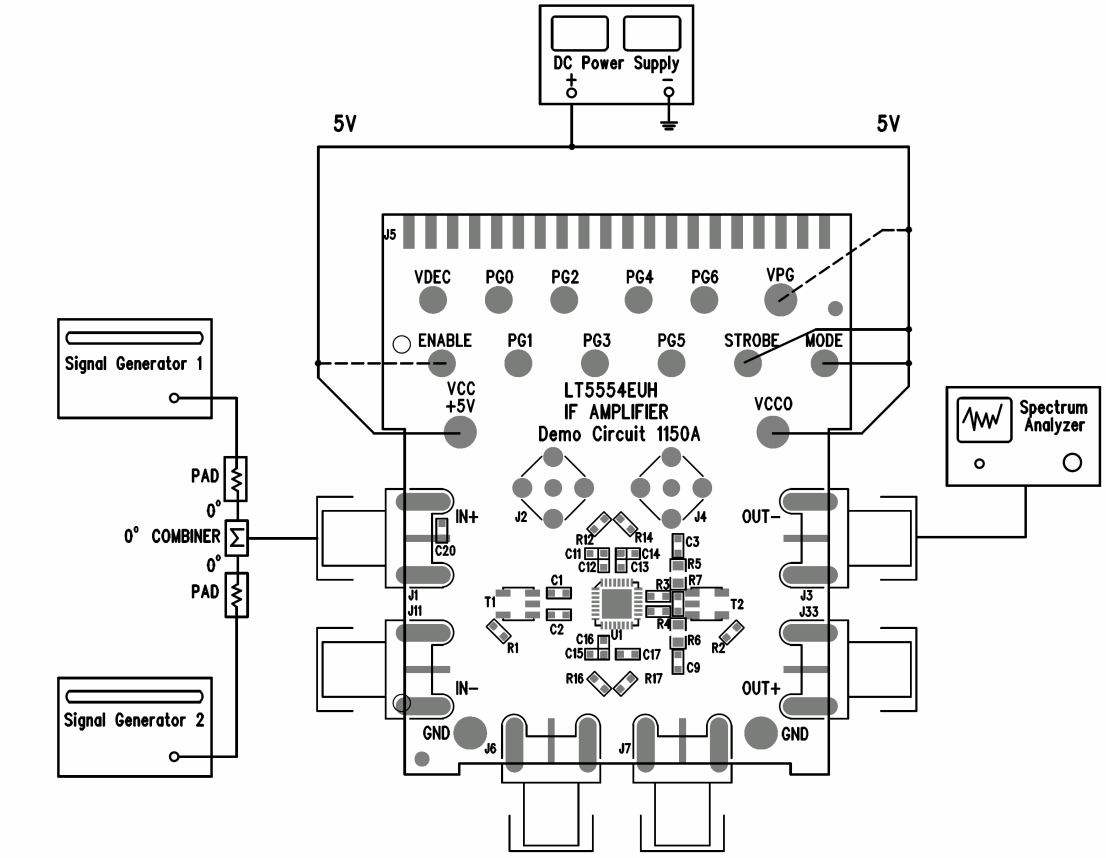
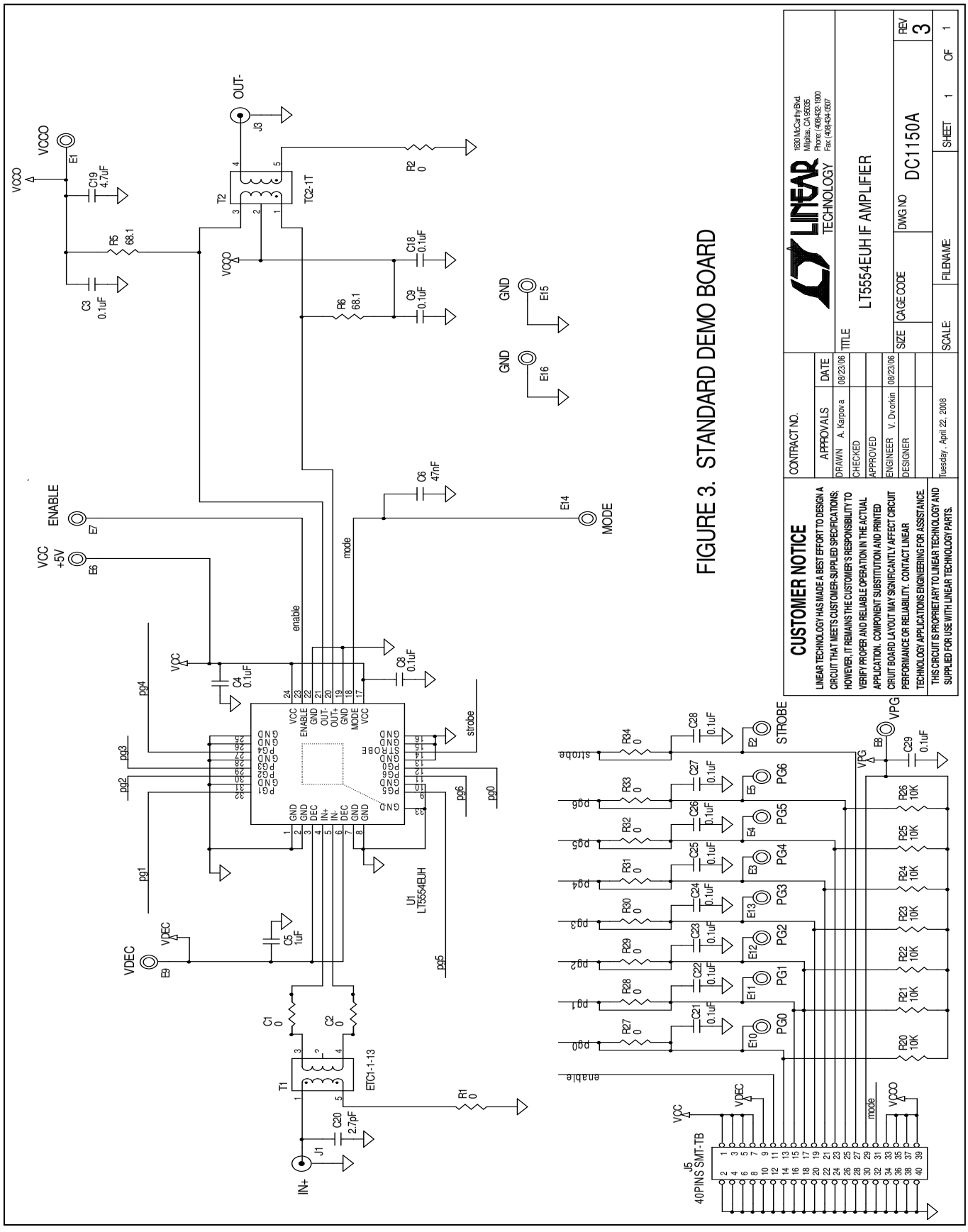


Figure 2. Proper Measurement Equipment Setup


VCCO
E1
C19
4.7uF
R5
68.1
C3
0.1uF
T2
TC2-1T
OUT-
J3
R2
0
C18
0.1uF
C9
0.1uF
R6
68.1
GND
E15
GND
E16
ENABLE
E7
VCC
+5V
E6
C6
47nF
E14
MODE
mode
enable
C4
0.1uF
C8
0.1uF
strobe
U1
LT5554EUH
VDEC
E9
C5
1uF
C1
0
C2
0
T1
ETC1-1-13
R1
0
C20
2.7pF
J1
IN+
pg4
pg3
pg2
pg1
pg0
pg6
pg5
R34
0
C28
0.1uF
E2
STROBE
R33
0
C27
0.1uF
E5
PG6
R32
0
C26
0.1uF
E4
PG5
R31
0
C25
0.1uF
E3
PG4
R30
0
C24
0.1uF
E13
PG3
R29
0
C23
0.1uF
E12
PG2
R28
0
C22
0.1uF
E11
PG1
R27
0
C21
0.1uF
E10
PG0
VPG
E8
C29
0.1uF
R26
10K
R25
10K
R24
10K
R23
10K
R22
10K
R21
10K
R20
10K
J5
40PINS SMT-TB
FIGURE 3. STANDARD DEMO BOARD
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THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.
CONTRACT NO.
APPROVALS
DATE
DRAWN A. Karpova 08/23/06
CHECKED
APPROVED
ENGINEER V. Dvorkin 08/23/06
DESIGNER
Tuesday, April 22, 2008
SCALE:
TITLE
LT5554EUH IF AMPLIFIER
SIZE
CAGE CODE
DWG NO
DC1150A
REV
3
FILENAME:
SHEET 1 OF 1
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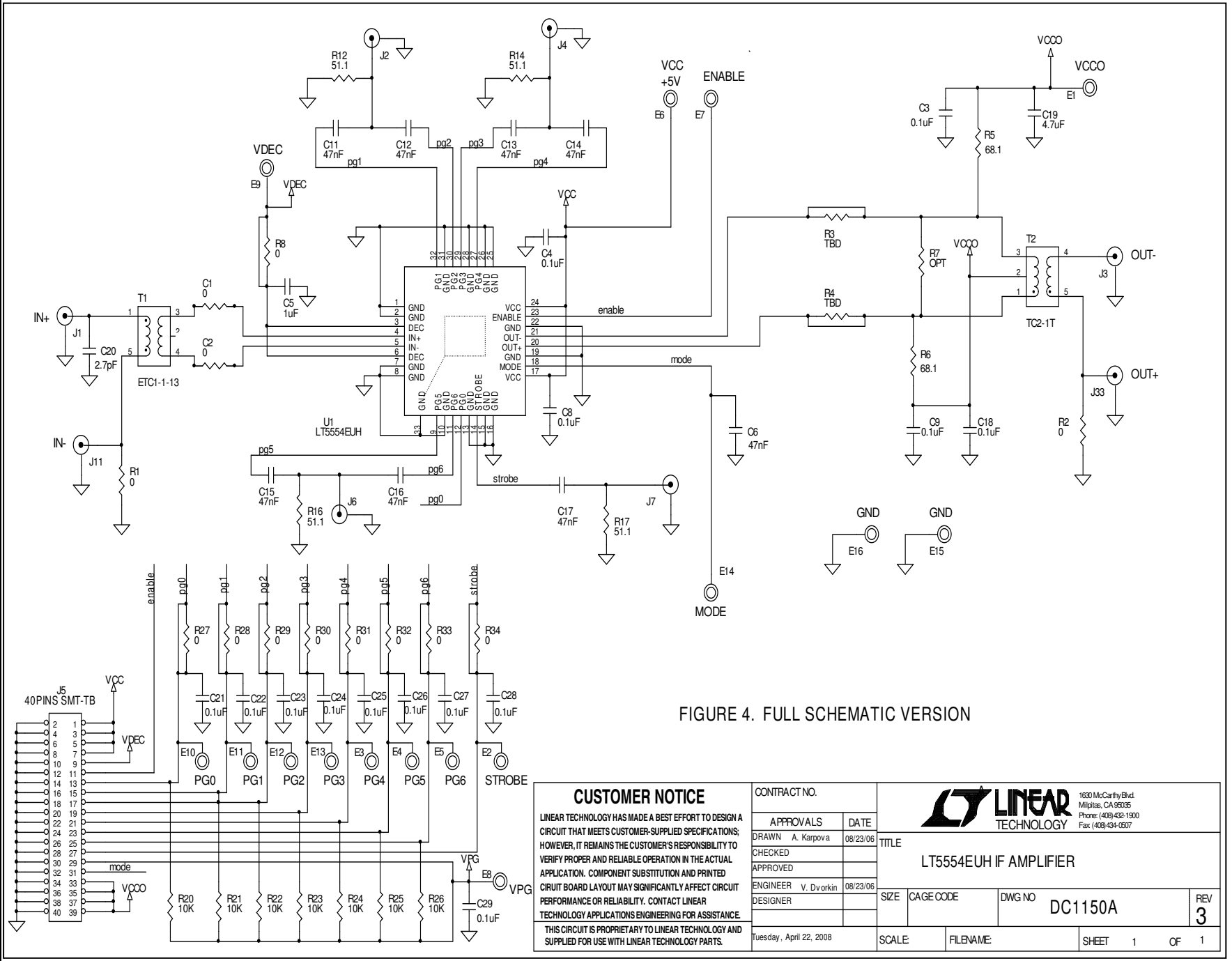


FIGURE 4. FULL SCHEMATIC VERSION

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APPROVALS	DATE
DRAWN A. Karpova	08/23/06
CHECKED	
APPROVED	
ENGINEER V. Dvorkin	08/23/06
DESIGNER	

Tuesday, April 22, 2008

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TITLE: LT5554EUH IF AMPLIFIER

SIZE	CAGE CODE	DWG NO	REV
		DC1150A	3

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