TLC320AC02C, TLC320AC02I
Data Manual

Single-Supply Analog Interface Circuit

SLAS084C
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TEXAS INSTRUMENTS

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1 Introduction

The TLC320AC02† analog interface circuit (AIC) is an audio-band processor that provides an analog-to-digital and digital-to-analog input/output interface system on a single monolithic CMOS chip. This device integrates a band-pass switched-capacitor antialiasing input filter, a 14-bit-resolution analog-to-digital converter (ADC), a 14-bit-resolution digital-to-analog converter (DAC), a low-pass switched-capacitor output-reconstruction filter, (sin x)/x compensation, and a serial port for data and control transfers.

The internal circuit configuration and performance parameters are determined by reading control information into the eight available data registers. The register data sets up the device for a given mode of operation and application.

The major functions of the TLC320AC02 are:

1. To convert audio-signal data to digital format by the ADC channel
2. To provide the interface and control logic to transfer data between its serial input and output terminals and a digital signal processor (DSP) or microprocessor
3. To convert received digital data back to an audio signal through the DAC channel

The antialiasing input low-pass filter is a switched-capacitor filter with a sixth-order elliptic characteristic. The high-pass filter is a single-pole filter to preserve low-frequency response as the low-pass filter cutoff is adjusted. There is a three-pole continuous-time filter that precedes this filter to eliminate any aliasing caused by the filter clock signal.

The output-reconstruction switched-capacitor filter is a sixth-order elliptic transitional low-pass filter followed by a second-order (sin x)/x correction filter. This filter is followed by a three-pole continuous-time filter to eliminate images of the filter clock signal.

The TLC320AC02 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously; data reception at the DAC channel and data transmission from the ADC channel occur during the same time interval. The data transfer is in 2s-complement format.

There are three basic modes of operation available: the stand-alone analog-interface mode, the master-slave mode, and the linear-codec mode. In the stand-alone mode, the TLC320AC02 generates the shift clock and frame synchronization for the data transfers and is the only AIC used. The master-slave mode has one TLC320AC02 as the master that generates the master-shift clock and frame synchronization; the remaining AICs are slaves to these signals. In the linear-codec mode, the shift clock and the frame-synchronization signals are externally generated and the timing can be any of the standard codec-timing patterns.

Typical applications for this device include modems, speech processing, analog interface for DSPs, industrial-process control, acoustical-signal processing, spectral analysis, data acquisition, and instrumentation recorders.

The TLC320AC02C is characterized for operation from 0°C to 70°C and the TLC320AC02I is characterized for operation from –40°C to 85°C.

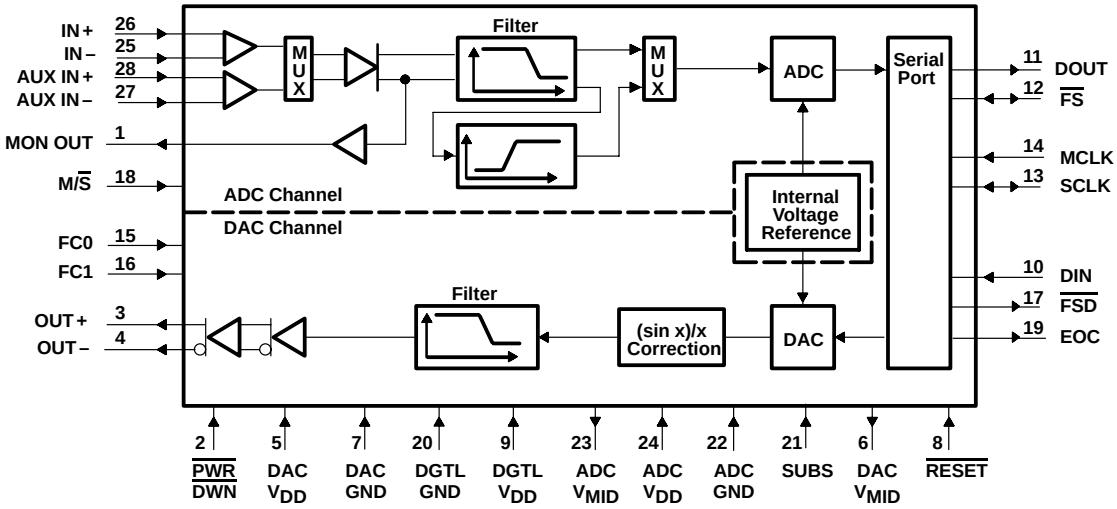
† The TLC320AC02 is functionally equivalent to the TLC320AC01 and differs in the electrical specifications as shown in Appendix C.

1.1 Features

- General-Purpose Signal-Processing Analog Front End (AFE)
- Single 5-V Power Supply
- Power Dissipation . . . 100 mW Typ
- Signal-to-Distortion Ratio . . . 70 dB Typ
- Programmable Filter Bandwidths (Up to 10.8 kHz) and Synchronous ADC and DAC Sampling
- Serial-Port Interface
- Monitor Output With Programmable Gains of 0 dB, –8 dB, –18 dB, and Squelch
- Two Sets of Differential Inputs With Programmable Gains of 0 dB, 6 dB, 12 dB, and Squelch
- Differential or Single-Ended Analog Output With Programmable Gains of 0 dB, –6 dB, –12 dB, and Squelch
- Differential Outputs Drive 3-V Peak Into a 600-Ω Differential Load
- Differential Architecture Throughout
- 1-μm Advanced LinEPIC™ Process
- 14-Bit Dynamic-Range ADC and DAC
- 2s-Complement Data Format

LinEPIC is a trademark of Texas Instruments Incorporated.

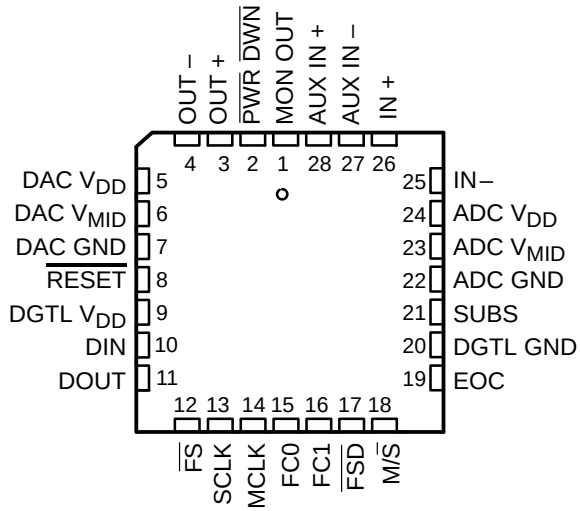
1.2 Functional Block Diagram



Terminal numbers shown are for the FN package.

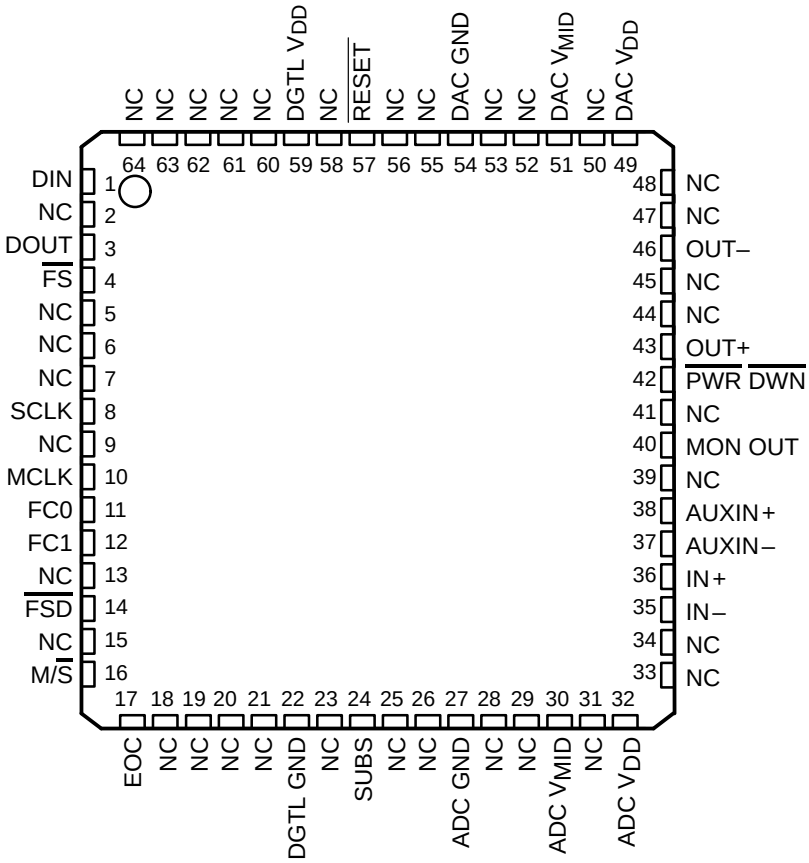
1.3 Terminal Assignments

FN PACKAGE
(TOP VIEW)



1.3 Terminal Assignments (Continued)

PM PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Terminal Functions

TERMINAL NAME	TERMINAL NO.†	TERMINAL NO.‡	I/O	DESCRIPTION
ADC V_{DD}	24	32	I	Analog supply voltage for the ADC channel
ADC V_{MID}	23	30	O	Midsupply for the ADC channel (requires a bypass capacitor). ADC V_{MID} must be buffered when used as an external reference.
ADC GND	22	27	I	Analog ground for the ADC channel
AUX IN+	28	38	I	Noninverting input to auxiliary analog input amplifier
AUX IN–	27	37	I	Inverting input to auxiliary analog input amplifier
DAC V_{DD}	5	49	I	Digital supply voltage for the DAC channel
DAC V_{MID}	6	51	O	Midsupply for the DAC channel (requires a bypass capacitor). DAC V_{MID} must be buffered when used as an external reference.
DAC GND	7	54	I	Analog ground for the DAC channel
DIN	10	1	I	Data input. DIN receives the DAC input data and command information and is synchronized with SCLK.
DOUT	11	3	O	Data output. DOUT outputs the ADC data results and register read contents. DOUT is synchronized with SCLK.
DGTL V_{DD}	9	59	I	Digital supply voltage for control logic
DGTL GND	20	22	I	Digital ground for control logic
EOC	19	17	O	End-of-conversion output. EOC goes high at the start of the ADC conversion period and low when conversion is complete. EOC remains low until the next ADC conversion period begins and indicates the internal device conversion period.
FC0	15	11	I	Hardware control input. FC0 is used in conjunction with FC1 to request secondary communication and phase adjustments. FC0 should be tied low if it is not used.
FC1	16	12	I	Hardware control input. FC1 is used in conjunction with FC0 to request secondary communication and phase adjustments. FC1 should be tied low if it is not used.
$\overline{FS}$	12	4	I/O	Frame synchronization. When $\overline{FS}$ goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, $\overline{FS}$ is low during the simultaneous 16-bit transmission to DIN and from DOUT. In slave mode, $\overline{FS}$ is externally generated and must be low for one shift-clock period minimum to initiate the data transfer.
$\overline{FSD}$	17	14	O	Frame-synchronization delayed output. This active-low output synchronizes a slave device to the frame synchronization timing of the master device. $\overline{FSD}$ is applied to the slave $\overline{FS}$ input and is the same duration as the master $\overline{FS}$ signal but delayed in time by the number of shift clocks programmed in the $\overline{FSD}$ register.
IN+	26	36	I	Noninverting input to analog input amplifier
IN–	25	35	I	Inverting input to analog input amplifier
MCLK	14	10	I	The master-clock input drives all the key logic signals of the AIC.
MON OUT	1	40	O	The monitor output allows monitoring of analog input and is a high-impedance output.
M/$\overline{S}$	18	16	I	Master/slave select input. When M/$\overline{S}$ is high, the device is the master and when low, it is a slave.

† Terminal numbers shown are for the FN package.

‡ Terminal numbers shown are for the PM package.

1.4 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.†	TERMINAL NO.‡	I/O	DESCRIPTION
OUT+	3	43	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in a differential connection or a single-ended configuration with a buffered V_{MID}.
OUT–	4	46	O	Inverting output of analog output power amplifier. OUT– is functionally identical with and complementary to OUT+.
$\overline{\text{PWR}}$ $\overline{\text{DWN}}$	2	42	I	Power-down input. When $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ is taken low, the device is powered down such that the existing internally programmed state is maintained. When $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ is brought high, full operation resumes.
$\overline{\text{RESET}}$	8	57	I	Reset input that initializes the internal counters and control registers. $\overline{\text{RESET}}$ initiates the serial data communications, initializes all of the registers to their default values, and puts the device in a preprogrammed state. After a low-going pulse on $\overline{\text{RESET}}$, the device registers are initialized to provide a 16-kHz data-conversion rate and 7.2-kHz filter bandwidth for a 10.368-MHz master clock input signal.
SCLK	13	8	I/O	Shift clock. SCLK clocks the digital data into DIN and out of DOUT during the frame-synchronization interval. When configured as an output (M/$\overline{\text{S}}$ high), SCLK is generated internally by dividing the master clock signal frequency by four. When configured as an input (M/$\overline{\text{S}}$ low), SCLK is generated externally and synchronously to the master clock. This signal clocks the serial data into and out of the device.
SUBS	21	24	I	Substrate connection. SUBS should be tied to ADC GND.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the PM package.

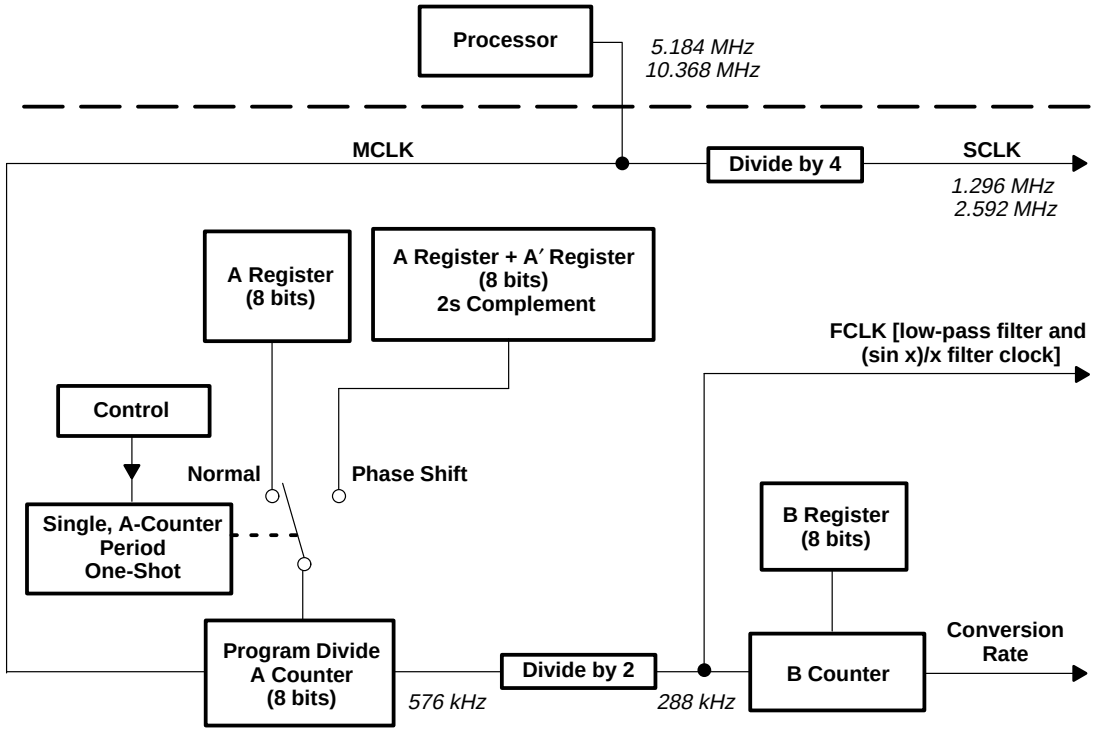


Figure 1–1. Control Flow Diagram

Table 1–1. Operating Frequencies

FCLK (kHz)	LOW-PASS FILTER BANDWIDTH (kHz)	B REGISTER CONTENTS (Program No. of Filter Clocks) (Decimal)	CONVERSION RATE (kHz)	HIGH-PASS POLE FREQUENCY (Hz)
144	3.6	20 (see Note 1)	7.2	36
		18	8	40
		15	9.6	48
		10 (see Note 2)	14.4	72
288	7.2	20 (see Note 1)	14.4	72
		18	16	80
		15	19.2	96
		10 (see Notes 2 and 3)	28.8	144
432	10.8	20 (see Note 1)	21.6	108
		18	24	120
		15 (see Note 3)	28.8	144
		10 (see Notes 2 and 3)	43.2	216

NOTES: 1. The B register can be programmed for values greater than 20; however, since the sample rate is lower than 7.2 kHz and the internal filter remains at 3.6 kHz, an external antialiasing filter is required.
2. When the B register is programmed for a value less than 10, the ADC and the DAC conversions are not completed before the next frame-sync signal and the results are in error.
3. The maximum sampling rate for the ADC channel is 43.2 kHz. The maximum rate for the DAC channel is 25 kHz.

1.5 Register Functional Summary

There are nine data registers that are used as follows:

Register 0 The No-op register. The 0 address allows phase adjustments to be made without reprogramming a data register.

Register 1 The A register controls the count of the A counter.

Register 2 The B register controls the count of the B counter.

Register 3 The A′ register controls the phase adjustment of the sampling period. The adjustment is equal to the register value multiplied by the input master period.

Register 4 The amplifier gain register controls the gains of the input, output, and monitor amplifiers.

Register 5 The analog configuration register controls:

- The addition/deletion of the high-pass filter to the ADC signal path
- The enable/disable of the analog loopback
- The selection of the regular inputs or auxiliary inputs
- The function that allows processing of signals that are the sum of the regular inputs and the auxiliary inputs (V_{IN} + $V_{AUX\ IN}$)

Register 6 The digital configuration register controls:

- Selection of the free-run function
- $\overline{\text{FSD}}$ [frame-synchronization (sync) delay] output enable/disable
- Selection of 16-bit function
- Forcing secondary communications
- Software reset
- Software power down

Register 7 The frame-sync delay register controls the time delay between the master-device frame sync and slave-device frame sync. Register 7 must be the last register programmed when using slave devices since all register data is latched and valid on the sixteenth falling edge of SCLK. On the sixteenth falling edge of SCLK, all delayed frame-sync intervals are shifted by this programmed amount.

Register 8 The frame-sync number register informs the master device of the number of slaves that are connected in the chain. The frame-sync number is equal to the number of slaves plus one.

2 Detailed Description

2.1 Definitions and Terminology

ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT
Codec Mode	The operating mode under which the device receives shift clock and frame-sync signals from a host processor. The device has no slaves.
d	The d represents valid programmed or default data in the control register format (see Section 2.19) when discussing other data-bit portions of the register.
Dxx	Bit position in the primary data word (xx is the bit number)
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUT+ and OUT–
Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks regardless of whether the shift clock is internally or externally generated. The data transfer is initiated by the falling edge of the frame-sync signal.
DSxx	Bit position in the secondary data word (xx is the bit number)
FCLK	An internal clock frequency that is a division of MCLK that controls the low-pass filter and (sinx)/x filter clock (see Figure 1–1 and Table 1-1).
f_i	The analog input frequency of interest
Frame Sync	The falling edge of the signal that initiates the data-transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals
Frame-Sync Interval	The time period occupied by 16 shift clocks. Regardless of the mode of operation, there is always an internal frame-sync interval signal that goes low on the rising edge of SCLK and remains low for 16 shift clocks. It is used for synchronization of the serial-port internal signals. It goes high on the seventeenth rising edge of SCLK.
f_S	The sampling frequency that is the reciprocal of the sampling period.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or $\overline{FS}$.
Master Mode	The operating mode under which the device generates and uses its own shift clock and frame-sync signal and generates all delayed frame-sync signals necessary to support slave devices.
Phase Adjustment	The programmed time variation from the falling edge of one frame-sync signal to the falling edge of the next frame sync signal. The time variation is determined by the contents of the A′ register. Since the time between falling edges of successive frame-sync signals is the the sampling period, the sampling period is adjusted.
Primary (Serial) Communications	The digital data-transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary (Serial) Communications	The digital control and configuration data-transfer interval into DIN and the register read-data cycle from DOUT. The data-transfer interval occurs when requested by hardware or software.
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software-control data.
Slave Mode	The operating mode under which the device receives shift clock and frame-sync signals from a master device.

Stand-Alone Mode	The operating mode under which the device generates and uses its own shift clock and frame-sync signal. The device has no slave devices.
X	The X represents a don't-care bit position within the control register format.

2.2 Reset and Power-Down Functions

2.2.1 Reset

The TLC320AC02 resets both the internal counters and registers, including the programmed registers, by any of the following:

- Applying power to the device, causing a power-on reset (POR)
- Applying a low reset pulse to $\overline{\text{RESET}}$
- Reading in the programmable software reset bit (DS01 in register 6)

$\overline{\text{PWR}}$ $\overline{\text{DWN}}$ resets the counters only and preserves the programmed register contents.

2.2.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are as follows:

1. Counter reset: This signal resets all flip-flops and latches that are not externally programmed with the exception of those generating the reset pulse itself. In addition, this signal resets the software power-down bit.

   Counter reset = power-on reset + $\overline{\text{RESET}}$ + RESET bit + $\overline{\text{PWR}}$ $\overline{\text{DWN}}$

2. Register reset: This signal resets all flip-flops and latches that are not reset by the counter reset except those generating the reset pulse itself.

   Register reset = power-on reset + $\overline{\text{RESET}}$ + RESET bit

Both reset signals are at least one master-clock period long and release on the falling edge of the master clock.

2.2.3 Software and Hardware Power-Down

Given the definitions and conditions of $\overline{\text{RESET}}$, the software-programmed power-down condition is cleared by resetting the software bit (DS00 in register 6) to zero. It is also cleared by either cycling the power to the device, bringing $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ low, or bringing $\overline{\text{RESET}}$ low.

$\overline{\text{PWR}}$ $\overline{\text{DWN}}$ powers down the entire chip (< 1 mA). The software-programmable power-down bit only powers down the analog section of the chip (< 3 mA), which allows a software power-up function. Cycling $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

When $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ is not used, it should be tied high.

2.2.4 Register Default Values After POR, Software Reset, or $\overline{\text{RESET}}$ Is Applied

Register 1 – The A Register

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 2 – The B Register

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 3 – The A′ Register

The default value of the A′-register data is decimal 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 4 – The Amplifier Gain-Select Register

The default value of the amplifier gain-select register data is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

Register 5 – The Analog Control-Configuration Register

The power-up and reset conditions are as shown below. In the read mode, 8 bits are read but the 4 LSBs are repeated as the 4 MSBs.

DS03	DS02	DS01	DS00
0	0	0	1

Register 6 – The Digital Configuration Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 7 – The Frame-Sync Delay Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 8 – The Frame-Sync Number Register

The default value of DS07 – DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

2.3 Master-Slave Terminal Function

Table 2–1 describes the function of the master/slave ($M/\overline{S}$) input. The only difference between master and slave operations in the TLC320AC02 is that SCLK and $\overline{FS}$ are outputs when $M/\overline{S}$ is high and inputs when $M/\overline{S}$ is low.

Table 2–1. Master-Slave Selection

MODE	$M/\overline{S}$†	$\overline{FS}$	SCLK
Master and Stand Alone	H	Output	Output
Slave and Codec Emulation	L	Input	Input

† When the stand-alone mode is desired or when the device is permanently in the master mode, $M/\overline{S}$ must be high.

2.4 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. The signal is amplified by the input amplifier at one of three software-selectable gains (typically 0 dB, 6 dB, or 12 dB). A squelch mode can also be programmed for the input amplifier.

The amplifier output is filtered and applied to the ADC input. The ADC converts the signal into discrete digital words in 2s-complement format corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address and with the read bit set to 1. When a register read is not requested, all 16 bits are 0.

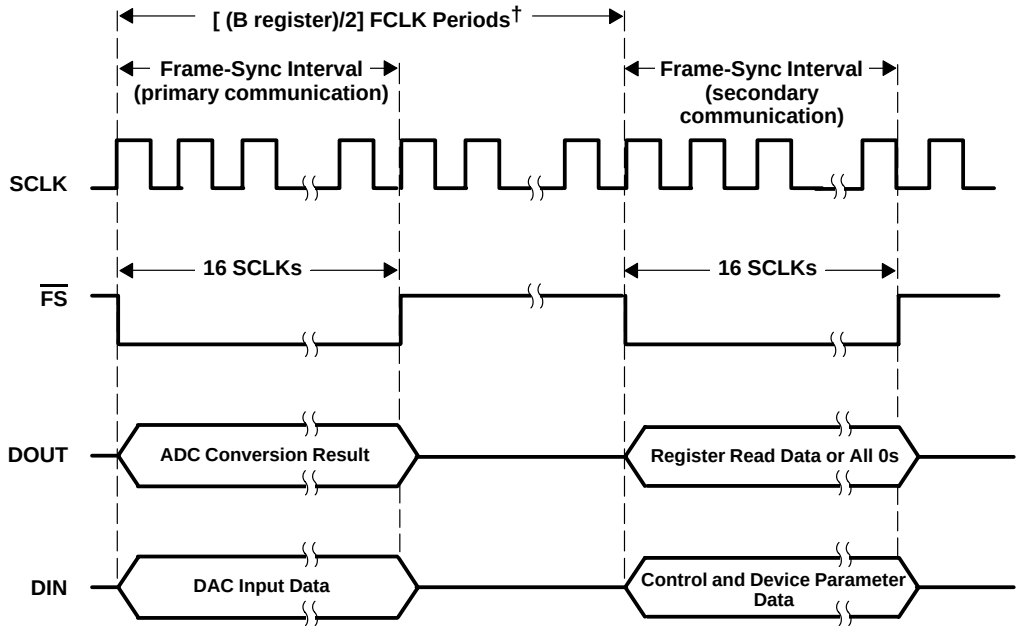
2.5 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC with a sample and hold and then through a (sin x)/x correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, –6 dB, and –12 dB), as shown in register 4, drives the differential outputs OUT+ and OUT–. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.6 Serial Interface

The digital serial interface consists of the shift clock, the frame-synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame-synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a 1. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 2–1.



† The time between the primary and secondary frame sync is the time equal to filter clock (FCLK) period multiplied by the B-register contents divided by two. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–1. Functional Sequence for Primary and Secondary Communication

2.7 Number of Slaves

The maximum number of slaves is determined by the sum of the individual device delays from the frame-sync ($\overline{FS}$) input low to the frame-sync delayed ($\overline{FSD}$) low for all slaves according to equation 1:

$$(n) / tp(FS - FSD) < 1/2 \text{ shift-clock period} \quad (1)$$

Where:

n is the number of slave devices.

Example:

From equation 1 above, the number of slaves is given by equation 2:

$$(n) \leq \frac{1}{2} \times (\text{SCLK period}) \times \frac{1}{tp(FS - FSD)} \quad (2)$$

assuming the master clock is 10.368 MHz and the shift clock is 2.5965 MHz and tp(FS – FSD) is 40 ns, then according to equation 3, the number of slaves is:

$$n \leq \frac{1}{2.5965\ \text{MHz}} \times \frac{1}{2} \times \frac{1}{40\ \text{ns}} = \frac{1000}{192} = 4.8 \quad (3)$$

The maximum number of slaves under these conditions is four.

2.8 Required Minimum Number of MCLK Periods

Master with slave operation is summarized in the following sections.

2.8.1 TLC320AC02 AIC Master-Slave Summary

After initial setup and the master and slave frame syncs are separated, when secondary communication is needed for a slave device, a 11 must be placed in the 2 LSBs of each primary data word for all devices in the system, master and slave, by the host processor. In other words, all AICs must receive secondary frame requests.

The host processor must issue the command by setting D01 and D00 to a 1 in the primary frame sync data word of all devices. Then the master generates the master primary frame sync and, after the number of shift clocks set by the FSD register value, the slave primary frame sync intervals. Then, after (B register value/2) FCLK periods, the master secondary frame sync occurs first, and then the slave secondary frame sync occurs. These are also rippled through the slave devices.

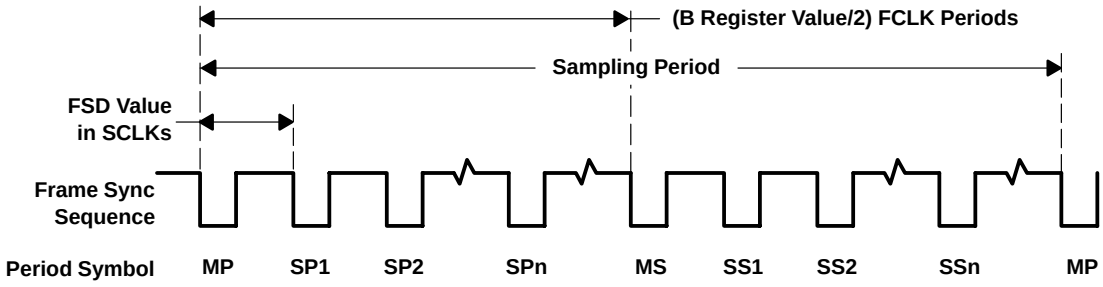
In other words, when a secondary communications interval is requested by the host processor as described above:

1. The master outputs the master primary frame sync interval, and then the slave primary frame sync intervals after the FSD register value number of shift clocks.
2. After (B register value/2) FCLK periods, the master then outputs the master secondary frame sync interval, and after the FSD register value number of shift clocks, the slave secondary frame sync intervals.

This sequence is shown in Figure 2–2.

The host must keep track of whether the master or a slave is then being addressed and also the number of slave devices. The master always outputs a 00 in the last 2 bits of the DOUT word, and a slave always outputs a 1 in the LSB of the DOUT word. This information allows the system to recognize a starting point by interrogating the least significant bit of the DOUT word. If the LSB is 0, then that device is the master, and the system is at the starting point.

Note: This identification always happens except in 16-bit mode when the 2 LSBs are not available for identification purposes.



Periods shown: Each period must be a minimum of 16 SCLKs plus 2 additional SCLKs

MP	**= Master Primary Period**	**MS**	**= Master Secondary Period**
SP1	**= 1st Slave Primary Period**	**SS1**	**= 1st Slave Secondary Period**
SP2	**= 2nd Slave Primary Period**	**SS2**	**= 2nd Slave Secondary Period**
SPn	**= nth Slave Primary Period**	**SSn**	**= nth Slave Secondary Period**

Figure 2–2. Timing Sequence

2.8.2 Notes on TLC320AC01/02 AIC Master-Slave Operation

Master/slave operational detail is summarized in the following notes:

1. The slave devices can be programmed independently of the master as long as the clock divide register numbers are not changed. The gain settings, for example, can be changed independently.

2. The method that is used to program a slave independently is to request a secondary communication of the master and all slaves and ripple the delayed frame sync to the desired slave device to be programmed.

3. Secondary frame syncs must be requested for all devices in the system or none. This is required so that the master generates secondary frames for the slaves and allows the slaves to know that the second frame syncs they receive are secondary frame syncs. Each device in the system must receive a secondary frame request in its corresponding primary frame sync period (11 in the last 2 LSBs).

4. Calculation of the sampling frequency in terms of the master clock and the shift clock and the respective register ratios is (see equations 4–6):

$$\text{Sampling frequency} = f_S = \frac{\text{FCLK}}{\text{B register value}}$$

$$= \frac{\text{f(MCLK)}}{2\ (\text{A register value}) \times (\text{B register value})} \tag{4}$$

Therefore,

$$\frac{\text{f(MCLK)}}{f_S} = 2 \times (\text{A register value}) \times (\text{B register value}) \tag{5}$$

and in terms of the shift clock frequency, since

$$\text{f(MCLK)} = 4 \times \text{f(SCLK)}$$

then

$$\frac{\text{f(SCLK)}}{f_S} = \frac{(\text{A register value}) \times (\text{B register value})}{2}$$

$$= \frac{\text{Number of SCLK periods}}{\text{Sampling period}} \tag{6}$$

5. The minimum number of shift clocks between falling edges of any two frame syncs is 18 because the frame sync delay register minimum number is 18.

   When a secondary communication is requested by the host, the master secondary frame sync begins at the middle of the sampling period (followed by the slave secondary frame syncs), so all primary frame sync intervals (master and slave) must occur within one-half the sampling time.

The first secondary frame-sync falling edge, therefore, occurs at the following time (see equation 7):

$$\text{Time to first secondary frame sync} = \frac{\text{B register value}}{2} \text{ (FCLK periods)} =$$

$$\text{A register value} \times \text{B register value (number of MCLK periods)} =$$

$$\frac{\text{A register value} \times \text{B register value}}{4} \text{ (number of SCLK periods)} \quad (7)$$

6. Number of frame sync intervals using equation 8.

   All master and slave primary frame sync intervals must occur within the time of equation 7.

   Since 18 shift clocks are required for each frame sync interval, then the number of frame sync intervals from equation 8 is:

$$\text{Number of frame sync intervals} = \frac{\text{A register value} \times \text{B register value}}{4 \times 18 \text{ (SCLKs/frame sync interval)}}$$

$$= \frac{\text{A register value} \times \text{B register value}}{72} \quad (8)$$

7. Number of devices, master and slave, in terms of f(MCLK) and f_S.

   Substituting the value from equation 5 for the A × B register value product gives the total number of devices, including the master and all slaves that can be used, for a given master clock and sampling frequency. Therefore, using equation 9:

$$\text{Number of devices} = \frac{\text{f(MCLK)}}{144 \times f_S} \quad (9)$$

8. Number of devices, master and slave, if slave devices are reprogrammed.

   Equation 9 does not include reprogramming the slave devices after the frame sync delay occurs. So if programming is required after shifting the slave frame syncs by the FSD register, then the total number of devices is given by equation 10 is:

$$\text{Number of devices} = \frac{\text{f(MCLK)}}{288 \times f_S} \quad (10)$$

9. Example of the maximum number of devices if the slave devices are reprogrammed assuming the following values:

   $\text{f(MCLK)} = 10.368 \text{ MHz}, \ f_S = 8 \text{ kHz}$

   then from equation 10,

$$\text{Maximum number of devices} = \frac{10.368 \text{ MHz}}{288 \text{ (8 kHz)}} = 4.5$$

   therefore, one master and three slaves can be used.

2.9 Operating Frequencies

2.9.1 Master and Stand-Alone Operating Frequencies

The sampling (conversion) frequency is derived from the master-clock (MCLK) input by equation 11:

$$f_S = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{(\text{A register value}) \times (\text{B register value}) \times 2} \quad (11)$$

The inverse is the time between the falling edges of two successive primary frame-synchronization signals. The input and output data clock (SCLK) frequency is given in equation 12:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{4} \quad (12)$$

2.9.2 Slave and Codec Operating Frequencies

The slave operating frequencies are either the default values or programmed by the control data word from the master and codec conversion and the data frequencies are determined by the externally applied SCLK and $\overline{FS}$ signals.

2.10 Switched-Capacitor Filter Frequency (FCLK)

The filter clock (FCLK) is an internal clock signal that determines the filter band-pass frequency and is the B counter clock. The frequency of the filter clock is derived by equation 13:

$$\text{FCLK} = \frac{\text{MCLK}}{(\text{A register value}) \times 2} \quad (13)$$

2.11 Filter Bandwidths

The low-pass (LP) filter –3 dB corner is derived in equation 14:

$$f\ (\text{LP}) = \frac{\text{FCLK}}{40} = \frac{\text{MCLK}}{40 \times (\text{A register value}) \times 2} \quad (14)$$

The high-pass (HP) filter –3 dB corner is derived in equation 15:

$$f\ (\text{HP}) = \frac{\text{Sampling frequency}}{200} = \frac{\text{MCLK}}{200 \times 2 \times (\text{A register value}) \times (\text{B register value})} \quad (15)$$

2.12 Master and Stand-Alone Modes

The difference between the master and stand-alone modes is that in the stand-alone mode there are no slave devices. Functionally these two modes are the same. In both, the AIC internally generates the shift clock and frame-sync signal for the serial communications. These signals and the filter clock (FCLK) are derived from the input master clock.The master clock applied at the MCLK input determines the internal device timing. The shift clock frequency is a divide-by-four of the master clock frequency and shifts both the input and output data at DIN and DOUT, respectively, during the frame-sync interval (16 shift clocks long). To begin the communication sequence, the device is reset (see Section 2.2.1), and the first frame sync occurs approximately 648 master clocks after the reset condition disappears.

2.12.1 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the sixteenth falling edge of SCLK. After a reset condition, eight primary and secondary communications cycles are required to set up the eight programmable registers. Registers 1 through 8 are programmed in secondary communications intervals 1 through 8, respectively. If the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during this communications. The no-op command allows phase shifts of the sampling period without reprogramming any register.

During the eight register programming cycles, DOUT is in the high-impedance state. DOUT is released on the rising edge of the eighth primary internal frame-sync interval. In addition, each register can be read back

during DOUT secondary communications by setting the read bit to 1 in the appropriate register. Since the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication (see Section 2.19 for detailed register description).

2.12.2 Master and Stand-Alone Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the filter clock (FCLK). The B counter is clocked by FCLK with the following functional sequence:

1. The B counter starts counting down from the B register value minus one. Each count remains in the counter for one FCLK period including the zero count. This total counter time is referred to as the B cycle. The end of the zero count is called the end of B cycle.
2. When the B counter gets to a count of nine, the analog-to-digital (A-to-D) conversion starts.
3. The A-to-D conversion is complete ten FCLK periods later.
4. $\overline{\text{FS}}$ goes low on a rising edge of SCLK after the A-to-D conversion is complete. That rising edge of SCLK must be preceded by a falling edge of SCLK, which is the first falling edge to occur after the end of B cycle.
5. The D-to-A conversion cycle begins on the rising edge of the internal frame-sync interval and is complete ten FCLK periods later.

2.13 Slave and Codec Modes

The only difference between the slave and codec modes is that the codec mode is controlled directly by the host and does not use a delayed frame-sync signal. In both modes, the shift clock and the frame sync are both externally generated and must be synchronous with MCLK. The conversion frequency is set by the time interval of externally applied frame-sync falling edges except when the free-run function is selected by bit 5 of register 6 (see Section 2.15.4). The slave device or devices share the shift clock generated by the master device but receive the frame sync from the previous slave in the chain. The Nth slave $\overline{\text{FS}}$ receives the (N–1)st slave $\overline{\text{FSD}}$ output and so on. The first slave device in the chain receives $\overline{\text{FSD}}$ from the master.

2.13.1 Slave and Codec Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the FCLK. The device function in the slave or codec mode is the same as steps 1 through 3 of the B cycle description in the master mode but differs as follows:

1. Same as master
2. Same as master
3. Same as master
4. All internal clocks stop 1/2 FCLK before the end of count 0 in the B counter cycle.
5. All internal clocks are restarted on the first rising edge of MCLK after the external $\overline{FS}$ input goes low. This operation provides the synchronization necessary when using an external $\overline{FS}$ signal.
6. The D-to-A conversion starts on the rising edge of the internally generated frame-sync interval at the end of the 16-shift clock data transfer.

In the slave mode, the master controls the phase adjustments for itself and all slaves since all devices are programmed in the same frame-sync interval. In the codec mode, the shift clock and frame sync are externally generated and provide the timing for the ADC and DAC if the free-run function has not been selected (see Subsection 2.15.4). In the codec mode, there is usually no need for phase adjustments; however, any required phase adjustments must be made by adjusting the external frame-sync timing (sampling time).

2.13.2 Slave Register Programming

When slave devices are used on power-up or reset, all slave frame-sync signals occur at the same time as the master frame-sync signal and all slave devices are programmed during the master secondary frame-sync interval with the same data as the master. The last register programmed must be the frame-sync delay (FSD) register because the delay starts immediately on the rising edge of the seventeenth shift clock of that frame- sync interval. After the FSD register programming is completed for the master and slave, the slave primary frame interval is shifted in time (time slot allocated) according to the data contained in the slave FSD registers. The master then generates frame-sync intervals for itself and each slave to synchronize the host serial port for data transfers for itself and all slave devices.

The number of slaves is specified in the FSN register (register 8); therefore, the number of frame-sync intervals generated by the master is equal to the number of slaves plus one (see Section 2.7). These master frame-sync intervals are separated in time by the delay time specified by the FSD register (register 7). These master-generated intervals are the only frame-sync interval signals applied to the host serial port to provide the data-transfer time slot for the slave devices.

2.14 Terminal Functions

2.14.1 Frame-Sync Function

The frame-sync signal indicates that the device is ready to send and receive data for both master and slave modes. The data transfer begins on the falling edge of the frame-sync signal.

2.14.1.1 Frame Sync ($\overline{FS}$), Master Mode

The frame sync is generated internally. $\overline{FS}$ goes low on the rising edge of SCLK and remains low for the 16-bit data transfer. In addition to generating its own frame-sync interval, the master also outputs a frame sync for each slave that is being used.

2.14.1.2 Frame-Sync Delayed ($\overline{\text{FSD}}$), Master Mode

For the master, the frame-sync delayed output occurs 1/2 shift-clock period ahead of $\overline{\text{FS}}$ to compensate for the time delay through the master and slave devices. The timing relationships are as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low on the falling edge of SCLK prior to the rising edge of SCLK when $\overline{\text{FS}}$ goes low (see Figure 4–4).
2. When the FSD register data is greater than 17, then $\overline{\text{FSD}}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Register data values from 1 to 17 should not be used.

2.14.1.3 Frame Sync ($\overline{\text{FS}}$), Slave Mode

The frame-sync timing is generated externally, applied to $\overline{\text{FS}}$, and controls the ADC and DAC timing (see Subsection 2.15.4). The external frame-sync width must be a minimum of one shift clock to be recognized and can remain low until the next data frame is required.

2.14.1.4 Frame-Sync Delayed ($\overline{\text{FSD}}$), Slave Mode

This output is fed from the master to the first slave and the first slave $\overline{\text{FSD}}$ output to the second and so on down the chain. The FSD timing sequence in the slave mode is as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low after $\overline{\text{FS}}$ goes low (see Figure 4–5).
2. When the FSD register data is greater than 17, $\overline{\text{FSD}}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Data values from 1 to 17 should not be used.

2.14.2 Data Out (DOUT)

DOUT is placed in the high-impedance state on the seventeenth rising edge of SCLK (internal or external) after the falling edge of frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/$\overline{\text{W}}$) bit with the eight MSBs set to 0 (see Section 2.16). If no register read is requested, the secondary word is all zeroes.

2.14.2.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of frame sync. The most significant data bit then appears on DOUT.

2.14.2.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the external frame sync or the rising edge of the external SCLK, whichever occurs first (see Figure 4–7). The falling edge of frame sync can occur $\pm$1/4 SCLK period around the SCLK rising edge (see Figure 4–3). The most significant data bit then appears on DOUT.

2.14.3 Data In (DIN)

In the primary communication, the data word is the digital input signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 2.16).

2.14.4 Hardware Program Terminals (FC1 and FC0)

These inputs provide for hardware programming requests for secondary communication or phase adjustment. These inputs work in conjunction with the control bits D01 and D00 of the primary data word or control bits DS15 and DS14 of the secondary data word. The data on FC1 and FC0 are latched on the rising edge of the next internally generated primary or secondary frame-sync interval. These inputs should be tied low if not used (see Section 2.17 and Table 2–3).

2.14.5 Midpoint Voltages (ADC V_{MID} and DAC V_{MID})

Since the device operates at a single-supply voltage, two midpoint voltages are generated for internal signal processing. ADC V_{MID} is used for the ADC channel reference, and DAC V_{MID} is used for the DAC channel reference. Two references minimize channel-to-channel noise and crosstalk. ADC V_{MID} and DAC V_{MID} must be buffered when used as a reference for external signal processing.

2.15 Device Functions

2.15.1 Phase Adjustment

In some applications, such as modems, the device sampling period may require an adjustment to synchronize with the incoming bit stream to improve the signal-to-noise ratio. The TLC320AC02 can adjust the sampling period through the use of the A′ register and the control bits.

2.15.1.1 Phase-Adjustment Control

A phase adjustment is a programmed variation in the sampling period. A sampling period is adjusted according to the data value in the A′ register, and the phase adjustment is that number of master clocks (MCLK). An adjustment is made during device operation with data bits D01 and D00 in the primary communication, with data bits DS15 and DS14 in the secondary word or in combination with the hardware terminals FC1 and FC0 (see Table 2–3). This adjustment request is latched on the rising edge of the next internal frame-sync interval and is only valid for the next sampling period. To repeat the phase adjustment, another phase request must be initiated.

2.15.1.2 Use of the A′ Register for Phase Adjustment

The A′ register value makes slight timing adjustments to the sampling period. The sampling period increases or decreases according to the sign of the programmed A′ register value and the state of data bits D01 and D00 in the primary data word.

The general equation for the conversion frequency is given in equation 16:

$$f_S = \text{conversion frequency} = \frac{\text{MCLK}}{(2 \times \text{A register value} \times \text{B register value}) \pm (\text{A}' \text{ register value})} \quad (16)$$

Therefore, if A′ = 0, the device conversion (sampling) frequency and period is constant.

If a nonzero A′ value is programmed, the sampling frequency and period responds as shown in Table 2–2.

Table 2–2. Sampling Variation With A′

D01	D00	SIGN OF THE A′ REGISTER VALUE	
		PLUS VALUE (+)	NEGATIVE VALUE (–)
0	1 (increase command)	Frequency decreases, period increases	Frequency increases, period decreases
1	0 (decrease command)	Frequency increases, period decreases	Frequency decreases, period increases

An adjustment to the sampling period, which must be requested through D01 and D00 of the primary data word to DIN, is valid for the following sampling period only. When the adjustment is required for the subsequent sampling period, it must be requested again through D01 and D00 of the primary data word. For each request, only the sampling period occurring immediately after the primary data word request is affected.

The amount of time shift in the entire sampling period ($1/f_S$) is as follows:

When the sampling period is set to 125 μs (8 kHz), the A′ register is loaded with decimal 10 and the TLC320AC02 master clock frequency is 10.386 MHz. The amount of time each sampling period is increased or decreased, when requested, is given in equation 17:

$$\text{Time shift} = (\text{A}' \text{ register value}) \times (\text{MCLK period}) \quad (17)$$

The device changes the entire sampling period by only the MCLK period times the A′ register value as given in equation 18:

$$\begin{aligned}\text{Change in sampling period} &= \text{contents of A}' \text{ register} \times \text{master clock period} \\ &= 10 \times 96.45 \text{ ns} = 964 \text{ ns (less than 1\% of the sampling period)}\end{aligned} \quad (18)$$

The sampling period changes by 964.5 ns each time the phase adjustment is requested by the primary data word (i.e., once per sampling period).

It is evident then that the change in sampling period is very small compared to the sampling period. To observe this effect over a long period of time (> sampling period), this change must be continuously requested by the primary data word. If the adjustment is not requested again, the sampling period changes only once and it may appear that there was no execution of the command. This is especially true when bench testing the device. Automatic test equipment can test for results within a single sampling period.

Internally, the A′ register value only affects one cycle (period) of the A counter. The A and A′ values are additive, but only for one A-counter period. The A counter begins the first count at the default or programmed A-register value and counts down to the A′-register value. As the A′ value increases or decreases, the first clock cycle from the A counter is lengthened or shortened. The initial A-counter period is the only counter period affected by the A′ register such that only this single period is increased or decreased.

2.15.2 Analog Loopback

This function allows the circuit to be tested remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. The DAC data bits D15 to D02 that are applied to DIN can be compared with the ADC output data bits D15 to D02 at DOUT. There are some differences due to the ADC and DAC channel offset. The loopback function is implemented by setting DS01 and DS00 to zero in control register 5 (see Section 2.19). When analog loopback is enabled, the external inputs to IN+ and IN– are disconnected, but the signals at OUT+ and OUT– may still be read.

2.15.3 16-Bit Mode

In the 16-bit mode, the device ignores the last two control bits (D01 and D00) of the primary word and requests continual secondary communications to occur. By ignoring the last two primary communication bits, compatibility with existing 16-bit software can be maintained. This function is implemented by setting bit DS03 to 1 in register 6. To return to normal operation, DS03 must be reprogrammed to 0.

2.15.4 Free-Run Mode

With the free-run bit set in register 6, the external shift clock and frame sync control only the data transfer. The ADC and DAC timing are controlled by the A and B register values, and the phase-shift adjustment must be done as if the device is in stand-alone mode (by the software or the state of FC1 and FC0).

Phase adjustment cannot be made by adjustment of the frame-sync timing. The external frame sync must occur within 1/2 FCLK period of the internal frame sync (FCLK as determined by the values of the A and B registers).

When the external frame sync occurs simultaneously with the internal load, the data-transfer request by the external frame sync takes precedence over an internal load command. The latching of the ADC conversion data in the output register is inhibited until the current 16 bits are shifted out of the register by the shift clock.

2.15.5 Force Secondary Communication

With bit 2 in register 6 set to 1, secondary communication is requested continuously. It overrides all software and hardware requests concerning secondary communication. Phase shifting, however, can still be performed with the software and hardware.

2.15.6 Enable Analog Input Summing

By setting bits DS01 and DS00 to 11 in register 5, the normal analog input voltage is summed with the auxiliary input voltage. The gain for the analog input amplifier is set by data bits DS03 and DS02 in register 4.

2.15.7 DAC Channel (sin x)/x Error Correction

The (sin x)/x compensation filter is designed for zero (sin x)/x error using a B-register value of 15. Since the filter cannot be removed from the signal path, operation using another B-register value results in an error in the reconstructed analog output. The error is given by equation 19. Any error compensation needed by a given application can be performed in the software.

$$\text{DAC channel frequency response error} = 20 \times \log_{10}\left[\frac{\sin\left(\frac{2\pi \times A \times B}{f_{MCLK}} \times f\right)}{\sin\left(\frac{30\pi \times A}{f_{MCLK}} \times f\right)} \times \frac{15}{B}\right] \quad (19)$$

where:

f = the frequency of interest
f_{MCLK} = the TLC320AC02 master-clock frequency
A = the A-register value
B = the B-register value

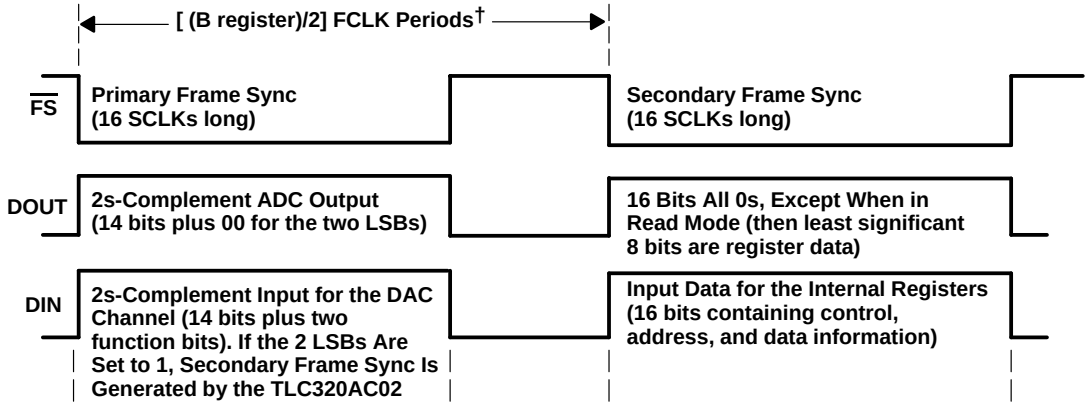
and the arguments of the sin functions are in radians.

2.16 Serial Communications

2.16.1 Stand-Alone and Master-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the stand-alone and master modes, the sequence in Figure 2–2 shows the relationship between the primary and secondary communications interval, the data content into DIN, and the data content from DOUT.

The TLC320AC02 can provide a phase-shift command or the next secondary communications interval by decoding 1) the programmed state of the FC1 and FC0 inputs and the D01 and D00 data bits in the primary data word, or 2) the state of the FC1 and FC0 inputs and the DS15 and DS14 data bits in the secondary data word (see Table 2–3). When DS13 (the R/$\overline{W}$ bit) is the default value of 0, all 16 bits from DOUT are 0 during secondary communication. However, when the R/$\overline{W}$ bit is set to 1 in the secondary communication control word, the secondary transmission from DOUT still contains 0s in the eight MSBs. The lower order 8 bits contain the data of the register currently being addressed. This function provides register status information for the host.

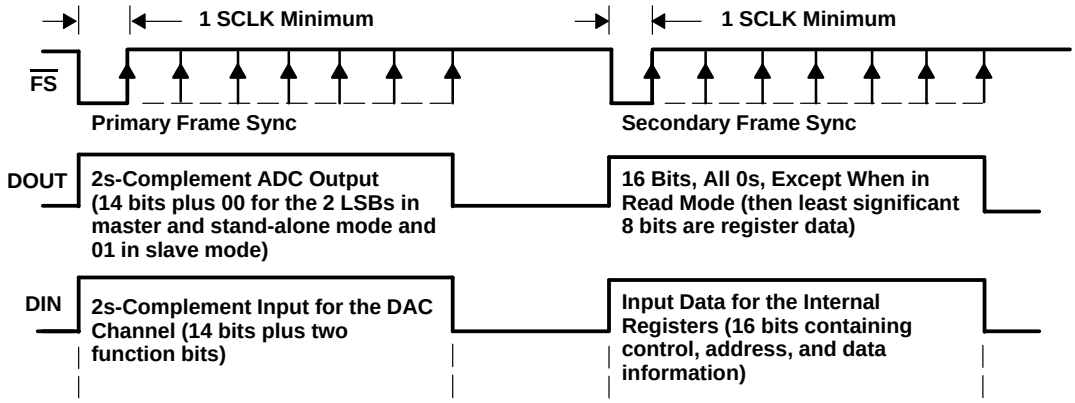


† The time between the primary and secondary frame sync is the time equal to filter clock (FCLK) period multiplied by the B-register contents divided by two. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–3. Master and Stand-Alone Functional Sequence

2.16.2 Slave and Codec-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the slave and codec modes, the sequence is basically the same as the stand-alone and master modes with the exception that the frame sync and the shift clock are generated and controlled externally as shown in Figure 2–3. For the codec mode, the frame-sync pulse width needs to be a minimum of one shift clock long. The timing relationship between the frame sync and shift clock is shown in the timing diagrams. Phase shifting is usually not required in the slave or codec mode because the frame-sync timing can be adjusted externally if required.



NOTE A: The time between the primary and secondary frame syncs is determined by the application; however, enough time must be provided so that the host can execute the required number of software instructions in the time between the end of the primary data transfer (rising edge of the primary frame-sync interval) and the falling edge of the secondary frame sync (start of secondary communications).

Figure 2–4. Slave and Codec Functional Sequence

2.17 Request for Secondary Serial Communication and Phase Shift

The following paragraphs describe a request for secondary serial communication and phase shift using hardware control inputs FC1 and FC0, primary data bits D01 and D00, and secondary data bits DS15 and DS14.

2.17.1 Initiating a Request

Combinations of FC1 and FC0 input conditions, bits D01 and D00 in the primary serial data word, FC1 and FC0, and bits DS15 and DS14 in the secondary serial data word can initiate a secondary serial communication or request a phase shift according to the following rules (see Table 2–3).

1. Primary word phase shifts can be requested by either the hardware or software when the other set of signals are 11 or 00. If both hardware and software request phase shifts, the software request is performed.
2. Secondary words can be requested by either the software or hardware at the same time that the other set of signals is requesting a phase shift.
3. Hardware inputs FC1 and FC0 are ignored during the secondary word unless DS15 and DS14 are 11. When DS15 and DS14 are 01 or 10, the corresponding phase shift is performed. When DS15 and DS14 are 00, no phase shift is performed even when the hardware requests a phase shift.

2.17.2 Normal Combinations of Control

The normal combinations of control are as follows:

1. Use D01 and D00 and DS15 and DS14 to request phase shifts and secondary words by holding FC1 and FC0 to 00.
2. Use FC1 and FC0 exclusively to request phase shifts and secondary words by holding D01 and D00 to 00 and DS15 and DS14 to 11.
3. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts once per period by holding DS15 and DS14 to 00.

2.17.3 Additional Control Options

Additional control options are unusual and are rarely needed or used; however, they are as follows:

1. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts twice per period by holding DS15 and DS14 to 11.
2. Use FC1 and FC0 exclusively to request secondary words and D01 and D00 and DS15 and DS14 to perform phase shifts twice per period.
3. Use FC1 and FC0 to perform the phase shift after the primary word and DS15 and DS14 to perform a phase shift after the secondary word by holding D01 and D00 to 11.

Table 2–3. Software and Hardware Requests for Secondary Serial-Communication and Phase-Shift Truth Table

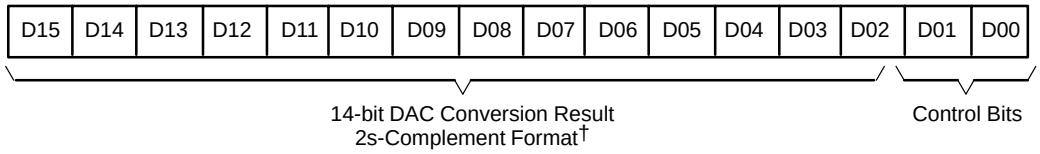
WITHIN PRIMARY OR SECONDARY DATA WORD	CONTROL BITS		HARDWARE TERMINALS		PHASE-SHIFT ADJUSTMENT (see Section 2.15.1)		SECONDARY REQUEST (see Note 1)
	D01	D00	FC1	FC0	EARLIER	LATER	
Primary	0	0	0	0	0	0	0
	0	0	0	1	0	1	0
	0	0	1	0	1	0	0
	0	0	1	1	0	0	1
	0	1	0	0	0	1	0
	0	1	0	1	0	1	0
	0	1	1	0	0	1	0
	0	1	1	1	0	1	1
	1	0	0	0	1	0	0
	1	0	0	1	1	0	0
	1	0	1	0	1	0	0
	1	0	1	1	1	0	1
	1	1	0	0	0	0	1
	1	1	0	1	0	1	1
	1	1	1	0	1	0	1
	1	1	1	1	0	0	1
Secondary	DS15	DS14	FC1	FC0	EARLIER	LATER	No request can be made for secondary communication within the secondary word.
	0	0	0	0	0	0	
	0	0	0	1	0	0	
	0	0	1	0	0	0	
	0	0	1	1	0	0	
	0	1	0	0	0	1	
	0	1	0	1	0	1	
	0	1	1	0	0	1	
	0	1	1	1	0	1	
	1	0	0	0	1	0	
	1	0	0	1	1	0	
	1	0	1	0	1	0	
	1	0	1	1	1	0	
	1	1	0	0	0	0	
	1	1	0	1	0	1	
	1	1	1	0	1	0	
	1	1	1	1	0	0	

NOTE 1: The 0 state indicates that a secondary communication is not being requested. The 1 state indicates that a secondary communication is being requested.

2.18 Primary Serial Communications

Primary serial communications transfer the 14-bit DAC input plus two control bits (D01 and D00) to DIN of the TLC320AC02.They simultaneously transfer the 14-bit ADC conversion result from DOUT to the processor. The 2 LSBs are set to 0 in the ADC result.

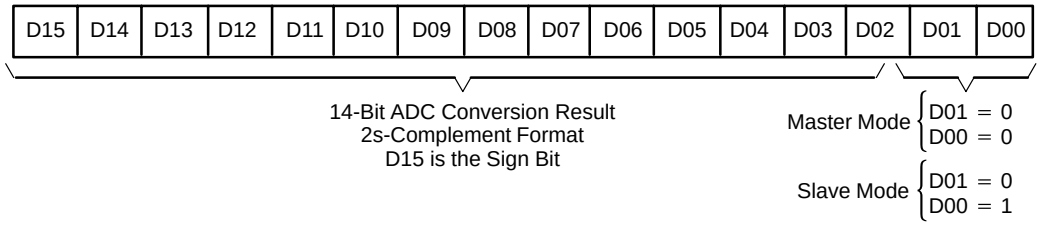
2.18.1 Primary Serial Communications Data Format



† Since the supply voltage is single ended, the reference for 2s-complement format is ADC V_{MID}. Voltages above this reference have a 0 as the MSB, and voltages below this reference have a 1 as the MSB.

During primary serial communications, when D01 and D00 are both high in the DAC data word to DIN, a subsequent 16 bits of control information is received by the device at DIN during a secondary serial-communication interval. This secondary serial-communication interval begins at 1/2 the programmed conversion time when the B register data value is even or 1/2 the programmed value minus one FCLK when the B register data value is odd. The time between primary and secondary serial communication is measured from the falling edge of the primary frame sync to the falling edge of the secondary frame sync (see Section 2.19 for function and format of control words).

2.18.2 Data Format From DOUT During Primary Serial Communications



2.19 Secondary Serial Communications

2.19.1 Data Format to DIN During Secondary Serial Communications

There are nine 16-bit configuration and control registers numbered from zero to eight. All register data contents are represented in 2s-complement format. The general format of the commands during secondary serial communications is as follows.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits (2 bits)		R/$\overline{W}$ Bit	Register Address (5 bits)					Register Data Value (8 bits)							

All control register words are latched in the register and valid on the sixteenth falling edge of SCLK.

2.19.2 Control Data-Bit Function in Secondary Serial Communication

2.19.2.1 DS15 and DS14

In the secondary data word, bits DS15 and DS14 perform the same control function as the primary control bits D01 and D00 do in the primary data word.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	Register Address					Register Data							

Hardware terminals FC1 and FC0 are valid inputs when DS15 and DS14 are both high, and they are ignored for all other conditions.

2.19.2.2 DS13 (R/$\overline{W}$ Bit)

Reset and power-up procedures set this bit to a 0, placing the device in the write mode. When this bit is set to 1, however, the previous data content of the register being addressed is read out to the host from DOUT as the least significant 8 bits of the 16-bit secondary word. The first 8 bits remain set to 0. Reading the data out is nondestructive, and the contents of the register remain unchanged.

A. Write Mode (DS13 = 0)

Data In. The data word to DIN has the following general format in the write mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		0	Register Address					Register Data							

Data Out. The shift clock shifts out all 0s as the pattern to the host from DOUT.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B. Read Mode (DS13 = 1)

Data In. The data word to DIN has the following format to allow a register read. Phase shifts can also be done in the read mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		1	Register Address					Ignored							

Data Out. The shift clock clocks out the data of the register addressed from DOUT in the read mode in the 8 LSBs.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	Register Data							

2.20 Internal Register Format

2.20.1 Pseudo-Register 0 (No-Op Address)

This address represents a no-operation command. No register I/O operation takes place, so the device can receive secondary commands for phase adjustment without reprogramming any register. A read of the no-op is 0. The format of the command word is as follows:

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		X	0	0	0	0	0	X	X	X	X	X	X	X	X

2.20.2 Register 1 (A Register)

The following command loads DS07 (MSB) – DS00 into the A register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	0	1	Register Data							

The data in DS07 – DS00 determines the division of the master clock to produce the internal FCLK.

FCLK frequency = MCLK/(A register contents $\times$ 2)

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.3 Register 2 (B Register)

The following command loads DS07 (MSB) – DS00 into the B register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	1	0	Register Data							

The data in DS07 – DS00 controls the division of FCLK to generate the conversion clock as given in equation 20:

$$\text{Conversion frequency} = \text{FCLK}/(\text{B register contents}) = \frac{\text{MCLK}}{2 \times \text{A register contents} \times \text{B register contents}} \quad (20)$$

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.4 Register 3 (A′ Register)

The following command contains the A′-register address and loads DS07(MSB) – DS00 into the A′ register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	1	1	Register Data							

The data in DS07 – DS00 is in 2s-complement format and controls the number of master-clock periods that the sampling time is shifted.

The default value of the A′-register data is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.5 Register 4 (Amplifier Gain-Select Register)

The following command contains the amplifier gain-select register address with selection code for the monitor output (DS05–DS04), analog input (DS03–DS02), and analog output (DS01–DS00) programmable gains.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	0	0	X	X	*	*	*	*	*	*
Monitor output gain = squelch →										0	0				
Monitor output gain = 0 dB →										0	1				
Monitor output gain = –8 dB →										1	0				
Monitor output gain = –18 dB →										1	1				
Analog input gain = squelch →												0	0		
Analog input gain = 0 dB →												0	1		
Analog input gain = 6 dB →												1	0		
Analog input gain = 12 dB →												1	1		
Analog output gain = squelch →														0	0
Analog output gain = 0 dB →														0	1
Analog output gain = –6 dB →														1	0
Analog output gain = –12 dB →														1	1

The default value of the monitor output gain is squelch, which corresponds to data bits DS05 and DS04 equal to 00 (binary).
The default value of the analog input gain is 0 dB, which corresponds to data bits DS03 and DS02 equal to 01 (binary).
The default value of the analog output gain is 0 dB, which corresponds to data bits DS01 and DS00 equal to 01 (binary).

The default data value is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

2.20.6 Register 5 (Analog Configuration Register)

The following command loads the analog configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	0	1	X	X	X	X	*	*	*	*
Must be set to 0 →												0			
High-pass filter disabled →													1		
High-pass filter enabled →													0		
Analog loopback enabled →														0	0
Enables IN+ and IN– (disables AUXIN+ and AUXIN–) →														0	1
Enables AUXIN+ and AUXIN– (disables IN+ and IN–) →														1	0
Enable analog input summing →														1	1

The default value of the high-pass-filter enable bit is 0, which places the high-pass filter in the signal path. The default values of DS01 and DS00 are 0 and 1 which enables IN+ and IN–.

The power-up and reset conditions are as shown below.

DS03	DS02	DS01	DS00
0	0	0	1

In the read mode, eight bits are read but the 4 LSBs are repeated as the 4 MSBs.

2.20.7 Register 6 (Digital Configuration Register)

The following command loads the digital configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	1	0	X	X	*	*	*	*	*	*
ADC and DAC conversion free run → / Inactive →										1 / 0					
$\overline{FSD}$ output disable → / Enable →											1 / 0				
16-Bit mode, ignore primary LSBs → / Normal operation →												1 / 0			
Force secondary communications → / Normal operation →													1 / 0		
Software reset → (upon reset, this bit is automatically reset to 0) / Inactive reset →														1 / 0	
Software power-down active (automatically reset to 0 after PWR DWN is cycled high to low and back to high) →															1
Power-down function external (uses PWR DWN) →															0

The default value of DS07–DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.8 Register 7 (Frame-Sync Delay Register)

The following command contains the frame-sync delay (FSD) register address and loads DS07 (MSB)–DS00 into the FSD register. The data byte (DS01–DS00) determines the number of SCLKs between $\overline{FS}$ and the delayed frame-sync signal, $\overline{FSD}$. The minimum data value for this register is decimal 18.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	1	1	Register Data							

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

When using a slave device, register 7 must be the last register programmed.

2.20.9 Register 8 (Frame-Sync Number Register)

The following command contains the frame-sync number (FSN) register address and loads DS07 (MSB)–DS00 into the FSN register. The data byte determines the number of frame-sync signals generated by the TLC320AC02. This number is equal to the number of slaves plus one.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	1	0	0	0	Register Data							

The default value of DS07–DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DGTL V_{DD} (see Notes 1 and 2) . . . . . −0.3 V to 6.5 V
Supply voltage range, DAC V_{DD} (see Notes 1 and 2) . . . . . −0.3 V to 6.5 V
Supply voltage range, ADC V_{DD} (see Notes 1 and 2) . . . . . −0.3 V to 6.5 V
Differential supply voltage range, DGTL V_{DD} to DAC V_{DD} . . . . . −0.3 V to 6.5 V
Differential supply voltage range, all positive supply voltages to
ADC GND, DAC GND, DGTL GND, SUBS . . . . . −0.3 V to 6.5 V
Output voltage range, DOUT . . . . . −0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range, DIN . . . . . −0.3 V to DGTL V_{DD} + 0.3 V
Ground voltage range, ADC GND, DAC GND,
DGTL GND, SUBS . . . . . −0.3 V to DGTL V_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage	4.5	5	5.5	V
	Steady-state differential voltage between any two supplies			0.1	V
V_{IH}	High-level digital input voltage	2.2			V
V_{IL}	Low-level digital input voltage			0.8	V
I_O	Load output current from ADC V_{MID} and DAC			100	µA
	Conversion time for the ADC and DAC channels	10 FCLK periods			
f_{MCLK}	Master-clock frequency		10.368	15	MHz
$V_{ID(PP)}$	Analog input voltage (differential, peak to peak)		6		V
R_L	Differential output load resistance	600			Ω
	Single-ended to buffered DAC V_{MID} voltage load resistance	300			
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values for DGTL V_{DD} are with respect to DGTL GND, voltage values for DAC V_{DD} are with respect to DAC GND, and voltage values for ADC V_{DD} are with respect to ADC GND. For the subsequent electrical, operating, and timing specifications, the symbol V_{DD} denotes all positive supplies. DAC GND, ADC GND, DGTL GND, and SUBS are at 0 V unless otherwise specified.

2. To avoid possible damage to these CMOS devices and associated operating parameters, the sequence below should be followed when applying power:
   (1) Connect SUBS, DGTL GND, ADC GND, and DAC GND to ground.
   (2) Connect voltages ADC V_{DD},and DAC V_{DD}.
   (3) Connect voltage DGTL V_{DD}.
   (4) Connect the input signals.
   When removing power, follow the steps above in reverse order.

3.3 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, MCLK = 5.184 MHz, V_{DD} = 5 V, Outputs Unloaded, Total Device

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{DD}	Supply current	$\overline{PWR}$ $\overline{DWN}$ = 1 and clock signals present		20	22	mA
		$\overline{PWR}$ $\overline{DWN}$ = 0 after 500 µs and clock signals present		1	2	mA
P_D	Power dissipation	$\overline{PWR}$ $\overline{DWN}$ = 1 and clock signals present		100		mW
		$\overline{PWR}$ $\overline{DWN}$ = 0 after 500 µs and clock signals present		5		mW
		Software power down, (bit D00, register 6 set to 1)		15	20	mW
ADC V_{MID}	Midpoint voltage	No load	ADC $V_{DD}/2$ −0.1		ADC $V_{DD}/2$ +0.1	V
DAC V_{MID}	Midpoint voltage	No load	DAC $V_{DD}/2$ −0.1		DAC $V_{DD}/2$ +0.1	V

3.4 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, Digital I/O Terminals (DIN, DOUT, EOC, FC0, FC1, $\overline{FS}$, $\overline{FSD}$, MCLK, M/$\overline{S}$, SCLK)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to DGTL V_{DD}			10	µA
I_{IL}	Low-level input current, any digital input	V_I = 0 V to 0.8 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

3.5 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, ADC and DAC Channels

3.5.1 ADC Channel Filter Transfer Function, FCLK = 144 kHz, f_s = 8 kHz

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 3)	f_i = 50 Hz		−2	dB
	f_i = 200 Hz	−1.8	−0.2	
	f_i = 300 Hz to 3 kHz	−0.15	0.2	
	f_i = 3.3 kHz	−0.35	0.03	
	f_i = 3.4 kHz	−1	−0.1	
	f_i = 4 kHz		−14	
	$f_i \geq$ 4.6 kHz		−32	

NOTE 3: The differential analog input signals are sine waves at 6 V peak to peak. The reference gain is at 1020 Hz.

3.5.2 ADC Channel Input, V_{DD} = 5 V, Input Amplifier Gain = 0 dB (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage (see Note 4)	Single-ended		3		V
		Differential		6		V
	ADC converter offset error	Band-pass filter selected		10	30	mV
CMRR	Common-mode rejection ratio at IN+, IN–, AUX IN+, AUX IN– (see Note 5)			55		dB
r_i	Input resistance at IN+, IN–, AUX IN+, AUX IN–			100		kΩ
	Squelch	DS03, DS02 = 0 in register 4		60		dB

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 4. The differential range corresponds to the full-scale digital output.

5. Common-mode rejection ratio is the ratio of the ADC converter offset error with no signal and the ADC converter offset error with a common-mode nonzero signal applied to either IN+ and IN– together or AUX IN+ and AUX IN– together.

3.5.3 ADC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_S = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = 6 dB		A_V = 12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
ADC channel signal-to-distortion ratio (see Note 6)	V_I = –6 dB to –1 dB	64		—		—		dB
	V_I = –12 dB to –6 dB	59		64		—		
	V_I = –18 dB to –12 dB	56		59		64		
	V_I = –24 dB to –18 dB	50		56		59		
	V_I = –30 dB to –24 dB	44		50		56		
	V_I = –36 dB to –30 dB	38		44		50		
	V_I = –42 dB to –36 dB	32		38		44		
	V_I = –48 dB to –42 dB	26		32		38		

NOTE 6: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog-input signal.

3.5.4 DAC Channel Filter Transfer Function, FCLK = 144 kHz, f_S = 9.6 kHz, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 7)	f_i < 200 Hz		0.15	dB
	f_i = 200 Hz	–0.5	0.2	
	f_i = 300 Hz to 3 kHz	–0.15	0.2	
	f_i = 3.3 kHz	–0.35	0.03	
	f_i = 3.4 kHz	–1	–0.1	
	f_i = 4 kHz		–14	
	$f_i \geq$ 4.6 kHz		–32	

NOTE 7: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak.

3.5.5 DAC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_S = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = –6 dB		A_V = –12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
DAC channel signal-to-distortion ratio (see Note 8)	V_O = –6 dB to 0 dB	64		—		—		dB
	V_O = –12 dB to –6 dB	59		64		—		
	V_O = –18 dB to –12 dB	56		59		64		
	V_O = –24 dB to –18 dB	50		56		59		
	V_O = –30 dB to –24 dB	44		50		56		
	V_O = –36 dB to –30 dB	38		44		50		
	V_O = –42 dB to –36 dB	32		38		44		
	V_O = –48 dB to –42 dB	26		32		38		

NOTE 8: The input signal, V_I, is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

3.5.6 System Distortion, V_{DD} = 5 V, f_S = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel attenuation	Second harmonic	Single-ended input (see Note 9)		82		dB
		Differential input (see Note 9)	64	82		
	Third harmonic and higher harmonics	Single-ended input (see Note 9)		77		
		Differential input (see Note 9)	64	77		
DAC channel attenuation	Second harmonic	Single-ended output (buffered DAC V_{MID}) (see Note 10)		82		
		Differential output (see Note 10)	64	82		
	Third harmonic and higher harmonics	Single-ended output (see Note 10)		77		
		Differential output (see Note 10)	64	77		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 9. The input signal is a 1020-Hz sine wave for the ADC channel. Harmonic distortion is defined for an input level of –1 dB.

10. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–. Harmonic distortion is specified for a signal input level of 0 dB.

3.5.7 Noise, Low-Pass and Band-Pass Switched-Capacitor Filters Included, V_{DD} = 5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC idle-channel noise		Inputs tied to ADC V_{MID}, f_S = 8 kHz, FCLK = 144 kHz, (see Note 11)		180	300	μVrms
DAC idle-channel noise	Broad-band noise	DIN INPUT = 00000000000000, f_S = 8 kHz, FCLK = 144 kHz, (see Note 12)		180	300	
	Noise (0 to 7.2 kHz)			180	300	
	Noise (0 to 3.6 kHz)			180	300	

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 11. The ADC channel noise is calculated by taking the RMS value of the digital output codes of the ADC channel and converting to microvolts.

12. The DAC channel noise is measured differentially from OUT+ to OUT– across 600 Ω.

3.5.8 Absolute Gain Error, V_{DD} = 5 V, f_S = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
ADC channel absolute gain error (see Note 13)	–1-dB input signal	T_A = –40 – 85°C		±1	dB
DAC channel absolute gain error (see Note 14)	0-dB input signal, R_L = 600 Ω	T_A = –40 – 85°C		±1	

NOTES: 13. ADC absolute gain error is the variation in gain from the ideal gain over the specified input signal levels. The gain is measured with a –1-dB, 1020-Hz sine wave. The –1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB input signal levels.

14. The DAC input signal is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at digital full-scale input = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

3.5.9 Relative Gain and Dynamic Range, V_{DD} = 5 V, f_S = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ADC channel relative gain tracking error (see Note 15)	–48-dB to –1-dB input signal range		±0.2	dB
DAC channel relative gain tracking error (see Note 16)	–48-dB to 0-dB input signal range $R_{L(diff)}$ = 600 Ω		±0.2	

NOTES: 15. ADC gain tracking is the ratio of the measured gain at one ADC channel input level to the gain measured at any other input level. The ADC channel input is a –1-dB 1020-Hz sine wave input signal. A –1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB ADC input signal levels.

16. DAC gain tracking is the ratio of the measured gain at one DAC channel digital input level to the gain measured at any other input level. The DAC-channel input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

3.5.10 Power-Supply Rejection, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 17)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC V_{DD}	Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		dB
		f_i = 30 to 50 kHz		55		
DAC V_{DD}	Supply-voltage rejection ratio, DAC channel	f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		
DGTL V_{DD}	Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		
		f_i = 30 to 50 kHz		55		
DGTL V_{DD}	Supply-voltage rejection ratio, DAC channel	Single ended, f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		
		Differential, f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTE 17: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

3.5.11 Crosstalk Attenuation, V_{DD} = 5 V (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel crosstalk attenuation	DAC channel idle with DIN = 00000000000000, ADC input = 0 dB, 1020-Hz sine wave, Gain = 0 dB (see Note 18)		80		dB
DAC channel crosstalk attenuation	ADC channel idle with INP, INM, AUX IN+, and AUX IN– at ADC V_{MID}		80		dB
	DAC channel input = digital equivalent of a 1020-Hz sine wave (see Note 19)		80		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 18. The test signal is a 1020-Hz sine wave with a 0 dB = 6-V peak-to-peak reference level for the analog input signal.

19. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

3.5.12 Monitor Output Characteristics, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 20)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage	Quiescent level = ADC V_{MID} Z_L = 10 kΩ and 60 pF	1.3	1.5		V
V_{OO}	Output offset voltage	No load, single ended relative to ADC V_{MID}		5	10	mV
V_{OC}	Output common-mode voltage	No load	0.4 ADC V_{DD}	0.5 ADC V_{DD}	0.6 ADC V_{DD}	V
r_o	DC output resistance			50		Ω
A_V	Voltage gain (see Note 21)	Gain = 0 dB	−0.2	0	0.2	dB
		Gain 2 = −8 dB	−8.2	−8	−7.8	
		Gain 3 = −18 dB	−18.4	−18	−17.6	
		Squelch (see Note 22)			−60	

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 20. All monitor output tests are performed with a 10-kΩ load resistance.

21. Monitor gains are measured with a 1020-Hz, 6-V peak-to-peak sine wave applied differentially between IN+ and IN−. The monitor output gains are nominally 0 dB, −8 dB, and −18 dB relative to its input; however, the output gains are −6 dB relative to IN+ and IN− or AUX IN+ and AUX IN−.

22. Squelch is measured differentially with respect to ADC V_{MID}.

3.6 Timing Requirements and Specifications in Master Mode

3.6.1 Recommended Input Timing Requirements for Master Mode, V_{DD} = 5 V

		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 4–2)	25			ns
$t_{h(DIN)}$	DIN hold time after SCLK low (see Figure 4–2)			20	ns

3.6.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{f(SCLK)}$	Shift clock fall time (see Figure 4–2)		13	18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 4–2)		13	18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH-FL)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figures 4–2 and 4–4 and Note 24)		5	20	ns
$t_{d(CH-FH)}$	Delay time from SCLK high to $\overline{\text{FS}}$ high (see Figure 4–2)		5	20	ns
$t_{d(CH-DOUT)}$	Delay time from SCLK high to DOUT valid (see Figures 4–2 and 4–7)			20	ns
$t_{d(CH-DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_{d(ML-EL)}$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_{d(ML-EH)}$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 4–9)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 4–9)		13		ns
$t_{d(MH-CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH-CL)}$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 23. All timing specifications are valid with C_L = 20 pF.

24. $\overline{\text{FSD}}$ occurs 1/2 shift-clock cycle ahead of $\overline{\text{FS}}$ when the device is operating in the master mode.

3.7 Timing Requirements and Specifications in Slave Mode and Codec Emulation Mode

3.7.1 Recommended Input Timing Requirements for Slave Mode, V_{DD} = 5 V

		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 4–3)	20			ns
$t_{h(DIN)}$	DIN hold time after SCLK high (see Figure 4–3)			20	ns
$t_{su(FL-CH)}$	Setup time from $\overline{\text{FS}}$ low to SCLK high			±SCLK/4	ns

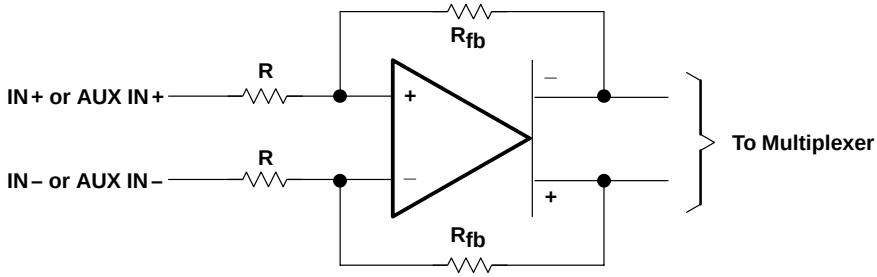
3.7.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock cycle time (see Figure 4–3)	125			ns
$t_{f(SCLK)}$	Shift clock fall time (see Figure 4–3)			18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 4–3)			18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH-FDL)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figure 4–6)			50	ns
$t_{d(CH-FDH)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ high			40	ns
$t_{d(FL-FDL)}$	Delay time from $\overline{\text{FS}}$ low to $\overline{\text{FSD}}$ low (slave to slave) (see Figure 4–5)			40	ns
$t_{d(CH-DOUT)}$	Delay time from SCLK high to DOUT valid (see Figures 4–3 and 4–7)			40	ns
$t_{d(CH-DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_{d(ML-EL)}$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_{d(ML-EH)}$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 4–9)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 4–9)		13		ns
$t_{d(MH-CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH-CL)}$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTE 23: All timing specifications are valid with C_L = 20 pF.

4 Parameter Measurement Information



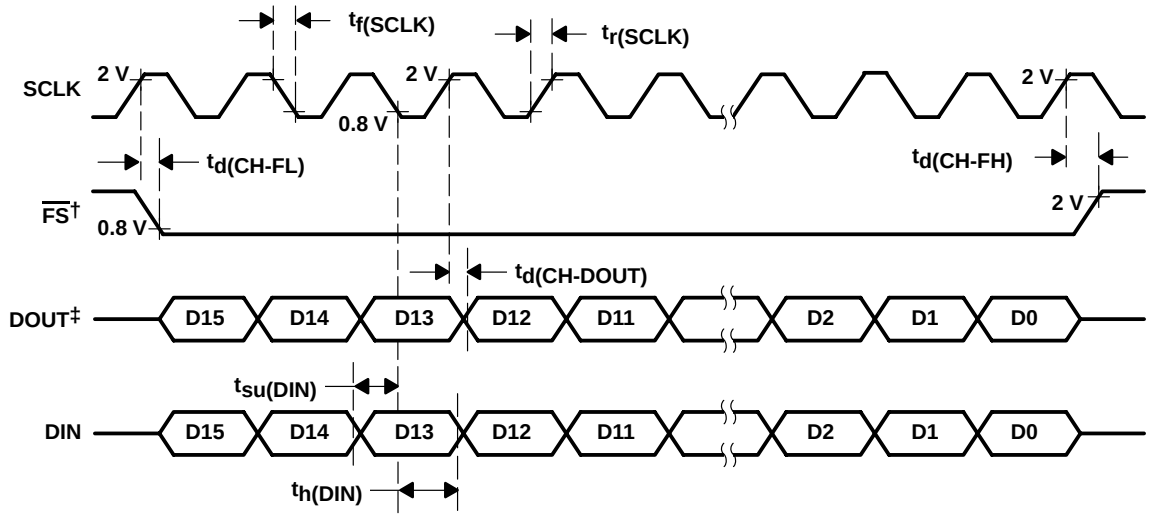
R_{fb} = R for DS03 = 0 and DS02 = 1
R_{fb} = 2R for DS03 = 1 and DS02 = 0
R_{fb} = 4R for DS03 = 1 and DS02 = 1
R = 100 kΩ nominal

Figure 4–1. IN+ and IN– Gain-Control Circuitry

Table 4–1. Gain Control (Analog Input Signal Required for Full-Scale Bipolar A/D-Conversion 2s Complement)†

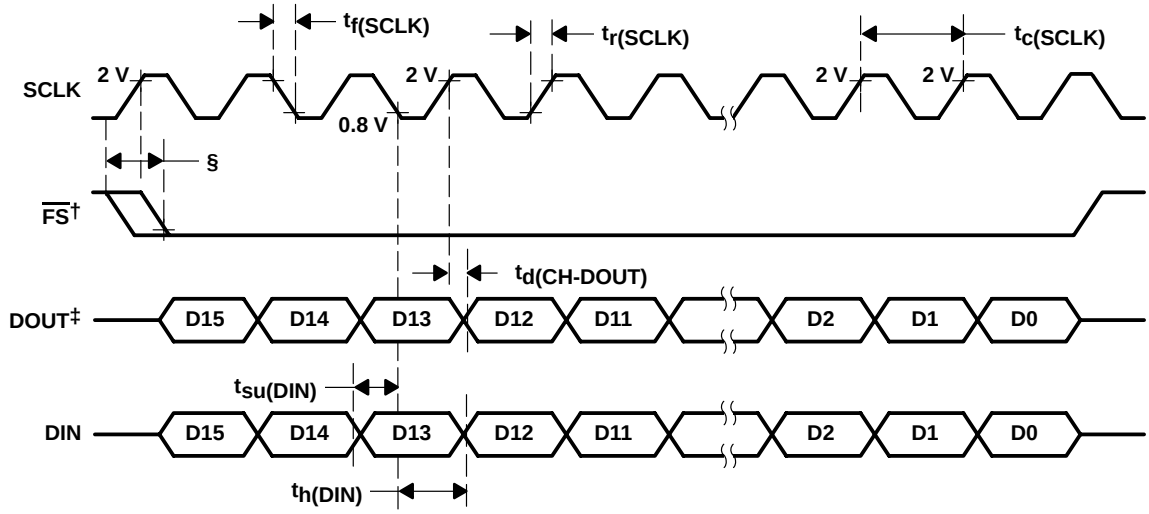
INPUT CONFIGURATION	CONTROL REGISTER 4		ANALOG INPUT‡	A/D CONVERSION RESULT
	DS03	DS02		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	0	0	All	Squelch
	0	1	V_{ID} = ±3 V	±Full scale
	1	0	V_{ID} = ±1.5 V	±Full scale
	1	1	V_{ID} = ±0.75 V	±Full scale
Single-ended configuration§ Analog input = IN+ – V_{MID} = AUX IN+ – V_{MID}	0	0	All	Squelch
	0	1	V_I = ±1.5 V	±Half scale
	1	0	V_I = ±1.5 V	±Full scale
	1	1	V_I = ±0.75 V	±Full scale

† V_{DD} = 5 V
‡ V_{ID} = differential input voltage, V_I = input voltage referenced to ADC V_{MID} with IN– or AUX IN– connected to ADC V_{MID}. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.
§ For single-ended inputs, the analog input voltage should not exceed the supply rails. All single-ended inputs should be referenced to the internal reference voltage, ADC V_{MID}, for best common-mode performance.



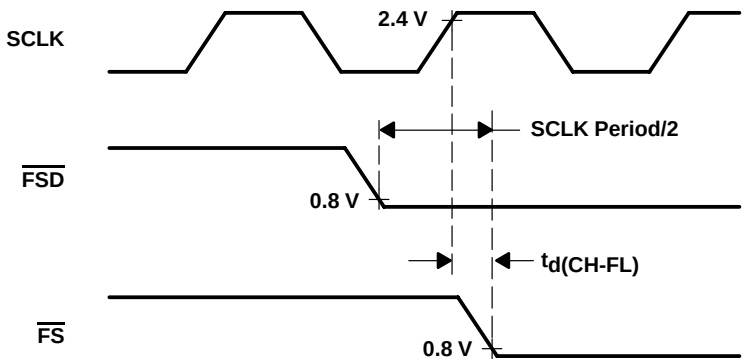
† The time between falling edges of two primary $\overline{FS}$ signals is the conversion period.
‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

Figure 4–2. AIC Stand-Alone and Master-Mode Timing



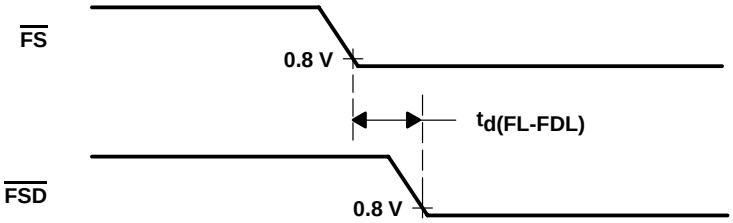
† The time between falling edges of two primary $\overline{FS}$ signals is the conversion period.
‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.
§ The high-to-low transition of $\overline{FS}$ must must occur within ±1/4 of a shift-clock period around the 2-V level of the shift clock for the codec mode.

Figure 4–3. AIC Slave and Codec Emulation Mode



NOTE A: Timing shown is for the TLC320AC02 operating as the master or as a stand-alone device.

Figure 4–4. Master or Stand-Alone $\overline{FS}$ and $\overline{FSD}$ Timing



NOTE A: Timing shown is for the TLC320AC02 operating in the slave mode ($\overline{FS}$ and SCLK signals are generated externally). The programmed data value in the FSD register is 0.

Figure 4–5. Slave $\overline{FS}$ to $\overline{FSD}$ Timing



NOTE A: Timing shown is for the TLC320AC02 operating in the slave mode ($\overline{FS}$ and SCLK signals are generated externally). There is a data value in the FSD register greater than 18 (decimal).

Figure 4–6. Slave SCLK to $\overline{FSD}$ Timing

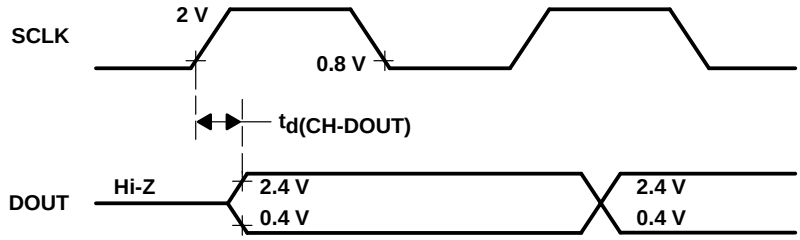


Figure 4–7. DOUT Enable Timing From Hi-Z

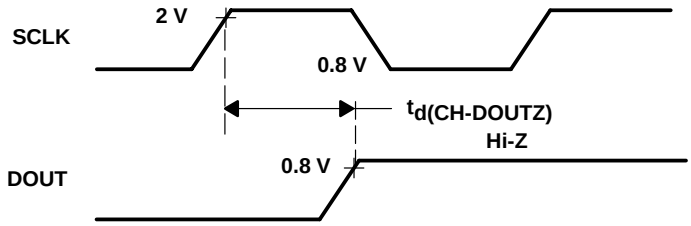


Figure 4–8. DOUT Delay Timing to Hi-Z

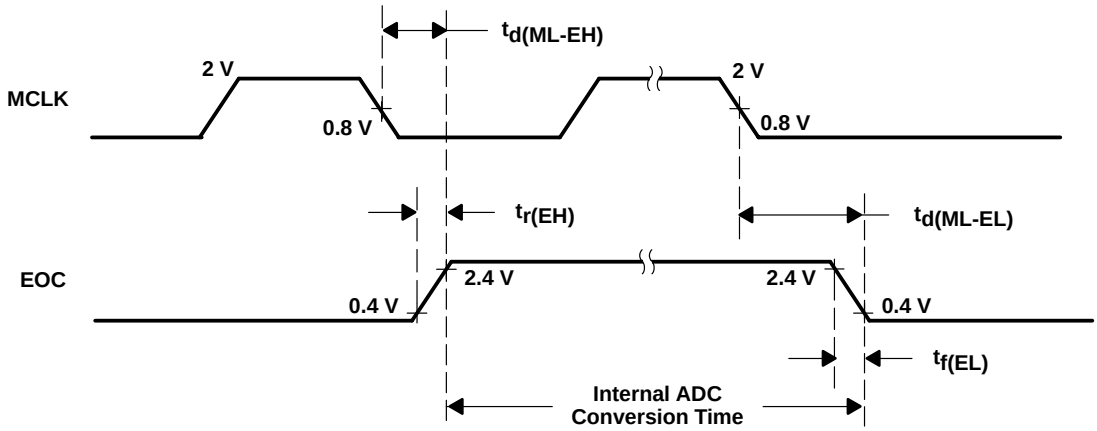
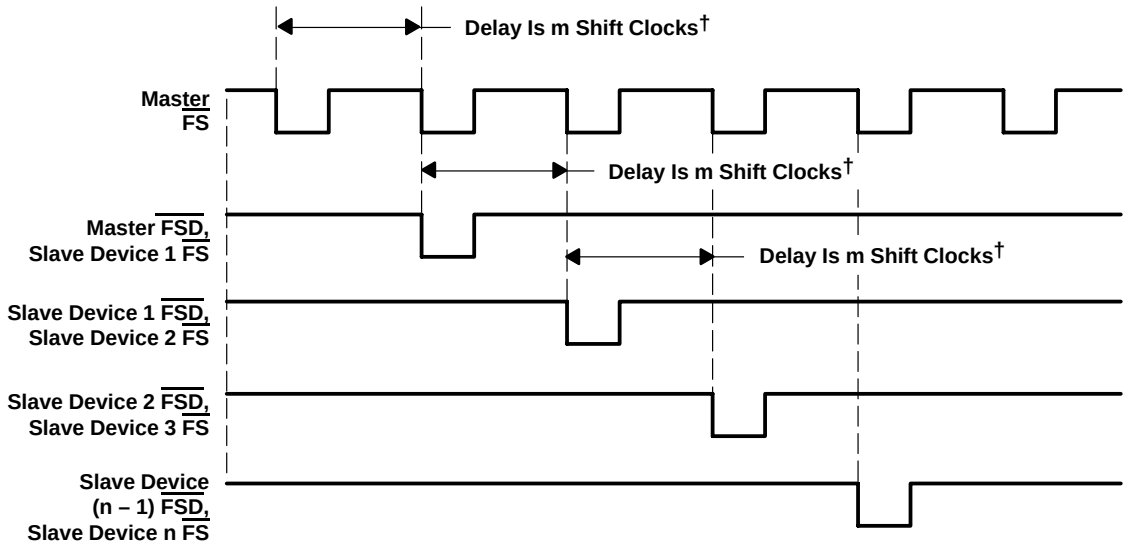


Figure 4–9. EOC Frame Timing



† The delay time from any $\overline{FS}$ signals to the corresponding $\overline{FSD}$ signals is m shift clocks with the value of m being the numerical value of the data programmed into the FSD register. In the master mode with slaves, the same data word programs the master and all slave devices; therefore, master to slave 1, slave 1 to slave 2, slave 2 to slave 3, etc., have the same delay time.

Figure 4–10. Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers

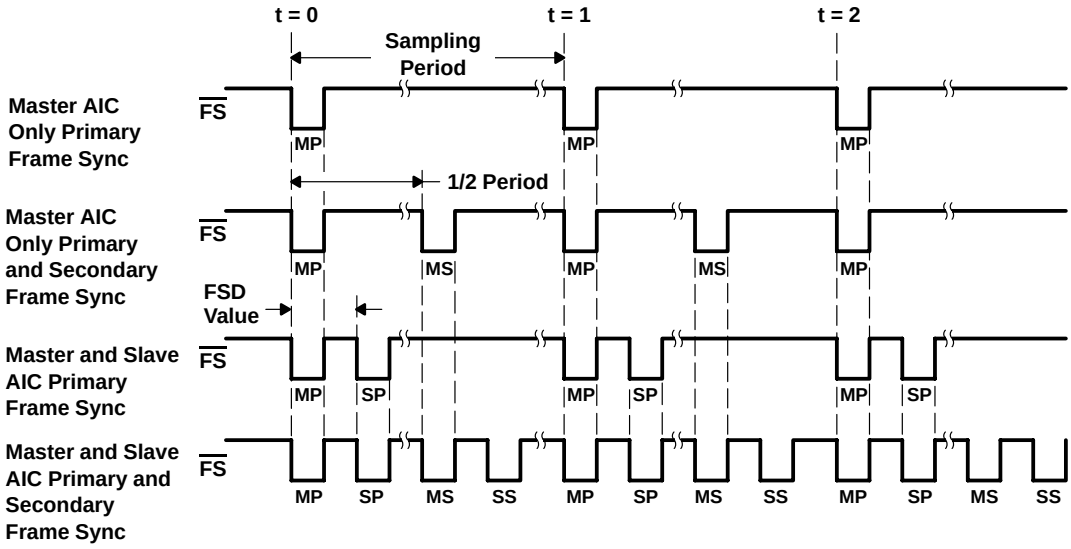
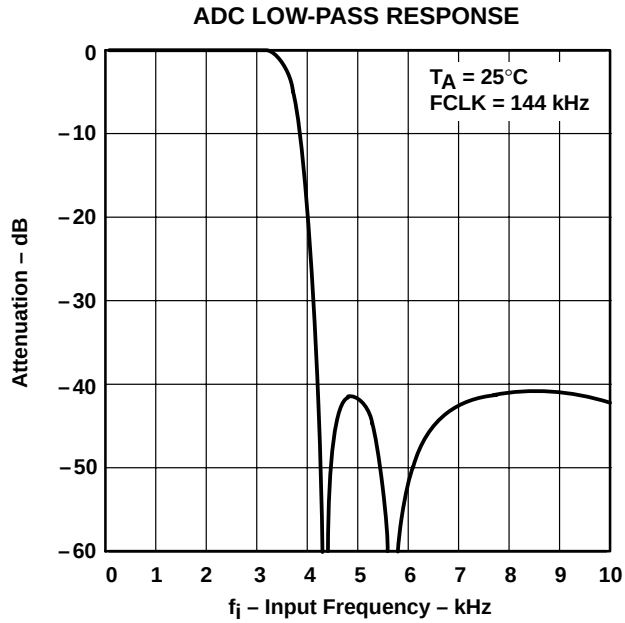


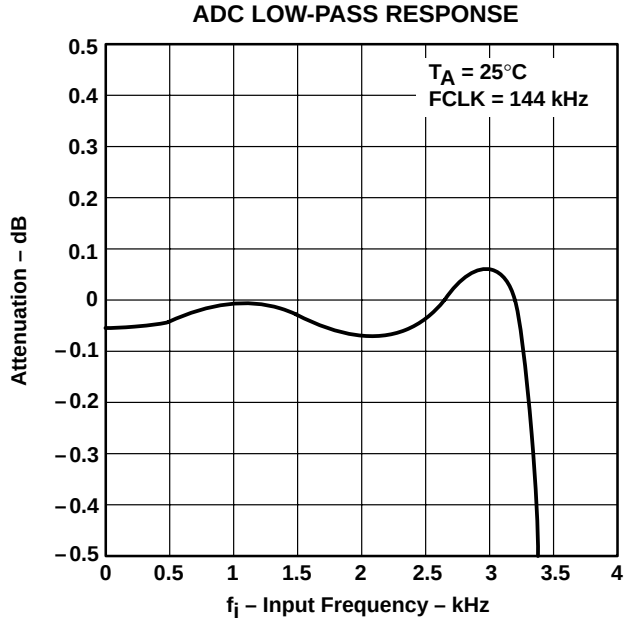
Figure 4–11. Master and Slave Frame-Sync Sequence with One Slave

5 Typical Characteristics



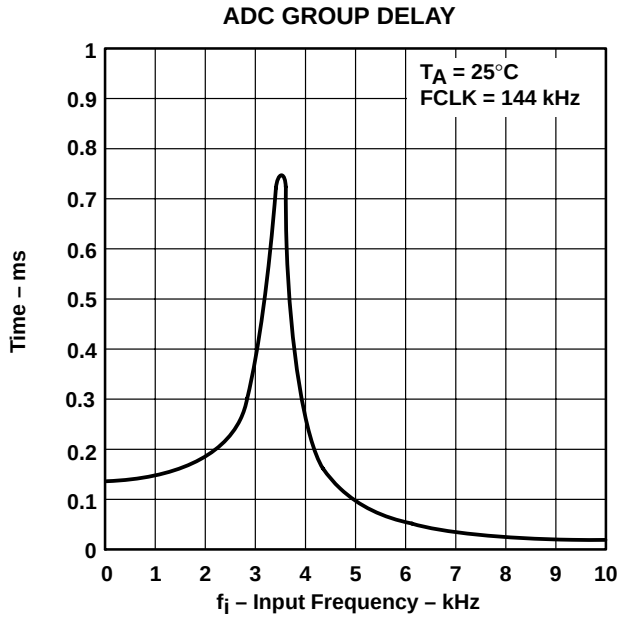
NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5–1



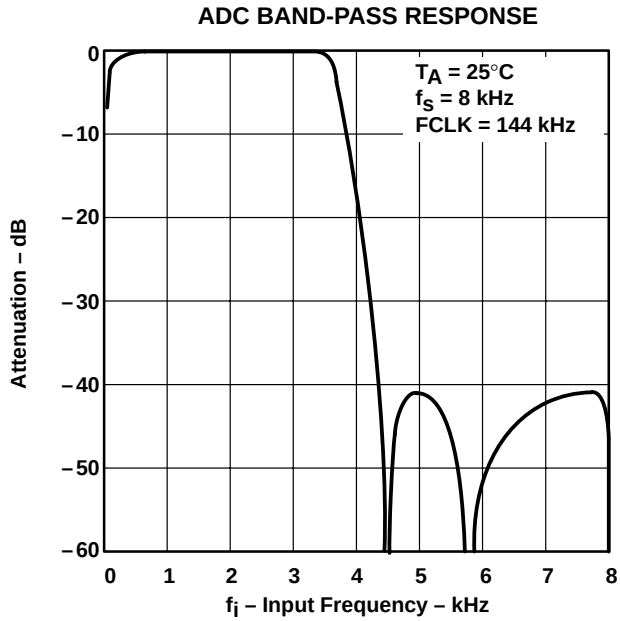
NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5–2



NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

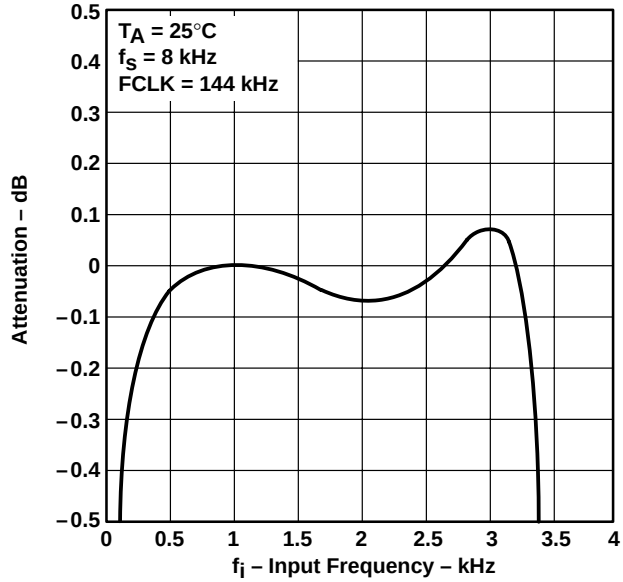
Figure 5–3



NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

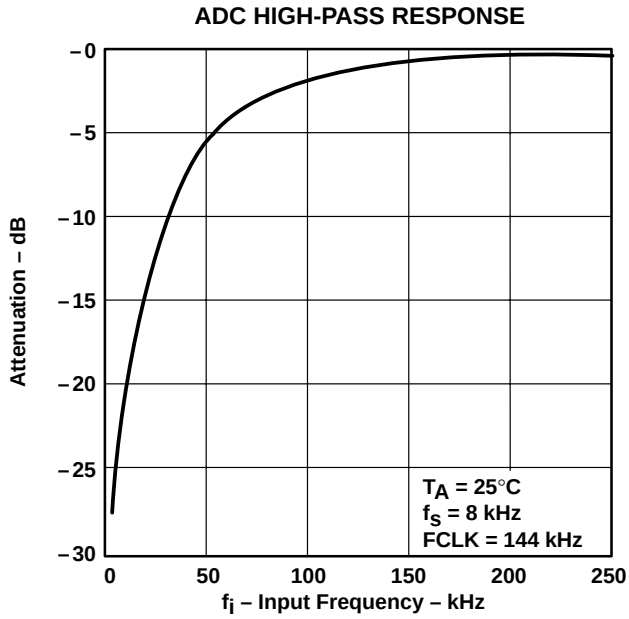
Figure 5–4

ADC BAND-PASS RESPONSE



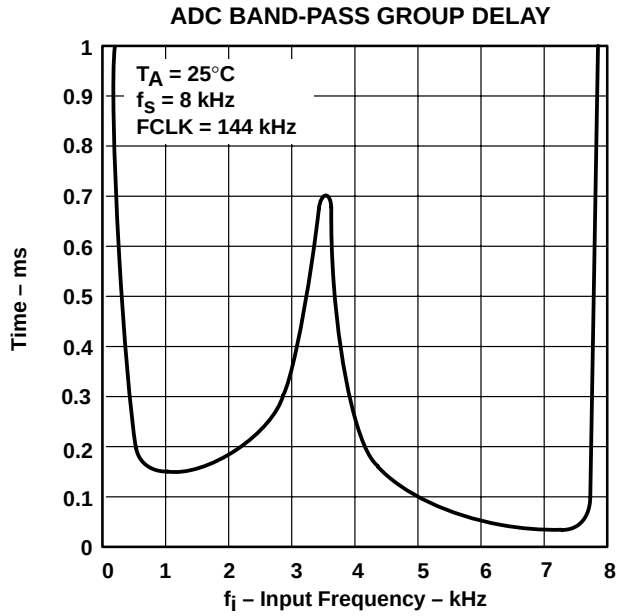
NOTE A: Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5–5



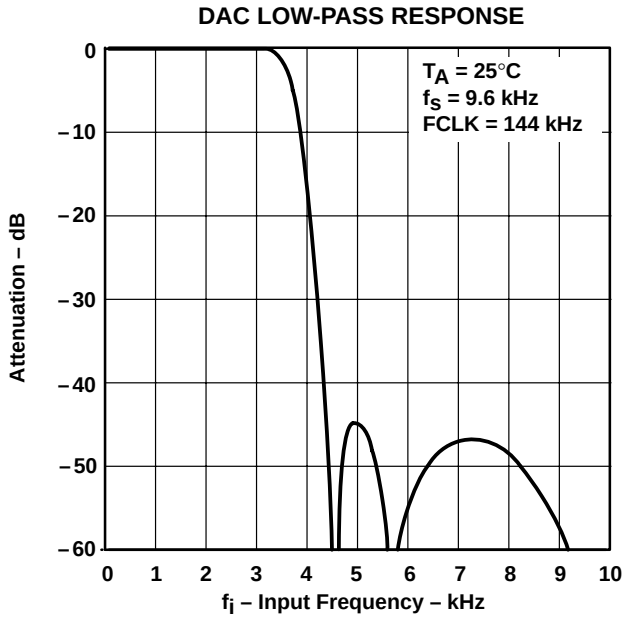
NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5–6



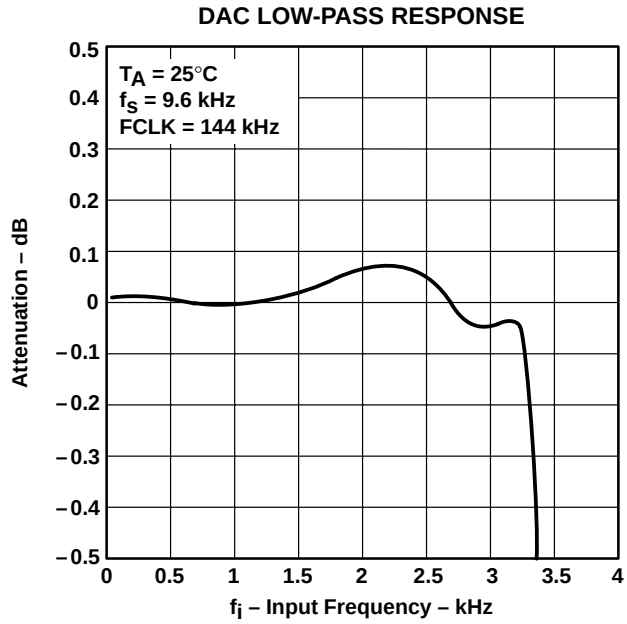
NOTE A : Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

Figure 5–7



NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

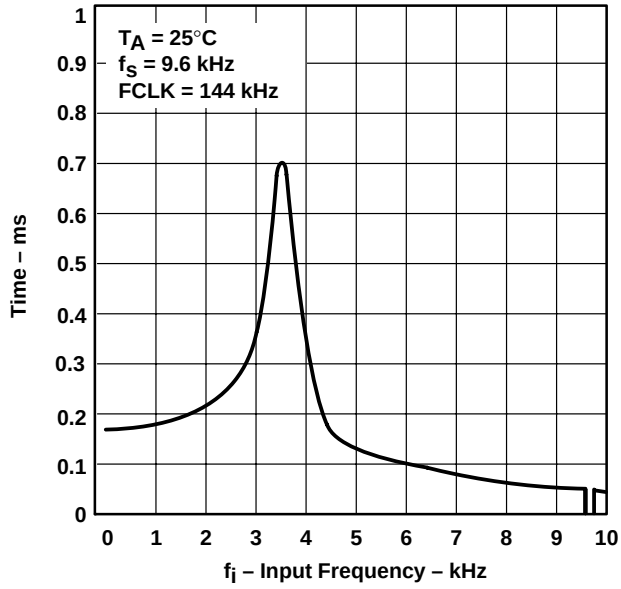
Figure 5–8



NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

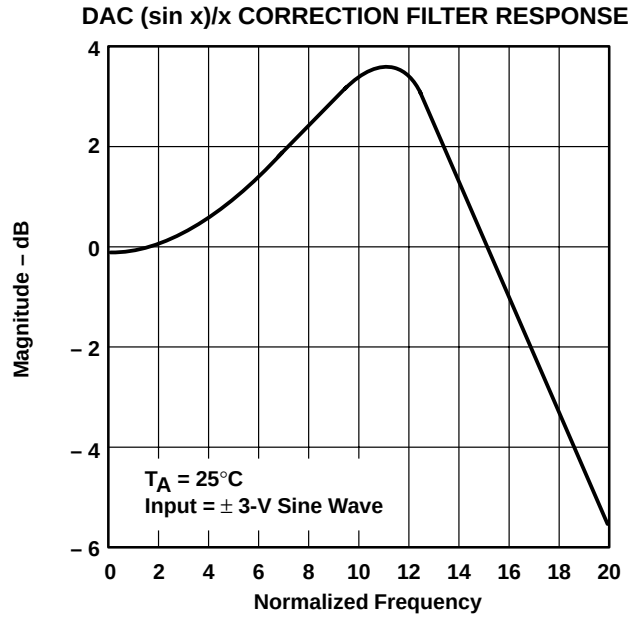
Figure 5–9

DAC LOW-PASS GROUP DELAY



NOTE A : Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

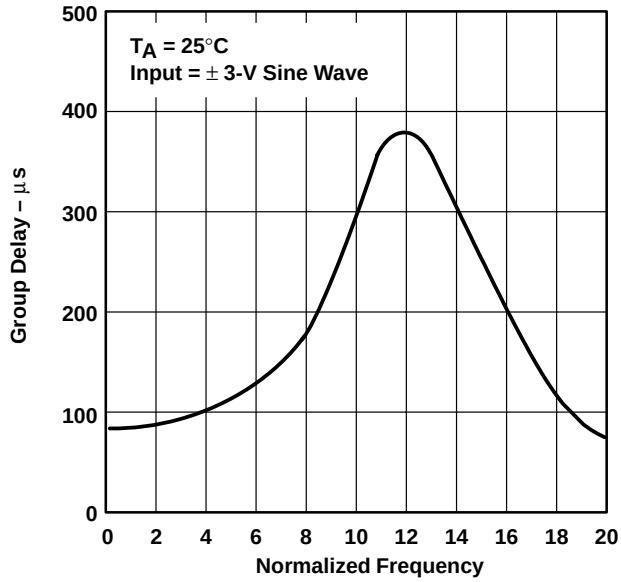
Figure 5–10



NOTE A : Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

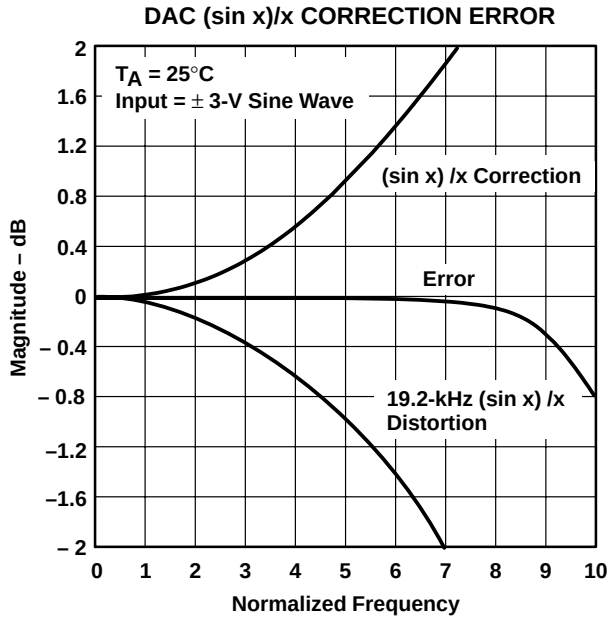
Figure 5–11

DAC (sin x)/x CORRECTION FILTER RESPONSE



NOTE A: Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

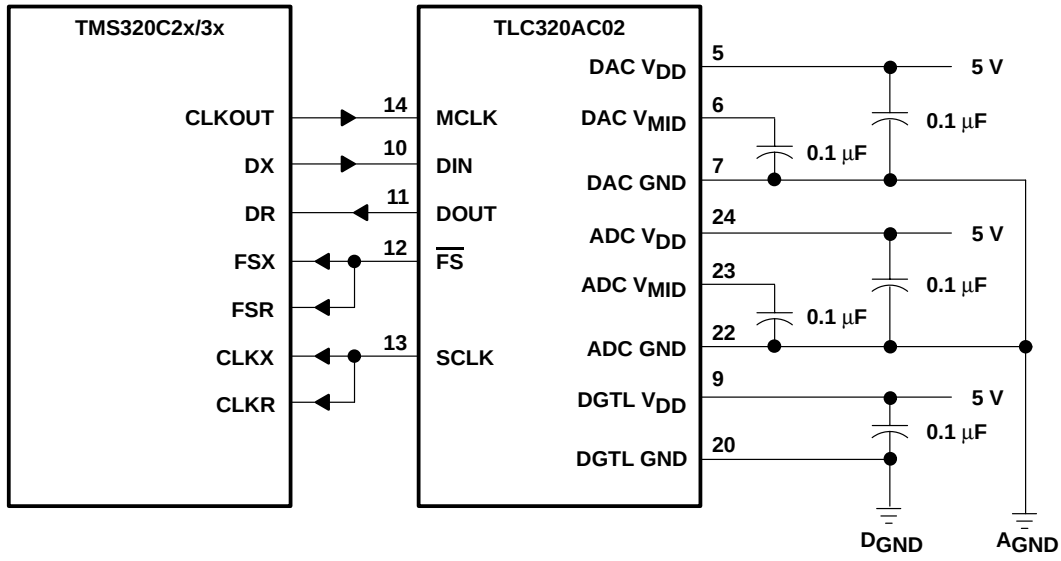
Figure 5–12



NOTE A : Absolute Frequency (kHz) $= \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

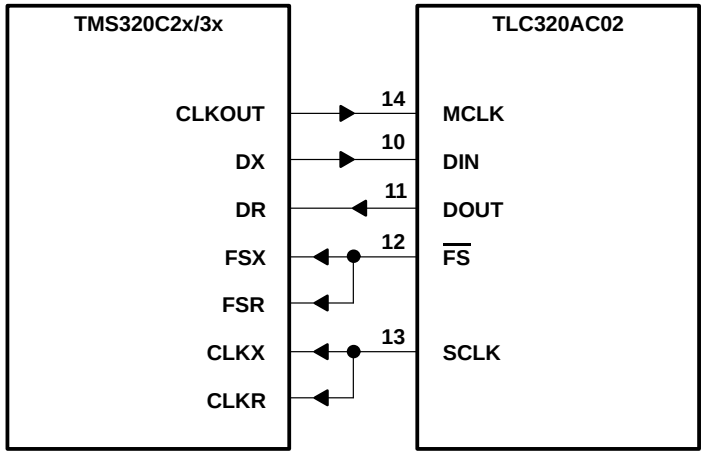
Figure 5–13

6 Application Information



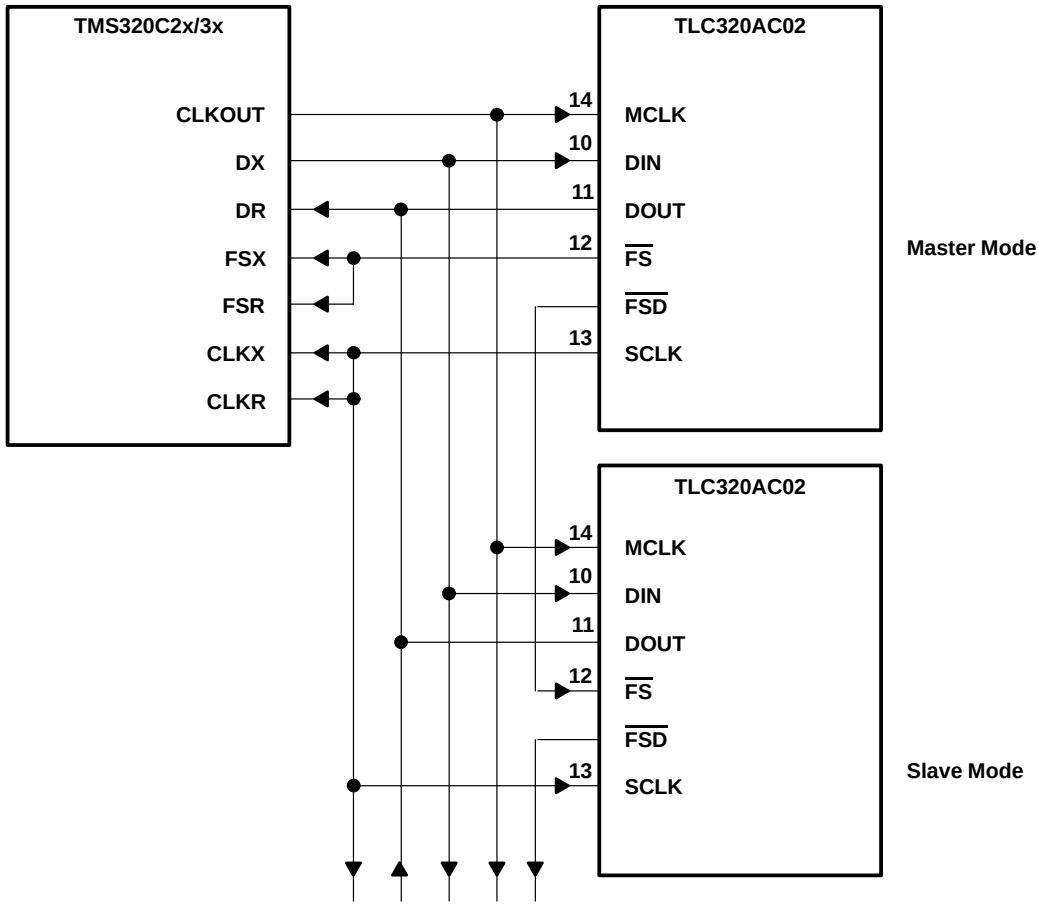
NOTE A: Terminal numbers shown are for the FN package.

Figure 6–1. Stand-Alone Mode (to DSP Interface)



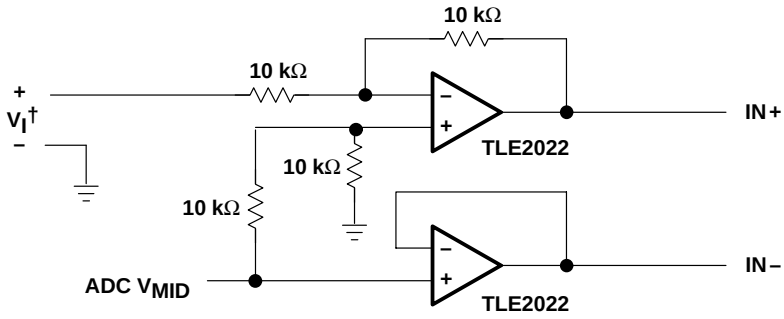
NOTE A: Terminal numbers shown are for the FN package.

Figure 6–2. Codec Mode (to DSP Interface)



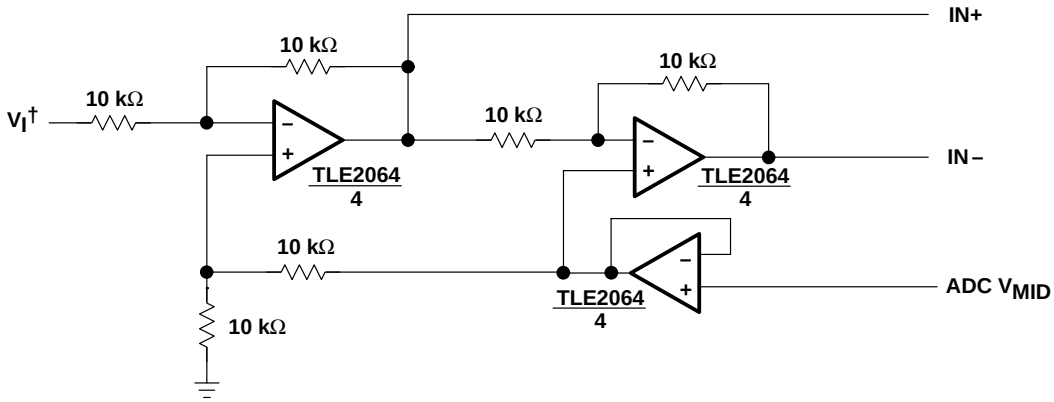
NOTE A: Terminal numbers shown are for the FN package.

Figure 6–3. Master With Slave (to DSP Interface)



† The V_I source must be capable of sinking a current equal to [ADC V_{MID} + $|V_I|$(max)]/10 kΩ.

Figure 6–4. Single-Ended Input (Ground Referenced)



† The V_I source must be capable of sinking a current equal to [(ADC V_{MID}/2) + |V_I|(max)]/10 kΩ.

Figure 6–5. Single-Ended to Differential Input (Ground Referenced)

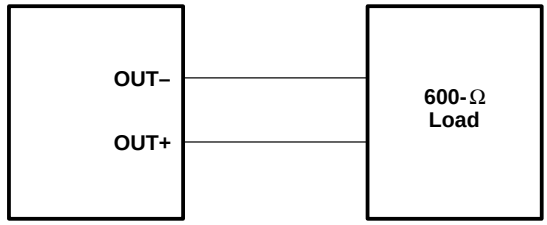
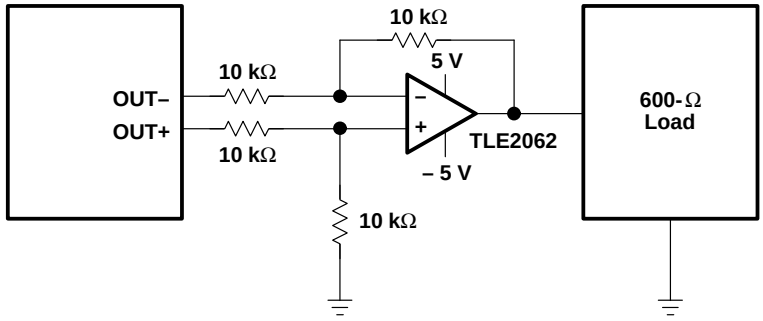


Figure 6–6. Differential Load



NOTE A: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6–7. Differential Output Drive (Ground Referenced)

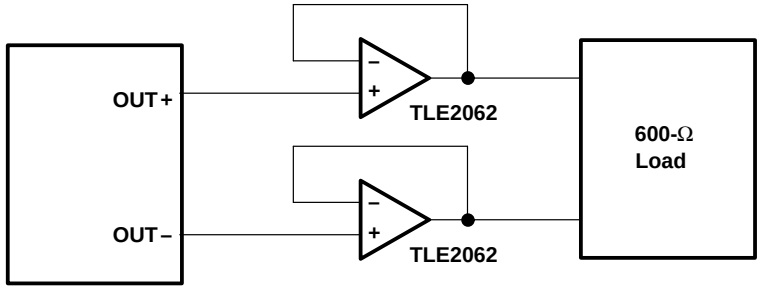
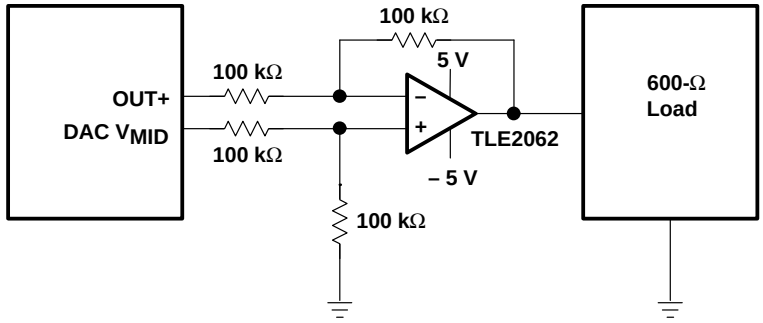


Figure 6–8. Low-Impedance Output Drive



NOTE A: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6–9. Single-Ended Output Drive (Ground Referenced)

Appendix A
Primary Control Bits

The function of the primary-word control bits D01 and D00 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of D01, D00, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF CONTROL BITS

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	0	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.
0	0	0	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of the next internal $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods equal to the value contained in the A′ register. When the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs earlier.
0	0	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the rising edge of the next internal $\overline{FS}$, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs later.
0	0	1	1	On the next falling edge of the primary $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
0	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, the falling edge of $\overline{FS}$ occurs earlier.
1	0	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs later.
1	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.

CONTROL FUNCTION OF CONTROL BITS (Continued)

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
1	0	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs later. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
1	1	1	1	On the next falling edge of the primary $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary $\overline{FS}$ occurs at 1/2 the sampling time measured from the falling edge of the primary $\overline{FS}$.
1	1	0	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary $\overline{FS}$ occurs at 1/2 the sampling time measured from the falling edge of the primary $\overline{FS}$.

Appendix B
Secondary Communications

The function of the control bits DS15 and DS14 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of DS15, DS14, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF SECONDARY COMMUNICATION

BITS		TERMINALS		
DS15	DS14	FC1	FC0	
0	0	Ignored		On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
0	1	Ignored		On the next falling edge of the $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of DS15 and DS14 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	0	Ignored		On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs later.
1	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
1	1	0	1	On the next falling edge of the $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs later.
1	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.

Appendix C
TLC320AC01C/TLC320AC02C Specification Comparisons

Texas Instruments manufactures the TLC320AC01C and the TLC320AC02C specified for the 0°C to 70°C commercial temperature range and the TLC320AC02I specified for the –40°C to 85°C temperature range. The TLC320AC02C and TLC320AC02I operate at a relaxed TLC320AC01C specification. The differences are listed in the following tables.

ADC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_S = 8 kHz (Unless Otherwise Noted) (see Note 1)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = 6 dB		A_V = 12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	V_I = –6 dB to –1 dB	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	V_I = –12 dB to –6 dB	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	V_I = –18 dB to –12 dB	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	V_I = –24 dB to –18 dB	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	V_I = –30 dB to –24 dB	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	V_I = –36 dB to –30 dB	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	V_I = –42 dB to –36 dB	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	V_I = –48 dB to –42 dB	27		33		39		
TLC320AC02		26		32		38		

NOTE 1: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog input signal.

DAC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted) (see Note 2)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = –6 dB		A_V = –12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	V_O = –6 dB to 0 dB	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	V_O = –12 dB to –6 dB	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	V_O = –18 dB to –12 dB	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	V_O = –24 dB to –18 dB	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	V_O = –30 dB to –24 dB	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	V_O = –36 dB to –30 dB	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	V_O = –42 dB to –36 dB	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	V_O = –48 dB to –42 dB	27		33		39		
TLC320AC02		26		32		38		

NOTE 2: The input signal, V_I, is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

System Distortion, ADC Channel Attenuation, V_{DD} = 5 V, f_S = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential input (see Note 3)	70		dB
TLC320AC02			64		dB
TLC320AC01	Third harmonic and higher harmonics		70		dB
TLC320AC02			64		dB

NOTE 3: The input signal is a 1020 Hz-sine wave for the ADC channel. Harmonic distortion is defined for an input level of –1 dB.

System Distortion, DAC Channel Attenuation, V_{DD} = 5 V, f_S = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential output (see Note 4)	70		dB
TLC320AC02			64		dB
TLC320AC01	Third harmonic and higher harmonics		70		dB
TLC320AC02			64		dB

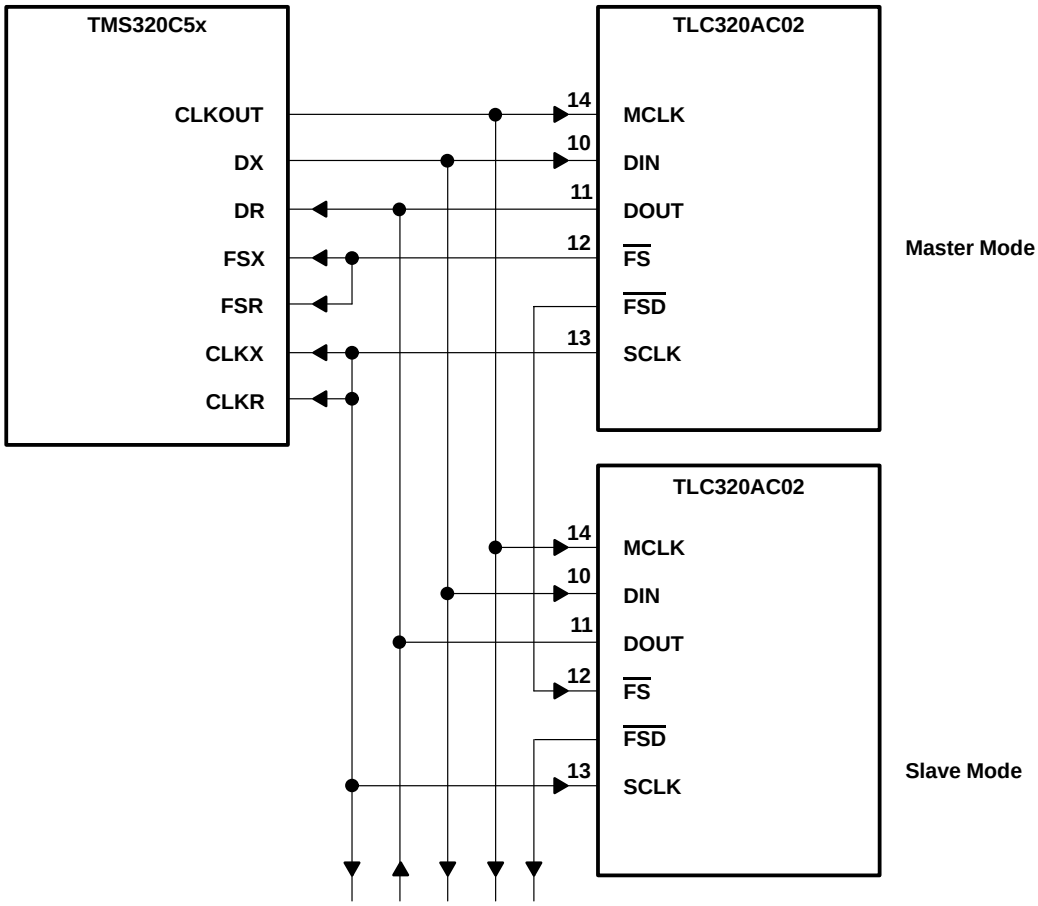
NOTE 4: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–. Harmonic distortion is specified for a signal input level of 0 dB.

Appendix D
Multiple TLC320AC01/02 Analog Interface Circuits on One TMS320C5X DSP Serial Port

In many applications, digital signal processors (DSP) must obtain information from multiple analog-to-digital (A/D) channels and transmit digital data to multiple digital-to-analog (D/A) conversion channels. The problem is how to do it easily and efficiently.

This application report addresses the issue of connecting two channels of an analog interface circuit (AIC) to one TMS320C5X DSP serial port. In this application report, the AIC is the TLC320AC02.

The TLC320AC02 (and TLC320AC01) analog interface circuit contains both A/D and D/A converters and using the master/slave mode, it is possible to connect two of them to one TMS320C5X DSP serial port with no additional logic. The hardware schematic is shown in Figure D–1.



NOTE A: Terminal numbers shown are for the FN package.

Figure D–1. Master With Slave (to DSP Interface)

HARDWARE AND SOFTWARE SOLUTION

Once the hardware connections are completed, the issue becomes distinguishing one channel from another. Fortunately, this is very easy to do in software and adds very little overhead. The mode that the AC02s run in is called master/slave mode. One AC02 is the master and all of the rest of the AC02s are slaves. The master can be distinguished from all of the slaves by examining the least significant bit (LSB) in the receive word coming from the AC02. The master has a 0 in the LSB and all of the slaves have a 1 in the LSB.

The AC02s in master/slave mode take turns communicating with the DSP serial port. They do this is a round robin or circular fashion. Synchronizing the system involves looking for the master AC02 and then starting the software associated with the first AC02. All other AC02s follow in order. It is possible to have different software for each AC02.

A reference design was constructed using a TMS320C5X DSP starter kit (DSK). The AC02s were connected to the TDM serial port which is available at the headers on the edge of the DSK.

A listing of the DSK assembly code for a simple stereo input/output program is included in the following section.

SOFTWARE MODULE

```
*******************************************************************************
*                                                                             *
*   MODULE NAME: INOUTB.ASM                                                   *
*                                                                             *
*   In-out routine for C5X DSK with two TLC320AC02s on the                    *
*   TDM serial port of the C5X in master/slave mode.                          *
*                                                                             *
*   This version performs the in/out task for both the master                 *
*   and slave TLC320AC02 in the receive interrupt service                     *
*   routine.                                                                  *
*                                                                             *
*******************************************************************************

*           .mmregs

            .ds         01000h
PR1         .word       0104h           ;A register
PR2         .word       0219h           ;B register
PR3         .word       0300h           ;A prime register
PR4         .word       0405h           ;amplifier gain register
PR5         .word       0501h           ;analog configuration register
PR6         .word       0600h           ;digital configuration register
PR7         .word       0730h           ;frame synch delay register
PR8         .word       0802h           ;frame synch number register
value       .word       0800h
value2      .word       0800h
val_add     .word       0200h
val_add2    .word       0400h
*******************************************************************************
*                                                                             *
*   Set up the ISR vector                                                     *
*                                                                             *
*******************************************************************************

            .ps         080ah
rint:       B           RECEIVE         ; 0A; Serial port receive interrupt RINT.
xint:       B           TRANSMIT        ; 0C; Serial port transmit interrupt XINT.
trint:      B           TDMREC
txint:      B           TDMTX
            ;———————————————————————————————————————————
*
*******************************************************************************
*                                                                             *
*   TMS320C5X INITIALIZATION                                                  *
*                                                                             *
*******************************************************************************

            .ps 0a00h
            .entry
START:      SETC        INTM            ; Disable interrupts
            LDP         #0              ; Set data page pointer
            OPL         #0834h,PMST
            LACC        #0
            SAMM        CWSR
            SAMM        PDWSR
```

```
            splk        #00c8h
            SPLK        082h,IMR
            call        AC02INIT

            CLRC        OVM             ; OVM = 0
            SPM         0               ; PM = 0
            SPLK        #042h,IMR       ; TDMA ser port rec interrupt
            SPLK        #0C8h,TSPC      ;
            CLRC        INTM            ; enable interrupts

loop                                    ; main program here does nothing.
            nop                         ; a user program can be inserted.
            b           loop            ;
;———————————————— end of main program ———————————————— ;
;
; TDM serial port receiver interrupt service routine
;
TDMREC:
                                        ; This loop insures that the master AC02
            ldp         #trcv           ; is the first one that is written to in the
            bit         trcv,15         ; loop. the slave AC02(s) will follow in
            bcnd        xxx,tc          ; sequential order. The master AC02 has a
                                        ; 0 in the 1sb. the slave AC02(s) have a 1
                                        ; in the 1sb of the receive word.
            ldp         #trcv
            lacc        trcv
            and         #0fffch
                                        ;
                                        ; user code would go here for master AC02
                                        ;
            sacl        tdxr
            b           yyy
xxx
            ldp         #trcv
            lacc        trcv
            and         #0fffch
                                        ;
                                        ; user code would go here for slave AC02
                                        ;
            sacl        tdxr
yyy
            rete
```

```
;
; TDM serial port transmit interrupt service routine
;
TDMTX:
            rete
;
; RECEIVER INTERRUPT SERVICE ROUTINE
;
RECEIVE:
            rete
TRANSMIT:
            RETE
```

```
AC02INIT
            SPLK        #020h,TCR
            SPLK        #01h,PRD
            MAR         *,AR0
            LACC        #0008h
            SACL        TSPC
            LACC        #00c8h
            SACL        TSPC
            SETC        SXM
;———————————————————————————————————————————————
            LDP         #PR1
            LACC        PR1
            CALL        AC02_2ND
;———————————————————————————————————————————————
            LDP         #PR2
            LACC        PR2
            CALL        AC02_2ND
;———————————————————————————————————————————————
            LDP         #PR8
            LACC        PR8
            CALL        AC02_2ND
;———————————————————————————————————————————————
            LDP         #PR7
            LACC        PR7
            CALL        AC02_2ND

            ret

AC02_2ND:
            LDP         #0
            SACH        TDXR          ;
            CLRC        INTM
            IDLE
            ADD         #6h, 15       ; 0000 0000 0000 0011 XXXX XXXX XXXX XXXX b
            SACH        TDXR          ;
            IDLE
            SACL        TDXR          ;
            IDLE
            LACL        #0            ;
            SACL        TDXR          ; make sure the word got sent
            IDLE
            SETC        INTM          ;
            RET
```

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC320AC02CFN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	0 to 70	TLC 320AC02CFN	Samples
TLC320AC02CPM	ACTIVE	LQFP	PM	64	160	TBD	NIPDAU	Level-3-220C-168 HR	0 to 70	320AC02C	Samples
TLC320AC02IFN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	-40 to 85	TLC 320AC02IFN	Samples
TLC320AC02IFNR	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	-40 to 85	TLC 320AC02IFN	Samples
TLC320AC02IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	320AC02I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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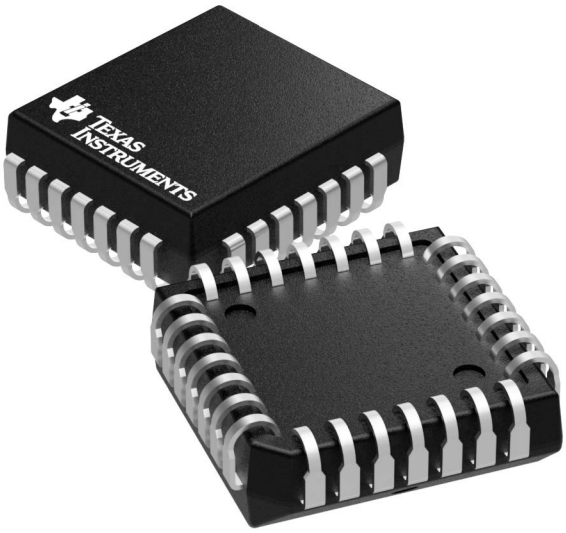
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GENERIC PACKAGE VIEW

FN 28

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

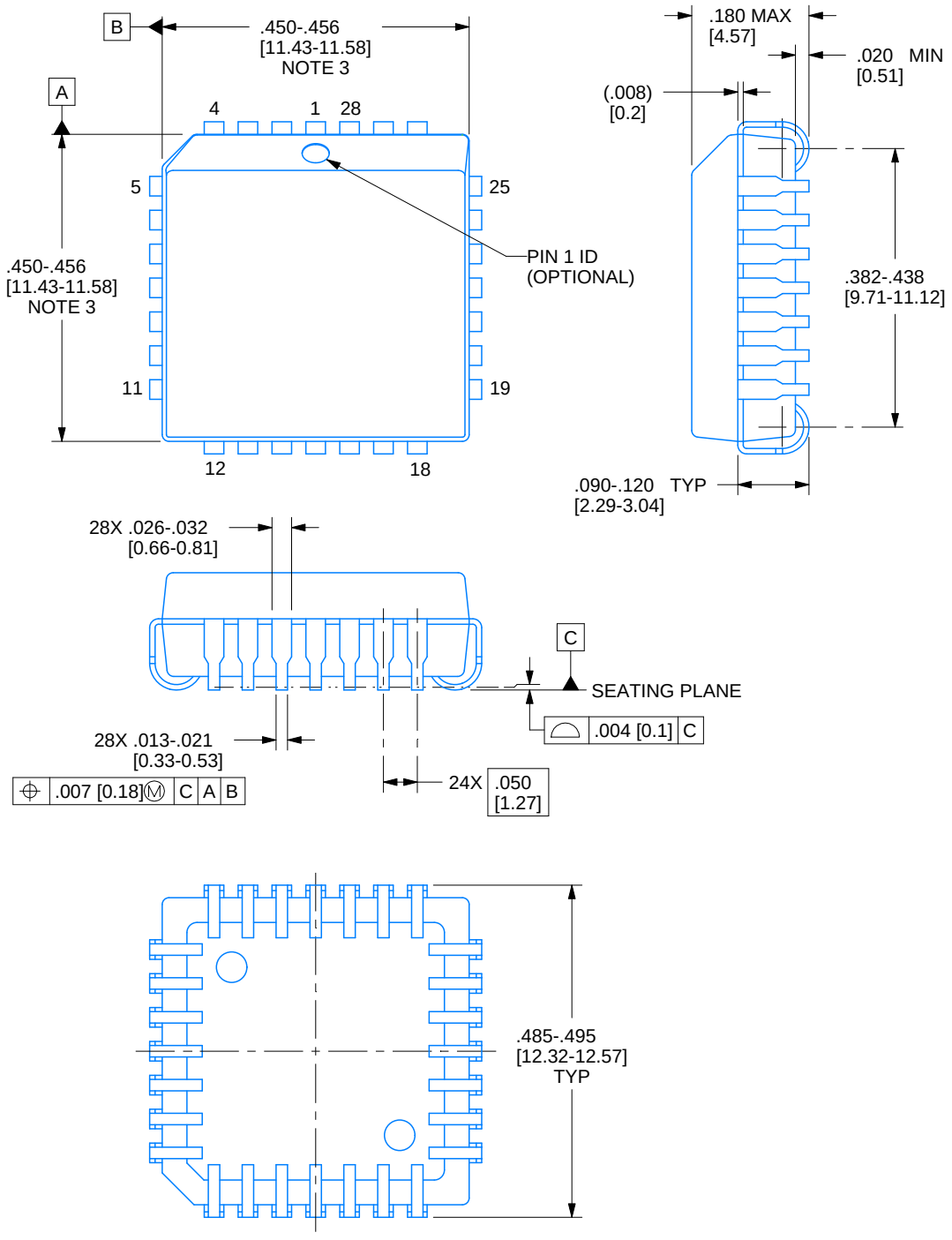
4040005-3/C

PACKAGE OUTLINE

FN0028A

PLCC - 4.57 mm max height

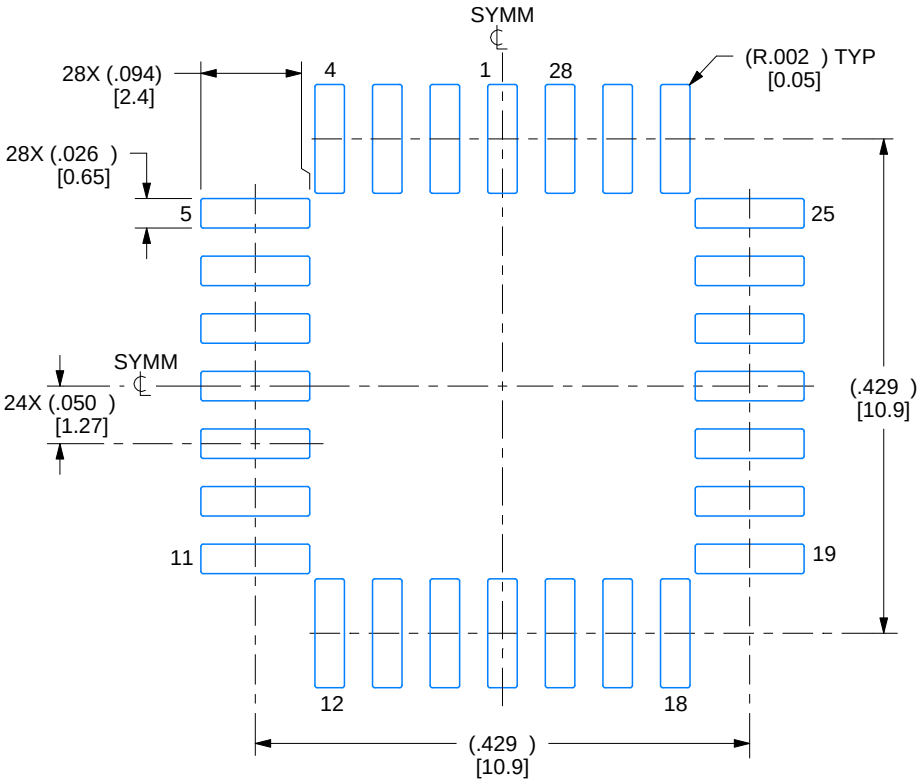
PLASTIC CHIP CARRIER



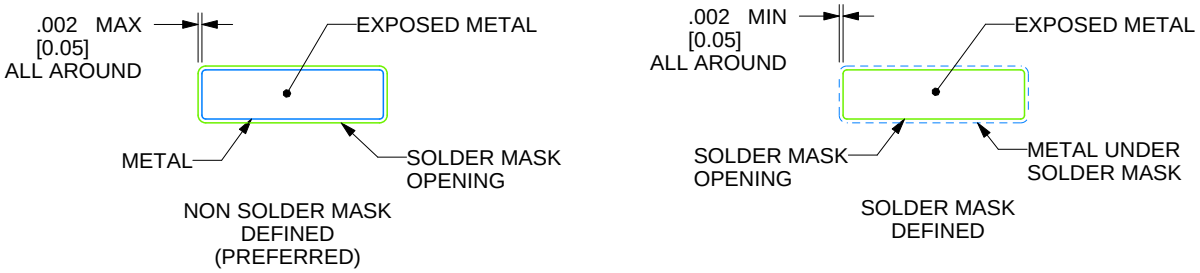
4215153/B 05/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

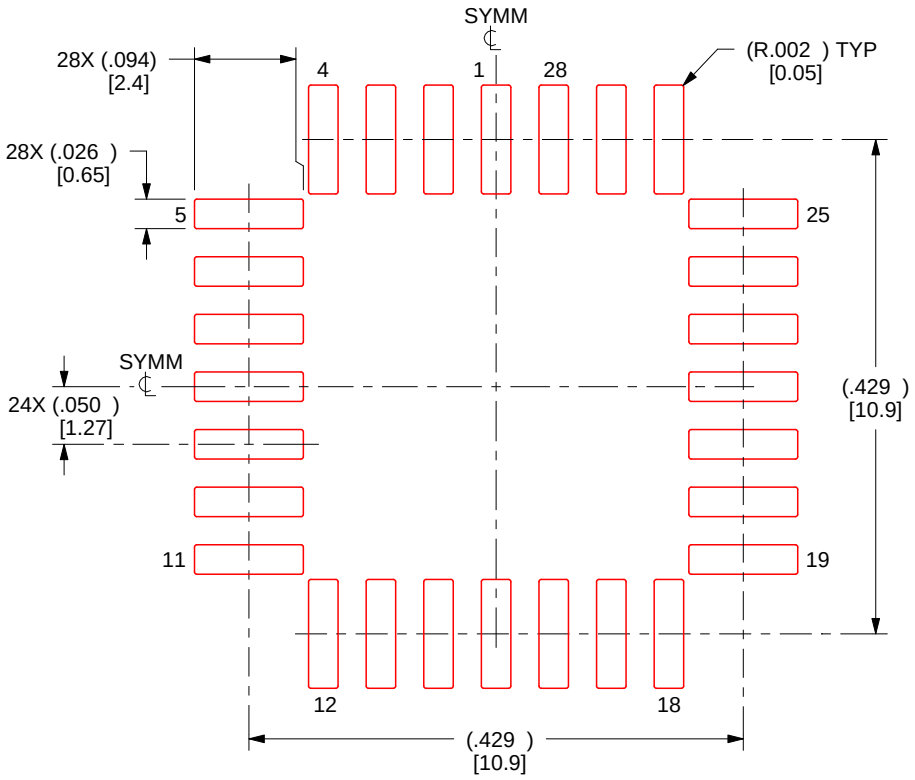


SOLDER MASK DETAILS

4215153/B 05/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215153/B 05/2017

NOTES: (continued)

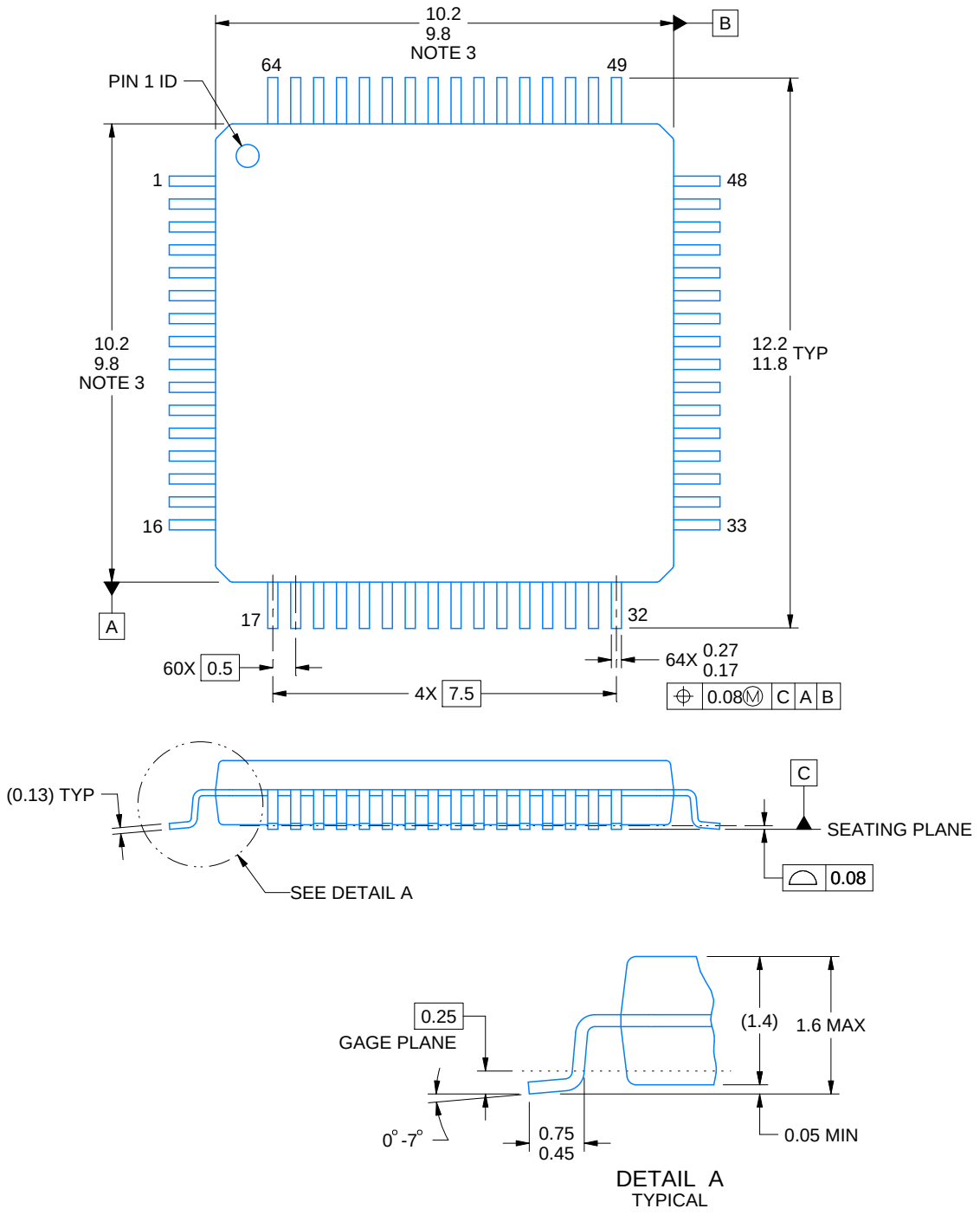
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

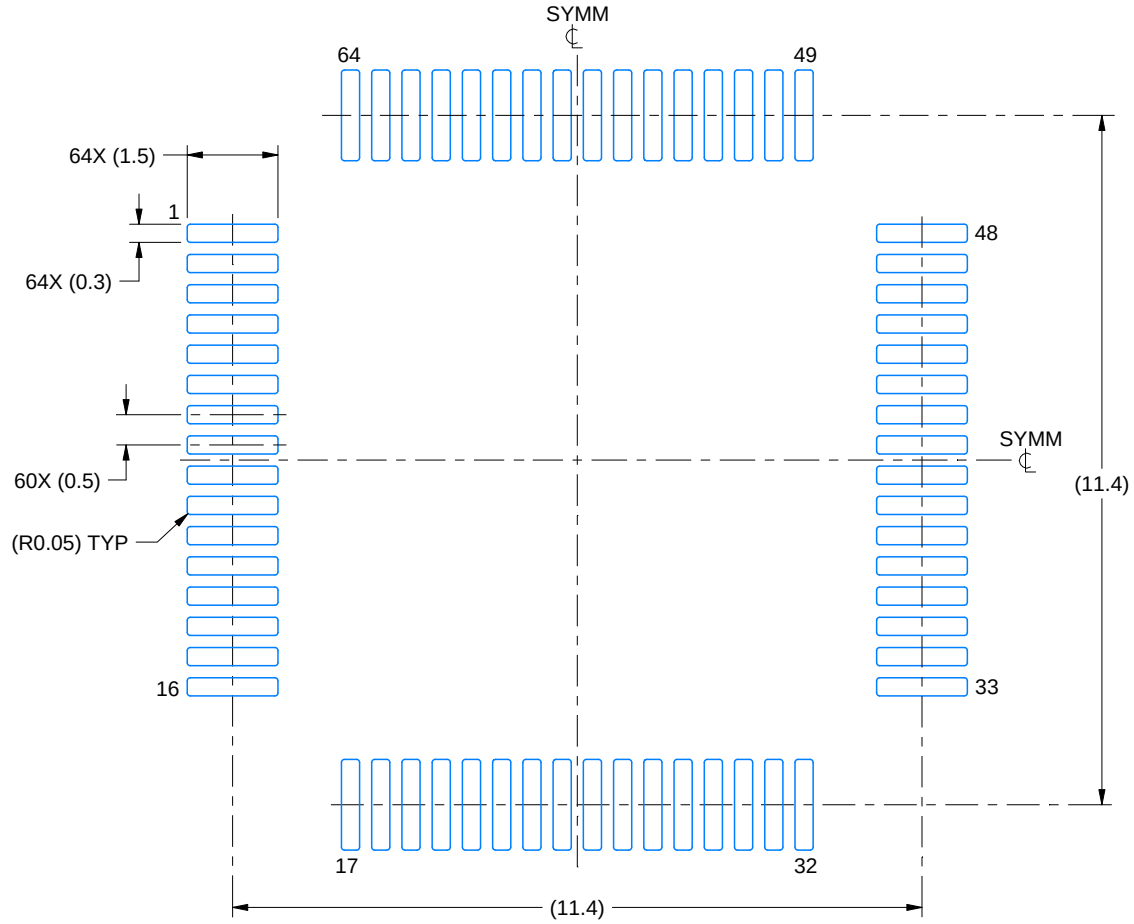
PLASTIC QUAD FLATPACK



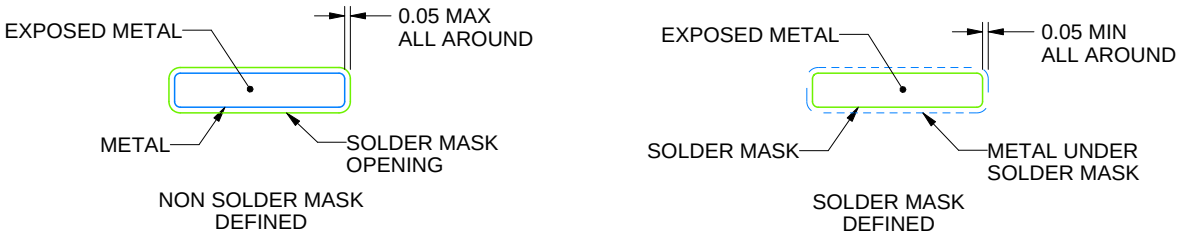
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

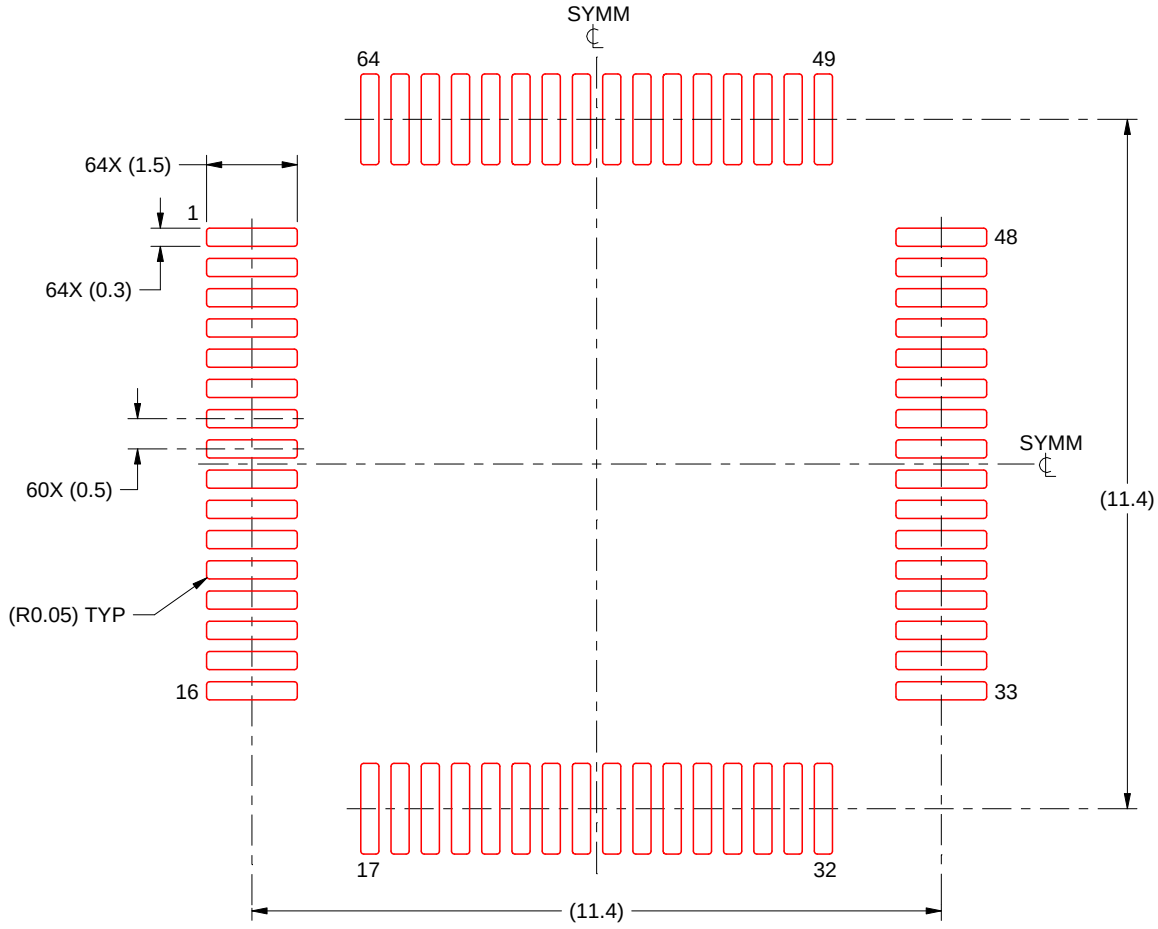


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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