

## N-channel 60 V, 0.012 $\Omega$ typ., 15 A STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data

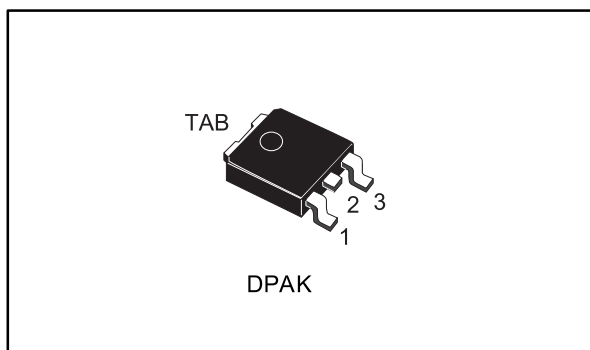
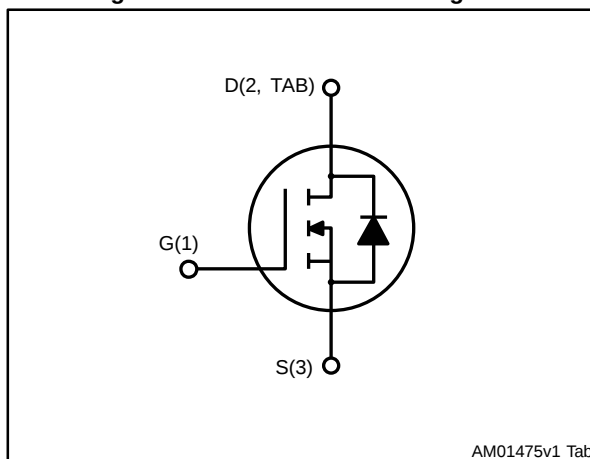


Figure 1: Internal schematic diagram



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STD46N6F7  | 60 V            | 0.014 $\Omega$           | 15 A           |

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

| Order code | Marking | Package | Packaging     |
|------------|---------|---------|---------------|
| STD46N6F7  | 46N6F7  | DPAK    | Tape and reel |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol            | Parameter                                                       | Value      | Unit             |
|-------------------|-----------------------------------------------------------------|------------|------------------|
| $V_{DS}$          | Drain-source voltage                                            | 60         | V                |
| $V_{GS}$          | Gate-source voltage                                             | $\pm 20$   | V                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 15         | A                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 15         | A                |
| $I_{DM}^{(1)(2)}$ | Drain current (pulsed)                                          | 60         | A                |
| $P_{TOT}^{(1)}$   | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$           | 60         | W                |
| $T_j$             | Operating junction temperature range                            | -55 to 175 | $^\circ\text{C}$ |
| $T_{stg}$         | Storage temperature range                                       |            |                  |

**Notes:**

<sup>(1)</sup>This value is limited by package and rated according to  $R_{thj-c}$

<sup>(2)</sup>Pulse width limited by safe operating area

Table 3: Thermal data

| Symbol              | Parameter                             | Value | Unit               |
|---------------------|---------------------------------------|-------|--------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb max.  | 50    | $^\circ\text{C/W}$ |
| $R_{thj-case}$      | Thermal resistance junction-case max. | 2.5   | $^\circ\text{C/W}$ |

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

Table 4: On/off states

| Symbol               | Parameter                         | Test conditions                                             | Min. | Typ.  | Max.  | Unit |
|----------------------|-----------------------------------|-------------------------------------------------------------|------|-------|-------|------|
| V <sub>(BR)DSS</sub> | Drain-source breakdown voltage    | I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V                | 60   |       |       | V    |
| I <sub>DSS</sub>     | Zero gate voltage drain current   | V <sub>GS</sub> = 0 V<br>V <sub>DS</sub> = 60 V             |      |       | 1     | μA   |
| I <sub>GSS</sub>     | Gate-body leakage current         | V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V               |      |       | 100   | nA   |
| V <sub>GS(th)</sub>  | Gate threshold voltage            | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA | 2    |       | 4     | V    |
| R <sub>DS(on)</sub>  | Static drain-source on-resistance | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A              |      | 0.012 | 0.014 | Ω    |

Table 5: Dynamic

| Symbol           | Parameter                    | Test conditions                                                                                                                                    | Min. | Typ. | Max. | Unit |
|------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C <sub>iss</sub> | Input capacitance            | V <sub>DS</sub> = 30 V, f = 1 MHz,<br>V <sub>GS</sub> = 0 V                                                                                        | -    | 1035 | -    | pF   |
| C <sub>oss</sub> | Output capacitance           |                                                                                                                                                    | -    | 450  | -    | pF   |
| C <sub>rss</sub> | Reverse transfer capacitance |                                                                                                                                                    | -    | 53   | -    | pF   |
| Q <sub>g</sub>   | Total gate charge            | V <sub>DD</sub> = 30 V, I <sub>D</sub> = 15 A,<br>V <sub>GS</sub> = 10 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> ) | -    | 17   | -    | nC   |
| Q <sub>gs</sub>  | Gate-source charge           |                                                                                                                                                    | -    | 5.7  | -    | nC   |
| Q <sub>gd</sub>  | Gate-drain charge            |                                                                                                                                                    | -    | 5.7  | -    | nC   |

Table 6: Switching times

| Symbol              | Parameter           | Test conditions                                                                                                                                                                       | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>d(on)</sub>  | Turn-on delay time  | V <sub>DD</sub> = 30 V, I <sub>D</sub> = 7.5 A,<br>R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> ) | -    | 14.5 | -    | ns   |
| t <sub>r</sub>      | Rise time           |                                                                                                                                                                                       | -    | 15.3 | -    | ns   |
| t <sub>d(off)</sub> | Turn-off delay time |                                                                                                                                                                                       | -    | 19.4 | -    | ns   |
| t <sub>f</sub>      | Fall time           |                                                                                                                                                                                       | -    | 8    | -    | ns   |

Table 7: Source-drain diode

| Symbol                         | Parameter                | Test conditions                                                                                                                                                          | Min. | Typ. | Max. | Unit |
|--------------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>SD</sub> <sup>(1)</sup> | Forward on voltage       | I <sub>SD</sub> = 15 A, V <sub>GS</sub> = 0 V                                                                                                                            | -    |      | 1.2  | V    |
| t <sub>rr</sub>                | Reverse recovery time    | I <sub>D</sub> = 15 A, di/dt = 100 A/μs<br>V <sub>DD</sub> = 48 V (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 26.8 |      | ns   |
| Q <sub>rr</sub>                | Reverse recovery charge  |                                                                                                                                                                          | -    | 14.2 |      | nC   |
| I <sub>RRM</sub>               | Reverse recovery current |                                                                                                                                                                          | -    | 1.06 |      | A    |

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300 μs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

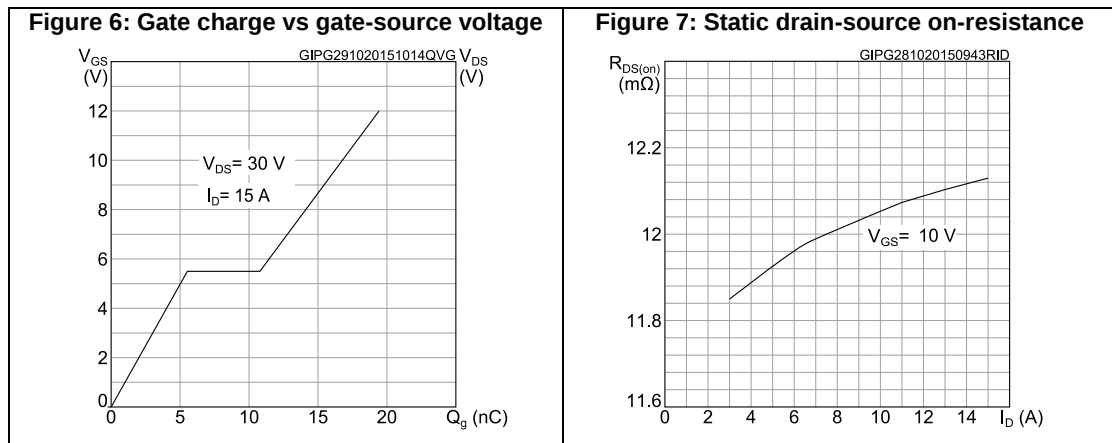
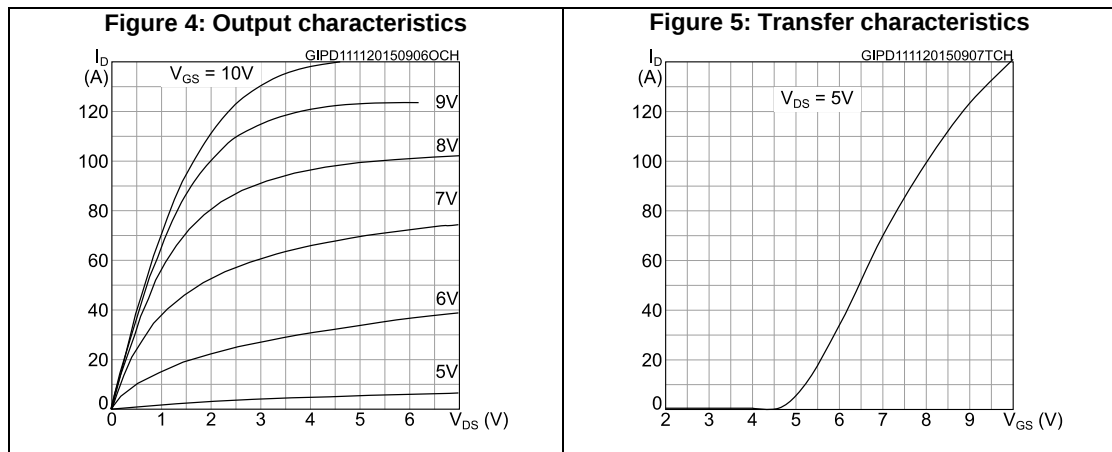
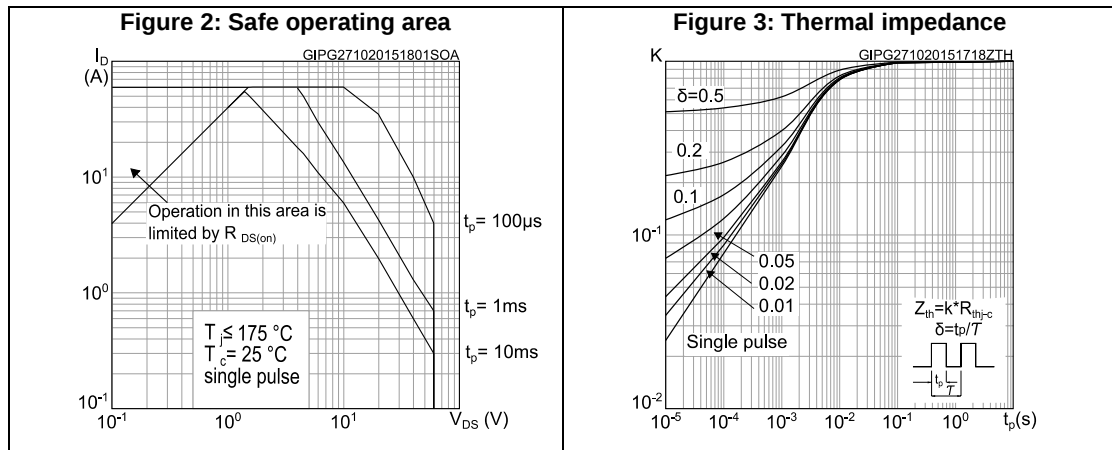


Figure 8: Capacitance variations

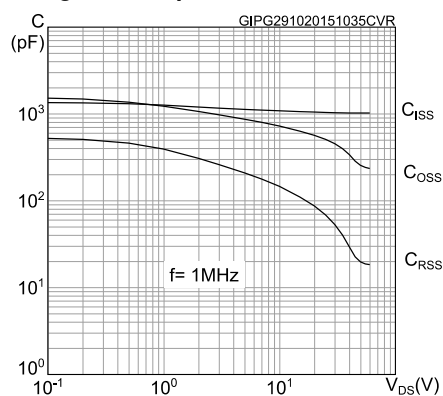


Figure 9: Normalized gate threshold voltage vs temperature

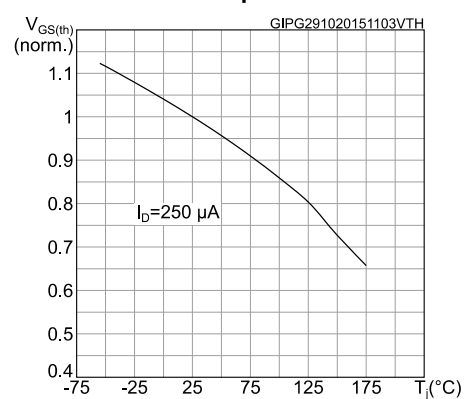


Figure 10: Normalized on-resistance vs temperature

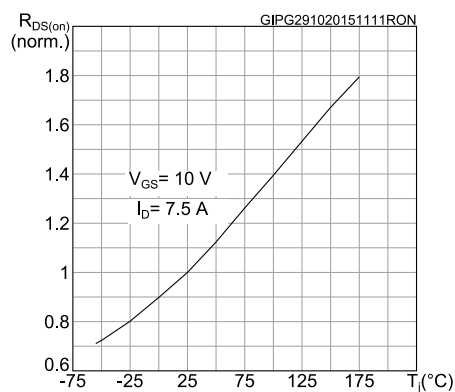


Figure 11: Normalized V(BR)DSS vs temperature

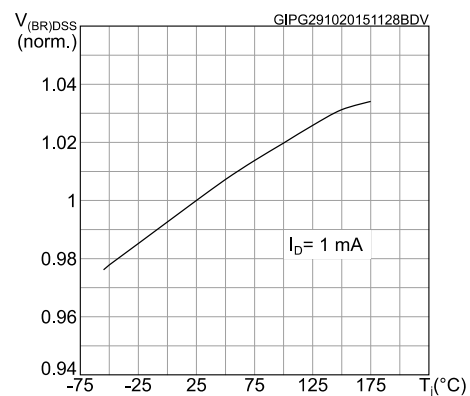
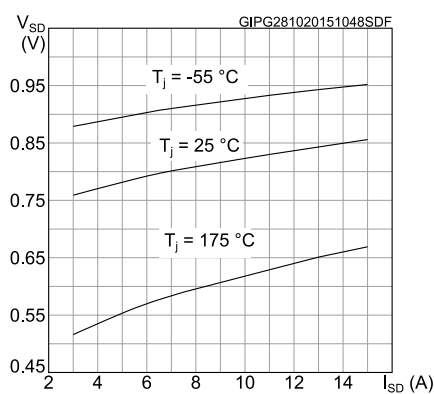
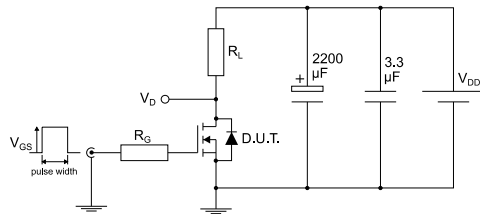


Figure 12: Source-drain diode forward characteristics



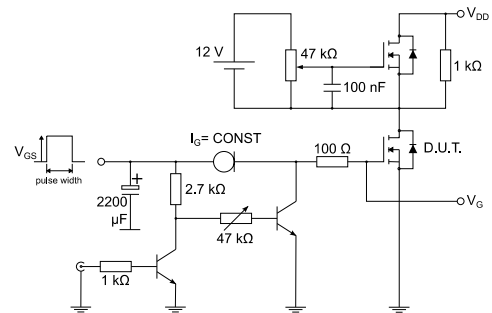
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



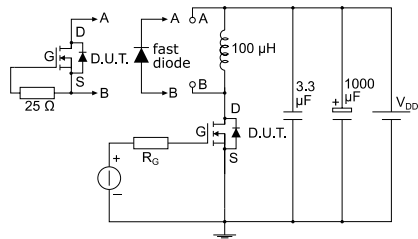
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**Figure 14: Test circuit for gate charge behavior**



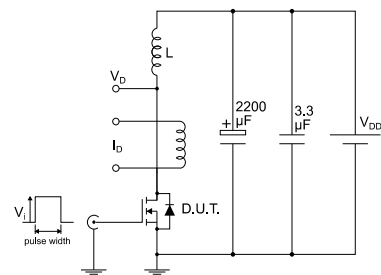
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



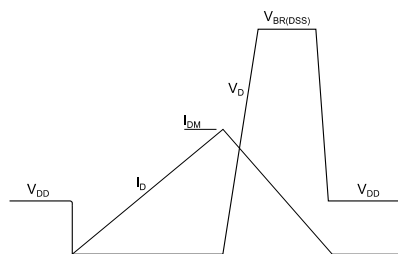
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**Figure 16: Unclamped inductive load test circuit**



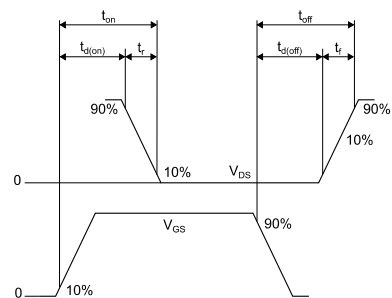
AM01471v1

**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 DPAK(TO-252) type A package information

Figure 19: DPAK (TO-252) type A package outline

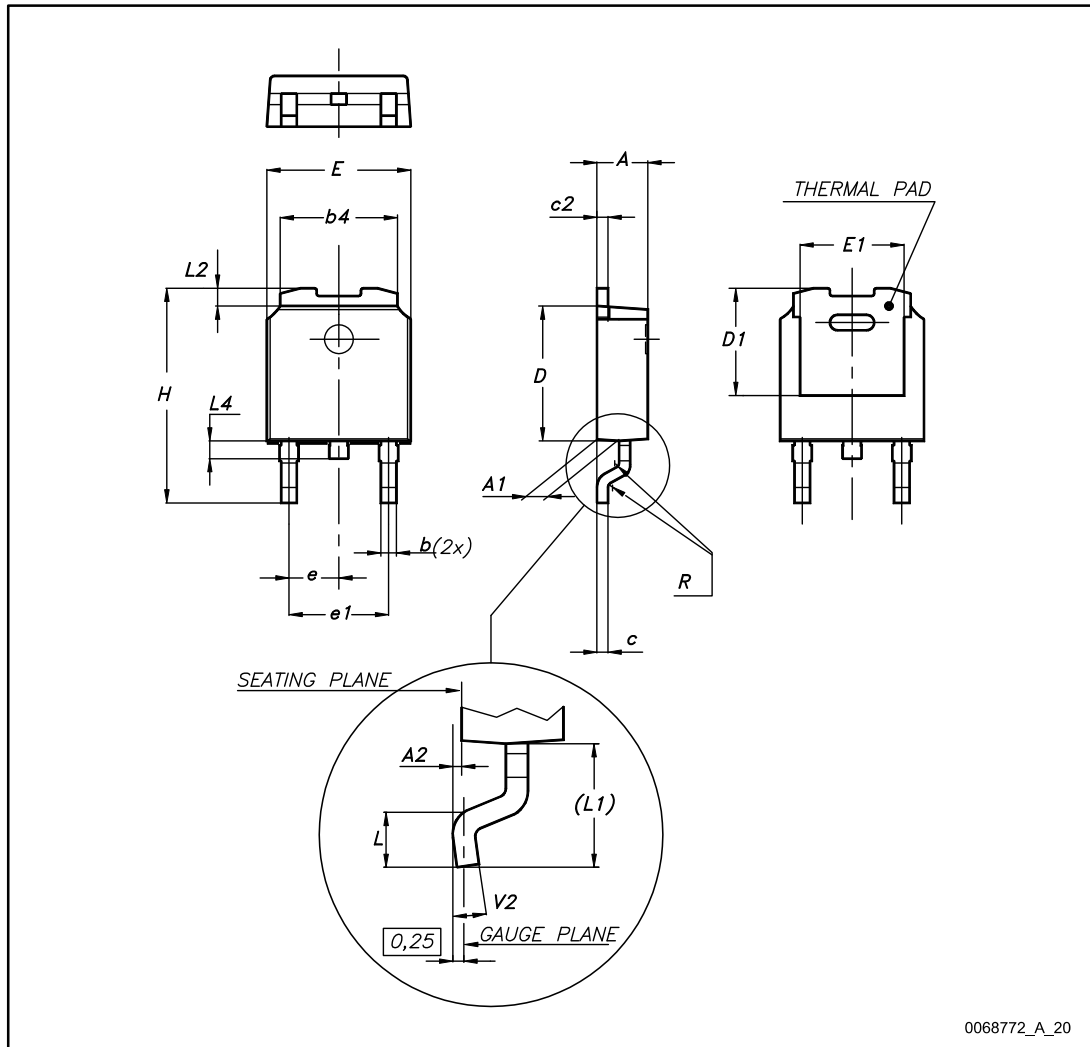
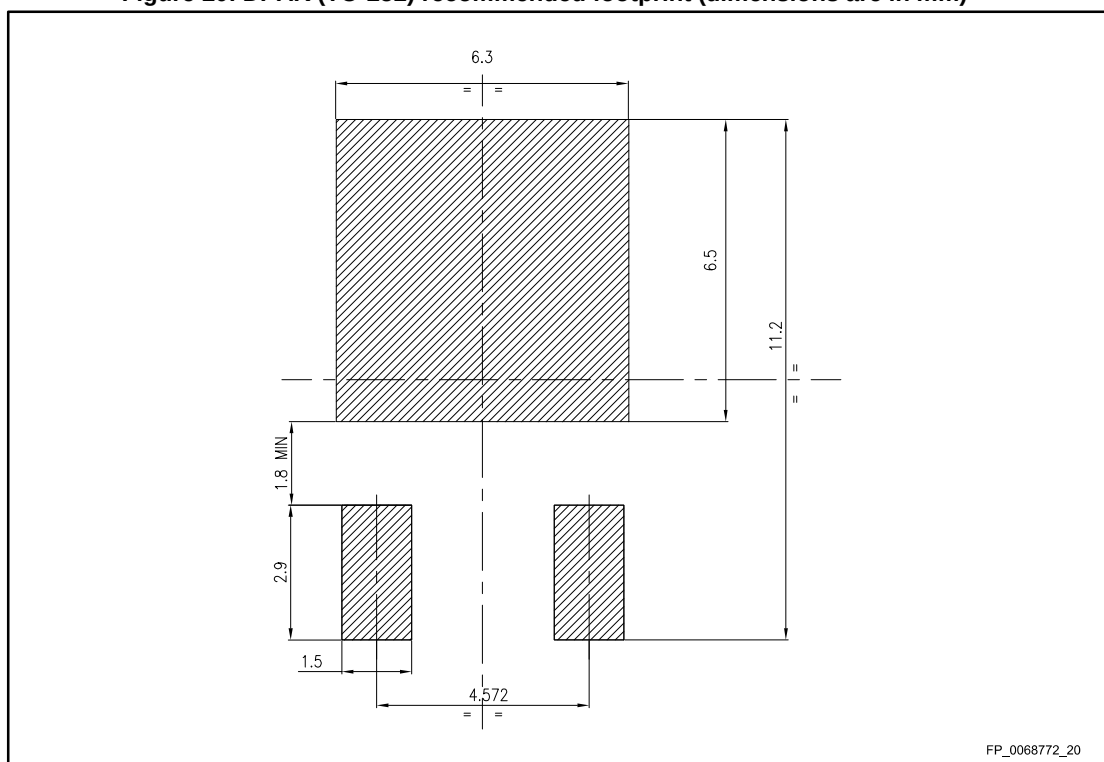


Table 8: DPAK (TO-252) type A mechanical data

| Dim. | mm   |      |       |
|------|------|------|-------|
|      | Min. | Typ. | Max.  |
| A    | 2.20 |      | 2.40  |
| A1   | 0.90 |      | 1.10  |
| A2   | 0.03 |      | 0.23  |
| b    | 0.64 |      | 0.90  |
| b4   | 5.20 |      | 5.40  |
| c    | 0.45 |      | 0.60  |
| c2   | 0.48 |      | 0.60  |
| D    | 6.00 |      | 6.20  |
| D1   | 4.95 | 5.10 | 5.25  |
| E    | 6.40 |      | 6.60  |
| E1   | 4.60 | 4.70 | 4.80  |
| e    | 2.16 | 2.28 | 2.40  |
| e1   | 4.40 |      | 4.60  |
| H    | 9.35 |      | 10.10 |
| L    | 1.00 |      | 1.50  |
| (L1) | 2.60 | 2.80 | 3.00  |
| L2   | 0.65 | 0.80 | 0.95  |
| L4   | 0.60 |      | 1.00  |
| R    |      | 0.20 |       |
| V2   | 0°   |      | 8°    |

Figure 20: DPAK (TO-252) recommended footprint (dimensions are in mm)



## 4.2 Packing information

Figure 21: DPAK (TO-252) tape outline

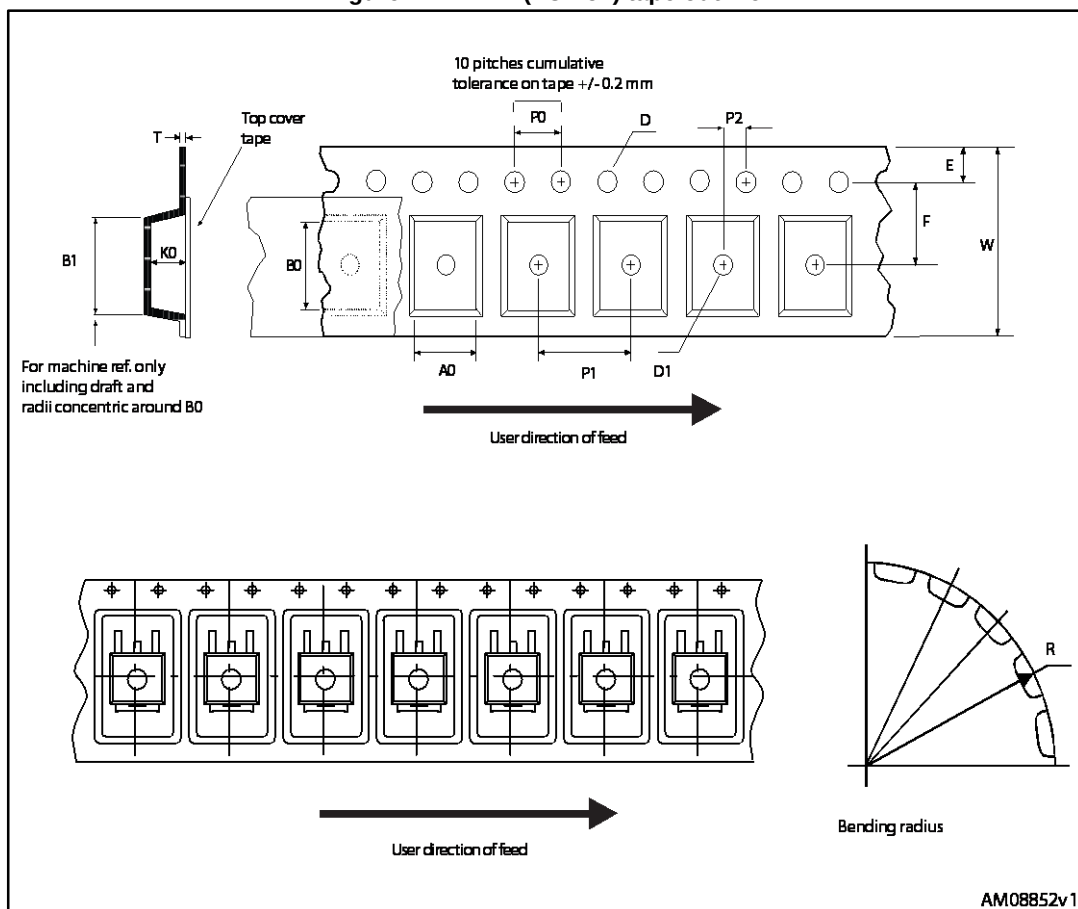


Figure 22: DPAK (TO-252) reel outline

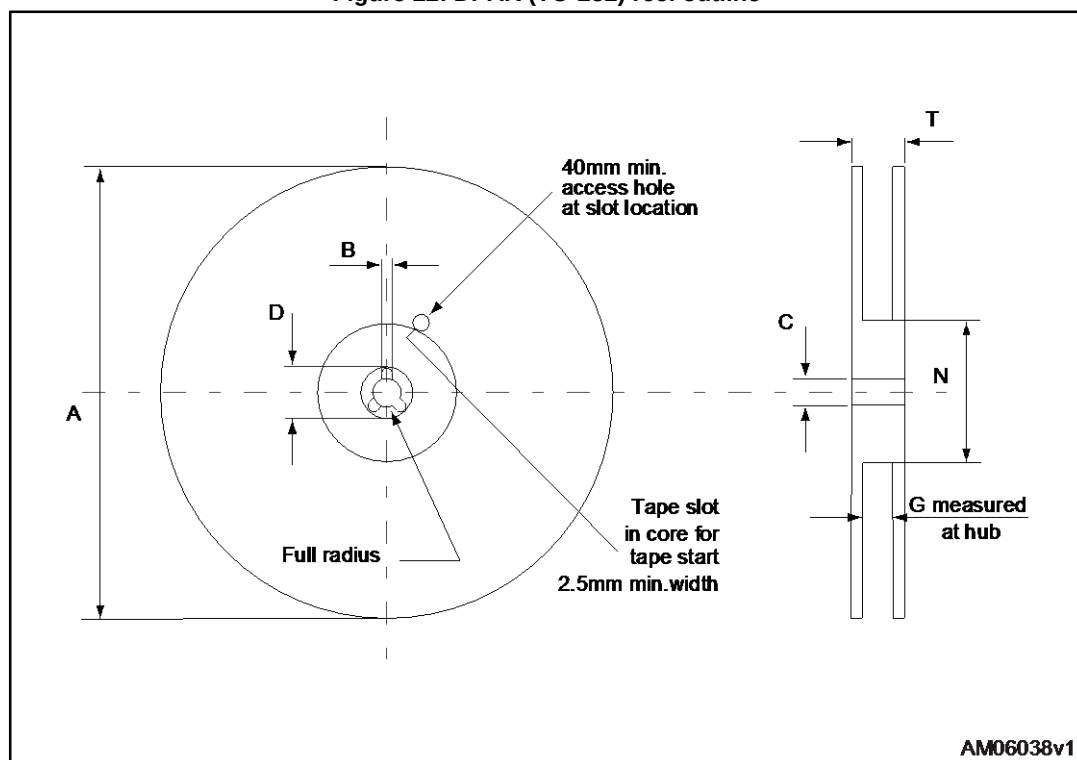


Table 9: DPAK (TO-252) tape and reel mechanical data

| Tape |      |      | Reel      |      |      |
|------|------|------|-----------|------|------|
| Dim. | mm   |      | Dim.      | mm   |      |
|      | Min. | Max. |           | Min. | Max. |
| A0   | 6.8  | 7    | A         |      | 330  |
| B0   | 10.4 | 10.6 | B         | 1.5  |      |
| B1   |      | 12.1 | C         | 12.8 | 13.2 |
| D    | 1.5  | 1.6  | D         | 20.2 |      |
| D1   | 1.5  |      | G         | 16.4 | 18.4 |
| E    | 1.65 | 1.85 | N         | 50   |      |
| F    | 7.4  | 7.6  | T         |      | 22.4 |
| K0   | 2.55 | 2.75 |           |      |      |
| P0   | 3.9  | 4.1  | Base qty. |      | 2500 |
| P1   | 7.9  | 8.1  | Bulk qty. |      | 2500 |
| P2   | 1.9  | 2.1  |           |      |      |
| R    | 40   |      |           |      |      |
| T    | 0.25 | 0.35 |           |      |      |
| W    | 15.7 | 16.3 |           |      |      |

## 5 Revision history

Table 10: Document revision history

| Date        | Revision | Changes                                                       |
|-------------|----------|---------------------------------------------------------------|
| 16-Dec-2015 | 1        | First release.                                                |
| 26-Jan-2016 | 2        | Document status promoted from preliminary to production data. |

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