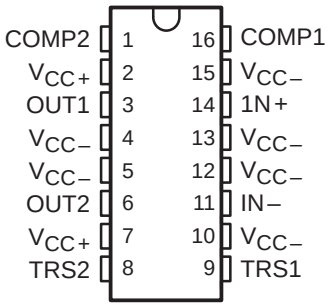
- **High Output Drive Capability . . . 1 A Min**
- **3-State Outputs**
- **High Gain-Bandwidth Product 8 MHz Typ**
- **Low Total Harmonic Distortion <0.08% Typ**
- **High Slew Rate . . . 12 V/μs Typ**
- **Class AB Output Stage**
- **Thermal Shutdown**
- **Mains-Line Driver Circuit Application Included**

NE PACKAGE
(TOP VIEW)



Terminals 4, 5, 12 and 13 are connected to the lead frame.

description

The TLE2301 is a power operational amplifier that can deliver an output current of 1 A at high frequencies with very low total harmonic distortion. The device has an integral 3-state mode to drive the output stage into a high-impedance state and also to reduce the supply current to less than 3.5 mA.

The combination of high output current and 3-state outputs makes the TLE2301 ideal for implementing the signalling transformer driver in mains-based telemetering modems. This combination of features also makes the device well suited for other high-current applications (e.g., motor drivers and audio circuits).

Using the Texas Instruments established Excalibur process, the TLE2301 is able to achieve slew rates in excess of 12 V/μs and a gain-bandwidth product of 8 MHz. The TLE2301 uses a 16-pin NE power package to provide better power handling capabilities than standard dual-in-line packages.

The TLE2301 is characterized for operation over the industrial temperature range of –40°C to 85°C.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

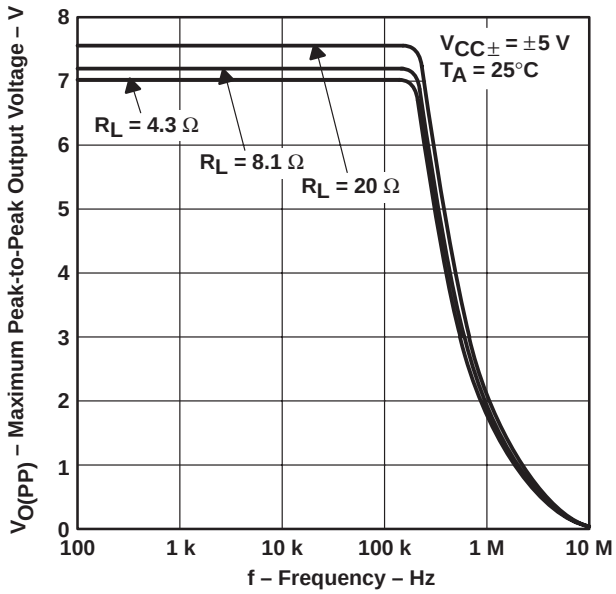


Figure 1

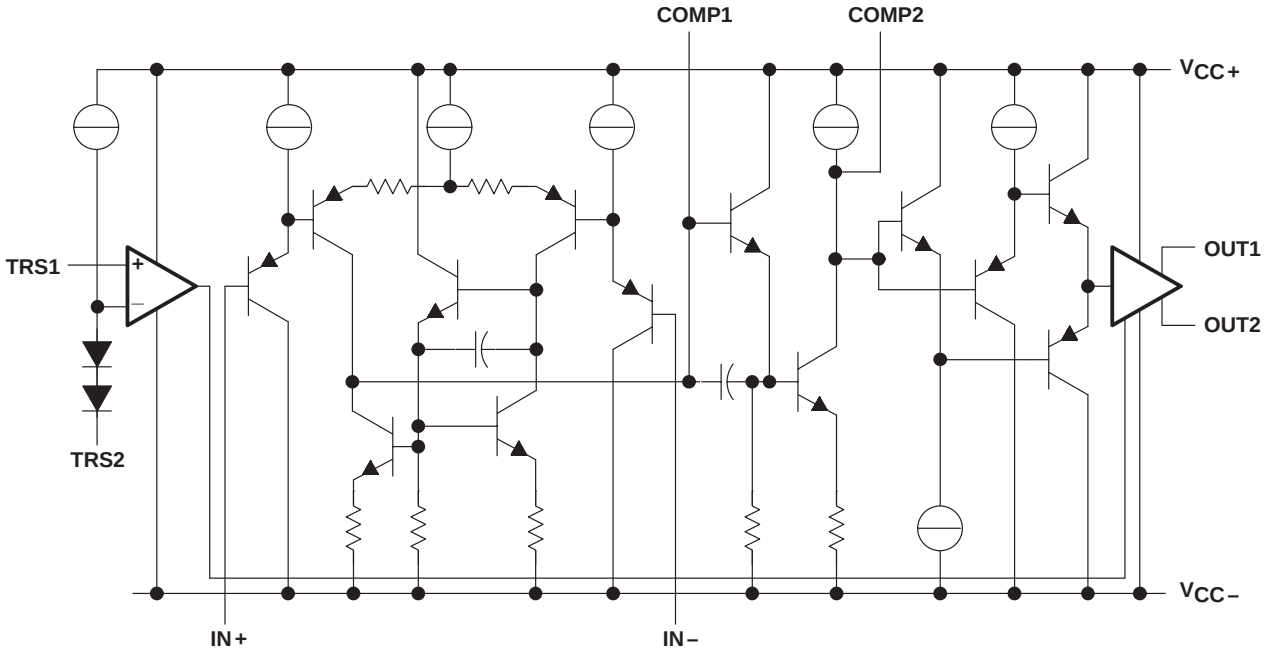
AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE
		THERMALLY-ENHANCED PLASTIC DIP (NE)
–40°C to 85°C	10 mV	TLE2301INE

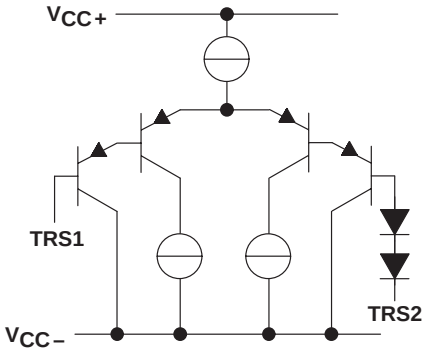
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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equivalent schematic (entire device)



equivalent schematic (TRS1 and TRS2 inputs)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
COMP1 COMP2	16 1	COMP1 and COMP2 are compensation network terminals
IN+	14	Noninverting input
IN–	11	Inverting input
OUT1 OUT2	3 6	Two low-distortion class-AB output stages. Each is capable of sourcing more than 500 mA. OUT1 and OUT2 should be connected together for all applications.
TRS1 TRS2	9 8	TRS1 and TRS2 are 3-state input terminals. TRS2 should be connected to the ground of the circuit generating the 3-state command (normally μP ground). The TLE2301 is brought into 3-state mode by raising TRS1 2 V above TRS2. Placing the TLE2301 in a 3-state mode reduces the supply current to below 2.2 mA (typ). Normal operation resumes by bringing TRS1 to within 0.8 V of TRS2. The 3-state function can be disabled by connecting both TRS1 and TRS2 to V_{CC-}.
V_{CC-}	10, 15	High-impedance V_{CC-} input terminals. Although these do not carry any of the device's supply current, they increase the stability of the device and should be connected to the negative supply terminal (V_{CC-}).
V_{CC-}	4, 5, 12, 13	Negative supply terminals and substrate. As with all NE packages, the substrate is directly connected to the lead frame. The result is that the junction-to-ambient thermal impedance ($Z_{\theta JA}$) is greatly reduced by soldering the negative supply terminals to the copper area of the printed-circuit board (PCB).
V_{CC+}	2, 7	Positive supply terminals. Both terminals should be connected to the positive voltage supply.

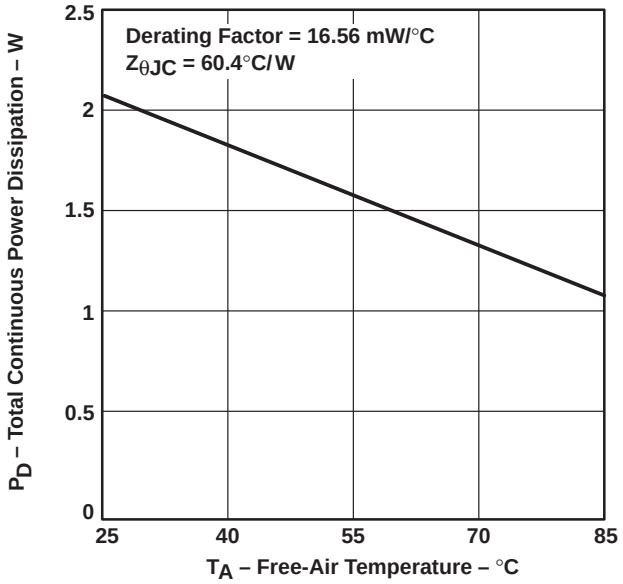
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	–22 V
Differential input voltage, V_{ID} (see Note 2)	±44 V
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 4 and 5)	2075 mW
Continuous total dissipation at 85°C case temperature (see Note 5)	4640 mW
Operating free-air temperature range, T_A	–40°C to 85°C
Operating case or virtual junction temperature range	–40°C to 150°C
Storage temperature range	–65°C to 150°C

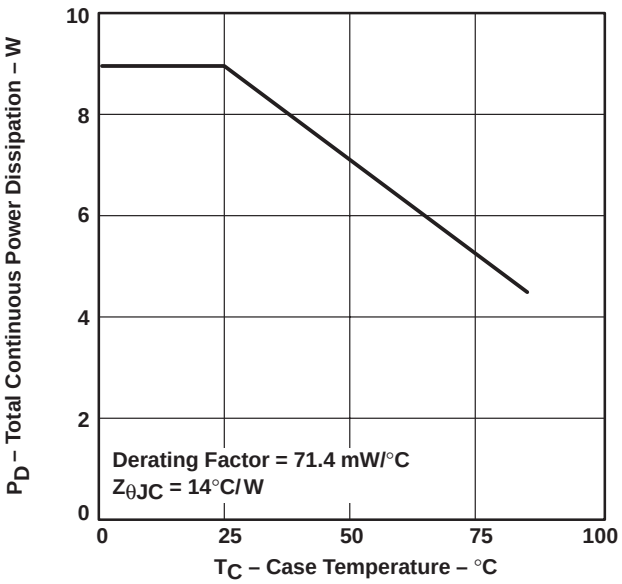
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The outputs when connected together may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 16.56 mW/°C.
5. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE



CASE TEMPERATURE DISSIPATION DERATING CURVE



recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±4.5	±20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	–4	1.6	V
	$V_{CC\pm}$ = ±15 V	–14	11.8	V
High-level 3-state enable voltage, V_{IH}		2		V
Low-level 3-state enable voltage, V_{IL}			0.8	V
Continuous output current			1	A
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V, C_C = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		0.4	7	mV
				Full range			10	
I_{IB}	Input bias current	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		283	450	nA
				Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		Full range	–4 to 1.6			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	3.3	3.5		V
				Full range	3.2			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	–3.2	–3.4		V
				Full range	–3.1			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2 V, R_L = 20 Ω	V_{IC} = 0,	25°C	65	87		dB
				Full range	60			
r_i	Differential input resistance			25°C		1		MΩ
r_o	Output resistance (see Note 7)	TRS1 = 0.8 V		25°C		1		Ω
		TRS1 = 2 V,	3-state mode			100		kΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	V_O = 0,	25°C	65	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4.5 V to ±20 V, V_{IC} = 0,	No load	25°C	70	100		dB
I_{IH}	Enable input current, high	V_I = 2 V,	3-state mode	25°C		0.01	0.5	µA
				Full range			0.5	
I_{IL}	Enable input current, low	V_I = 0.8 V		25°C		0.01	0.5	µA
				Full range			0.5	
I_{OS}	Short-circuit output current (see Note 8)	V_O = 0,	$t_p \le 50$ µs	25°C	1	1.8		A
I_{CC}	Supply current	V_O = 0,	No load	25°C		10	21	mA
				Full range			25	
		V_O = 0, 3-state mode	No load,	25°C		1.73	2.7	
				Full range			3.5	

† Full range is –40°C to 85°C.

NOTES: 6. OUT1 and OUT2 are connected together for all tests.
7. TRS1 voltage is measured with respect to TRS2 potential.
8. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately (t_p = pulse duration time).

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, C_C = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		0.3	10	mV
				Full range			15	
I_{IB}	Input bias current	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		260	450	nA
				Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		Full range	–14 to 11.8			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	13	13.5		V
				Full range	13			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	–12.6	–13		V
				Full range	–12.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±6 V, R_L = 20 Ω	V_{IC} = 0,	25°C	70	102		dB
				Full range	65			
r_i	Differential input resistance			25°C		1		MΩ
r_o	Output resistance (see Note 7)	TRS1 = 0.8 V		25°C		1		Ω
		TRS1 = 2 V,	3-state mode			100		kΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	V_O = 0,	25°C	70	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4.5 V to ±20 V, V_{IC} = 0,	No load	25°C	70	100		dB
I_{IH}	Enable input current, high	V_I = 2 V,	3-state mode	25°C		0.01	0.5	µA
				Full range			0.5	
I_{IL}	Enable input current, low	V_I = 0.8 V		25°C		0.01	0.5	µA
				Full range			0.5	
I_{OS}	Short-circuit output current (see Note 8)	V_O = 0,	$t_p \le 50$ µs	25°C	1	3		A
I_{CC}	Supply current	V_O = 0,	No load	25°C		11	25	mA
				Full range			30	
		V_O = 0, 3-state mode	No load,	25°C		2.2	3.5	
				Full range			5	

† Full range is –40°C to 85°C.

NOTES: 6. OUT1 and OUT2 are connected together for all tests.
7. TRS1 voltage is measured with respect to TRS2 potential.
8. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately (t_p = pulse duration time).

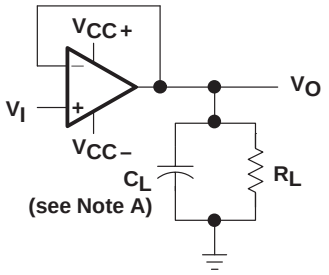
operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V, C_C = 15 pF, T_A = 25°C (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	V_O = ±1.5 V, R_L = 20 Ω, C_L = 100 pF	9	12		V/μs
t_s	Settling time (see Figure 1)	R_L = 20 Ω, C_L = 100 pF, 3-V step to 30 mV (1%)		0.7		μs
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 50 Ω, f = 1 kHz		44		nV/√Hz
THD	Total harmonic distortion	V_O = 1 V_{rms}, f = 50 kHz, R_L = 20 Ω, C_L = 100 pF		0.04%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		8		MHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		30°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, C_C = 15 pF, T_A = 25°C (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	V_O = ±10 V, R_L = 20 Ω, C_L = 100 pF	9	14		V/μs
t_s	Settling time (see Figure 1)	R_L = 20 Ω, C_L = 100 pF, 20-V step to 200 mV (1%)		1.8		μs
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 50 Ω, f = 1 kHz		44		nV/√Hz
THD	Total harmonic distortion	V_O = 2 V_{rms}, f = 50 kHz, R_L = 20 Ω, C_L = 100 pF		0.08%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		8		MHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		35°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes the fixture capacitance.

Figure 2. Slew-Rate Test Circuit

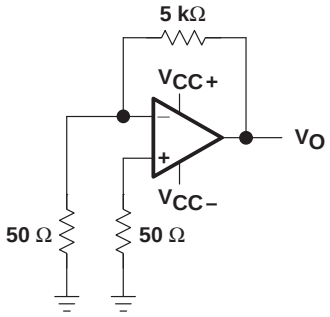
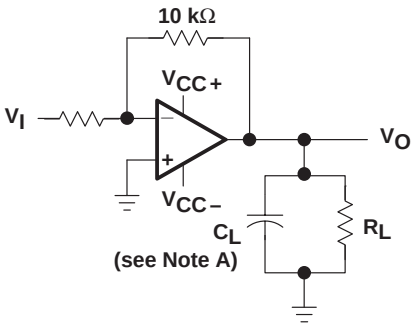


Figure 3. Noise-Voltage Test Circuit



NOTE A: C_L includes the fixture capacitance.

Figure 4. Gain-Bandwidth and Phase-Margin Test Circuit

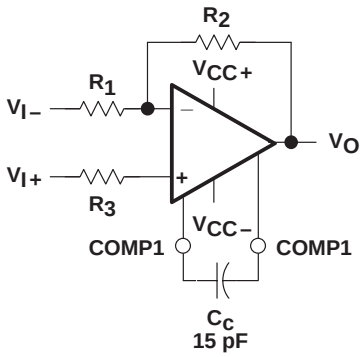


Figure 5. Compensation Configuration

typical values

Typical values presented in this data sheet represent the median (50% point) of the device parametric performance.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	6, 7
I_{IO}	Input offset current	vs Free-air temperature	6, 7
A_{VD}	Differential voltage amplification	vs Frequency	8
		vs Free-air temperature	9
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	10, 11
V_{OM}	Maximum peak output voltage	vs Output current	12, 13
		vs Supply voltage	14
$Z_{\theta JA}$	Transient junction-to-ambient thermal impedance	vs Time	15
I_{CC}	Supply current	vs Supply voltage	16
		vs Free-air temperature	17
	Pulse response	Small signal	18, 19
		Large signal	20, 21
z_o	Output impedance	vs Frequency	22, 23

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

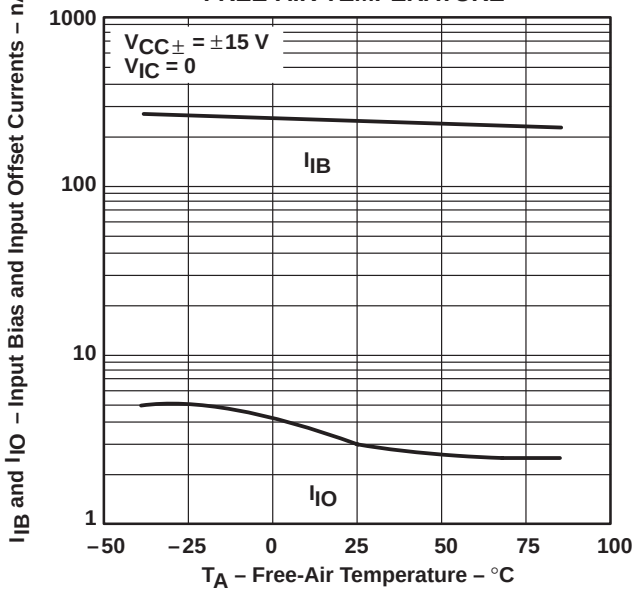


Figure 6

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

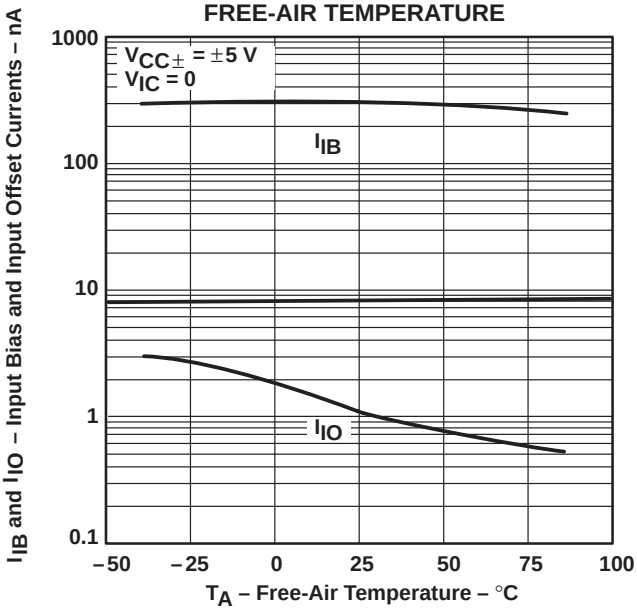


Figure 7

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

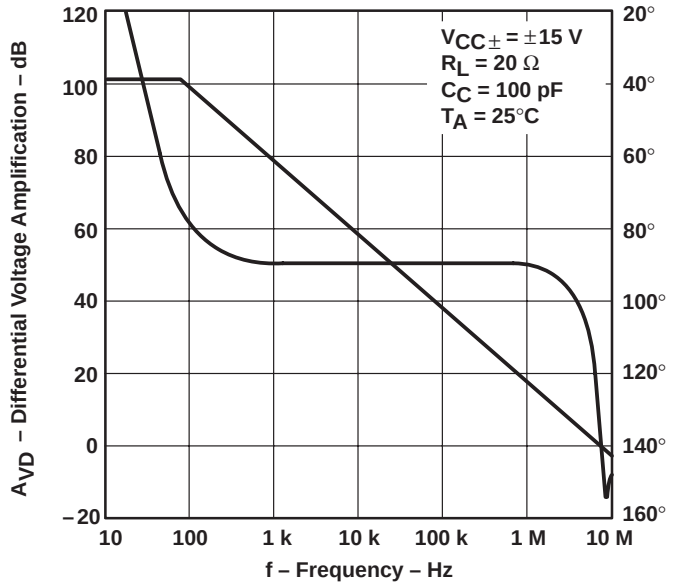


Figure 8

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

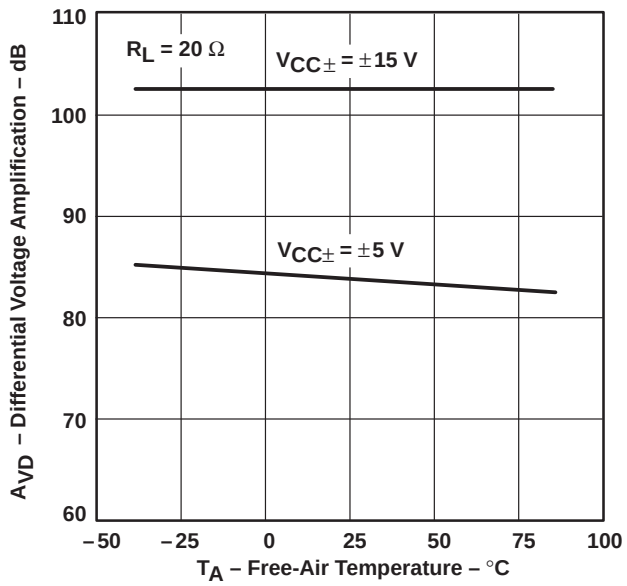


Figure 9

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

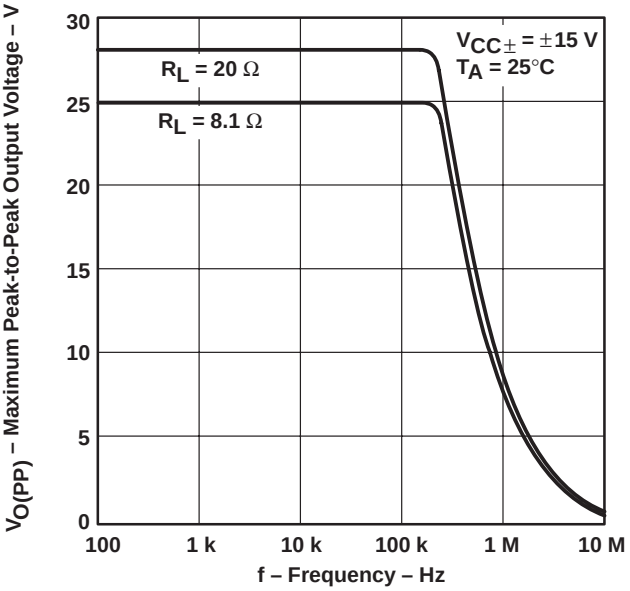


Figure 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

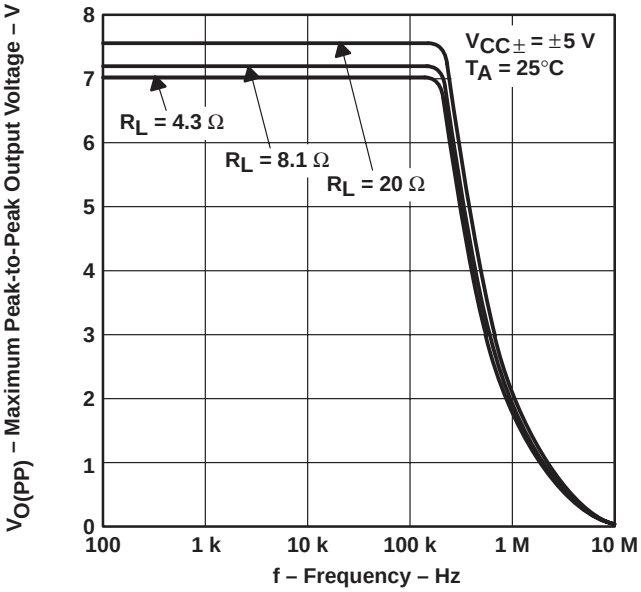


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

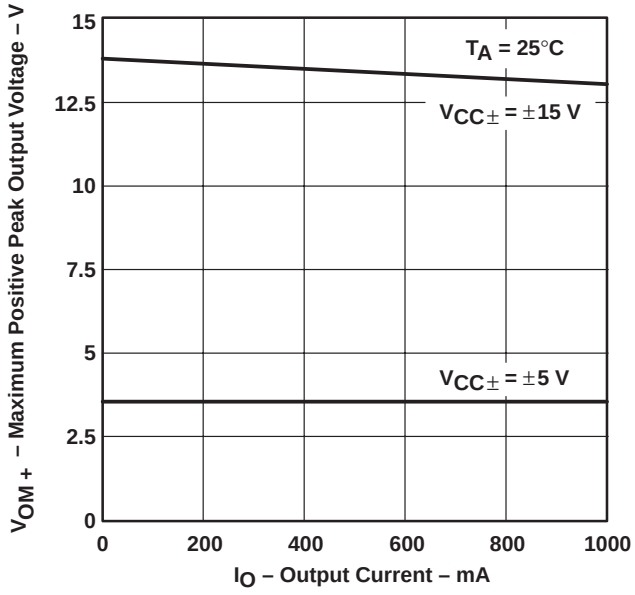


Figure 12

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

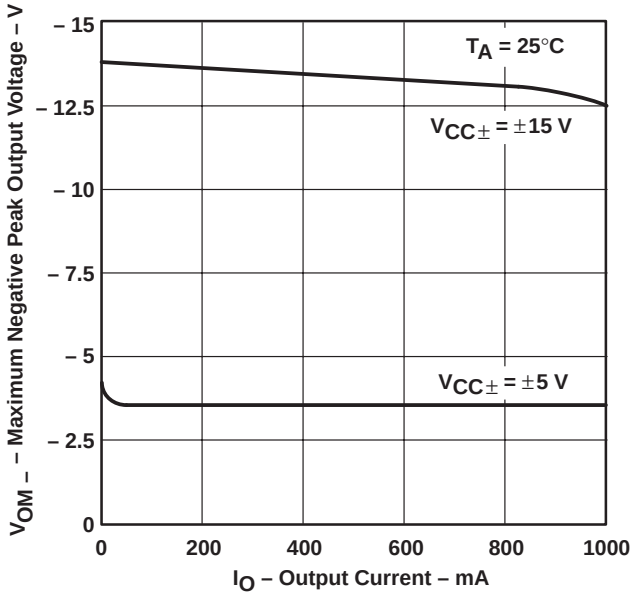


Figure 13

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

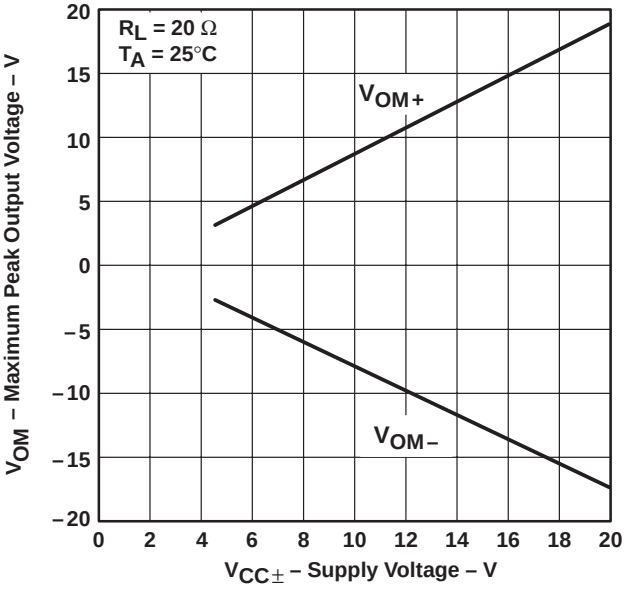


Figure 14

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE†
vs
ON TIME

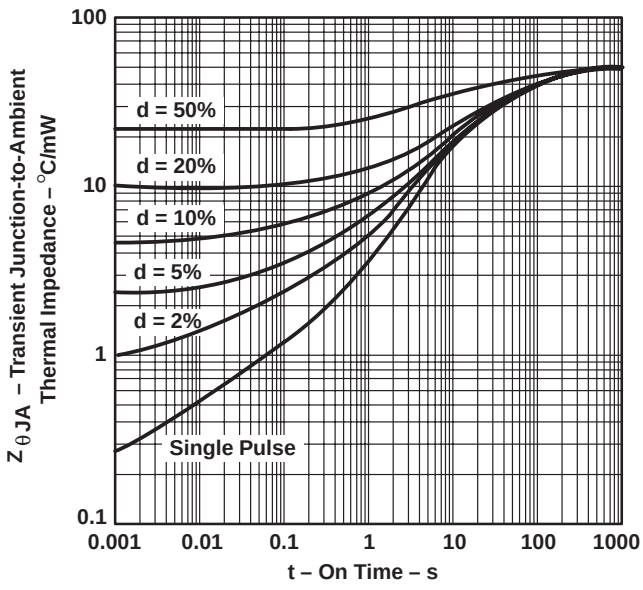


Figure 15

† d = duty cycle

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

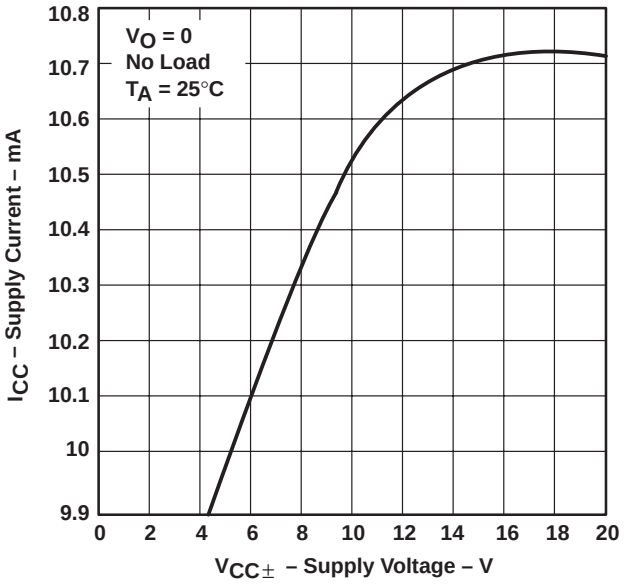


Figure 16

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

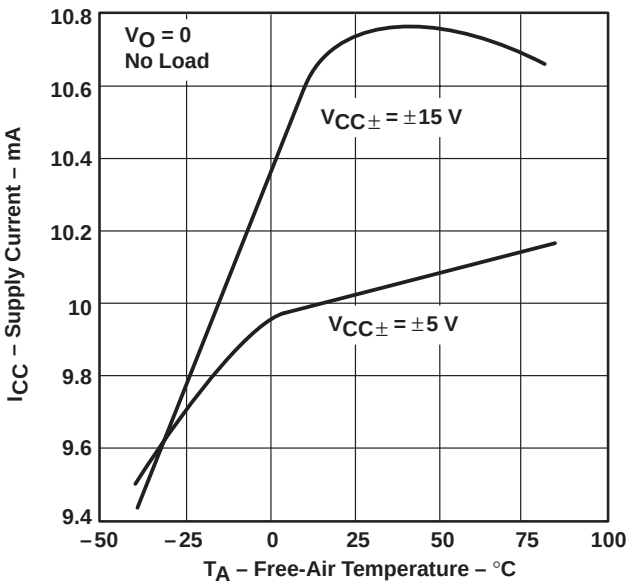


Figure 17

VOLTAGE FOLLOWER SMALL-SIGNAL PULSE RESPONSE

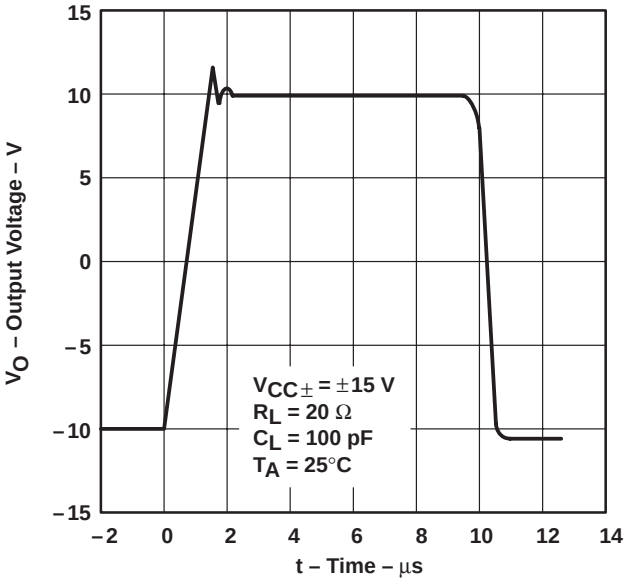


Figure 18

VOLTAGE FOLLOWER SMALL-SIGNAL PULSE RESPONSE

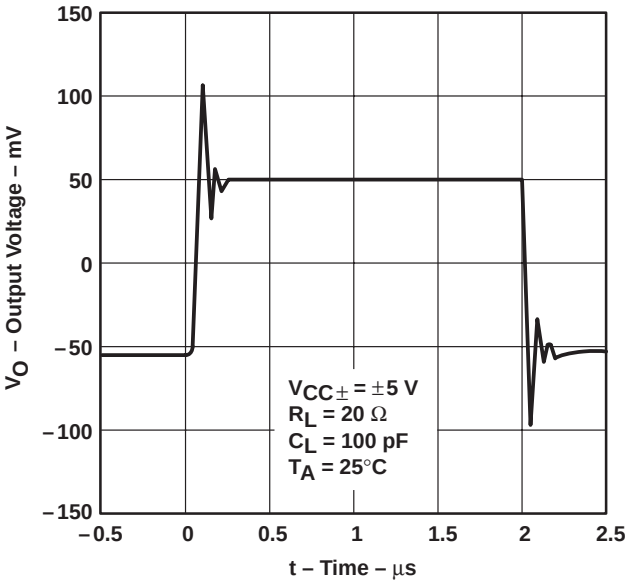


Figure 19

TYPICAL CHARACTERISTICS

VOLTAGE FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

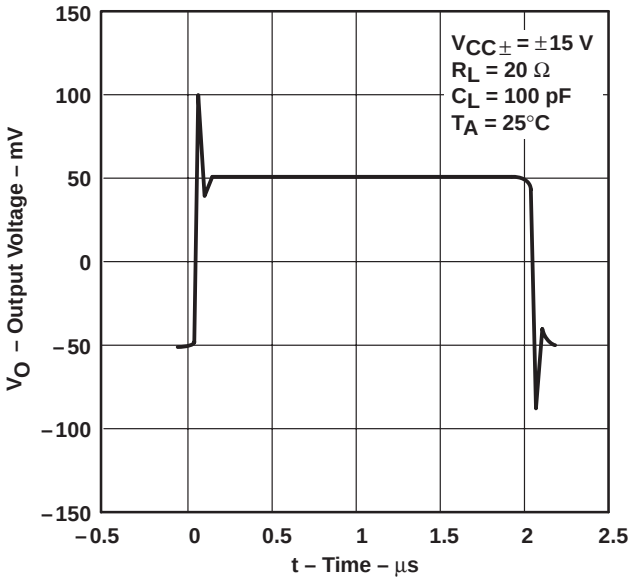


Figure 20

VOLTAGE FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

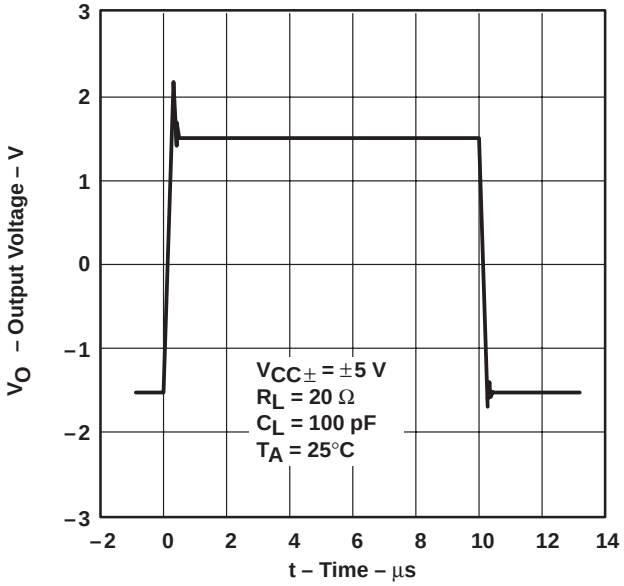


Figure 21

OUTPUT IMPEDANCE
vs
FREQUENCY

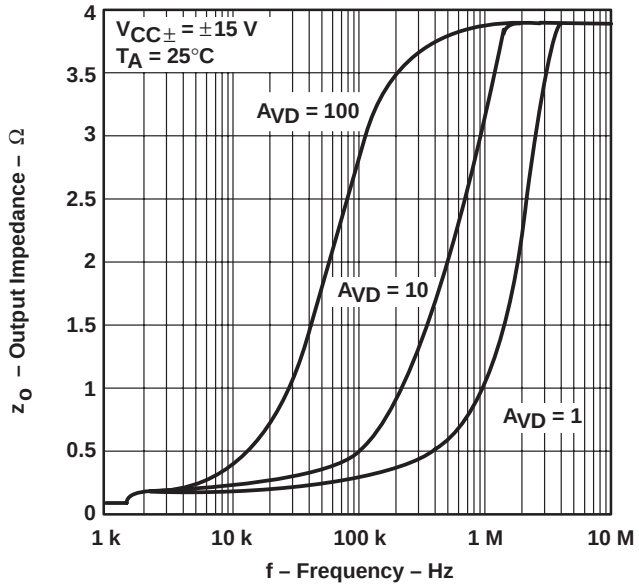


Figure 22

OUTPUT IMPEDANCE
vs
FREQUENCY

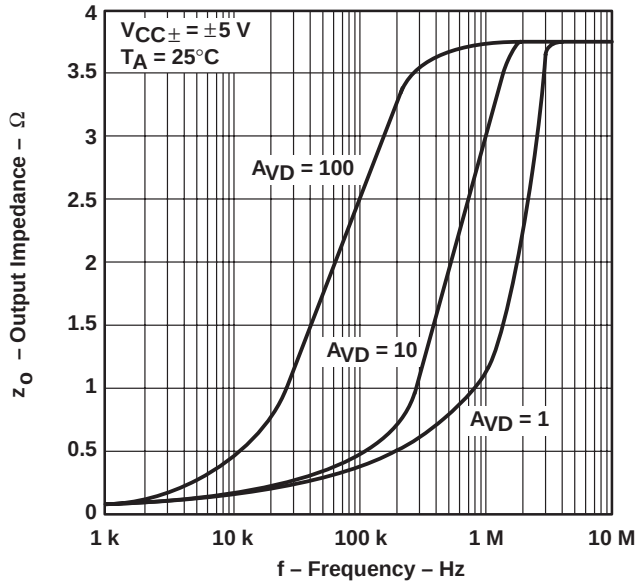


Figure 23

APPLICATION INFORMATION

circuit for mains-line driver over 40-kHz-to-90-kHz utility band

The following application is a circuit for *a mains-line driver over 40-kHz-to-90-kHz utility band* and is based around the European standard (EN56065–1) describing utility and consumer applications. This example shows a possible implementation for differential transmission on the mains line. This applications circuit is designed around the requirements of a domestic electricity meter operating over a utility band of 40 kHz to 90 kHz. A dual-rail power supply of ±5 V is used for this design example to limit device power dissipation. The same design principles, however, can be applied to other applications.

frequency band

The frequency band for utility applications extends over an enormous range from 3 kHz to 95 kHz. In order to have a coupling network that is economical and implemented with readily available components, this circuit is designed for a subband from 40 kHz to 90 kHz.

This subband is sufficiently wide to support multichannel operation; i.e., 10 channels of 5 kHz width or more if the channel widths are smaller. To avoid transmission spillover into the next band, a guard band of 5 kHz is allowed. The upper frequency of this circuit is set to 90 kHz, and the lower frequency is chosen for an economical coupling network and still has sufficient bandwidth to support multichannel operation.

output drive

The impedance of the mains network at these signalling frequencies is relatively low (<1 Ω to 30 Ω). This circuit has been designed to drive a 4-Ω mains line over the 40-kHz-to-90-kHz bandwidth.

The signalling impedance of the mains network fluctuates as different loads are switched on during the day or over a season, and it is influenced by many factors such as:

- Localized loading from appliances connected to the mains supply near to the connection of the communication equipment; e.g., heavy loads such as cookers and immersion heaters and reactive loads such as EMC filters and power factor correctors
- Distributed loading from consumers connected to the same mains cable, where their collective loading reduces the mains signalling impedance during times of peak electricity consumption; e.g., meal times
- Network parameters; e.g., transmission properties of cables and the impedance characteristics of distribution transformers and other system elements

With such a diversity of factors, the signalling environment fluctuates enormously, irregularly, and can differ greatly from one installation to another. The signalling system should be designed for reliable communications over a wide range of mains impedances and signalling conditions. Consequently, the transmitter must be able to drive sufficient signal into the mains network under these loading conditions.

The TLE2301 amplifier has 1-A output drive capability with short-circuit protection; hence, it adequately copes with the high current demands required for implementing mains signalling systems.

3-state facility

When transmitting, the transmitter appears as a low-impedance signal source on the mains network. If transmitters are left in the active mode whether transmitting or not and a large number of transmitters are installed in close proximity, their combined loading would reduce the mains impedance to unacceptable levels. Not only would each transmitter need to drive into an extremely low mains impedance, but signals arriving from distant transmitters would be severely attenuated.

To overcome this problem, the transmitters need to present a high impedance to the mains network when they are not transmitting. The mains network is then only loaded by a few transmitters at any one time, and the mains signalling impedance is not adversely affected.

APPLICATION INFORMATION

3-state facility (continued)

The TLE2301 incorporates an output 3-state facility, removing the need for additional circuitry to achieve this function. In addition, the TLE2301 has a low standby current in the 3-state mode, making it ideal for applications where low power consumption is also essential.

circuit configuration

The design methodology is to minimize power dissipation in the TLE2301 by maximizing the use of the available output voltage swing of the amplifier. The amplifier's output can swing to within 2 V of the supply rail before saturation begins. With a chosen supply of ± 5 V, the maximum peak-to-peak voltage swing is 6 V. To ensure that the amplifier's output is not likely to clip under heavy loads, the maximum output voltage swing has been reduced by 0.5 V, giving a usable peak-to-peak output voltage swing of 5.5 V.

It is assumed that the input signal to the transmitter stage has a peak-to-peak amplitude of 2.8 V (1 Vrms) as might be expected if the transmission signal is digitally synthesized by circuitry operating solely from the 5-V supply. The gain of the amplifier stage is appropriately set to:

$$\text{Gain} = \frac{\text{peak-to-peak output voltage swing}}{\text{peak-to-peak input voltage}}$$

$$= \frac{5.5\ \text{V}}{2.8\ \text{V}}$$

$$= 1.96$$

An inverting amplifier configuration is chosen for this example, as the input signal source is assumed to have a relatively low impedance in relation to the gain-setting resistors.

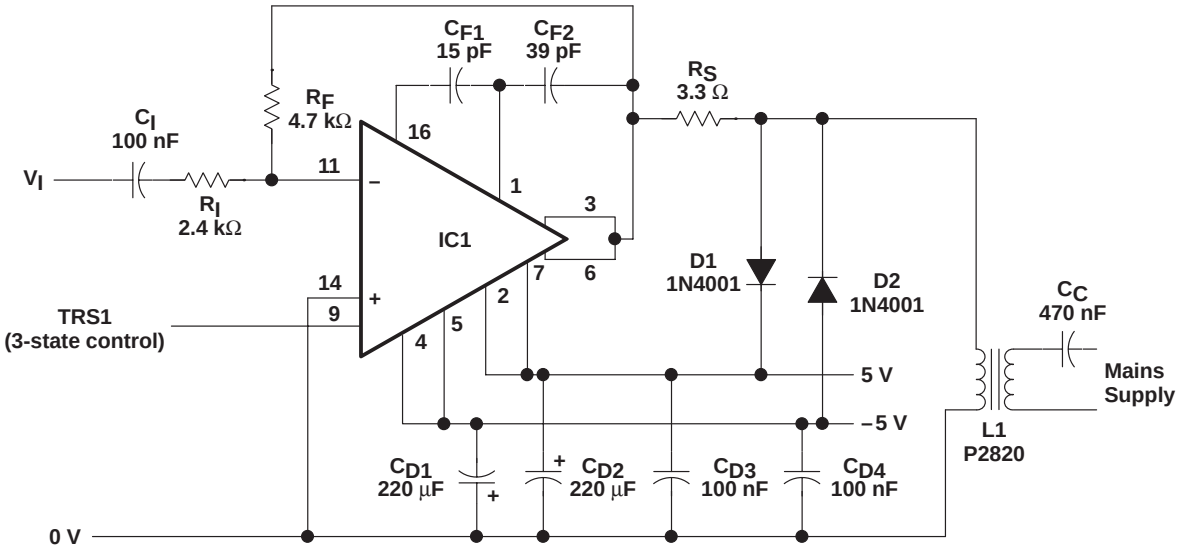


Figure 24. Full-Circuit Diagram for Utility Band

A noninverting amplifier configuration could be used when the input signal needs to be terminated with high impedance, but the user should take care that the amplitude of the input signal does not exceed the common-mode input range ($-4\ \text{V} < V_{ICM} < 1.8\ \text{V}$ at $V_{CC} = \pm 5\ \text{V}$) for low-gain implementations.

APPLICATION INFORMATION

component calculations

The following sections contain the calculations for input capacitors, gain resistors, coupling network, coupling capacitors, transformer-leakage inductance, series resistors, decoupling, and frequency compensation.

input capacitor

The incoming signal is ac coupled to remove any incoming dc offset and to provide only unity gain for the amplifier's input offset voltage. The value of 100 nF is chosen for this input capacitor as it has very little influence on the amplifier's signal gain over the frequency band.

gain resistors

The gain-setting resistors are chosen for a gain of 1.96; i.e., choosing:

$$\text{Gain} = \frac{R_F}{R_I}$$

$$R_F = 4.7\ \text{k}\Omega \text{ and } R_I = 2.4\ \text{k}\Omega$$

$$= \frac{4.7\ \text{k}\Omega}{2.4\ \text{k}\Omega}$$

$$= 1.96$$

The resistor values are low enough to ensure that the circuit does not suffer from stray capacitance and signal pick-up problems but not too low as to significantly load the mains impedance when the amplifier is in its high-impedance state.

coupling network

The function of the line interface is to provide isolation from the mains supply while coupling the communication signals onto the mains network. As the mains voltage is large in comparison with the communication signals, the mains voltage needs to be isolated from the electronic circuitry. The simple coupling network limits the current flowing from the mains supply as well as providing a convenient point at which to implement the safety isolation barrier between the mains supply and the communications circuitry. The transformer can easily achieve an isolation of 4 kV between primary and secondary windings, and the capacitor provides the low frequency roll-off to impede the mains voltage.

The transformer has two other useful properties. First, the turns ratio can be selected to provide efficient power transfer between the TLE2301 amplifier and the mains network. Second, the transformer possesses leakage inductance that can be tuned with the coupling capacitor to form a band-pass filter.

By altering the turns ratio, the power dissipated in the TLE2301 can be reduced while maintaining the required voltage levels on the mains line. A turns ratio of 1.67:1 was selected in this design to apply a 120-μdBV signal onto the mains line. The calculation for the turns ratio is not straightforward due to the presence of numerous complex impedances. The simplest method for deriving the turns ratio is to model the circuit with an analog simulation program such as PSpice™. It is from these simulations that the 1.67:1 turns ratio has been selected.

PSpice is a registered trademark of MicroSim Corporation.

APPLICATION INFORMATION

coupling capacitor

With such a wide frequency band, the quality factor of the coupling filter needs to be low in order to avoid unacceptably large attenuation at the band edges and to achieve a good coupling performance that is insensitive to a wide range of loads. For a band-pass filter of this configuration, the quality factor is proportional to the reciprocal of the coupling capacitance. For low Q, the value of C_C needs to be large.

Q = quality factor and C_C = coupling capacitor

$$Q \propto \frac{1}{C_C}$$

Counterbalancing this need for a large value of C_C creates two more considerations. First, the capacitance should not be so large as to allow significant 50-Hz mains current through the transformer ($I = 2 \times \pi \times f \times C_C \times V$). Second, the coupling capacitor is required to meet certain safety standards. The coupling capacitor is actually an RFI-suppression capacitor that has been designed by the manufacturers to provide an adequate level of protection when connected across the various conductors of the mains supply (consult the UL1283 or UL1414 standards for RFI capacitors). These types of capacitors can be expensive, physically large, restricted in capacitance value, and limited in the number of manufacturers.

As a reasonable compromise between all these factors, a coupling capacitor of 470 nF is chosen. This value is multisourced, moderately priced, limits the mains current through the transformer to less than 36 mA rms, and has sufficient capacitance to form the desired low-Q filter.

transformer leakage inductance

The transformer leakage inductance, inherent to the transformer, can be used to form an LC band-pass filter. If the capacitor alone is used to couple onto the mains network, its capacitance value needs to be quite large for it to have a reasonably low reactance at the signalling frequencies. Forming an LC filter greatly reduces the value of capacitor required. The center frequency of the filter is not the same as the midband frequency of 65 kHz. Band-pass filters show a symmetrical shape only when plotted against the logarithm of frequency, so the center frequency (f_o) is given by the following formula:

$$f_o = \sqrt{f_{lower} \times f_{upper}}$$

$$= \sqrt{(40 \times 90)}\ \text{kHz}$$

$$= 60\ \text{kHz}$$

The leakage inductance of the transformer, as viewed from the winding connected to the coupling capacitor, is derived from $2\pi f_O = 1/\sqrt{LC}$. The required leakage inductance of the transformer is:

$$L = \frac{1}{(2\pi f_o)^2 \times C_C}$$

$$= \frac{1}{(2\pi \times 60\ \text{kHz})^2 \times 470\ \text{nF}}$$

$$= 15\ \mu\text{H}$$

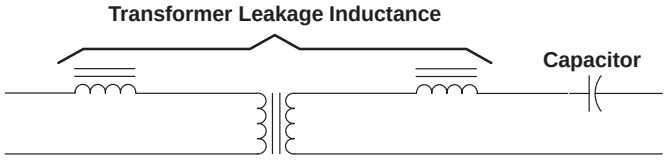


Figure 25. Band-Pass Coupling Filter

APPLICATION INFORMATION

series resistor

The series resistor, R_S, is included to limit the turn-on current, the amplifier's offset current, and the signalling current through the filter. With dual supply rails, there is always a potential problem of large turn-on currents as the amplifier powers up. If one supply rail turns on before the other, the output of the TLE2301 amplifier could saturate near to the applied supply rail, causing a large current to flow through the transformer winding ($R_{winding}$ = 0.1 Ω for the P2820 transformer). The power supply needs to be of sufficient rating to ensure that its rails could rise to the minimum operating voltage of the amplifier, at which point the amplifier is ensured to have returned to stable operation.

With a series resistor of 3.3 Ω and assuming the output saturates at the maximum peak-to-peak voltage excursion of 3 V, this turn-on current is limited to less than the device's 1-A rating ($I_{transient}$ = 3 V/3.3 Ω = 0.91 A). Further reduction of this turn-on current by raising the value of the series resistor deteriorates the filter's performance into low signalling impedances on the mains network.

Alternatively, this turn-on current could be blocked by means of a series capacitor, but for this frequency band the capacitor has to be large in value (≥3.3 μF) so as not to adversely affect the filter. A nonpolarized capacitor of this value is relatively expensive, and the resistor is still required to fulfill other functions.

Another way of preventing overcurrent at power up is to use the TLE2301 3-state mode. As the TRS2 control line is intended to be tied to the microprocessor's 0-V rail, the TRS1 control line must be taken high to activate the 3-state mode, which implies that the positive rail is required to turn on first. Other schemes could be devised to take TRS2 below the 0-V rail until the power supply has stabilized if the negative rail turns on first. Instead of relying on a definite power-supply sequence or elaborate control circuitry, it is simpler to limit the current either with a series resistor or capacitor.

The second function of the series resistor is to limit the dc current flow through the transformer winding due to the dc offset at the amplifier's output, which is caused by its input offset voltage. For a worst case input offset of 20 mV, the output offset is also 20 mV as the dc gain of the circuit is unity. Offsets due to input bias currents are negligible since the values of the gain-setting resistors are low. The dc current through the transformer is therefore less than 7 mA (20 mV/3.3 Ω). This low level of dc current does not appreciatively increase the power dissipation of the amplifier or noticeably diminish the harmonic performance of the transformer.

The final function of the series resistor is to limit the signalling current in the event that the mains impedance might appear as solely reactive; i.e., without a resistive component. As a rough estimate, the peak signal current from the amplifier is:

$$I_{OM} = \frac{V_{O(PP)}}{R_S} = \frac{\left(\frac{5.5\ V}{2}\right)}{3.3\ \Omega} = 833\ mA$$

where:

$V_{O(PP)}$ = Peak-to-peak output voltage swing

I_{OM} = Peak-output-signalling current from amplifier

APPLICATION INFORMATION

series resistor (continued)

Again, the value of the series resistor is sufficient to limit the peak-signal current below the device's maximum rating. This calculation does not take into account other resistive impedances in the signal path, which would further reduce the peak signal current from the amplifier.

decoupling

Power-supply decoupling for the amplifier is provided by a 220-μF electrolytic capacitor and a 100-nF ceramic capacitor per supply rail located close to the supply terminals of the TLE2301 device.

The decoupling capacitors for the negative supply should be connected to a pair of V_{CC-} terminals (4 and 5 or 12 and 13), whichever pair is most convenient from a printed-circuit-board (PCB) layout point of view. In order to minimize parasitic lead inductances, these capacitors should be located as close as possible to the device terminals to which they are connected. As the V_{CC+} terminals are not adjacent on the package, the decoupling capacitors should be connected to one terminal with a thick PCB track going to the other terminal.

The 220-μF electrolytic capacitor is chosen to provide good decoupling performance (less than 25-mV ripple under the worst-case loading for the utility circuit). This value could be reduced to 100 μF for higher-frequency consumer bands. The level of ripple depends on the source impedance of the power supply and the equivalent series resistance of the chosen decoupling capacitors. The 100-nF ceramic capacitor provides high-frequency decoupling for the amplifier.

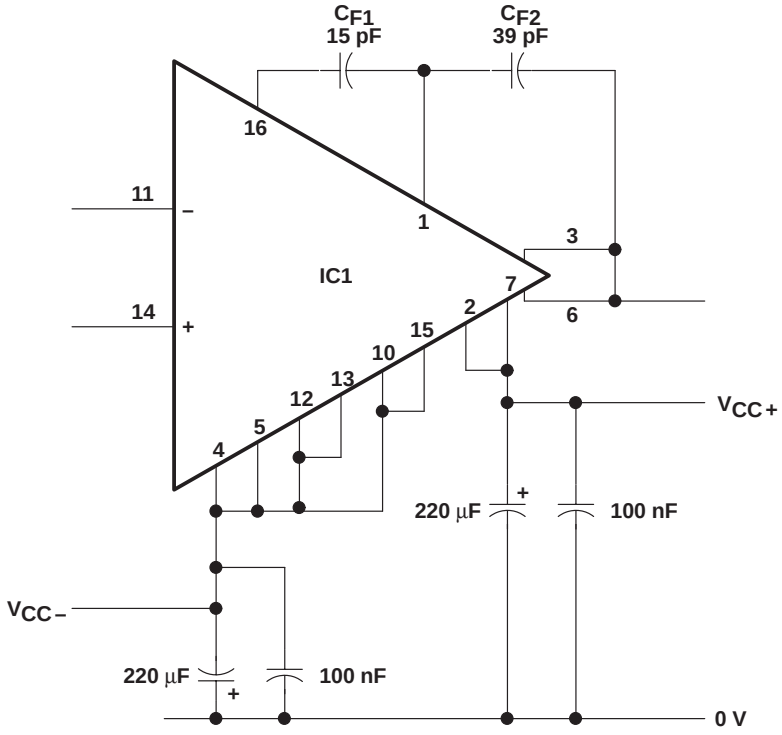


Figure 26. Amplifier Decoupling and Compensation

APPLICATION INFORMATION

frequency compensation

The TLE2301 amplifier requires one compensation capacitor. However, when driving heavy loads, stability can be increased by connecting V_{CC-} terminals 10 and 15 to V_{CC-} terminals 12 and 13 and using another capacitor between COMP2 and the outputs. The circuit included in this application has been designed with two compensation capacitors. The component values chosen are:

$C_{F1} = 15$ pF
$C_{F2} = 33$ pF

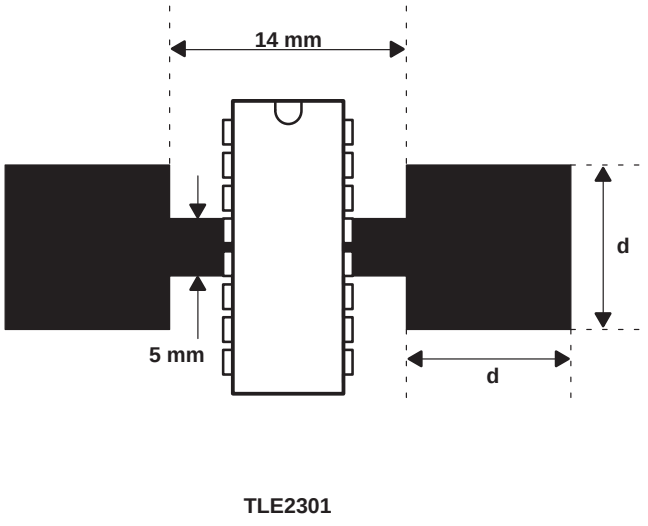
These component values could be adjusted if the amplifier is used for higher-frequency applications.

power dissipation

The impedance of the mains network fluctuates greatly for many reasons, but its impedance at the supply-distribution transformer is typically very low, less than 1 Ω, whereas the mains impedance in a house commonly has a higher value, from 4 Ω to 40 Ω. For utility-metering applications, a master transmitter may be sited at the supply-distribution transformer and would need to deliver more power into the mains network than the household transmitter when generating comparable signal amplitudes.

NE thermally-enhanced dual in-line package

The TLE2301 utilizes the four center terminals of the dual-in-line package (NE) to transfer heat to a copper area on the PCB. A copper area of 1290 mm^2 provides a junction-to-ambient thermal impedance, $Z_{\theta JA}$, of 34°C/W, allowing the device to dissipate up to 1.9 W at 85°C for a junction temperature of 150°C or up to 1.5 W at 85°C for a junction temperature of 135°C.



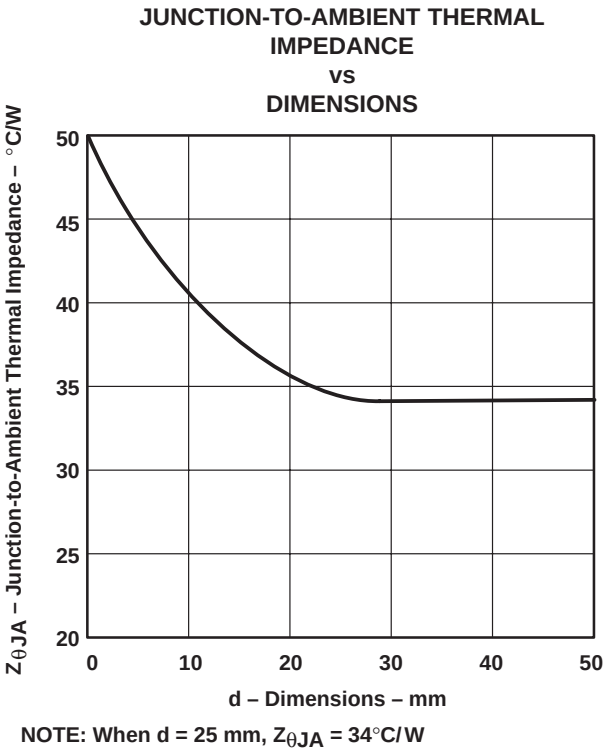


Figure 27. PCB Heatsink

APPLICATION INFORMATION

power dissipation in amplifier

For sinusoidal waveforms, the dissipation in the amplifier, P_{AMP}, is:

$$P_{AMP} = \left(2 \times V_{CC} \times I_{CC}\right) + \frac{\left(2 \times V_{CC} \times I_{OM}\right)}{\pi} - P_O$$

where:

I_{CC} = Amplifier's quiescent current
I_{OM} = Peak-output-signalling current from amplifier
P_O = Output power consumed by coupling network and load

The power dissipated in the amplifier is minimized if the amplifier's peak output current, I_{OM}, is minimized. Since the output power consumed by the coupling and load is a function of current and voltage ($P_O \approx I_O \times V_O$), the amplifier's peak output current can be minimized by maximizing the amplifier's output voltage swing.

circuit parts list

The associated parts list is:

REFERENCE	FIGURE	COMPONENT	DESCRIPTION
IC1	Figure 24, Figure 26	TLE2301 operational amplifier	Texas Instruments TLE230INE
L1	Figure 24	1.67:1, 15-μH leakage transformer	Electronics Techniques P2820 (European manufacturer)
C_C	Figure 24	470-nF capacitor	Metalized paper, safety standards UL1414
C_I	Figure 24	100-nF capacitor	Ceramic, general purpose
C_{F1}	Figure 24, Figure 26	15-pF capacitor	Ceramic, general purpose
C_{F2}	Figure 24, Figure 26	39-pF capacitor	Ceramic, general purpose
C_{D1}, C_{D2}	Figure 24	220-μF, 10-V min capacitors	Aluminum electrolytic, general purpose
C_{D3}, C_{D4}	Figure 24	100-nF capacitors	Ceramic, general purpose
R_F	Figure 24	4.7-kΩ, 0.125-W min resistor	Metal film, general purpose
R_I	Figure 24	2.4-kΩ, 0.125-W min resistor	Metal film, general purpose
R_S	Figure 24	3.3-kΩ, 1-W min, resistor	
D1, D2	Figure 24	1N4001 series, 1-A min diodes	General purpose

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLE2301INE	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLE2301INEE4	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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