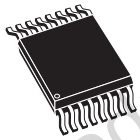
TDA7333

RDS/RBDS processor

Features

- 3rd order high resolution sigma delta converter for MPX sampling
- Digital decimation and filtering stages
- Demodulation of european radio data system (RDS)
- Demodulation of USA radio broadcast data system (RBDS)
- Automatic group and block synchronization with flywheel mechanism
- Error detection and correction
- RAM buffer with a storage capacity of 24 RDS blocks and related status information
- Programmable interrupt source (RDS block TA)
- I^2C/SPI bus interface
- Common quartz frequency 8.55 MHz or 8.664 MHz
- 3.3 V power supply, 0.35 µm CMOS technology



TSSOP16

Description

The TDA7333 circuit is a RDS/RDBS signal processor, intended for recovering the inaudible RDS/RBDS informations which are transmitted on most FM radio broadcasting stations.

Table 1. Device summary

Order code(1)	Operating temp. range, °C	Package	Packing
E-TDA7333	-40 to +85	TSSOP16	Tube
E-TDA7333013TR	-40 to +85	TSSOP16	Tape and reel

1. Devices in ECOPACK® package (see *Section 5: Package information*).

Contents

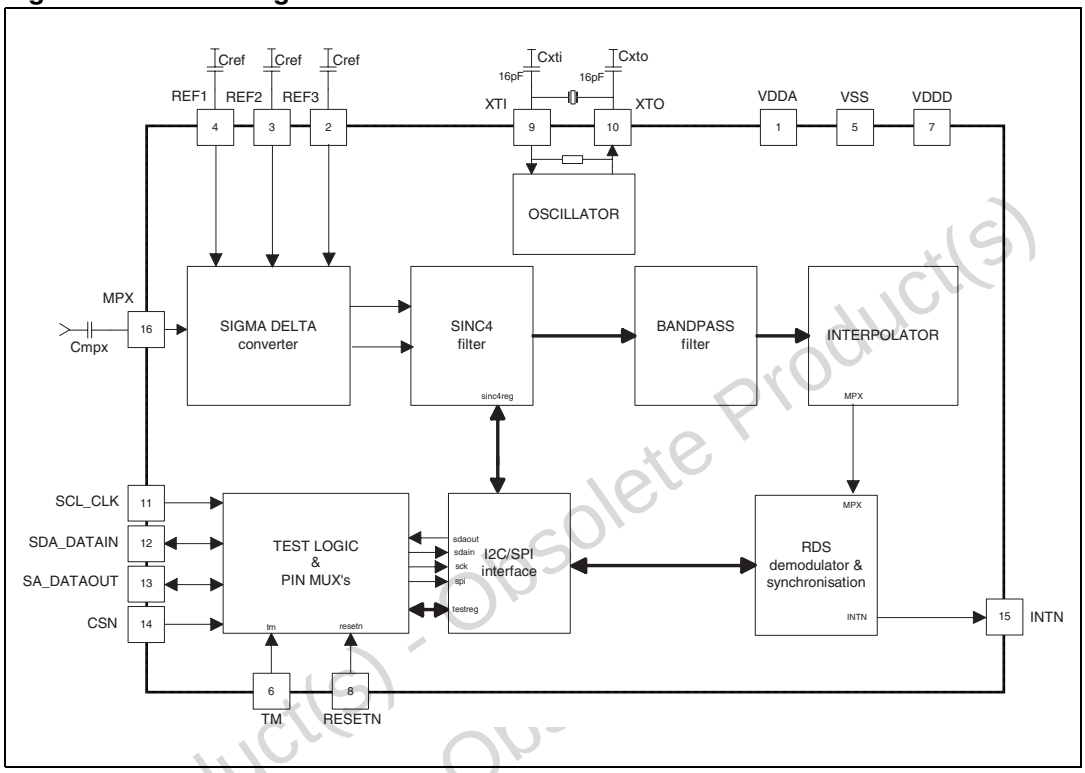
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

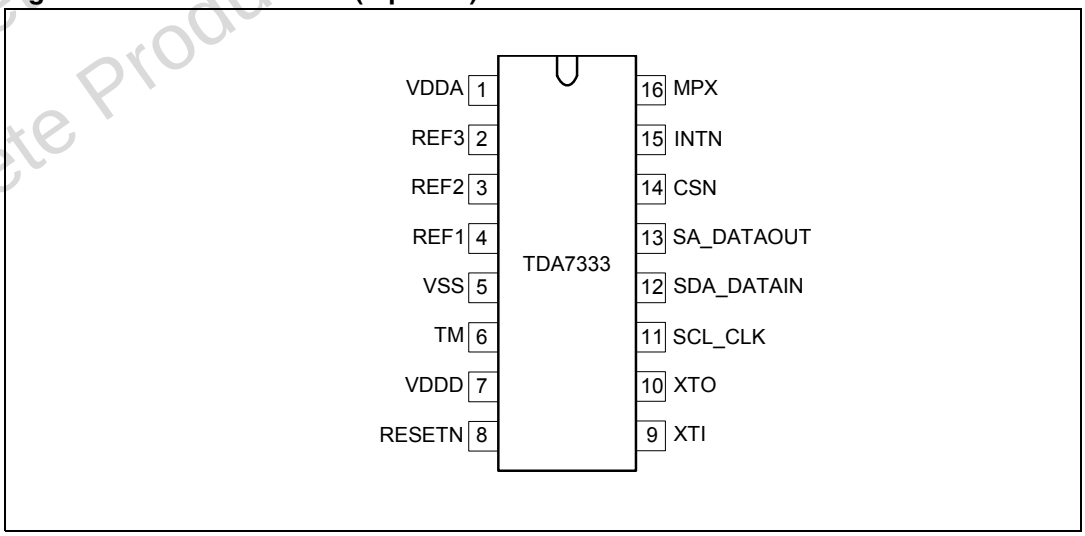


Table 2. Pin description

Pin #	Pin name	Function
1	VDDA	Analog supply voltage
2	REF3	Reference voltage 3 of A/D converter (2.65 V)
3	REF2	Reference voltage 2 of A/D converter (1.65 V)
4	REF1	Reference voltage 1 of A/D converter (0.65 V)
5	VSS	Common ground
6	TM	Testmode selection (scan test). Normal mode must be connected to gnd.
7	VDDD	Digital supply voltage
8	RESETN	External reset input (active low)
9	XTI	Oscillator input
10	XTO	Oscillator output
11	SCL_CLK	Clock signal for I^2C and SPI modes
12	SDA_DATAIN	Data line in I^2C mode, data input in SPI mode
13	SA_DATAOUT	Slave address in I^2C mode, data output in SPI mode
14	CSN	Chip select (1 = I^2C mode, 0=SPI mode)
15	INTN	Interrupt output (active low), prog. at buff.not empty, buff. full, block A,B,D ,TA, TA EON
16	MPX	Multiplex input signal

2 Electrical specifications

2.1 Quick reference

Table 3. Quick Reference

(T_{amb} = 25 °C, VDDA/VDDD = 3.3 V, f_{osc} = 8.55 MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDA}/V_{DDD}	Analog/digital power supply	3.0	3.3	3.6	V
T_{amb}	Operating temperature	-40		+85	°C
f_{osc}	Quartz frequency		8.55 or 8.664		MHz
I_{dd}	Total supply current		10		mA
P_d	Power dissipation		33		mW
S_{RDS}	RDS input sensitivity	1			mVrms
V_{MPX}	Input range of MPX signal			750	mVrms
f_{SPI}	Maximum speed in SPI mode			1	MHz
f_{i2c}	Maximum speed in I^2C mode			400	kHz

2.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	3.3 V power supply voltages		-0.5		4	V
V_{in}	Input voltage	5 V tolerant inputs	-0.5		5.5	V
V_{out}	Output voltage	5 V tolerant output buffers in tri-state	-0.5		5.5	V
V_{peak}	Maximum peak voltage				6	V

2.3 General interface electrical characteristics

Table 5. General interface electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{il}	Low level input current	V_i = 0 V			1	µA
I_{ih}	High level input current	$V_i = V_{DD}$			1	µA
I_{oz}	Tri-state output leakage	V_o = 0 V or V_{DD}			1	µA
		V_o = 5.5 V		1	3	µA

2.4 Electrical characteristics

Table 6. Electrical characteristics

T_{amb} = -40 to +85 °C, V_{DDA}/V_{DDD} = 3.0 to 3.6 V, f_{osc} = 8.55 MHz, unless otherwise specified
V_{DDD} and V_{DDA} must not differ more than 0.15 V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply (pin 1,5,7)						
V_{DDD}	Digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	Analog supply voltage		3.0	3.3	3.6	V
I_{DDD}	Digital supply current			2		mA
I_{DDA}	Analog supply current			8		mA
P_d	Total power dissipation			33		mW
Digital inputs (pin 6,8,11,12,13,14)						
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2.0			V
V_{ilhyst}	Low level threshold input falling		1.0		1.15	V
V_{ihhyst}	High level threshold input rising		1.5		1.7	V
V_{hst}	Schmitt trigger hysteresis		0.4		0.7	V
Digital outputs (pin 12,13,15) are open drains						
V_{oh}	High level output voltage	Open drain, depends on external circuitry			V_{DDD}	V
V_{ol}	Low level output voltage	I_{ol} = 4 mA, takes into account 200 mV drop in the supply voltage			0.4	V
Analog inputs (pin 16)						
V_{MPX}	Input range of MPX signal				0.75	Vrms
S_{RDS}	RDS detection sensitivity		1			mVrms
R_{MPX}	Input Impedance of MPX pin			55k		Ohm
Crystal parameters						
f_{osc}	Quartz frequency			8.55 or 8.664		MHz
t_{su}	Start up time				10	ms
g_m	Transconductance		0.0006			A/V
C_{xti},C_{xto}	Load capacitance			16		pF

Table 6. Electrical characteristics (continued)

T_{amb} = -40 to +85 °C, V_{DDA}/V_{DDD} = 3.0 to 3.6 V, f_{osc} = 8.55 MHz, unless otherwise specified
V_{DDD} and V_{DDA} must not differ more than 0.15 V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Sigma delta modulator						
F_s	Sample rate	f_{osc} = 8.55 MHz		4.275		MHz
OVR	Oversampling ratio	f = 57 kHz		38		
THD+N	Relative total harmonic dist. plus noise	BW = 54.5 to 59.5 kHz, unweigted, V_{rds} = 3 mVrms		27		dB
Sinc4/16 decimation filter						
f_s	Decimated sample rate	f_{osc} = 8.55 MHz		267.2		kHz
A57	Attenuation at 57 kHz			-2.6		dB
	Attenuation difference	BW = 54.5 to 59.5 kHz		0.4		dB
Bandpass filter						
f_s	Sample rate	f_{osc} = 8.55 MHz		267.2		kHz
f_p	Pass-band frequencies		55.6		58.4	kHz
R_p	Pass-band ripple		-0.5		+0.5	dB
f_{stop}	Stop-band corner frequencies		53.0		61	kHz
R_s	Stop-band attenuation			-43		dB
M_i	Interpolation factor			32		
I^2C						
f_{I2C}	Clock frequency in I^2C mode				400	kHz
SPI						
f_{SPI}	Clock frequency in SPI mode				1	MHz
t_{ch}	Clock high time		450			ns
t_{cl}	Clock low time		450			ns
t_{csu}	Chip select setup time		500			ns
t_{csh}	Chip select hold		500			ns
t_{odv}	Output data valid				250	ns
t_{oh}	Output hold		0			ns
t_d	Deselect time		1000			ns
t_{su}	Data setup time		200			ns
t_h	Data hold time		200			ns

3 Functional description

3.1 Overview

The new RDS/RBDS processor contains all RDS/RBDS relevant functions on a single chip. It recovers the inaudible RDS/RBDS information which are transmitted on most FM radio broadcasting stations.

Due to an integrated 3rd order sigma delta converter, which samples the MPX signal, all further processing is done in the digital domain and therefore very economical. After filtering the highly oversampled output of the A/D converter, the RDS/RBDS demodulator extracts the RDS DataClock, RDS Data Signal and the Quality information. A next RDS/RBDS decoder will synchronize the bitwise RDS stream to a group and block wise information. This processing includes an error detection and error correction algorithm. In addition, an automatic flywheel control avoids exhaustive data exchange between the RDS/RBDS processor and the host.

The device operates in accordance with the EBU (European Broadcasting Union) specifications.

3.2 Sigma delta converter

The sigma delta modulator is a 3rd order (second order-first order cascade) structure. Therefore a multibit output (2 bit streams) represents the analog input signal. A next digital noise canceller will take the 2 bit streams and calculates a combined stream which is then fed to the decimation filter. The modulator works at a sampling frequency of XTI/2. The oversampling factor in relation to the band of interest (57 kHz ±2.4 kHz) is 38.

3.3 Sinc4/16 decimation filter

The oversampled data delivered from the modulator are decimated by a value of 16 with a 4th order Sinc Filter.

This is considered to be the optimum solution for high decimation factors and for a 3rd order sigma delta modulator.

The architecture is a very economical implementation because digital multipliers are not required. It is implemented by cascading 4 integrators operating at full sampling rate (XTI/2) followed by 4 differentiates operating at the reduced sampling rate (XTI/2/16). Also wrap around logic is allowed and the internal overflow will not affect the output signal as long as a minimum required bit width is maintained.

The transfer function of this Sinc4/16 filter is:

$$H(z) = \left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^{K}$$

with K = 4, M = 16

and its frequency response is:

$$\left|H(e^{j\omega})\right| = \left(\frac{1}{M}\frac{\sin\left(\frac{M\omega}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}\right)^{K}$$

with

$$\omega = 2\pi\frac{f}{fs}$$

Figure 3. Transfer function of a 4th order sinc. filter, decimation factor is 16.

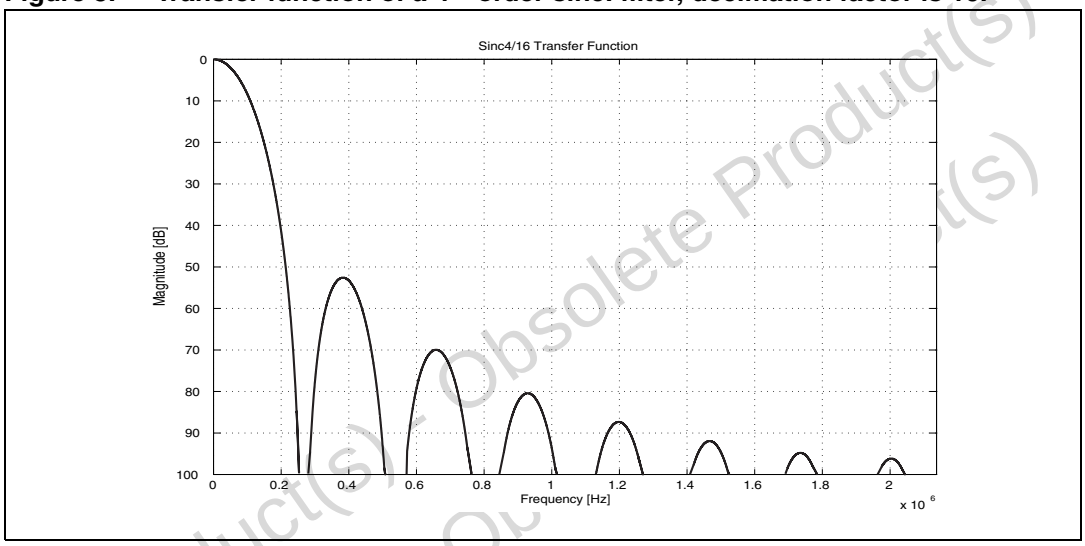
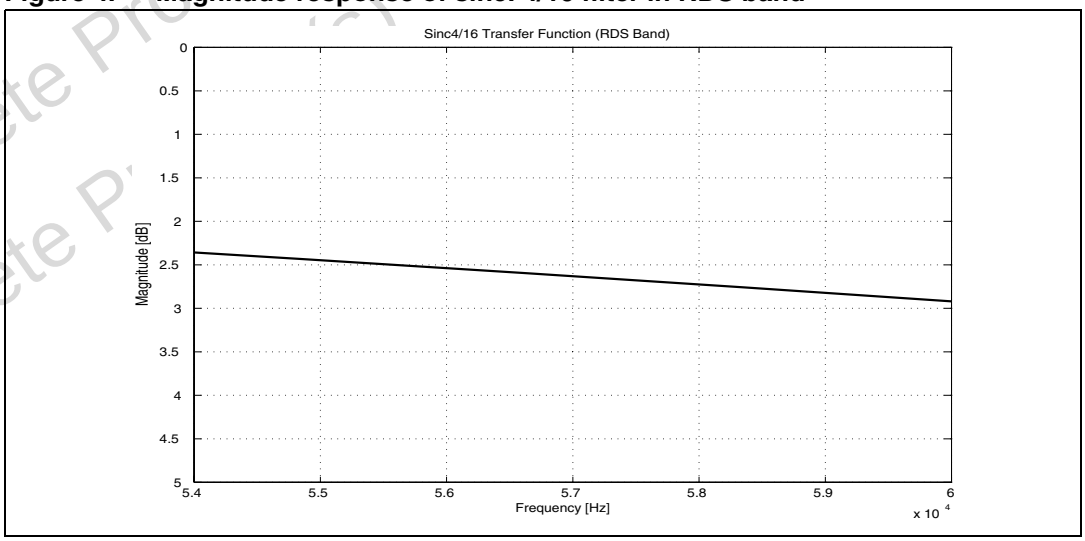


Figure 4. Magnitude response of sinc. 4/16 filter in RDS band



3.4 RDS bandpass filter and interpolator

The 8th order digital RDS bandpass filter is of type Tschebyscheff and centered at 57 kHz. With linear phase characteristics in the passband and approximately flat group delay it guarantees best filter function of the RDS and ARI signal. Four biquads are cascaded working at a common sampling frequency of XTI/2/16.

Figure 5. Transfer function of RDS bandpass filter

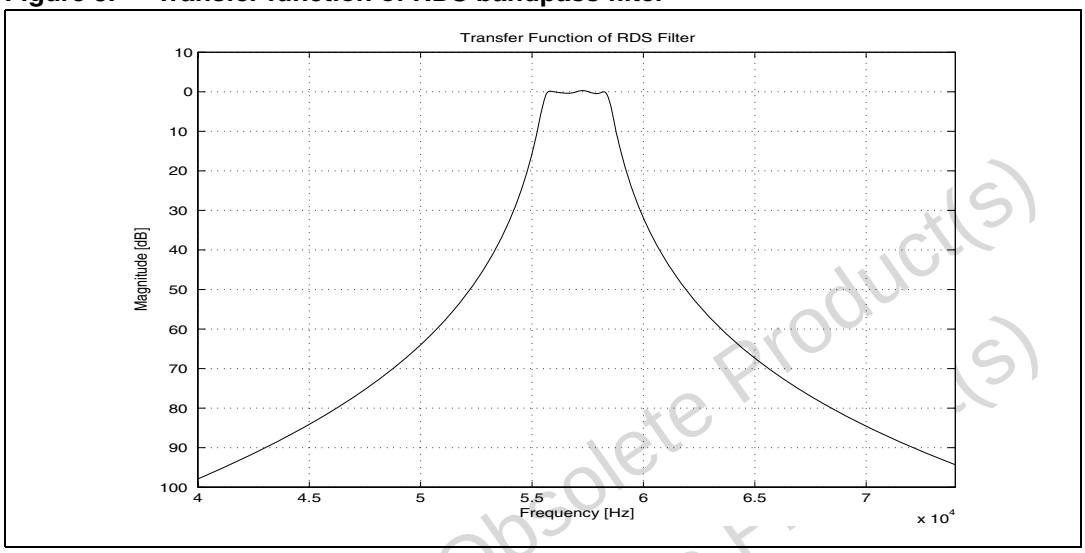
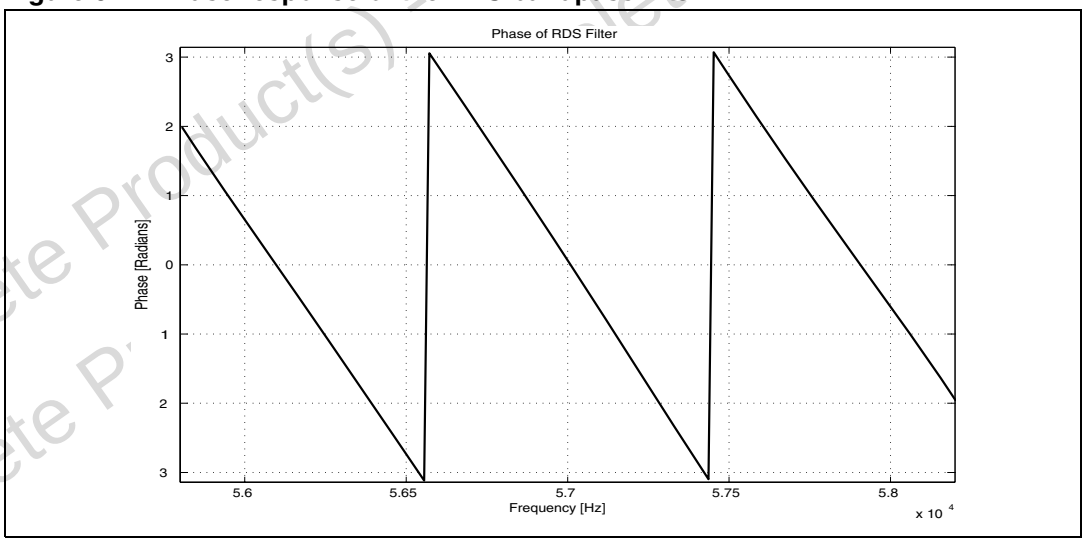


Figure 6. Phase response of the RDS bandpass filter



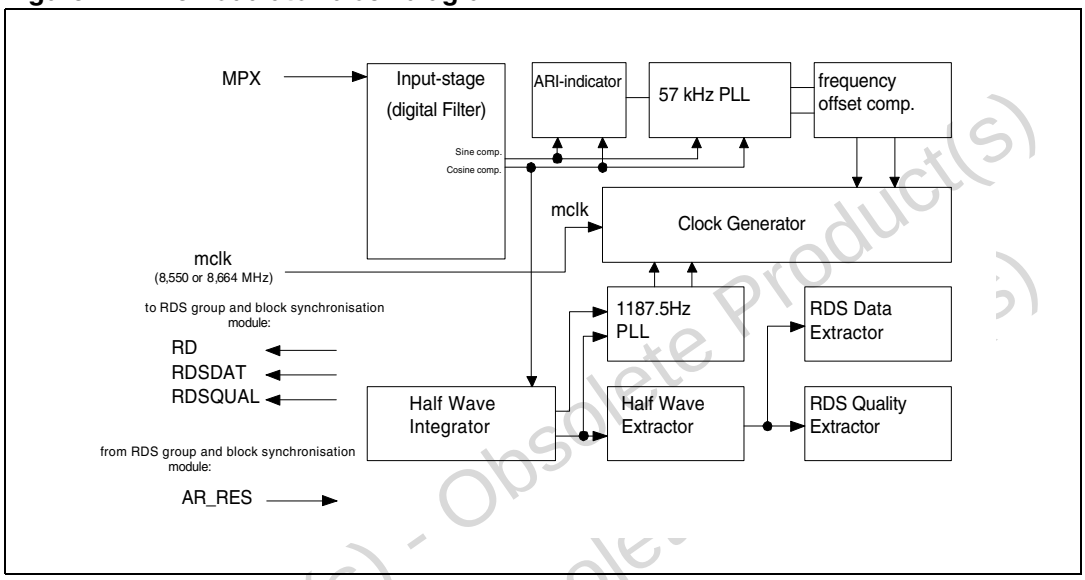
The output sample of the bandpass filter is picked up from a linear interpolator with sinc2 characteristics. The interpolation factor is 32. A zero cross detection is simply formed by taking the sign bit of the interpolated signal. This signal which contains only phase informations is processed by the RDS Demodulator.

3.5 Demodulator

The demodulator includes:

- RDS quality indicator with selectable sensitivity
- Selectable time constant of 57 kHz PLL
- Selectable time constant of bit PLL
- time constant selection done automatically or by software

Figure 7. Demodulator block diagram



The demodulator is fed by the 57 kHz bandpass filter and interpolated multiplex signal. The input signal passes a digital filter extracting the sinus and cosinus components, to be used for further processing.

The sign of both channels are used as input for the ARI indicator and for the 57 kHz PLL.

A fast ARI indicator determines the presence of an ARI carrier. If an ARI carrier is present, the 57 kHz PLL is operating as a normal PLL, else it is operating as a Costas loop.

One part of the PLL is compensating the integral offset (frequency deviation between oscillator and input signal).

One channel of the filter is fed into the half wave integrator. Two half waves are created, with a phase deviation of 90 degrees. One wave represents the RDS component, whereas the other wave represents the ARI component. The sign of both waves are used as reference for the bit PLL (1187.5 Hz).

The RDS wave is then fed into the half wave extractor. This leads into an RDS signal, which after integration and differential decoding represents the RDS data.

In a similar way a quality bit can be calculated. This is useful to optimize error correction.

The module needs a fixed clock of 8.55 MHz. Optionally an 8.664 MHz clock may be used by setting the corresponding bit in rds_bd_ctrl register (see *Chapter 3.7.6*).

In order to optimize the error correction in the group and block synchronization module, the sensitivity level of the quality bit can be adjusted in three steps (see *Chapter 3.7.6*). Only

bits marked as bad by the quality bit are allowed to be corrected in the group and block synchronization module. Thus the error correction is directly influenced by this setup.

The time constant of the 57 kHz PLL and the 1187.5 Hz PLL may be influenced by software (see *Chapter 3.7.6*).

This is useful in order to achieve a fast synchronization after a program resp. frequency change (fast time constant) and to get a maximum of noise immunity after synchronization (slow time constant).

The user may choose between 2 possibilities via bit rds_bd_ctrl[1] (see *Chapter 3.7.6*):

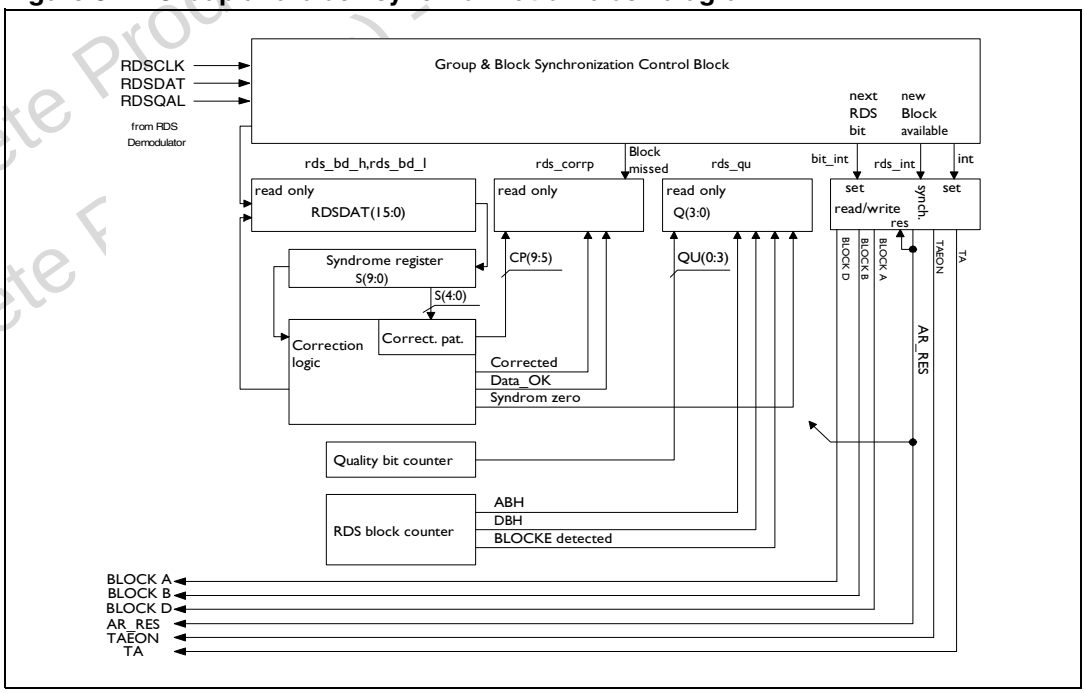
1. Hardware selected time constant - In this case both pll time constants are reset to the fastest one with a reset from the group and block synchronization module. If the software decides to re synchronize, it generates a reset. Both PLL are set to the fastest time constant, which is automatically increased to the slowest one. This is done in four steps within a total time of 215.6 ms (256 RDS clocks).
2. Software selected time constant - In this case the time constant of both PLL can be selected individually by software.PLL time constants can be set independently.

3.6 Group and block synchronization module

The group and block synchronization module has the following features:

- Hardware group and block synchronization
- Hardware error detection
- Hardware error correction using the quality bit information of the demodulator
- Hardware synchronization flywheel
- TA information extraction
- reset by software (ar_res)

Figure 8. Group and block synchronization block diagram



This module is used to acquire group and block synchronization of the received RDS data stream, which is provided in a modified shortened cyclic code. For the theory and implementation of the modified shortened cyclic code, please refer to the specification of the radio data system (RDS) EN50067.

It further detects errors in the data stream. Depending on the quality bit information of the demodulator an error correction is made.

The RDS data bytes are available to the software together with status bits giving an indication on the reliability of the data.

It also extracts TA information which can be used as interrupt source (see *Chapter 3.7.1*).

3.7 Programming through serial bus interface

The serial bus interface is used to access the different registers of the chip. It is able to handle both I^2C and SPI transfer protocols, the selection between the two modes is done thanks to the pin CSN:

- if the pin CSN is high, the interface operates as an I^2C bus.
- if the pin CSN is asserted low, the interface operates as a SPI bus.

In both modes, the device is a slave, i.e the clock pin SCL_CLK is only an input for the chip.

Depending on the transfer mode, external pins have alternate functions as following:

Table 7. External pins alternate functions

Pin	Function in SPI mode (CSN =0)	Function in I^2C mode (CSN=1)
SCL_CLK	CLK (serial clock)	SCL (serial clock)
SDA_DATAIN	DATAIN (data input)	SDA (data line)
SA_DATAOUT	DATAOUT (data output)	SA (slave address)

Eight registers are available with read or read/write access rights as the following:

Table 8. Registers description

Register	Access rights	Function
rds_int[7:0] (see *3.7.1*)	read/write	Interrupt source setting, sync., bne information
rds_qu[7:0] (see *3.7.2*)	read	Quality counter, actual block name
rds_corrp[7:0] (see *3.7.3*)	read	Error correction status, buffer ovf information
rds_bd_h[7:0] (see *3.7.4*)	read	High byte of current RDS block
rds_bd_l[7:0] (see *3.7.5*)	read	Low byte of current RDS block
rds_bd_ctrl[7:0] (see *3.7.6*)	read/write	Frequency, quality sensitivity, demodulator pll settings
sinc4reg[7:0]	read/write	Sinc4 filter settings (for internal use only)
testreg[7:0]	read/write	Test modes (for internal use only)

The meaning of each bit is described below:

3.7.1 rds_int register

Figure 9. rds_int register

rds_int	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	write	bne	ar_res	synch	itsrc2	itsrc1	itsrc0	int
access	r/w	r	r/w	r	r/w	r/w	r/w	r

interrupt bit. It is set to one on every programmed interrupt. It is reset by reading rds_int register.
interrupt source itsrc[2:0] select the interrupt source (1)
synchronization information. 1: the module is already synchronized. 0: the module is synchronizing
It is used to force a resynchronization. If it is set to one, the RDS modules are forced to resynchronization state. The bit is automatically reset. So it is always read as zero.
RDS block. if 1, one block has been detected
rds_int and rds_bd_ctrl write order (when in SPI mode) 1: rds_int and rds_bd_ctrl are updated with data shifted in. 0: rds_int and rds_bd_ctrl are not updated.

(1)

interrupt source	tsrc2	itsrc1	itsrc0
no interrupt	0	0	0
RDS Block	0	0	1
block A	0	1	1
block B	1	0	0
block D	1	0	1
TA	1	1	0
TAEON	1	1	1

Note : when changing the interrupt mode, one has to perform a reset of the module (i.e set the bit "ar_res" at one)

3.7.2 rds_qu register

Figure 10. rds_qu register

rds_qu	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	qu3	qu2	qu1	qu0	blk1	blk0	e	synz
access	r	r	r	r	r	r	r	r

It indicates if the error correction was successfull. 1: the syndrome was zero after the error correction. 0: the syndrome did not become zero and therefore the correction was not successfull.
1: a block E is detected.This indicates a paging block which is defined in the RBDS specification used in the united states of America. 0: an ordinary RDS block A, B, C, c·or D is detected, or no valid syndrome was found.
bit 0 of block counter (2)
bit 1 of block counter (2)
bit 0 of quality counter (3)
bit 1 of quality counter (3)
bit 2 of quality counter (3)
bit 3 of quality counter (3)

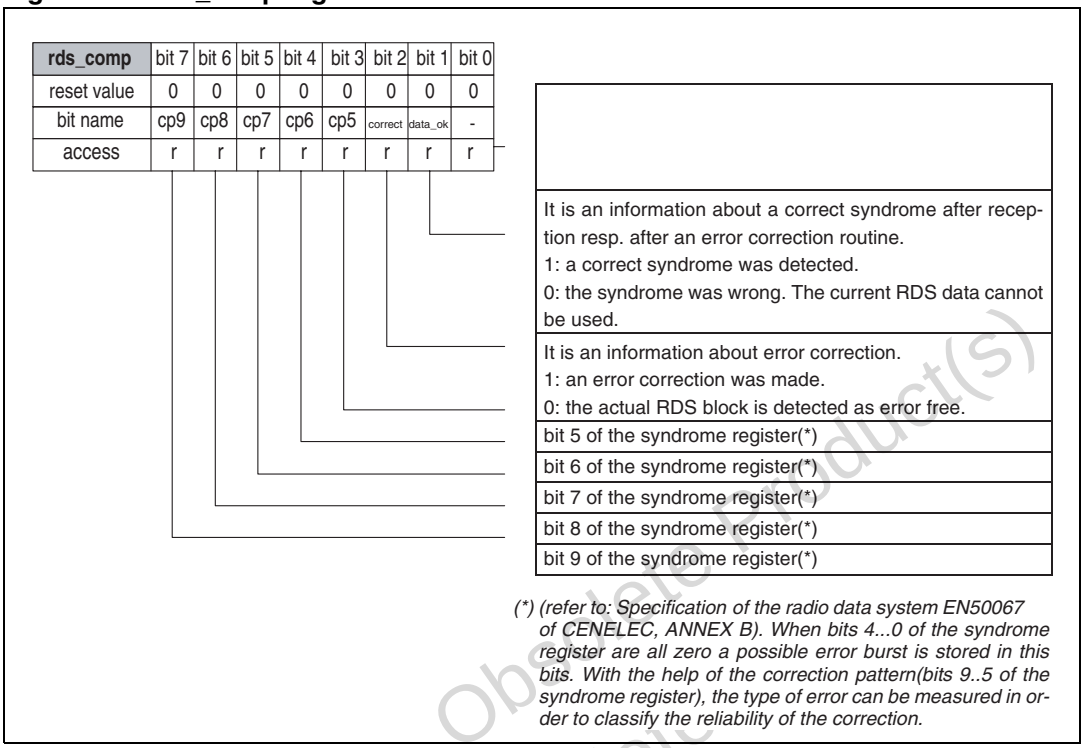
(2)

block name	blk1	blk0
block A	0	0
block B	0	1
block C,C'	1	0
block D	1	1

(3) qu[3..0] is a counter of the quality bit information coming from the RDS demodulator. It is counting the number of bits which are marked as bad by the demodulator. Only those bits are allowed to be corrected. Thus the quality bit counter indicates the maximum possible number of bits being corrected.

3.7.3 rds_corrp register

Figure 11. rds_corrp register



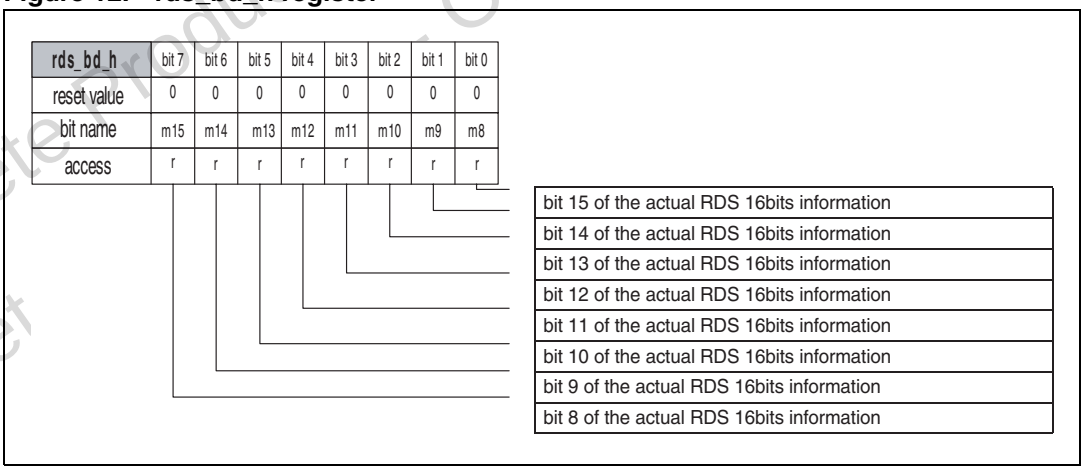
rds_comp	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	cp9	cp8	cp7	cp6	cp5	correct	data_ok	-
access	r	r	r	r	r	r	r	r

It is an information about a correct syndrome after reception resp. after an error correction routine. 1: a correct syndrome was detected. 0: the syndrome was wrong. The current RDS data cannot be used.
It is an information about error correction. 1: an error correction was made. 0: the actual RDS block is detected as error free.
bit 5 of the syndrome register(*)
bit 6 of the syndrome register(*)
bit 7 of the syndrome register(*)
bit 8 of the syndrome register(*)
bit 9 of the syndrome register(*)

(*) (refer to: Specification of the radio data system EN50067 of CENELEC, ANNEX B). When bits 4...0 of the syndrome register are all zero a possible error burst is stored in this bits. With the help of the correction pattern(bits 9..5 of the syndrome register), the type of error can be measured in order to classify the reliability of the correction.

3.7.4 rds_bd_h register

Figure 12. rds_bd_h register

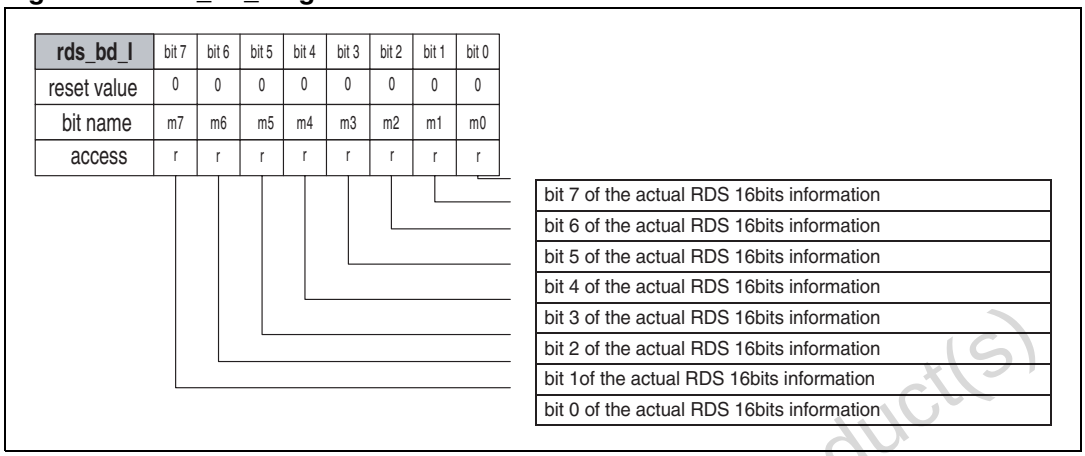


rds_bd_h	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	m15	m14	m13	m12	m11	m10	m9	m8
access	r	r	r	r	r	r	r	r

bit 15 of the actual RDS 16bits information
bit 14 of the actual RDS 16bits information
bit 13 of the actual RDS 16bits information
bit 12 of the actual RDS 16bits information
bit 11 of the actual RDS 16bits information
bit 10 of the actual RDS 16bits information
bit 9 of the actual RDS 16bits information
bit 8 of the actual RDS 16bits information

3.7.5 rds_bd_l register

Figure 13. rds_bd_l register

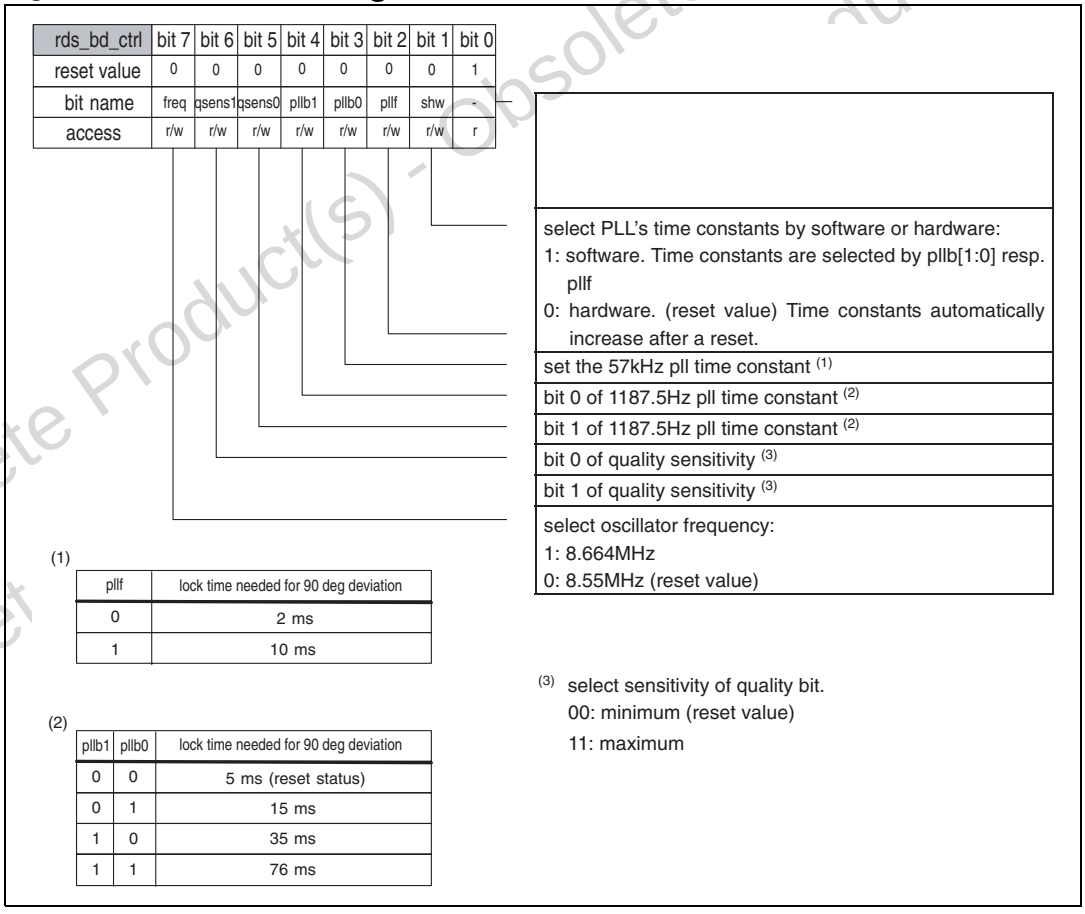


rds_bd_l	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	m7	m6	m5	m4	m3	m2	m1	m0
access	r	r	r	r	r	r	r	r

bit 7 of the actual RDS 16bits information
bit 6 of the actual RDS 16bits information
bit 5 of the actual RDS 16bits information
bit 4 of the actual RDS 16bits information
bit 3 of the actual RDS 16bits information
bit 2 of the actual RDS 16bits information
bit 1of the actual RDS 16bits information
bit 0 of the actual RDS 16bits information

3.7.6 rds_bd_ctrl register

Figure 14. rds_bd_ctrl register



rds_bd_ctrl	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	1
bit name	freq	qsens1	qsens0	pllb1	pllb0	pllf	shw	-
access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r

select PLL's time constants by software or hardware: 1: software. Time constants are selected by pllb[1:0] resp. pllf 0: hardware. (reset value) Time constants automatically increase after a reset.
set the 57kHz pll time constant (1)
bit 0 of 1187.5Hz pll time constant (2)
bit 1 of 1187.5Hz pll time constant (2)
bit 0 of quality sensitivity (3)
bit 1 of quality sensitivity (3)
select oscillator frequency: 1: 8.664MHz 0: 8.55MHz (reset value)

(1)

pllf	lock time needed for 90 deg deviation
0	2 ms
1	10 ms

(2)

pllb1	pllb0	lock time needed for 90 deg deviation
0	0	5 ms (reset status)
0	1	15 ms
1	0	35 ms
1	1	76 ms

(3) select sensitivity of quality bit.
00: minimum (reset value)
11: maximum

Note: Sinc4reg and testreg are reserved registers dedicated to testing and evaluation.

3.8 I²C transfer mode

This interface consists of three lines: a serial data line (SDA), a bit clock (SCL), and a slave address select (SA).

The interface is capable of operating in fast mode (up to 400kbits/s) but also at lower rates (<100kbits/s).

Data transfers follow the format shown in *Figure 15*. After the START condition (S), a slave address is sent. The address is 7 bits long followed by an eighth bit which is a data direction bit (R/_W).

A 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ).

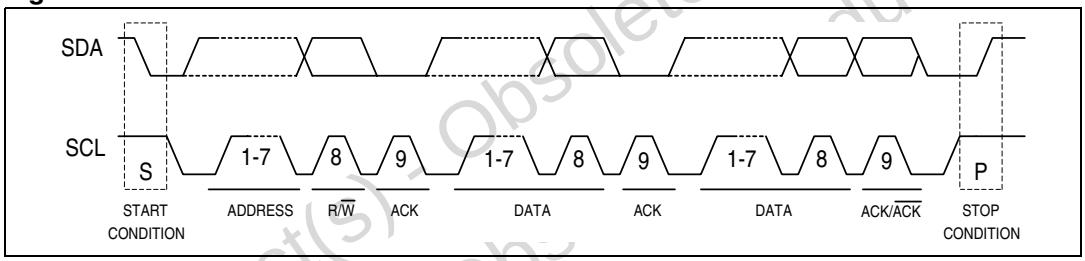
The slave address of the chip is set to 001000S, where S is the least significant bit of the slave address set externally via the pin SA_DATAOUT. This allows to choose between two addresses in case of conflict with another device of the radio set.

Each byte has to be followed by an acknowledge bit (SDA low).

Data is transferred with the most significant (MSB) bit first.

A data transfer is always terminated by a stop condition (P) generated by the master.

Figure 15. I²C data transfer



3.8.1 Write transfer

Figure 16. I²C write transfer

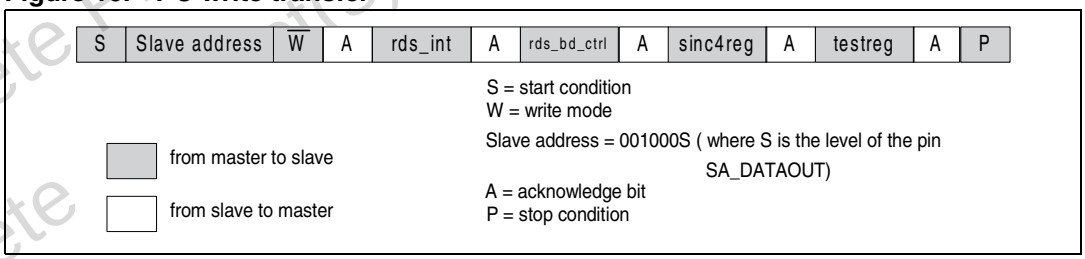
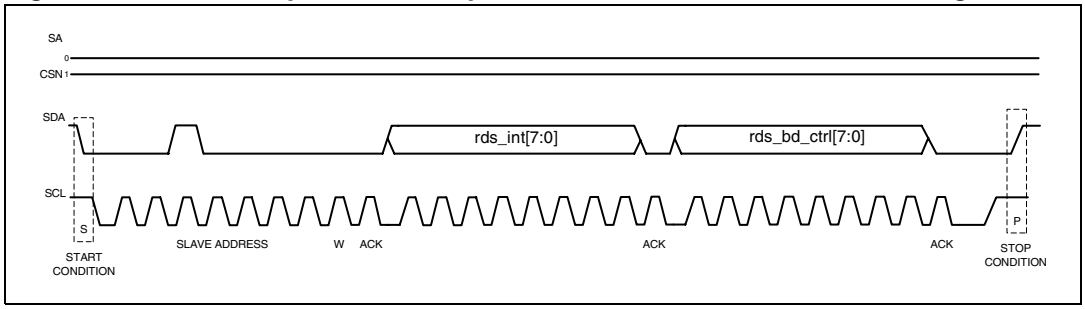
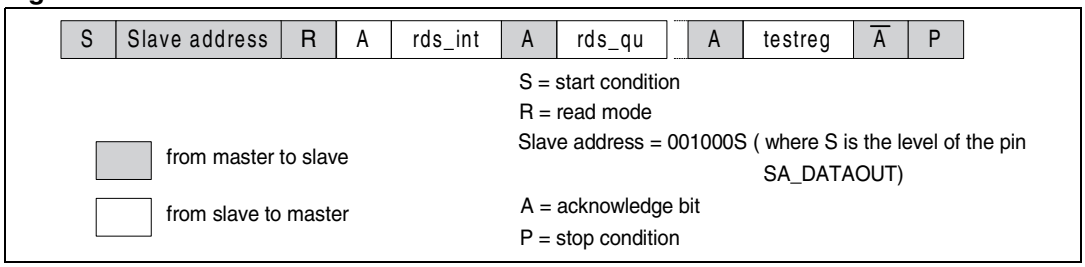


Figure 17. I²C write operation example: write of rds_int and rds_bd_ctrl registers



3.8.2 Read transfer

Figure 18. I²C read transfer



Eight bytes can be read at a time (please refer to *Section 3.7* for the meaning of each bit).

The master has always the possibility to read less than eight registers by not sending the acknowledge bit and then generating a stop condition after having read the needed amount of registers.

There are two typical read access:

- read only the first register rds_int to check the interrupt bit.
- read the first five registers rds_int, rds_qu, rds_corrp, rds_bd_h, rds_bd_l to get the RDS data

The registers are read in the following order: rds_int, rds_qu, rds_corrp, rds_bd_h,rds_bd_l, rds_bd_ctrl, sinc4reg, testreg.

Figure 19. I²C read access example 1: read of 5 bytes

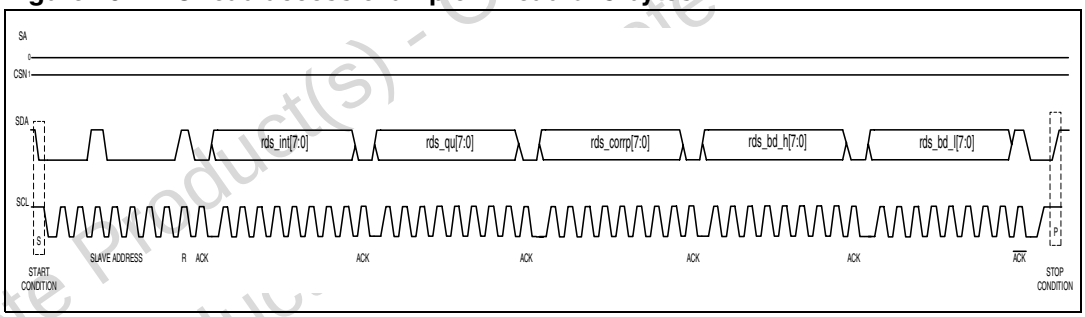
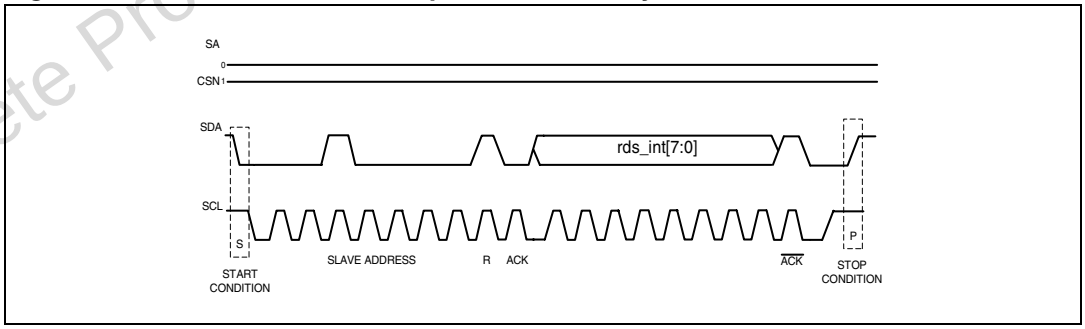
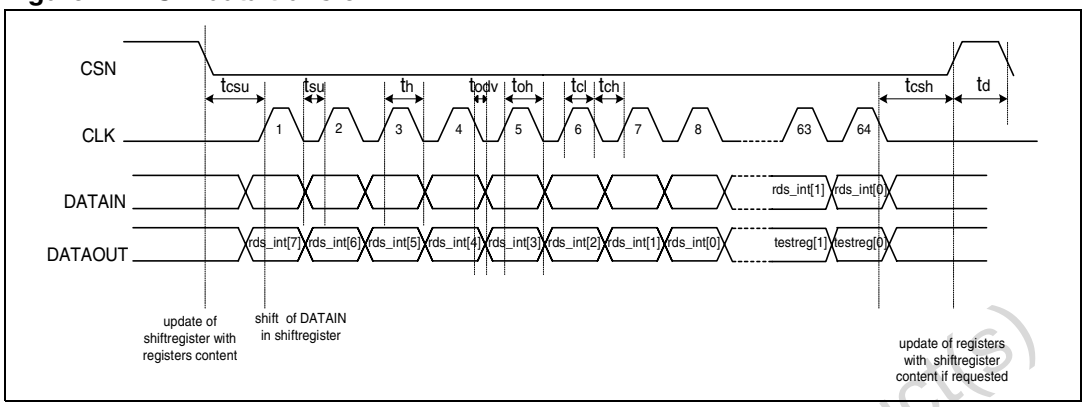


Figure 20. I²C read access example 2: read of 1 byte



3.9 SPI mode

Figure 21. SPI data transfer



This interface consists of four lines. A serial data input (DATAIN), a serial data output (DATAOUT), a chip select input (CSN) and a bit clock input (CLK).

The chip select input signals the begin and end of the data transfer. If the data transfer starts, at each

bit clock one bit is clocked out via the serial data output and one bit is clocked in via the serial data input.

When chip enable signals the begin of the data transfer the internal 64 bits shift register is updated with the current registers content of the V324.

When chip enable signals the end of the data transfer the registers with write access can be updated with the bits which have been last shifted in.

The last byte on DATAIN input is always rds_int[7:0] and the former last one is rds_bd_ctrl[7:0]. In other words, the master has to take in account the amount of bytes transmitted when intending to perform a write operation so that the last two bytes sent on DATAIN are rds_bd_ctrl[7:0] and rds_int[7:0].

If the update of both rds_int and rds_bd_ctrl registers is actually taking place depends on the MSB of rds_int, i.e. rds_int[7] = 0 - no update, rds_int[7] = 1 update of both registers.

Hereafter you can find typical read/write access in SPI mode:

Figure 22. Write rds_int and rds_bd_ctrl registers in SPI mode, reading RDS data and related flags

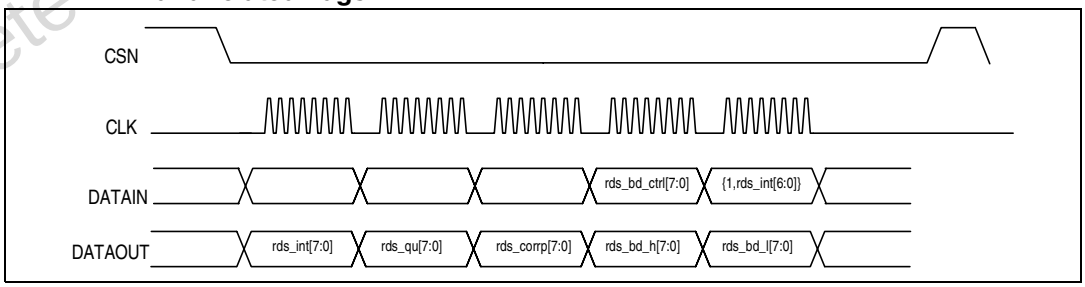


Figure 23. Read out RDS data and related flags, no update of rds_int and rds_bd_ctrl registers

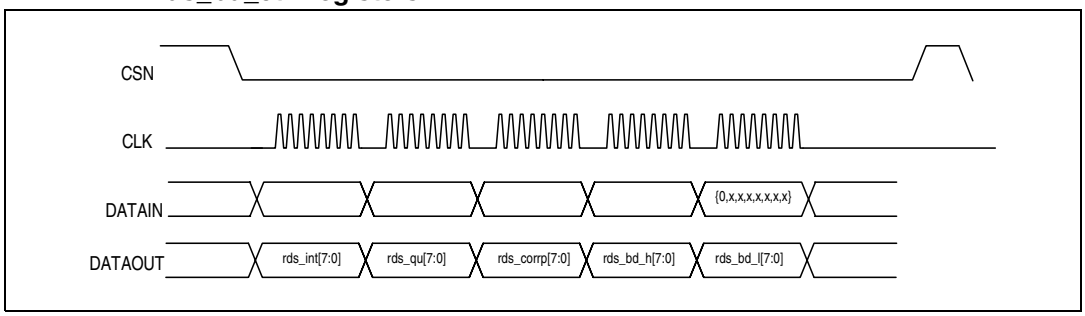
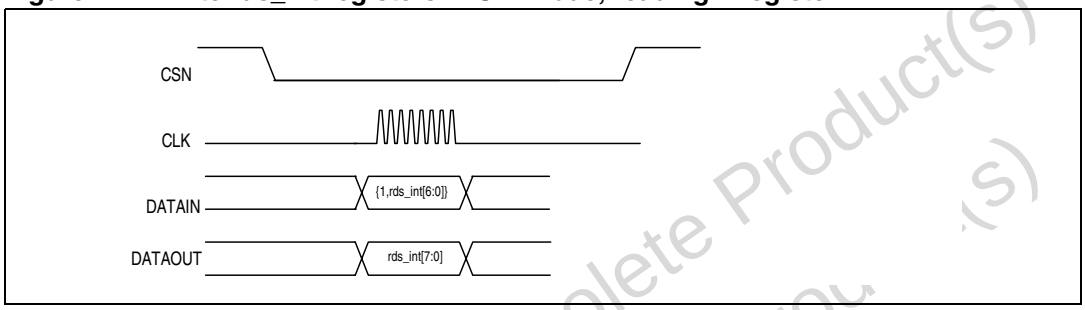


Figure 24. Write rds_int registers in SPI mode, reading 1 register



The content of the rds registers is clocked out on DATAOUT pin in the following order:

rds_int[7:0], rds_qu[7:0], rds_corrp[7:0], rds_bd_l[7:0], rds_bd_h[7:0], rds_ctrl[7:0], sinc4reg[7:0], testreg[7:0]

For the meaning of the single bits please refer to the *Section 3.7*.

Note: After 40 bit clocks the whole RDS data and flags are clocked out.

4 Application notes

A typical rds data transfer could work like this:

1. The micro sets the interrupt source to “RDS block” interrupt by setting itsrc[2:0] to 001.
2. The micro continuously checks the rds_int[7:0] bits for the first interrupt (rds_int[0] goes high). If there is no interrupt it stops the transfer after these 8 bits. No update of the rds_int[7:0] is performed.
3. Once there is an interrupt detected the micro will also clock out all the other RDS bits (rds_qu[7:0], rds_corrp[7:0], rds_bd_h[7:0], rds_bd_l[7:0]).
4. The next interrupt can not be expected before 22ms.

The above example is working by polling the rds_int[0] bit. An easier and better application is possible by checking the RDS interrupt pin INTN (see below) and starting the transfer only when this interrupt is present.

The output pin INTN acts as an interrupt pin. The source of interrupt is programmable through the register rds_int (see *Section 3.7.1*), the value on the pin is the inverted value of the bit rds_int[0] (i.e this interrupt pin is active low). With the help of this pin an interrupt driven request of the rds data is possible (the external processor only starts the transfer if an interrupt is active).

5 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

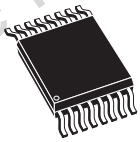
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 25. TSSOP16 mechanical data and package dimensions

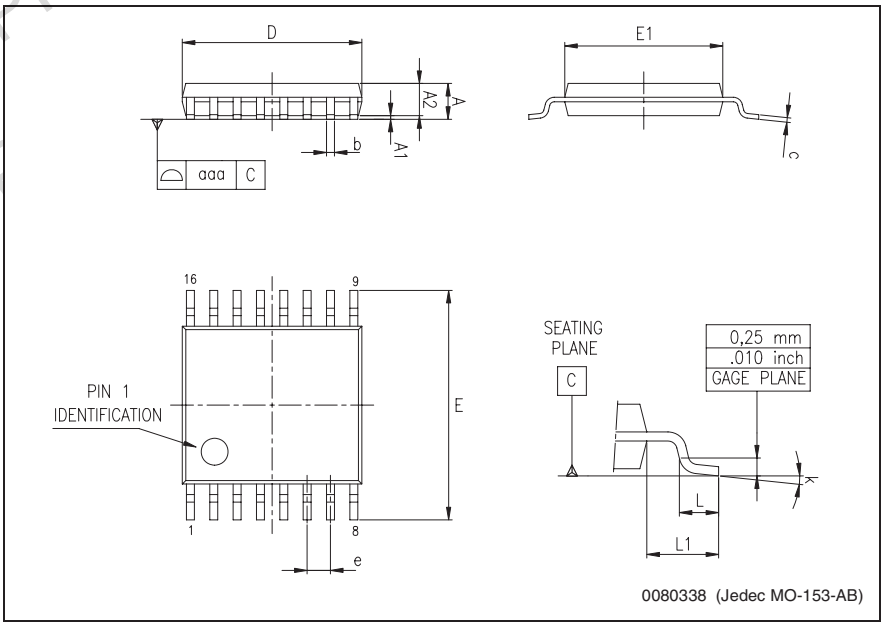
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.200			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.005		0.009
D (1)	4.900	5.000	5.100	0.114	0.118	0.122
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 (1)	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° (min.) 8° (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

OUTLINE AND MECHANICAL DATA



TSSOP16 (Body 4.4mm)



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
25-Jun-2008	1	Initial release.