

## TPD6F002-Q1 Automotive ESD Protection and EMI Filter for LCD Displays and FPD-Link

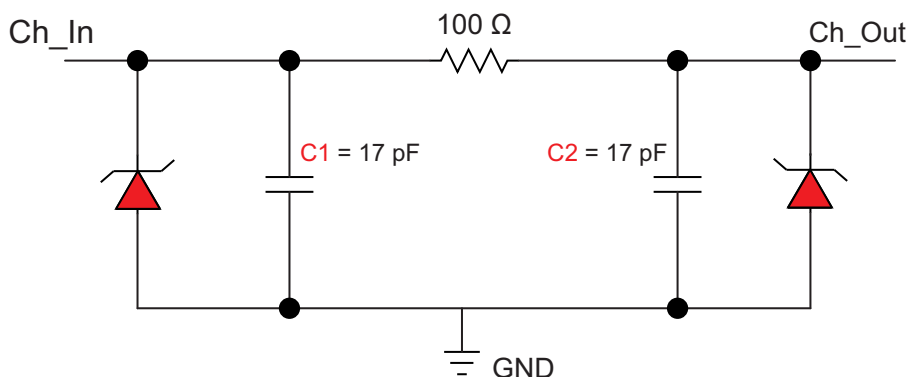
### 1 Features

- AEC-Q101 Qualified
- Six-Channel EMI Filtering for Data Ports
  - –47 dB Crosstalk Attenuation at 100 MHz
  - –30 dB Insertion Loss at 800 MHz
  - –3 dB Bandwidth 100 MHz
- Pi-Style (C-R-C) Filter Configuration  
( $R = 100\ \Omega$ ,  $C_{TOTAL} = 34\ \text{pF}$ )
- Robust ESD Protection Exceeds IEC 61000-4-2 (Level 4)
  - $\pm 20\text{-kV}$  IEC 61000-4-2 Contact Discharge
  - $\pm 30\text{-kV}$  IEC 61000-4-2 Air-Gap Discharge
- Low Leakage Current 20 nA (Max)
- Space-Saving SON Package (3 mm x 1.35 mm)

### 2 Applications

- LCD Display Interface
- GPIO
- Memory Interface
- Data Lines at Flex Cable
- FPD-Link

### 4 Simplified Schematic



### 3 Description

The TPD6F002-Q1 is a highly integrated device that provides a six channel Electromagnetic Interference (EMI) filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD6F002-Q1	SON (12)	3.00 mm x 1.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.2 Functional Block Diagram .....	<b>6</b>
<b>2 Applications</b> .....	<b>1</b>	8.3 Feature Description .....	<b>6</b>
<b>3 Description</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>7</b>
<b>4 Simplified Schematic</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>7</b>
<b>5 Revision History</b> .....	<b>2</b>	9.1 Application Information .....	<b>7</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	9.2 Typical Application .....	<b>8</b>
<b>7 Specifications</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>10</b>
7.1 Absolute Maximum Ratings .....	<b>3</b>	<b>11 Layout</b> .....	<b>10</b>
7.2 ESD Ratings .....	<b>3</b>	11.1 Layout Guidelines .....	<b>10</b>
7.3 Recommended Operating Conditions .....	<b>3</b>	11.2 Layout Example .....	<b>10</b>
7.4 Thermal Information .....	<b>4</b>	<b>12 Device and Documentation Support</b> .....	<b>11</b>
7.5 Electrical Characteristics .....	<b>4</b>	12.1 Trademarks .....	<b>11</b>
7.6 Typical Characteristics .....	<b>5</b>	12.2 Electrostatic Discharge Caution .....	<b>11</b>
<b>8 Detailed Description</b> .....	<b>6</b>	12.3 Glossary .....	<b>11</b>
8.1 Overview .....	<b>6</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>11</b>

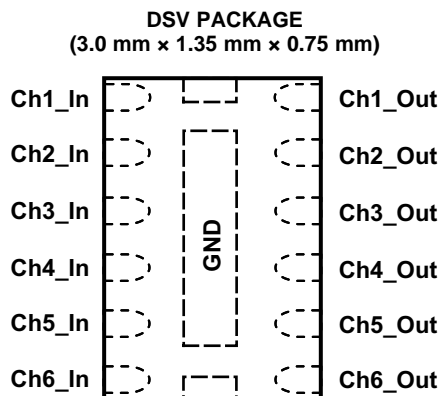
## 5 Revision History

### Changes from Original (December 2014) to Revision A

**Page**

• Initial release of full version datasheet. ....	<b>1</b>
---	----------

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
ChX_In	1, 2, 3, 4, 5, 6	IO	ESD-protected channel, connected to corresponding ChX_Out
ChX_Out	7, 8, 9, 10, 11, 12	IO	ESD-protected channel, connected to corresponding ChX_In
GND	G	G	Ground

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IO</sub>	IO to GND		5.75	V
T <sub>J</sub>	Junction temperature		125	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins <sup>(1)</sup>	±10
		Charged device model (CDM), per AEC Q101-005, all pins	±1.5
		IEC 61000-4-2 Contact Discharge	±20
		IEC 61000-4-2 Air-Gap Discharge	±30

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IO</sub>	Input pin voltage	0		5.5	V
T <sub>A</sub>	Operating free-air temperature	-40		125	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD6F002-Q1		UNIT
		DSV		
		12 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	120.7		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	104.4		
R <sub>θJB</sub>	Junction-to-board thermal resistance	78.5		
ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.0		
ψ <sub>JB</sub>	Junction-to-board characterization parameter	77.7		
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	66.5		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

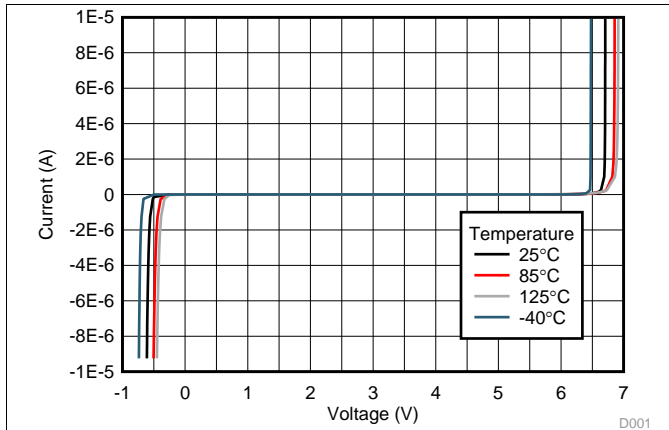
T<sub>A</sub> = –40°C to 125°C (Unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>BR</sub>	DC breakdown voltage	I <sub>IO</sub> = 10 μA			V
R	Resistance	V <sub>IN</sub> = 3.3 V, I <sub>In-to-out</sub> = 1 mA			Ω
C	Capacitance (C1 or C2)	V <sub>IO</sub> = 2.5 V			pF
I <sub>IO</sub>	Channel leakage current	V <sub>IO</sub> = 3.3 V			nA
f <sub>C</sub>	Cut-off frequency	Z <sub>SOURCE</sub> = 50 Ω, Z <sub>LOAD</sub> = 50 Ω			MHz

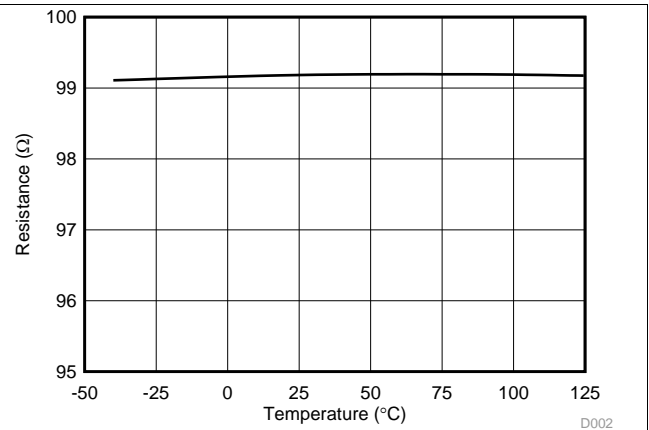
(1) Typical values are at T<sub>A</sub> = 25°C.

## 7.6 Typical Characteristics

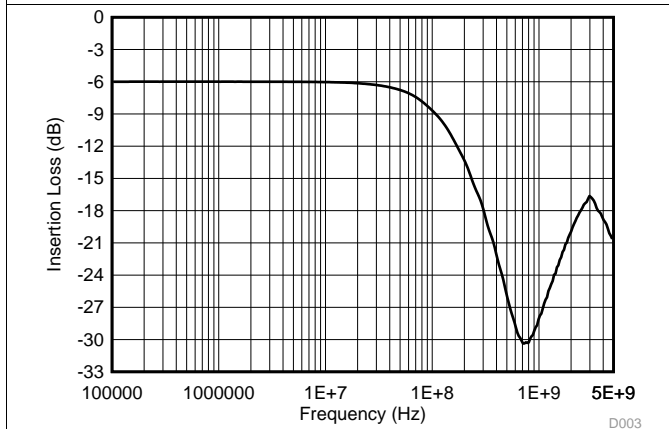
T<sub>A</sub> = 25°C unless otherwise noted



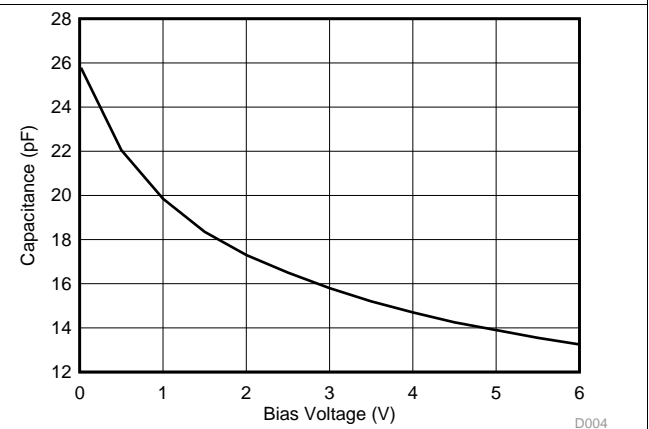
**Figure 1. DC Voltage-Current Sweep across Input, Output Pins**



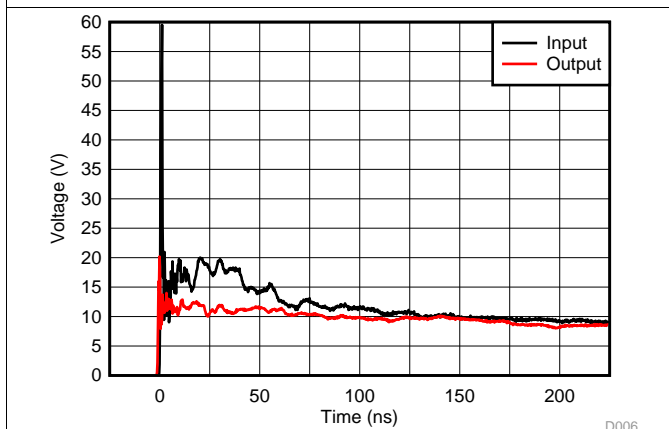
**Figure 2. Series Resistance vs Temperature**



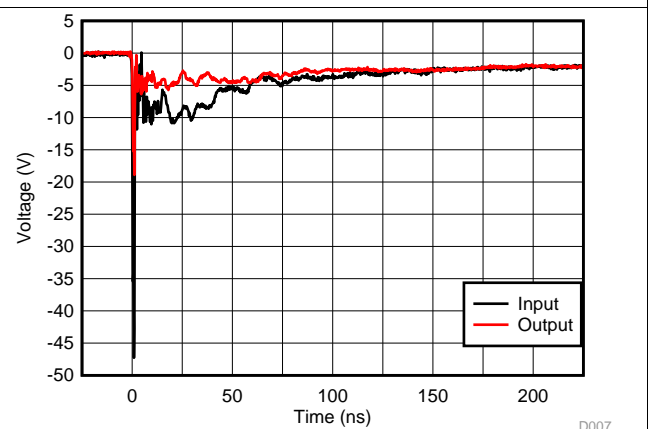
**Figure 3. Typical Insertion-loss Characteristics (DC Bias = 0 V, 50 Ω Environment)**



**Figure 4. Capacitance (C1 or C2) vs. Bias Voltage**



**Figure 5. +8-kV IEC Waveform**



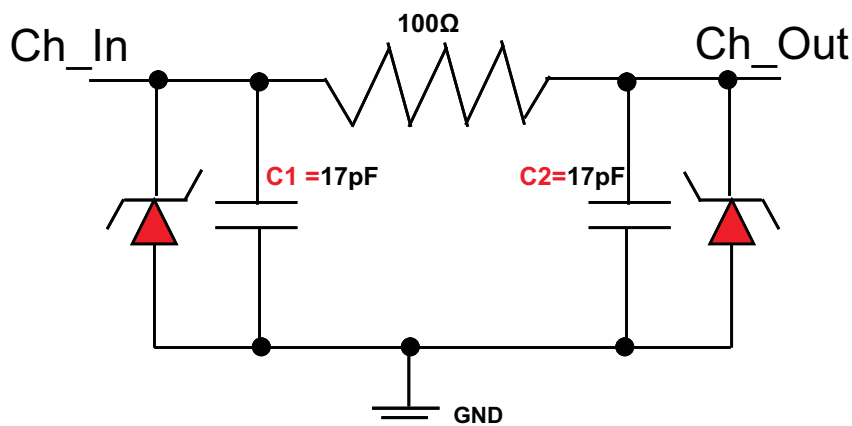
**Figure 6. -8-kV IEC Waveform**

## 8 Detailed Description

### 8.1 Overview

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TPD6F002-Q1 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, makes this device ideal for protecting interfaces like LCD displays, memory interfaces, and FPD-Link.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

#### 8.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards. It passes HBM H3B ( $\pm 8$  kV) and CDM C5 ( $\pm 1$  kV) ESD ratings and is qualified to operate from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### 8.3.2 Six-Channel EMI Filtering

This device provides six channels for EMI filtering of data lines with the following parameters:

- $-47$  dB Crosstalk Attenuation at 100 MHz
- $-30$  dB Insertion Loss at 800 MHz
- $-3$  dB Bandwidth: 100 MHz

#### 8.3.3 Pi-Style Filter Configuration

This device has a pi-style filtering configuration composed of a series resistor and two capacitors in parallel with the I/O pins. The typical resistor value is  $100\ \Omega$  and the typical capacitor values are  $17\ \text{pF}$  each.

#### 8.3.4 Robust ESD Protection

The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact ESD is rated at  $\pm 20$  kV and Air-gap ESD is rated at  $\pm 30$  kV.

## Feature Description (continued)

### 8.3.5 Low Leakage Current

The I/O pins feature an ultra-low leakage current of 20-nA (max) with a bias of 3.3 V

### 8.3.6 Space-Saving SON Package

The layout of this device makes it easy to add protection to existing layouts. The packages offer flow-through routing which requires minimal changes to existing layout for addition of these devices. Additionally, the device offers a small space-saving package that takes a minimal footprint on the board.

## 8.4 Device Functional Modes

The TPD6F002-Q1 is a passive integrated circuit that passively filters EMI and triggers when voltages are above  $V_{BR}$  or below the lower diode voltage ( $-0.6$  V). During ESD events, voltages as high as  $\pm 30$  kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels, the device reverts to passive.

## 9 Application and Implementation

---

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 9.1 Application Information

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

9.2 Typical Application

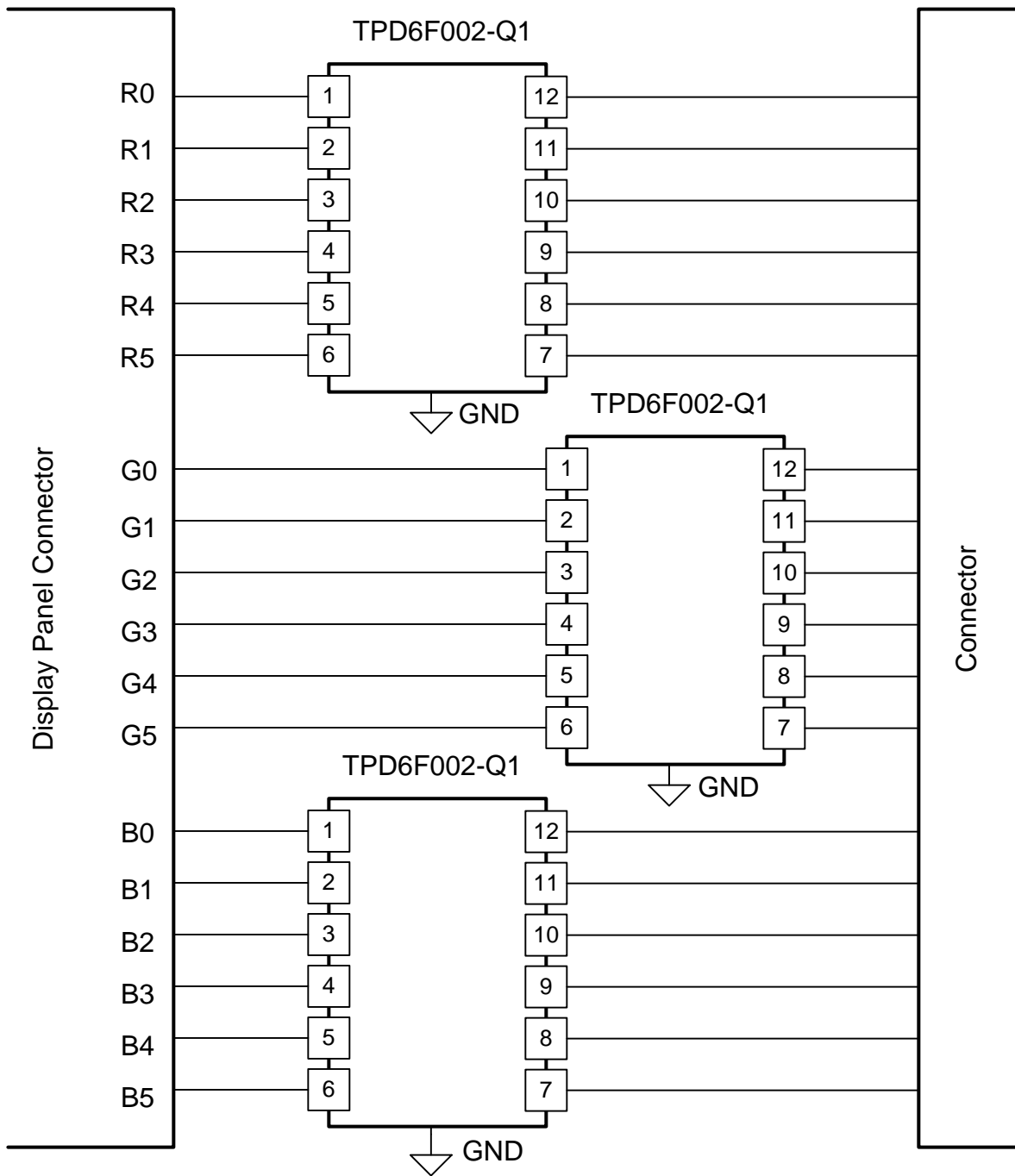


Figure 7. Display Panel Schematic



## Typical Application (continued)

### 9.2.1 Design Requirements

For this design example, three TPD6F002-Q1 devices are being used in an 18-bit display panel application. This will provide a complete ESD and EMI protection solution for the display connector.

Given the display panel application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on all pins except GND	0 V to 5 V
Operating Frequency	50 MHz

### 9.2.2 Detailed Design Procedure

To begin the design process, some design parameters must be decided; the designer needs to know the following:

- Signal range of all the protected lines
- Operating frequency
- Crosstalk response

#### 9.2.2.1 Signal Range on All Protected Lines

The TPD6F002-Q1 has 6 identical protection channels for signal lines. All I/O pins will support a signal range from 0 to 5.5 V.

#### 9.2.2.2 Operating Frequency

The TPD6F002-Q1 has a 100 MHz –3 dB bandwidth, which supports the operating frequency for this display.

#### 9.2.2.3 Crosstalk Response

The TPD6F002-Q1 has a –47 dB near-side crosstalk attenuation at 100 MHz, sufficient for this display.

### 9.2.3 Application Curves

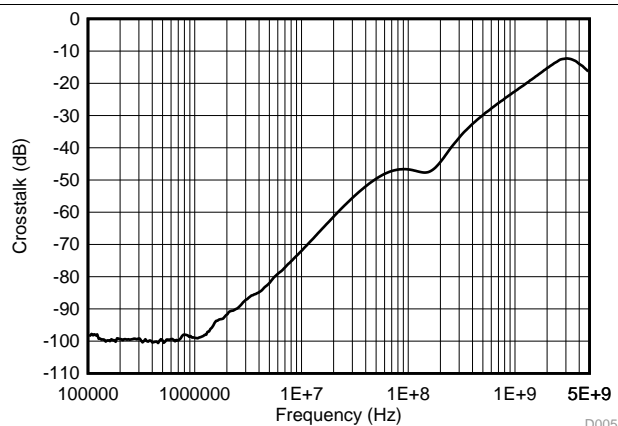


Figure 8. Near-Side Crosstalk

## 10 Power Supply Recommendations

This device is a passive EMI and ESD device so there is no need to power it. Care should be taken to not violate the recommended  $V_{IO}$  specification (5.5 V) to ensure the device functions properly.

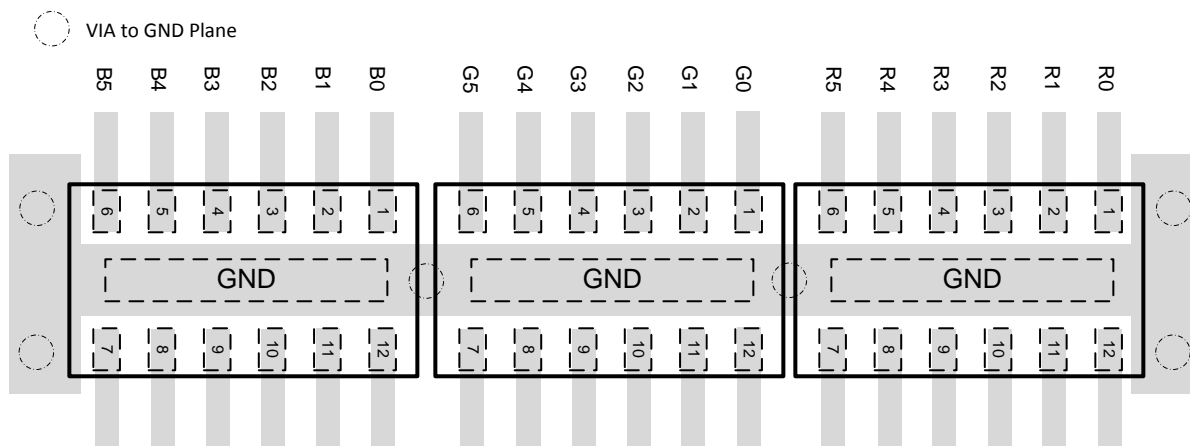
## 11 Layout

### 11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 11.2 Layout Example

This application is typical of an 18-bit RGB display panel layout.



**Figure 9. TPD6F002-Q1 Layout**

## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD6F002QDSVRQ1	ACTIVE	SON	DSV	12	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UNS	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPD6F002-Q1 :**

- Catalog: [TPD6F002](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6F002QDSVRQ1	SON	DSV	12	3000	180.0	8.4	1.74	3.33	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

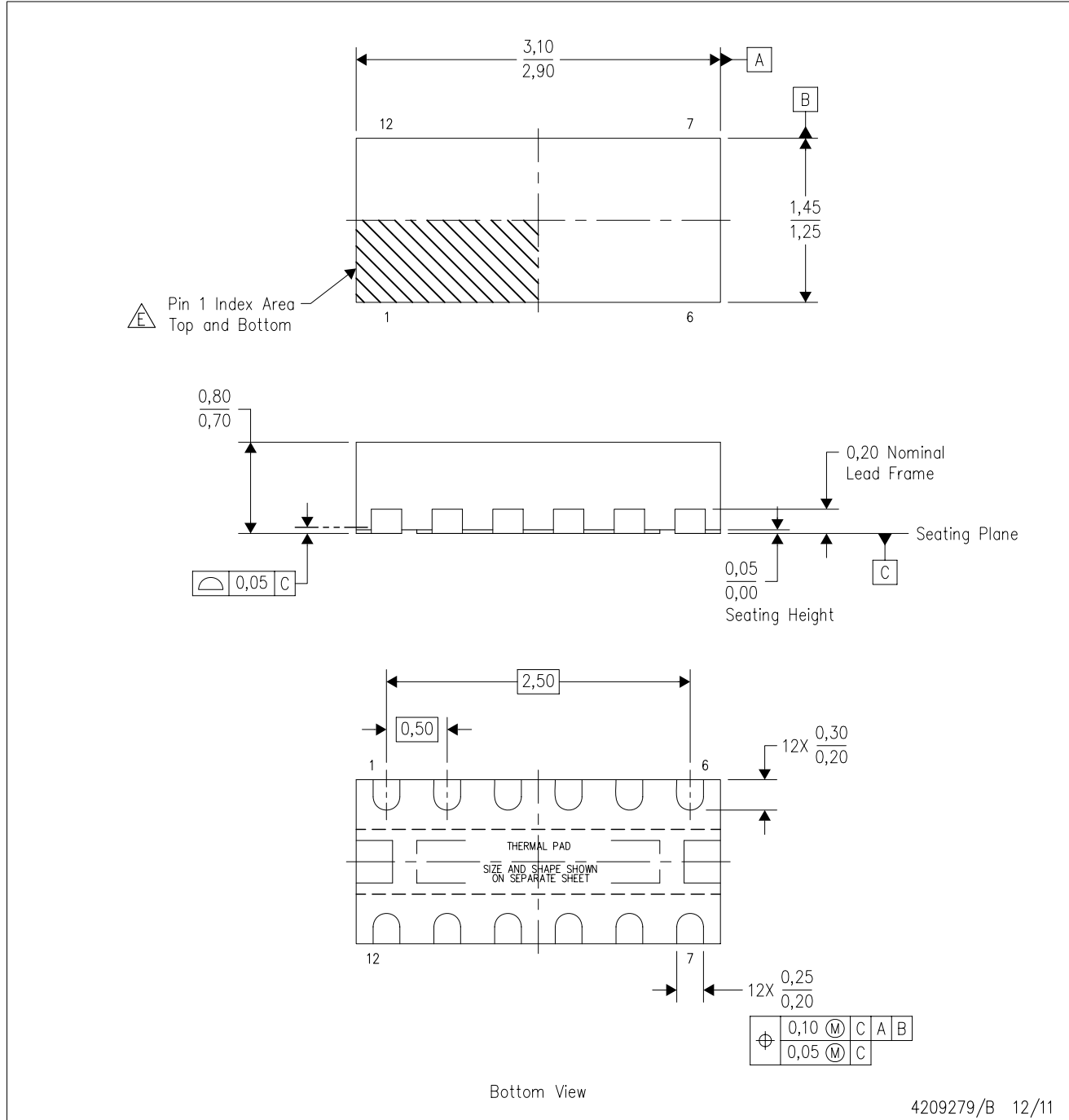


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6F002QDSVRQ1	SON	DSV	12	3000	213.0	191.0	35.0

DSV (R-PWSON-N12)

PLASTIC SMALL OUTLINE NO-LEAD



4209279/B 12/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.



## THERMAL PAD MECHANICAL DATA

DSV (R-PWSON-N12)

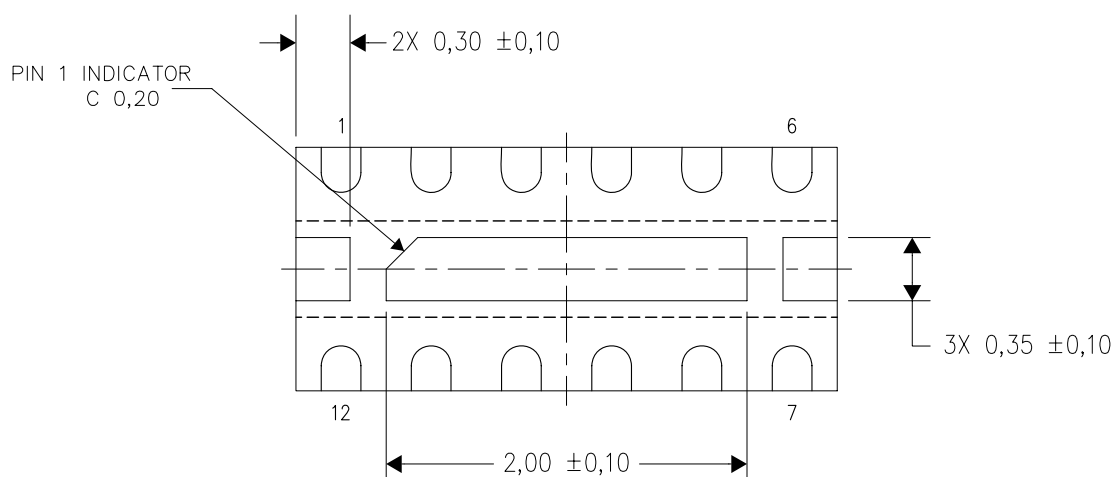
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

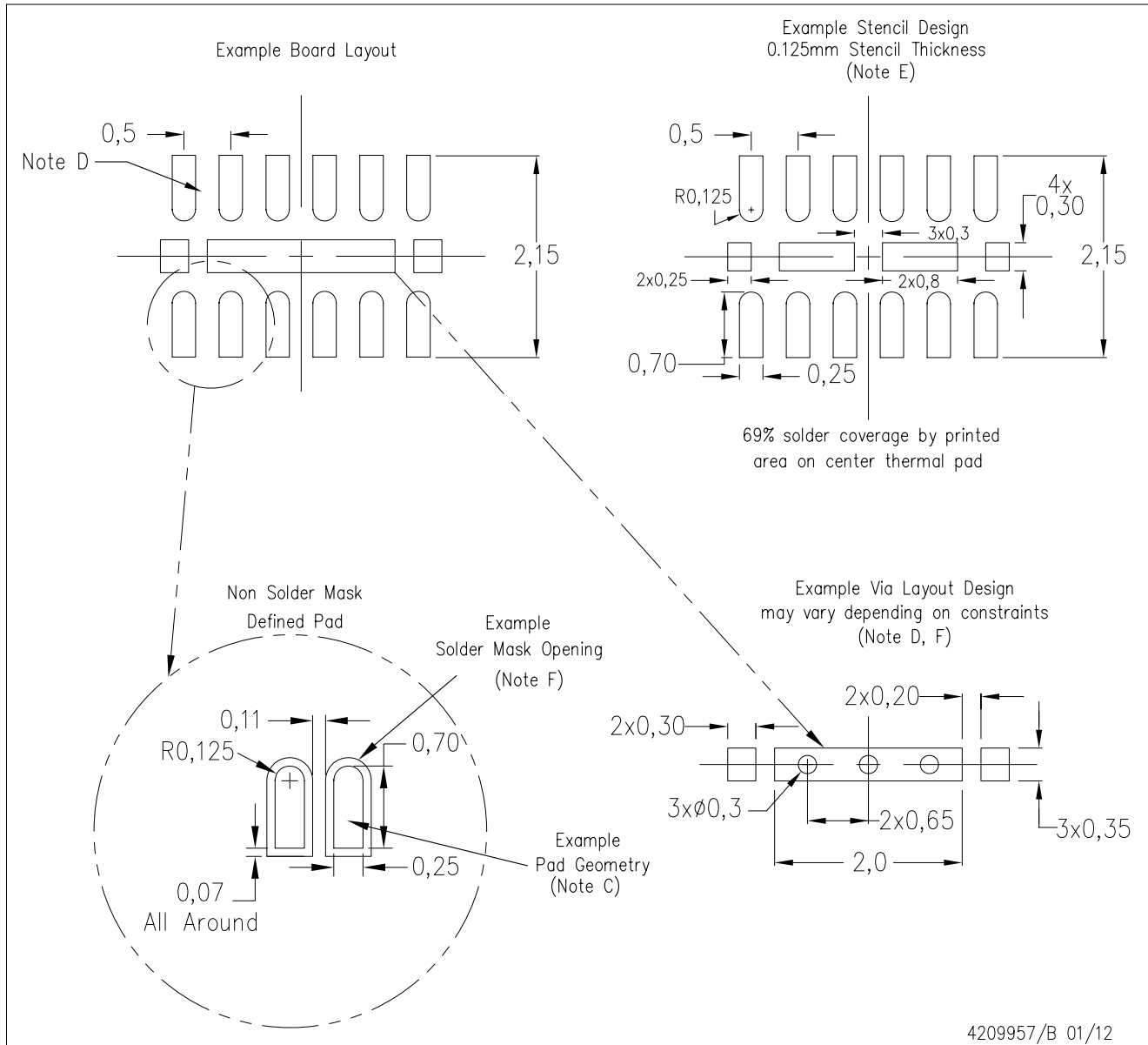
Exposed Thermal Pad Dimensions

4209318/B 12/11

NOTE: All linear dimensions are in millimeters

DSV (R-PWSON-N12)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated