RELIABILITY REPORT

FOR

MAX14548AEEWL+T

WAFER LEVEL PRODUCT

January 18, 2011

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX14548AEEWL+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX14548E/MAX14548AE 16-channel, bidirectional level translators (LLTs) provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. Logic signals present on the VL side of the device appear as a high-voltage logic signal on the VCC side of the device and vice versa. The devices feature a programming frequency input (PF) that adjusts the one-shot accelerator on-time to guarantee a bit rate of 100Mbps with a load capacitance L > 1.1V (MAX14548E) or VL > 1.4V (MAX14548AE) when driven low. The MAX14548E can drive capacitive loads up to 50pF with a guaranteed bit rate of 40Mbps when VL >= 1.1V and PF is driven high. The MAX14548AE can drive capacitive loads up to 50pF with a guaranteed bit rate of 40Mbps when VL >= 1.1V and PF is driven high. The device operate at full speed with external drivers that source as low as 4mA output current. Each I/O channel is pulled up to VCC or VL by an internal 35µA current source, allowing both devices to be driven by either push-pull or open-drain drivers. The devices feature multiple power-saving features including an enable input (EN) that places the device into a low-power shutdown mode when driven low and an automatic shutdown mode that disables the part when VCC is less than VL. The MAX14548AE output driver is designed to operate at full speed (100Mbps) with VL > 1.4V, which reduces the dynamic supply current vs. the MAX14548E. The state of I/O VCC_ and I/O VL_ are in high-impedance state during shutdown. The devices operate with VCC voltages from +1.7V to +3.6V and VL voltages from +1.1V to +3.6V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The devices are available in a 40-bump WLP (2.16mm x 3.46mm) package with 0.4mm ball pitch, and operate over the extended -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	100Mbps, 16-Channel LLTs
B. Process:	S4
C. Number of Device Transistors:	5264
D. Fabrication Location:	Texas
E. Assembly Location:	Japan
F. Date of Initial Production:	April 23, 2010

III. Packaging Information

A. Package Type:	40-bump WLP 5x8 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3674
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°
K. Single Layer Theta Jc:	N/A°
L. Multi Layer Theta Ja:	45°C/W
M. Multi Layer Theta Jc:	6°C/W

IV. Die Information

A. Dimensions:	89 X 140 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.05 @ 25C and 0.83 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TVKYAQ001E D/C 0909)

The LT14-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14548AEEWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TVKYAQ001E, D/C 0909

Note 1: Life Test Data may represent plastic DIP qualification lots.

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