

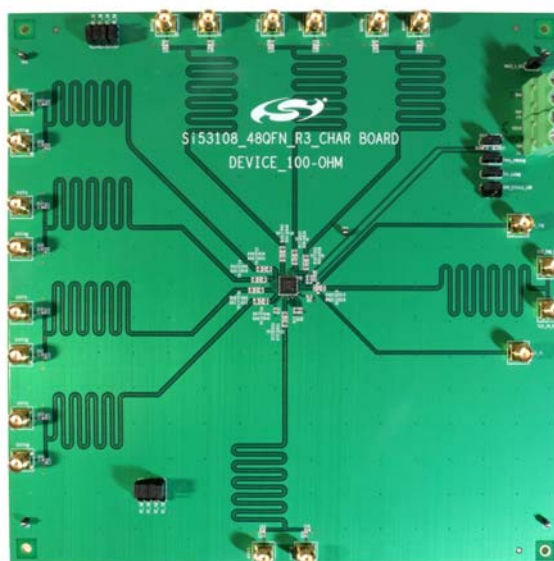
Si53108 EVALUATION BOARD USER'S GUIDE

Description

The Si53108-EVB can be used to evaluate the Si53108-A01AGM, an 8-output PCIe Gen1/2/3 buffer that can operate in either fanout or zero delay mode.

Features

- 10-inch traces to evaluate signal integrity
- The signal traces of the input and outputs have a single-ended impedance of 50 ohms, and differential impedance of 100 ohms.
- The series resistance on the outputs are set to match to this impedance design.
- DC pin controls per data sheet specification.
- Ability to measure input to output propagation delay.
- Ability to measure PCIe clock jitter.
- Ability to program features of Si53108-A01AGM via I²C interface.



Si53108-EVB

1. Schematics

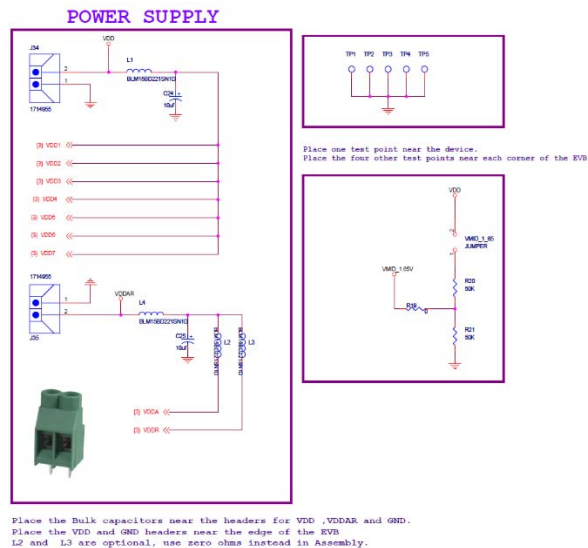
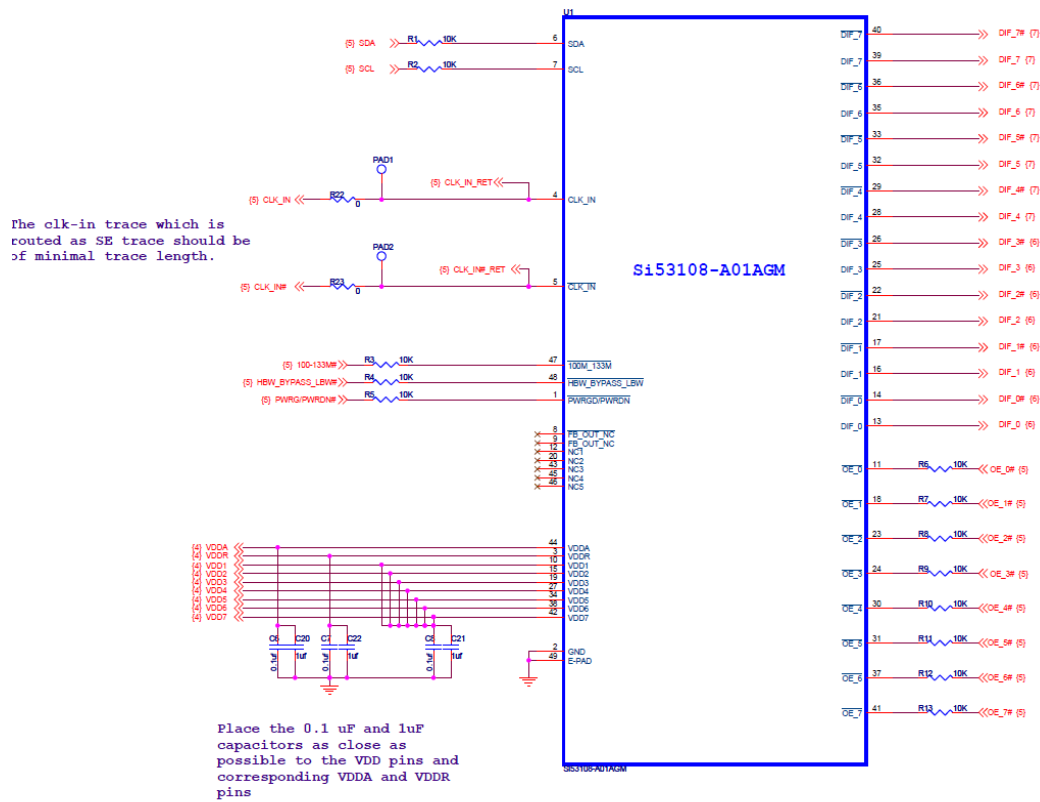


Figure 1. Schematic 1

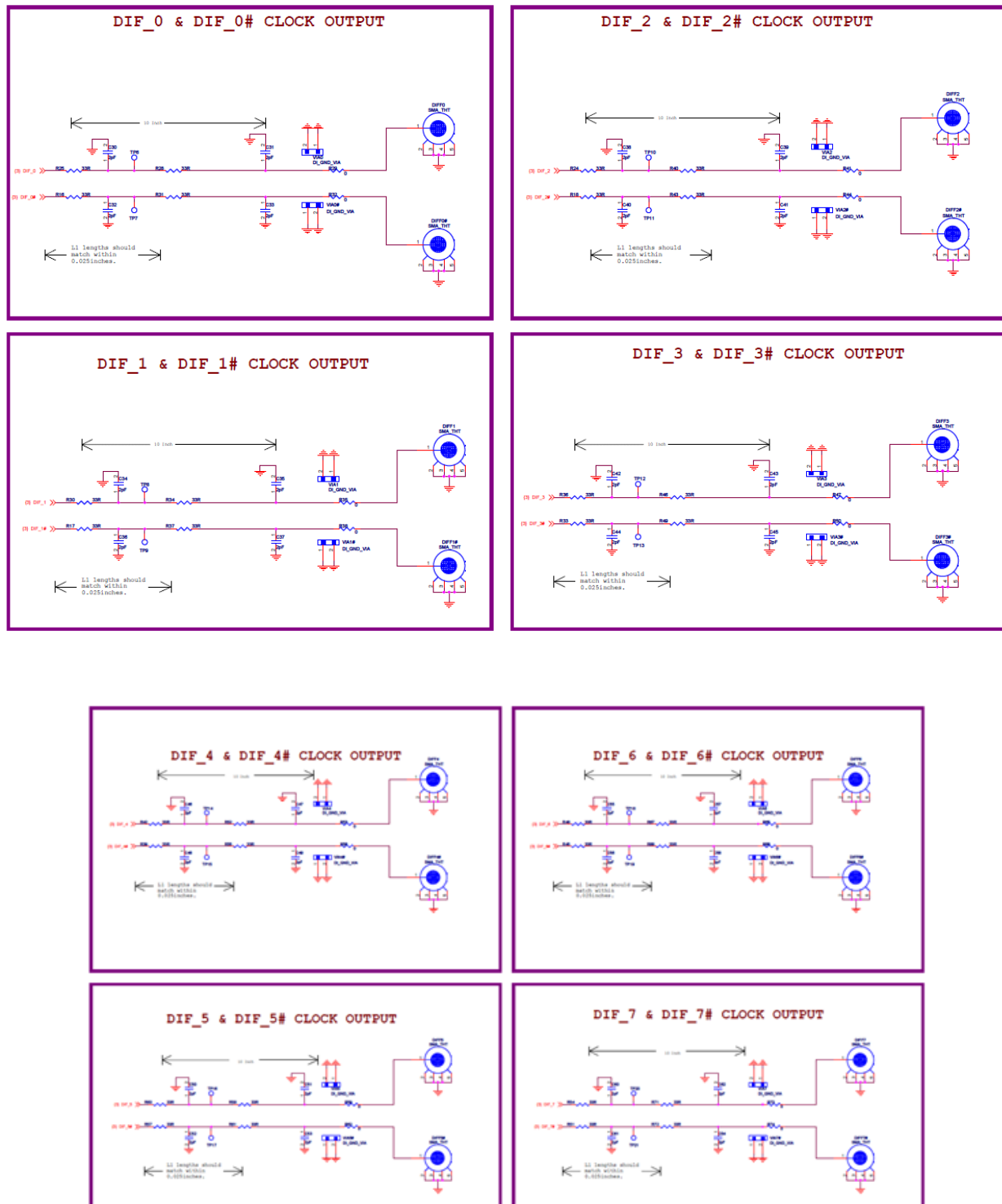


Figure 2. Schematic 2

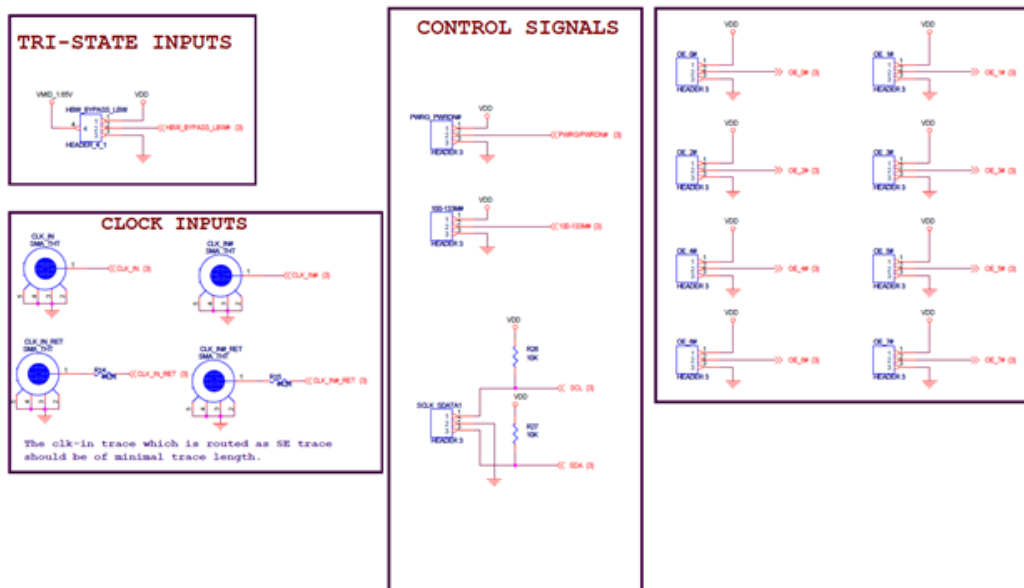


Figure 3. Schematic 3

2. Input and Power Supply Sequencing

The Si53108-A01AGM should be powered up with supply at both the VDD and VDD_IO nodes (at the jumpers available on the EVB). A 100MHz or 133MHz HCSL input clock should be applied to pins 8 and 9. There is no internal or on-board resistive termination, therefore HCSL termination needs to be provided at the input if needed by the driver. The input clock should be applied only after the supplies are stable.

3. Quick Start Guide:

1. Enable supply on the VDD pin.
2. Enable supply on the VDDIO pin.
3. Apply input clock on the SMA connectors CLK_IN/CLK_IN# and measure the return path clock on CLK_IN_RET, CLK_IN#_RET.

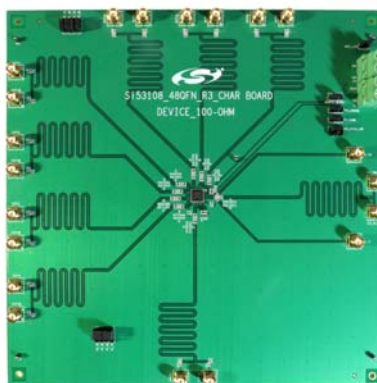


Figure 4. Clock Return Path

- a. The input clock measured at J32, J33 needs a 50-ohm termination on the scope.
 - b. The attenuation will be 1:10 after the above termination. Appropriate scaling (10x) needs to be set at the scope to adjust for the scaling.
4. The output clocks are now set up and can be measured on an oscilloscope or frequency domain measurement instrument.

4. Usage of the EVB

1. Once the EVB has been set up, the following can be evaluated:
2. Signal integrity of the device when driving 10-inch, 100-ohm differential traces.
3. Effect of capacitance load on output signal integrity.
4. Output-to-output skew over 10-inch traces.
5. Input-to-output propagation delay in BYPASS, HBW, and LBW modes using the input clock return path.
6. Measuring the power consumption of the device.
7. Modification of the device settings via the I²C interface.

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