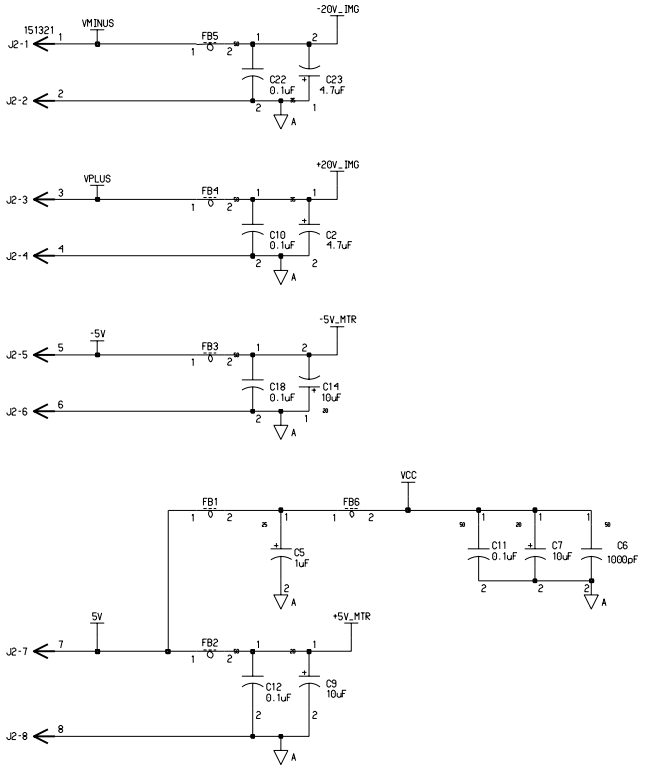
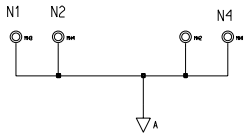
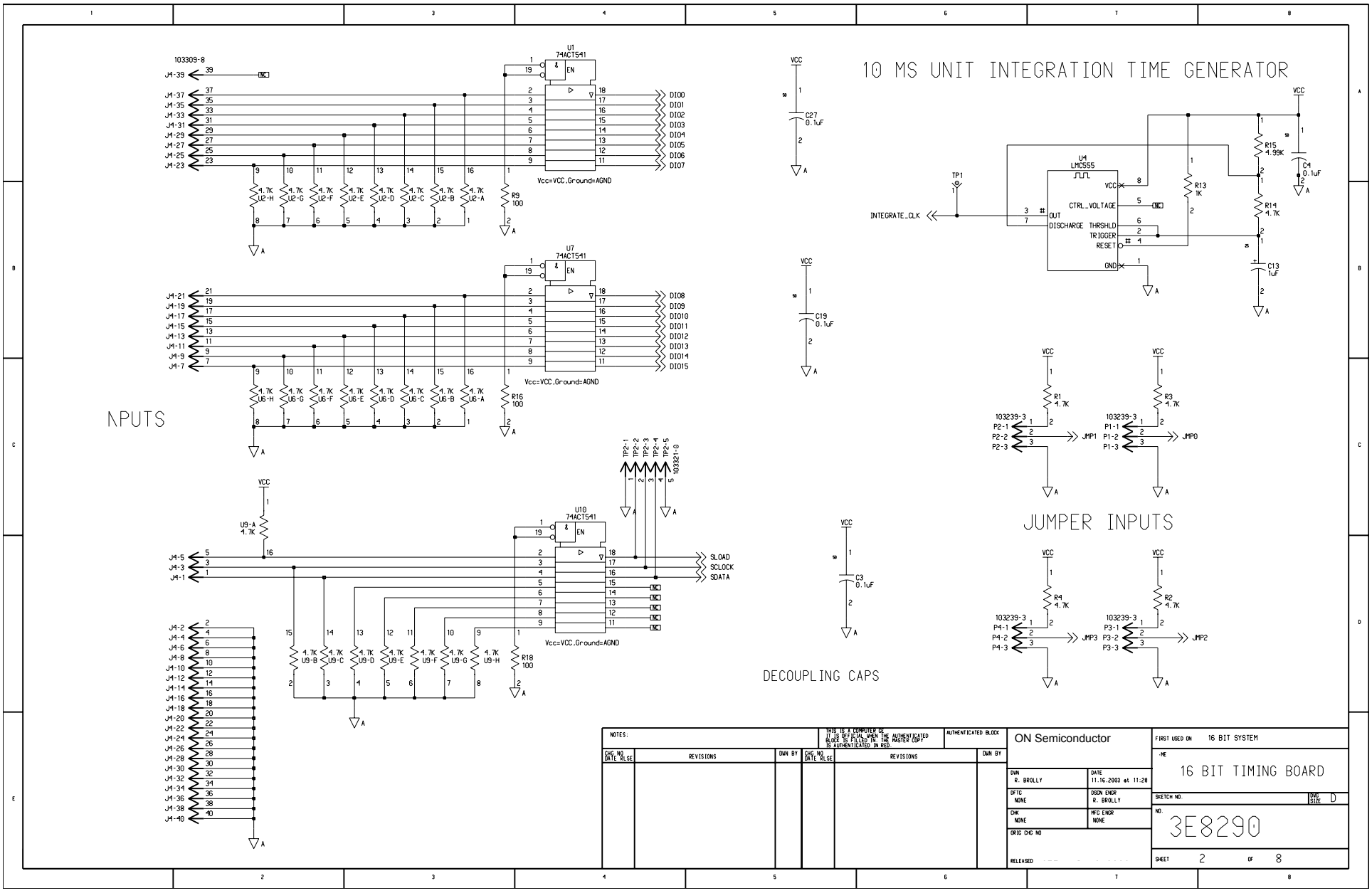
POWER CONNECTOR

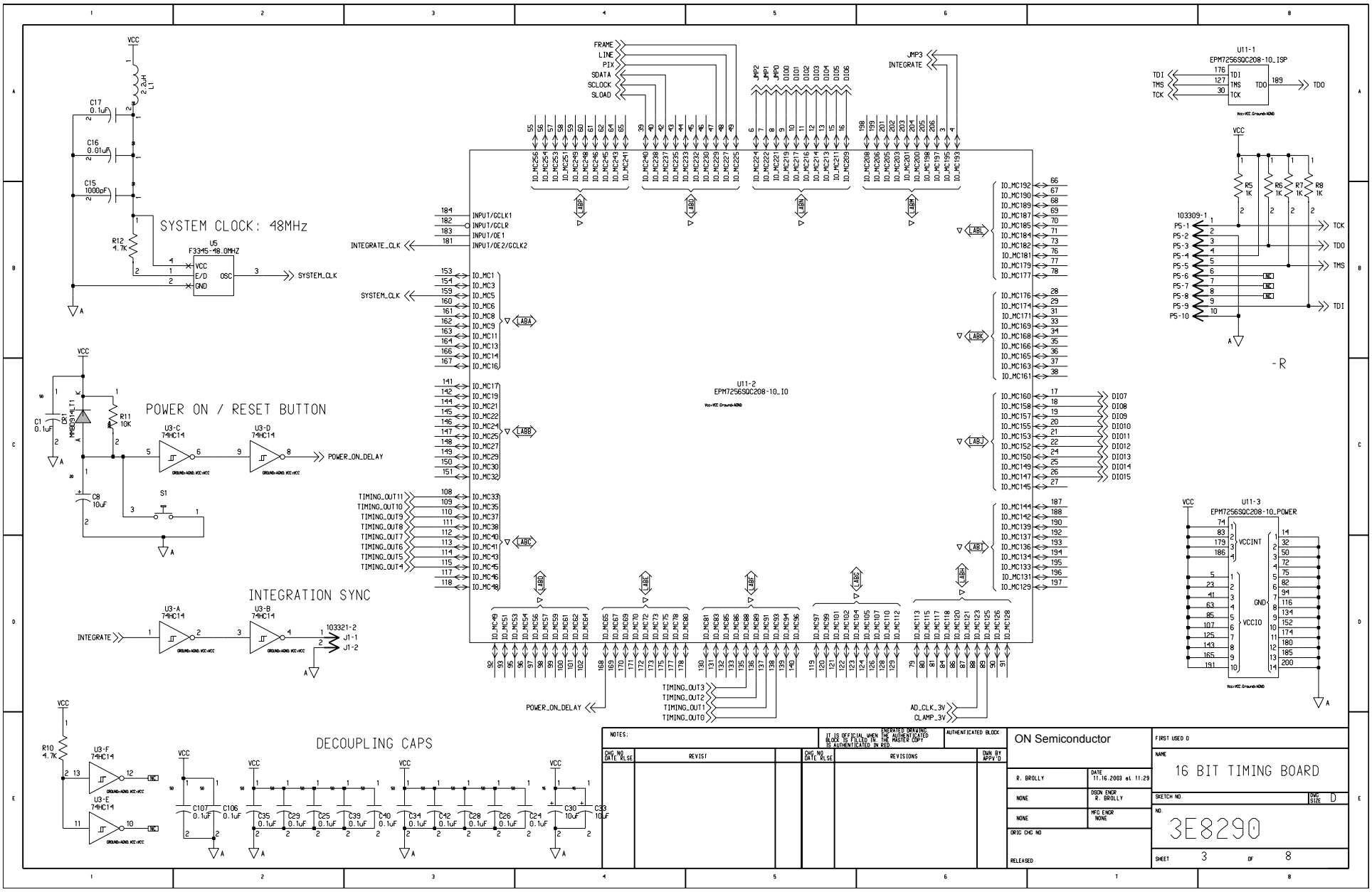


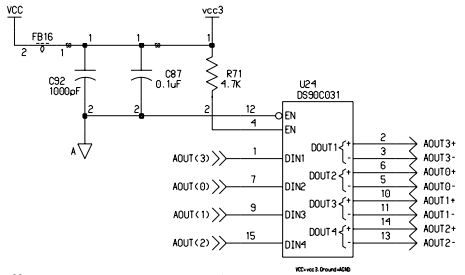


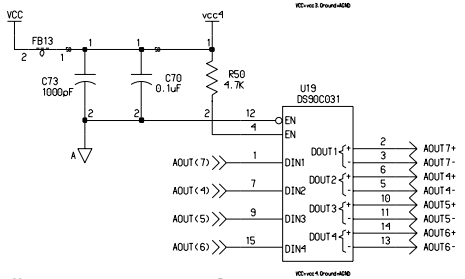
BOARD MOUNTING HOLES

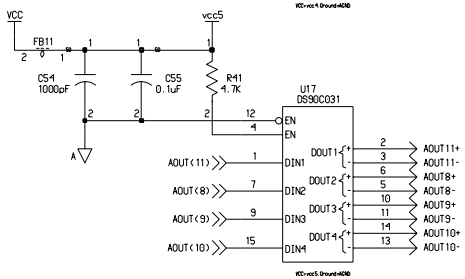
NOTES:									

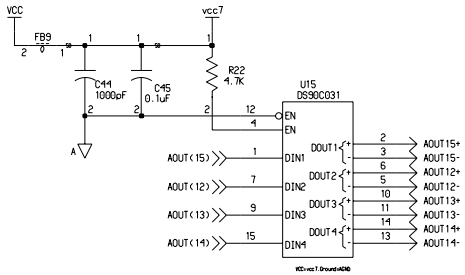

10 MS UNIT INTEGRATION TIME GENERATOR
INPUTS
JUMPER INPUTS
DECOUPLING CAPS
103309-8
U1
74ACT541
U7
74ACT541
U10
74ACT541
Vcc=VCC,Ground=AGND
DI00
DI01
DI02
DI03
DI04
DI05
DI06
DI07
DI08
DI09
DI010
DI011
DI012
DI013
DI014
DI015
SLOAD
SCLOAD
SDATA
U4
LM555
INTEGRATE_CLK
TP1
TP2-1
TP2-2
TP2-3
TP2-4
TP2-5
103321-0
JMP0
JMP1
JMP2
JMP3
C27 0.1uF
C19 0.1uF
C3 0.1uF
C4 0.1uF
C13 1uF
R15 1.99K
R14 4.7K
R13 1K
R1 4.7K
R2 4.7K
R3 4.7K
R4 4.7K
R9 100
R16 100
R18 100
ON Semiconductor
16 BIT TIMING BOARD
3E8290
SHEET 2 OF 8

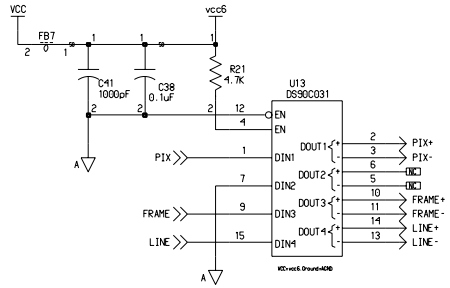

SYSTEM CLOCK: 48MHz
POWER ON / RESET BUTTON
INTEGRATION SYNC
DECOUPLING CAPS
U11-2
EPM7256SQC208-10_IO
U11-1
EPM7256SQC208-10_ISP
U11-3
EPM7256SQC208-10_POWER
ON Semiconductor
16 BIT TIMING BOARD
3E8290



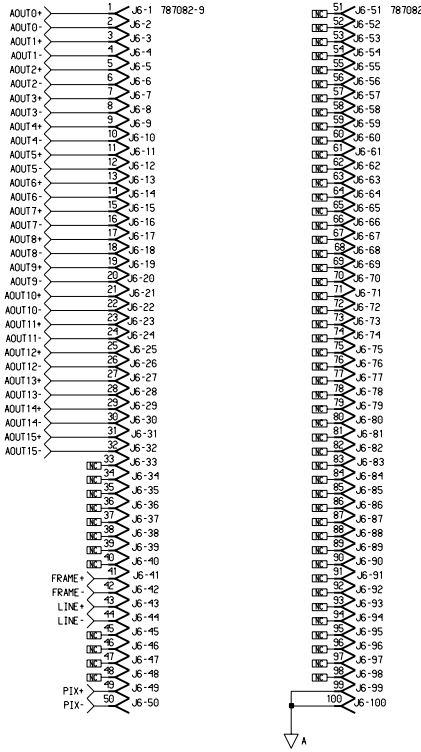








LVDS DRIVERS



LVDS OUTPUT CONNECTOR

NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.	AUTHENTICATED BLOCK	
CHG NO DATE BLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE	REVISIONS	DWN BY	

ON Semiconductor

R. BROLLY	DATE 11.16.2003 at 11:29
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
HC NO	
RELEASED	

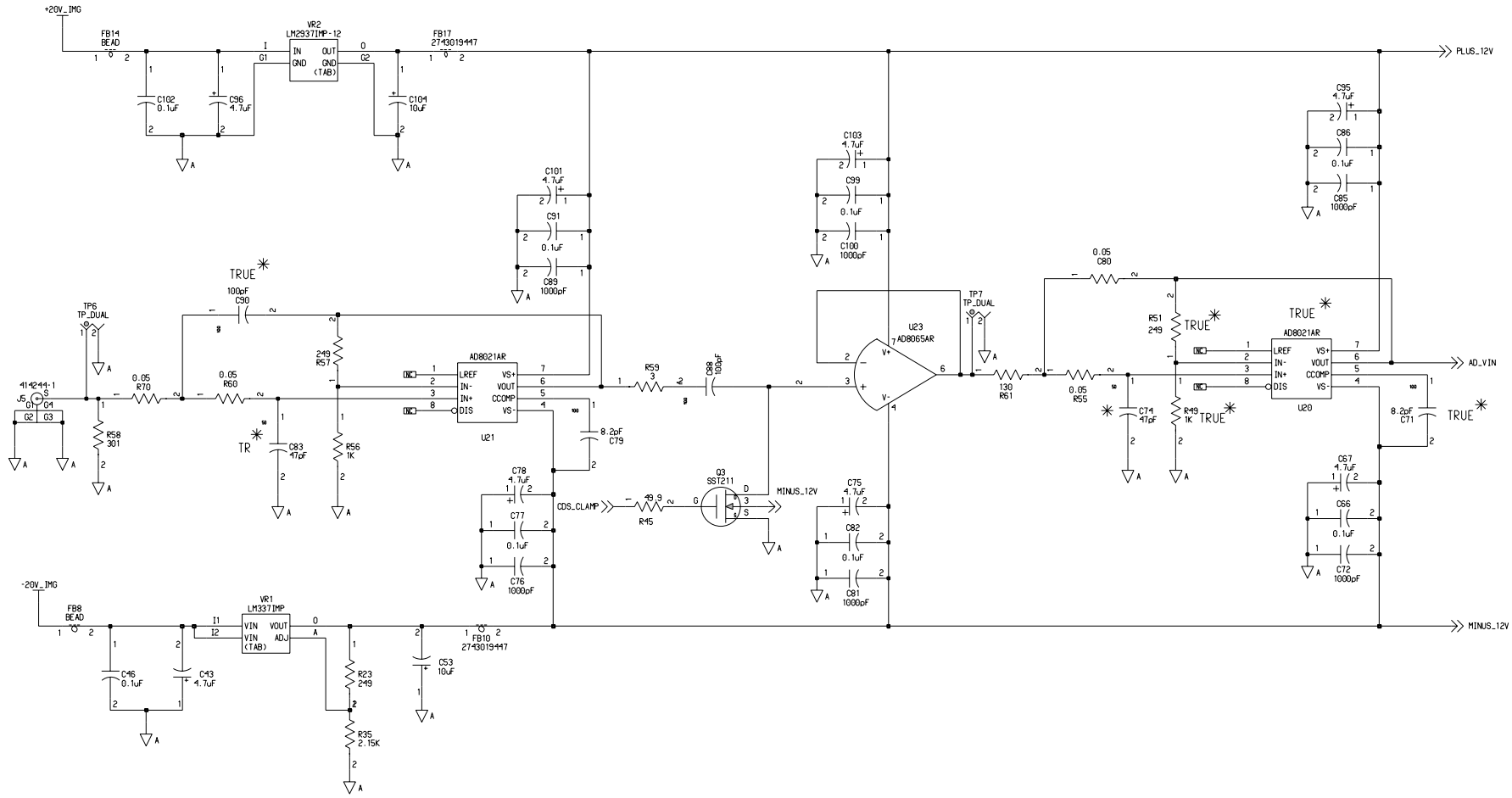
FIRST USED ON 16 BIT SYSTEM

NAME 16 BIT TIMING BOARD

SIZE D

NO. 3E8290

SHEET 4 OF 8



* "TRUE" INDICATES THAT THIS COMPONENT IS NOT POPULATED

NOTES:			THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.	THENTICATED BLOCK		
DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	ISIONS	DWN BY APPV'D	

ON Semiconductor

DWN R. BROLLY	DATE 11.16.2003 at 11:29
DFTG NONE	DSGN ENGR R. BROLLY
NONE	MFG ENGR NONE
ORIG CHG NO	
RELEASED	

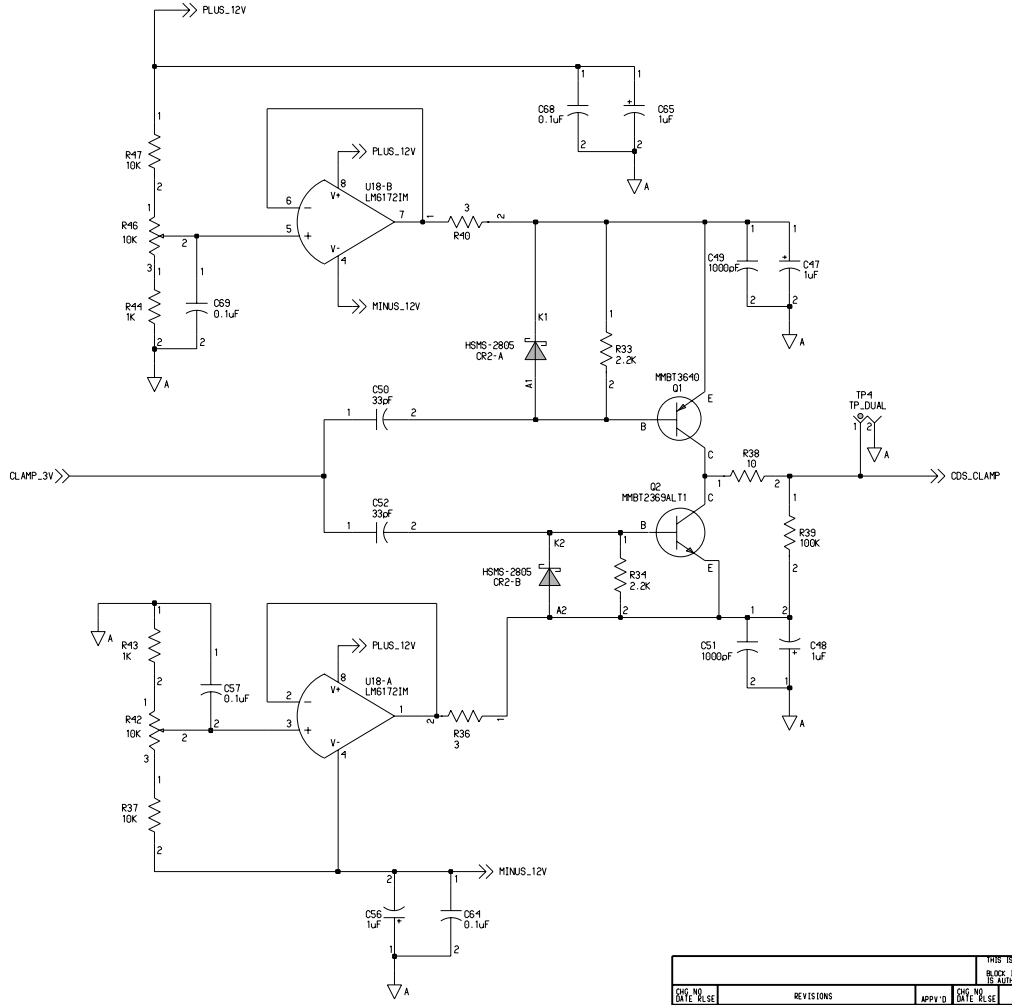
FIRST USED ON 16 BIT SYSTEM

NAME 16 BIT TIMING BOARD

SKETCH NO. | DWG SIZE

NO. 3E8290

SHEET 5 OF 8



			THIS IS A COMPUTER GENERATED DRAWING. HE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER IS AUTHENTICATED IN RED.	AUTHENTICATED BLOCK	
CHG NO DATE RLSE	REVISIONS	APPV'D	CHG NO DATE RLSE	REVISIONS	

ON Semiconductor

DWN R. BROLLY	DATE 11.16.2003 at 11:43
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	
RELEASED	

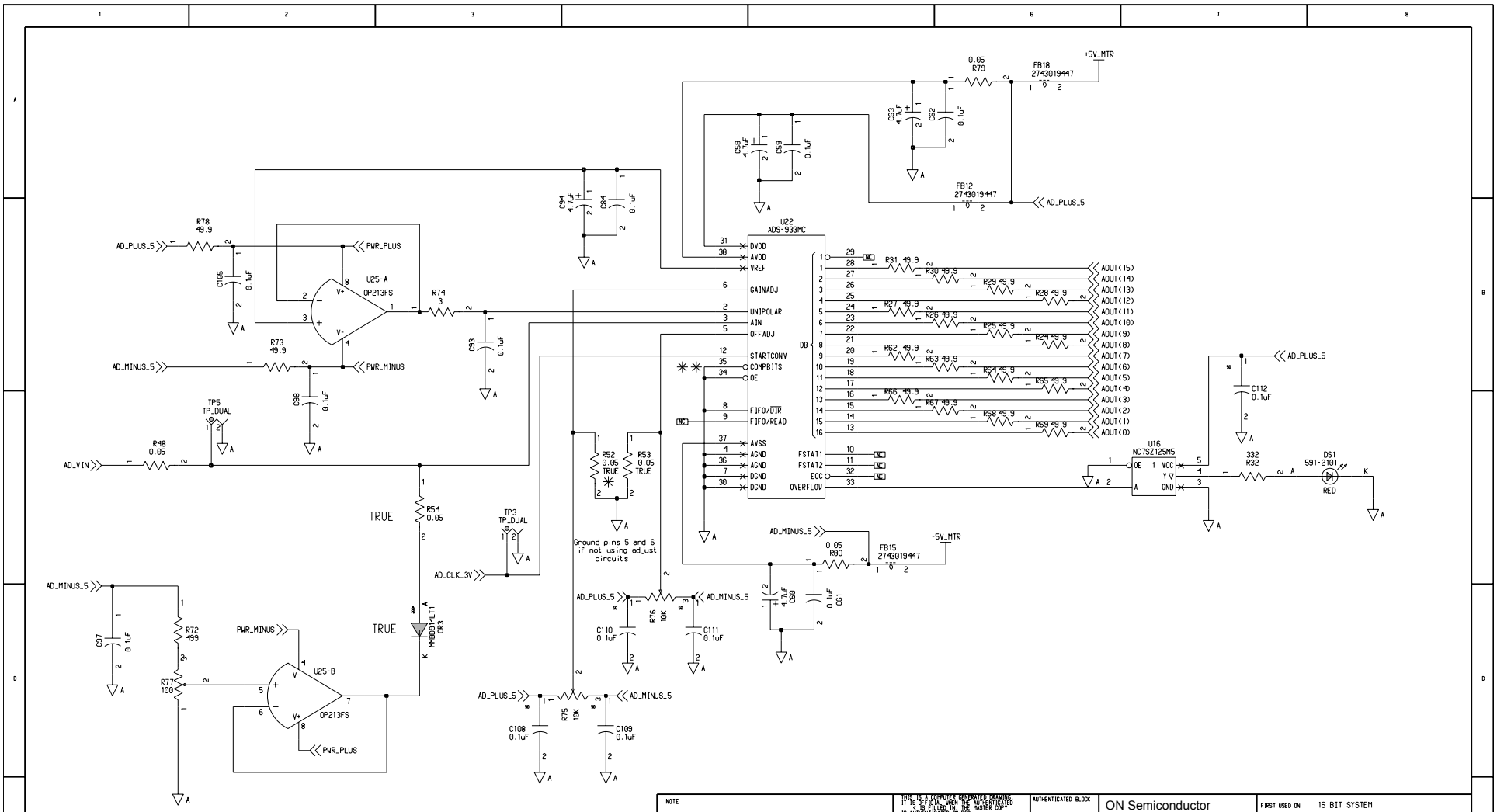
FIRST US 16 BIT SYSTEM

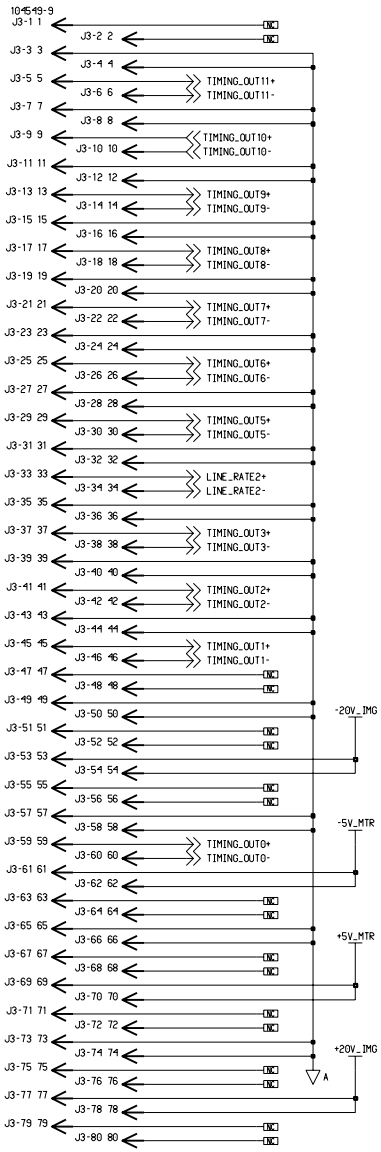
NAME 16 BIT TIMING BOARD

SKETCH NO. | DWG SIZE D

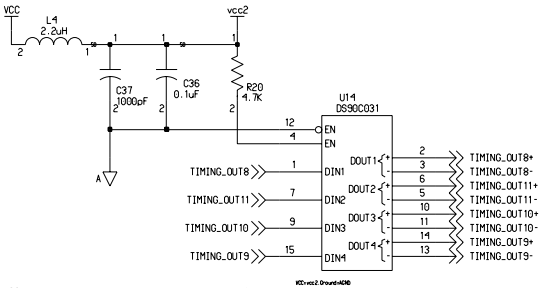
3E8290

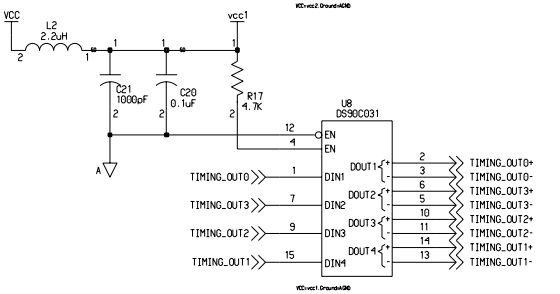
SHEET 6 OF 8

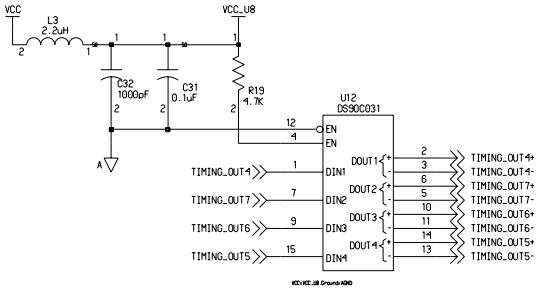

+5V_MTR
0.05
R79
FB18
2743019447
C63
4.7uF
C62
0.1uF
C58
4.7uF
C59
0.1uF
FB12
2743019447
AD_PLUS_5
C94
4.7uF
C84
0.1uF
U22
ADS-933MC
DVDD
AVDD
VREF
GAINADJ
UNIPOLAR
AIN
OFFADJ
STARTCONV
COMPBITS
OE
FIFO/DTR
FIFO/READ
AVSS
AGND
AGND
DGND
DGND
FSTAT1
FSTAT2
EOC
OVERFLOW
DB
AOUT(15)
AOUT(14)
AOUT(13)
AOUT(12)
AOUT(11)
AOUT(10)
AOUT(9)
AOUT(8)
AOUT(7)
AOUT(6)
AOUT(5)
AOUT(4)
AOUT(3)
AOUT(2)
AOUT(1)
AOUT(0)
R78
49.9
AD_PLUS_5
PWR_PLUS
C105
0.1uF
U25-A
OP213FS
R74
3
C93
0.1uF
R73
49.9
AD_MINUS_5
PWR_MINUS
C98
0.1uF
TP5
TP_DUAL
R48
0.05
AD_VIN
R52
0.05
TRUE
R53
0.05
TRUE
R54
0.05
TRUE
TP3
TP_DUAL
AD_CLK_3V
Ground pins 5 and 6
if not using adjust
circuits
AD_MINUS_5
0.05
R80
FB15
2743019447
-5V_MTR
C60
4.7uF
C61
0.1uF
AD_PLUS_5
R76
10K
AD_MINUS_5
C110
0.1uF
C111
0.1uF
AD_PLUS_5
R75
10K
AD_MINUS_5
C108
0.1uF
C109
0.1uF
AD_MINUS_5
C97
0.1uF
R72
499
R77
100
PWR_MINUS
U25-B
OP213FS
PWR_PLUS
TRUE
MMBD914LT1
D63
U16
NC7SZ125M5
OE
VCC
Y
GND
332
R32
DS1
591-2101
RED
AD_PLUS_5
C112
0.1uF
INDICATES THAT THIS COMPONENT IS NOT POPULATED
** U22 PIN 35 SHOULD BE LIFTED FOR STRAIGHT BINARY OUTPUT A/D OPERATION
NOTE
THIS IS A COMPUTER GENERATED DRAWING.
IT IS OFFICIAL WHEN THE AUTHENTICATED
IS FILLED IN THE MASTER COPY
IS AUTHENTICATED IN RED.
AUTHENTICATED BLOCK
CHG NO
DATE RLSE
REVIS
DWN BY
DATE RLS'
REVISIONS
DWN BY
APPV'D
ON Semiconductor
VN
R. BROLLY
DATE
11.16.2003 at 11:44
DFTG
NONE
R. BROLLY
CHK
NONE
MFG ENGR
NONE
ORIG CHG NO
RELEASED
FIRST USED ON
16 BIT SYSTEM
NAME
16 BIT TIMING BOARD
SKETCH NO.
SHEET
7
OF
8
NO.
3E8290



-RFACE CONNECTOR







NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

-ENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APP'D	DATE RLSE	REVIS	DJ

ON Semiconductor

DWN R. BROLLY	DATE 11.16.2003 at 11:47
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	
RELEASED	

FIRST USED ON 16 BIT SYSTEM

NAME 16 BIT TIMING BOARD

SKETCH NO. | DWG SIZE D

3E8290

SHEET 8 OF 8

Components
For Circuit Board Assembly

NO. 3E8290
SHEET 1 NEXT SHEET 2

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
1	7B9716	TOP-31	C1 C3 C4 C12 C17 C19 C27 C38 C45 C55 C57 C59 C61 C62 C66 C69 C70 C77 C82 C84 C86 C87 C91 C93 C97 C99 C108 C109 C110 C111 C112	56	0805_h.055	0.1uF_50V_.10 Ceramic Monolithic Chip
		BOT-25	C10 C11 C18 C20 C22 C24 C25 C26 C28 C29 C31 C34 C35 C36 C39 C40 C42 C46 C64 C68 C98 C102 C105 C106 C107			
2	254471	TOP-9	C15 C49 C51 C72 C76 C81 C85 C89 C100	9	0805_h.055	1000pF_50V_.05 MONOLITHIC, CERAMIC CHIP
3	980646	TOP-1	C16	1	0805_h.055	0.01uF_50V_.10 MONOLITHIC, CERAMIC CHIP
4	1C3731	BOT-4	C2 C23 C43 C96	4	pcap_6032_c_	4.7uF_35V_.10 ELECTROLYTIC, TANTALUM, CHIP
5	232271	BOT-2	C30 C33	2	case_c_h.110	10uF_16V_.20 ELECTROLYTIC, TANTALUM
6	4B4492	TOP-5 BOT-4	C41 C44 C54 C73 C92 C6 C21 C32 C37	9	0805_h.055	1000pF_50V_.20 MONOLITHIC, CERAMIC CHIP
7	785076	BOT-6	C5 C13 C47 C48 C56 C65	6	case_a_h.075	1uF_25V_.20 ELECTROLYTIC, TANTALUM
8	4B3897	TOP-2	C50 C52	2	0805_h.055	33pF_50V_.05 CAPACITOR-CERAMIC MONOLITHIC CHIP (PF)
9	4B4495	TOP-10	C58 C60 C63 C67 C75 C78 C94 C95 C101 C103	10	case_b_h.085	4.7uF_20V_.20 ELECTROLYTIC TANTALUM CHIP
10	2B1897	TOP-1	C79	1	0805_h.055	8.2pF_100V_.05 MONOLITHIC CERAMIC CHIP

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	PRELIMINARY DESIGN	RBB
REV 2	INITIAL RELEASE	RBB
REV 3	MODIFY DESIGN	RBB

SEE SHEET FOR ADD'L RE/

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8290 REV3

ON Semiconductor

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
16 BIT TIMING BOARD

XXXX

ES. ENG. RB | PKG. MATL.

SKETCH NO. | DWG. SIZE B

CK. RBB DFTG. | MFG. ENG.

3E8290

ORIG. CHG. NO. RELEASED

SHEET 1 NEXT SHEET 2

Components
For Circuit Board Assembly

NO. 3E8290
SHEET 2 NEXT SHEET 3

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
11	273746	TOP-1	C88	1	0805_h.055	100pF_100V_.05 MONOLITHIC, CERAMIC CHIP
12	258541	TOP-1 BOT-5	C9 C7 C8 C14 C53 C104	6	case_c_h.110	10uF_20V_.20 ELECTROLYTIC TANTALUM CHIP
13	616293	TOP-1	CR1	1	sot23_akn_sp	MMBD914LT1 DIODE, SWITCHING, 100V, 200mA
14	902510	TOP-1	CR2	1	sot143_kkaa_	HSMS-2805 DIODE, SCHOTTKY BARRIER, DUAL, 70V, 15mA
15	980654	TOP-1	DS1	1	led_591-2xxx	591-2101 RED SMT, 3mm PRISM, ROUND LENS
16	233152	TOP-9 BOT-9	FB2 FB7 FB9 FB11 FB12 FB13 FB15 FB16 FB18 FB1 FB3 FB4 FB5 FB6 FB8 FB10 FB14 FB17	18	fb_274301944	2743019447 - FERRITE, SMT BEADS
17	7E7515	TOP-1	J1	1	p02s_103321-	103321-2 STRAIGHT HEADER CONNECTOR
18	7E7653	TOP-1	J2	1	p08ra_151321	151321 RIGHT ANGLE HEADER CONNECTOR
19	999979	TOP-1	J3	1	p80s_104549-	104549-9 SMT, AMPMODU, SHROUDED HEADER CONNECTOR
20	7E7514	TOP-1	J4	1	p40s_103309-	103309-8 LOW PROFILE STRAIGHT HEADER
21	6C4636	TOP-1	J5	1	j01s_414244-	414244-1 RF COAXIAL RECEPTACLE
22	5C3152	TOP-1	J6	1	j100ra_78708	787082-9 AMPLIMITE VERTICLE RECEPTICLE CONNECTOR
23	1E1112	TOP-1 BOT-3	L1 L2 L3 L4	4	ind_1008cs_h	2.2uH SMT WIREWOUND ENCAPSULATED
24	323043	TOP-4	P1 P2 P3 P4	4	p03s_103239-	103239-3 3 PIN SQ. POST HDR. CONNECTOR/JUMPER

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	PRELIMINARY DESIGN	RBB
REV 2	INITIAL RELEASE	RBB
REV 3	MODIFY DESIGN	RBB

SEE SHEET FOR ADD'L REVISIO

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8290 REV3

ON Semiconductor

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
16 BIT TIMING BOARD

XXXX

ENG. RB
PKG. MATL.
CK. RBB
DFTG.
MFG. ENG.
ORIG. CHG. NO.
RELEASED

SKETCH NO.
DWG. SIZE B
3E8290
SHEET 2 NEXT SHEET 3

Components
For Circuit Board Assembly

NO. 3E8290
SHEET 3 NEXT SHEET 4

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
25	954067	TOP-1	P5	1	p10s_103309-	103309-1 LOW PROFILE STRAIGHT HEADER
26	236307	TOP-1	Q1	1	sot23_bce_sp	MMBT3640 TRANSISTOR, PNP, 12V, SWITCHING
27	4B4317	TOP-1	Q2	1	sot23_bce_sp	MMBT2369ALT1 TRANSISTOR, NPN, 15V, SWITCHING
28	232268	TOP-1	Q3	1	sot143_sdg3_	SST211 TRANSISTOR, N-CHANNEL, 30V, DEPLETION JFET
29	253549	TOP-7 BOT-8	R10 R12 R21 R22 R41 R50 R71 R1 R2 R3 R4 R14 R17 R19 R20	15	0805_h.030	4.7K Ohms_.100W_.05 THICK METAL FILM
30	233981	TOP-3	R11 R37 R47	3	0805_h.025	10K Ohms_.100W_.01 FLAT, THICK METAL FILM CHIP
31	902564	TOP-1 BOT-1	R13 R56	2	0805_h.025	1K Ohms_.100W_.01 FLAT, THICK METAL FILM CHIP
32	255502	BOT-1	R15	1	0805_h.030	4.99K Ohms_.100W_.01 FLAT, THICK METAL FILM, CHIP
33	902504	TOP-1 BOT-1	R23 R57	2	0805_h.030	249 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
34	8C8682	TOP-1	R32	1	0805_h.030	332 Ohms_.100W_.01 FLAT, THICK METAL FILM, CHIP
35	257083	BOT-2	R33 R34	2	0805_h.030	2.2K Ohms_.100W_.01 FLAT, THICK METAL FILM, CHIP
36	999707	TOP-1	R35	1	0805_h.030	2.15K Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
37	903960	TOP-4	R36 R40 R59 R74	4	0805_h.030	3 Ohms_.100W_.05 FLAT, THICK METAL FILM, CHIP
38	232841	TOP-1	R38	1	0805_h.030	10 Ohms_.100W_.05 FLAT, THICK

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	PRELIMINARY DESIGN	RBB
REV 2	INITIAL RELEASE	RBB
REV 3	MODIFY DESIGN	RBB

SEE SHEET FOR ADD'L REVISIO

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8290 REV3

ON Semiconductor

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
16 BIT TIMING BOARD

XXXX

ENG. RB
PKG. MATL.
CK. RBB
DFTG.
MFG. ENG.
ORIG. CHG. NO.
RELEASED

SKETCH NO.
DWG. SIZE B

3E8290

SHEET 3 NEXT SHEET 4

Components
For Circuit Board Assembly

NO. 3E8290
SHEET 4 NEXT SHEET 5

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
						METAL FILM, CHIP
39	254478	TOP-1	R39	1	0805_h.030	100K Ohms_.100W_.05 FLAT, THICK METAL FILM, CHIP
40	770026	TOP-4	R42 R46 R75 R76	4	pot_3266w_h.	10K POT, MULTI-TURN
41	250796	TOP-2 BOT-4	R43 R44 R5 R6 R7 R8	6	0805_h.030	1K Ohms_.100W_.05 FLAT, THICK METAL FILM, CHIP
42	901801	TOP-1 BOT-18	R45 R24 R25 R26 R27 R28 R29 R30 R31 R62 R63 R64 R65 R66 R67 R68 R69 R73 R78	19	0805_h.030	49.9 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
43	257516	TOP-6 BOT-1	R48 R55 R60 R70 R79 R80 C80	7	0805_h.030	0.05 Ohms_.100W_- ZERO OHM CHIP JUMPER
44	992869	TOP-1	R58	1	0805_h.030	301 Ohms_.100W_.01 FLAT, THICK METAL FILM, CHIP
45	941226	TOP-1	R61	1	0805_h.030	130 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
46	902559	TOP-1	R72	1	0805_h.030	499 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
47	7E8582	TOP-1	R77	1	pot_3266w_h.	100 POT, MULTI-TURN
48	283602	BOT-3	R9 R16 R18	3	0805_h.030	100 Ohms_.100W_.05 FLAT, THICK METAL FILM, CHIP
49	449610	TOP-1	S1	1	sw_tpa11cgpc	TPA11CGPC0 TP/TPA SERIES PUSHBUTTON SWITCH
50	901614	TOP-1	TP1	1	tp_tp104_h.2	TP-104-01-02 PRESS MOUNT TERMINAL - RED
51	7E7662	TOP-1	TP2	1	p05s_103321-	103321-0 STRAIGHT HEADER CONNECTOR

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	PRELIMINARY DESIGN	RBB
REV 2	INITIAL RELEASE	RBB
REV 3	MODIFY DESIGN	RBB

SEE SHEET FOR ADD'L REVISI

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8290 REV3

ON Semiconductor

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
16 BIT TIMING BOARD

XXXX

ENG. RB
PKG. MATL.
CK. RBB DFTG.
MFG. ENG.
ORIG. CHG. NO. RELEASED

SKETCH NO.
DWG. SIZE B

3E8290

SHEET 4 NEXT SHEET 5

Components
For Circuit Board Assembly

NO. 3E8290
SHEET 5 NEXT SHEET 6

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
52	TPDUAL	TOP-5	TP3 TP4 TP5 TP6 TP7	5	tpdual_.1_p4	TP_DUAL DUAL TEST PADS (THRU HOLE)
53	903888	TOP-3	U1 U7 U10	3	sol20_.370_h	74ACT541 BUFFER/DRIVER, OCTAL, W/ 3-STATE OUTPUT
54	3H0724	TOP-1	U11	1	qfp208_.0197	EPM7256SQC208-10_IO CPLD, MAX7000S, EPM7256SQC208-10
55	1E3787	TOP-1	U16	1	sot23-5_h.05	NC7SZ125M5 BUFFER/DRIVER, SINGLE, W/ 3-STATE OUTPUT
56	7E8545	TOP-1	U18	1	so08_.200_h.	LM6172IM DUAL VOLTAGE FEEDBACK AMPLIFIER
57	283585	BOT-3	U2 U6 U9	3	som16_.250_h	4.7K Ohms_.02 THICK FILM RESISTOR NETWORKS
58	7E9363	TOP-1	U21	1	so08_.200_h.	AD8021AR LOW NOISE, HIGH SPEED AMPLIFIER
59	7E9390	BOT-1	U22	1	dip40_.900_2	ADS-933MC A/D CONVERTER, 16-BIT, SAMPLING
60	7E9930	TOP-1	U23	1	so08_.200_h.	AD8065AR RAIL TO RAIL AMPLIFIER
61	7B8486	TOP-1	U25	1	so08_.200_h.	OP213FS DUAL, LOW NOISE, LOW DRIFT, OP AMP
62	263526	TOP-1	U3	1	so14_.210_h.	74HC14 INVERTER, HEX, W/ SCHMITT TRIGGER
63	263515	TOP-1	U4	1	so08_.210_h.	LMC555 ANALOG IC, TIMER
64	4B4464	TOP-1	U5	1	xtal_dip4_.3	F3345-48.0MHZ "48.000 MHz" FIXED FREQUENCY OSCILLATOR
65	5C2042	TOP-3 BOT-5	U8 U12 U14 U13 U15 U17 U19 U24	8	so16_.210_h.	DS90C031 DIFFERENTIAL LINE DRIVER, QUAD
66	6E8813	BOT-1	VR1	1	sot223_aioi_	LM337IMP 1A_3-40V_-1.2 to -37V VOLTAGE REGULATOR, NEG ADJ, 1A, 3-

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	PRELIMINARY DESIGN	RBB
REV 2	INITIAL RELEASE	RBB
REV 3	MODIFY DESIGN	RBB

SEE SHEET FOR ADD'L REVISI

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8290 REV3

ON Semiconductor

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
16 BIT TIMING BOARD

XXXX

ENG. RB | PKG. MATL.
CK. RBB DFTG. | MFG. ENG.
ORIG. CHG. NO. RELEASED

SKETCH NO. | DWG. SIZE B

3E8290

SHEET 5 NEXT SHEET 6

Components
For Circuit Board Assembly

NO. 3E8290
SHEET 6 NEXT SHEET 7

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
67	7E7010	BOT-1	VR2	1	sot223_igog_	LM2937IMP-12 500mA_26V_12V VOLTAGE REGULATOR, 12V, 500mA, 3-TERMINAL,
68	3E8290	HW-T-1	XXX1	1	HDWR	BARE BOARD For BRD1
69	755551	TOP-2	C74 C83	2NL	0805_h.060	NO LOAD 47pF_50V_.05 CAPACITOR-CERAMIC MONOLITHIC CHIP
70	2B1897	TOP-1	C71	1NL	0805_h.055	NO LOAD 8.2pF_100V_.05 MONOLITHIC CERAMIC CHIP
71	273746	BOT-1	C90	1NL	0805_h.055	NO LOAD 100pF_100V_.05 MONOLITHIC, CERAMIC CHIP
72	616293	BOT-1	CR3	1NL	sot23_akn_sp	NO LOAD MMBD914LT1 DIODE, SWITCHING, 100V, 200mA
73	902564	BOT-1	R49	1NL	0805_h.025	NO LOAD 1K Ohms_.100W_.01 FLAT, THICK METAL FILM CHIP
74	902504	BOT-1	R51	1NL	0805_h.030	NO LOAD 249 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
75	257516	TOP-3	R52 R53 R54	3NL	0805_h.030	NO LOAD 0.05 Ohms_.100W_- ZERO OHM CHIP JUMPER
76	7E9363	TOP-1	U20	1NL	so08_.200_h.	NO LOAD AD8021AR LOW NOISE, HIGH

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	PRELIMINARY DESIGN	RBB
REV 2	INITIAL RELEASE	RBB
REV 3	MODIFY DESIGN	RBB

SEE SHEET FOR ADD'L REVISIO

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8290 REV3

ON Semiconductor

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
16 BIT TIMING BOARD

XXXX

ENG. RB
PKG. MATL.

SKETCH NO.
DWG. SIZE B

CK. RBB
DFTG.
MFG. ENG.

3E8290

ORIG. CHG. NO.
RELEASED

SHEET 6 NEXT SHEET 7

REVISION BLOCK				
ZONE	REV.	DESCRIPTION	ESC#/DATE	APVD/DWN

NOTES:

1. MANUFACTURE BOARD IN ACCORDANCE WITH IPC-6011 & 6012, CLASS 3.

2. MATERIAL SPECIFICATIONS:
   2.1 CORE MATERIAL: POLYIMIDE LAMINATE, TYPE GIN, PER IPC-4101, HTE COPPER CLAD, SIZE AND CONSTRUCTION PER DETAIL A.
   2.2 PRE-PREG MATERIAL: POLYIMIDE, TYPE GIN, B STAGE PER IPC-4101, SIZE PER DETAIL A.
   2.3 MODIFICATIONS TO THE LAYER STACKUP AS SHOWN IN DETAIL A ARE PERMISSIBLE WITH THE FOLLOWING CONSTRAINTS:
      2.3.1 CONDUCTIVE LAYERS SHALL BE EVENLY SPACED THROUGHOUT.
      2.3.2 OVERALL THICKNESS SHALL BE UNCHANGED.

3. COPPER PLATE:
   3.1 HOLES: COPPER PLATING ON WALL OF HOLES SHALL BE 0.0015 MIN. UNLESS OTHERWISE SPECIFIED

4. SOLDER PLATE:
   4.1 SURFACE AND HOLES: EXPOSED LANDS AND LINES, EXCLUDING CONTACT FINGERS, SHALL BE TIN-LEAD COATED IN ACCORDANCE WITH THE SOLDERABILITY REQUIREMENTS OF J-STD-003.

5. CONDUCTOR WIDTH AND SPACING:
   5.1 WIDTH: 0.006 MIN
   5.2 SPACING: 0.007 MIN
   5.3 DESIGN FABRICATION ALLOWANCE IS 0.015.

6. HOLE REQUIREMENTS:
   6.1 ANNULAR RING: 0.002 MIN
   6.2 HOLE LOCATIONS TO BE 0.003 (DTP - DIAMETRICAL TRUE POSITION)
   6.3 HOLE SIZES APPLY AFTER SOLDER PLATING, REFLOW OR DEPOSITION

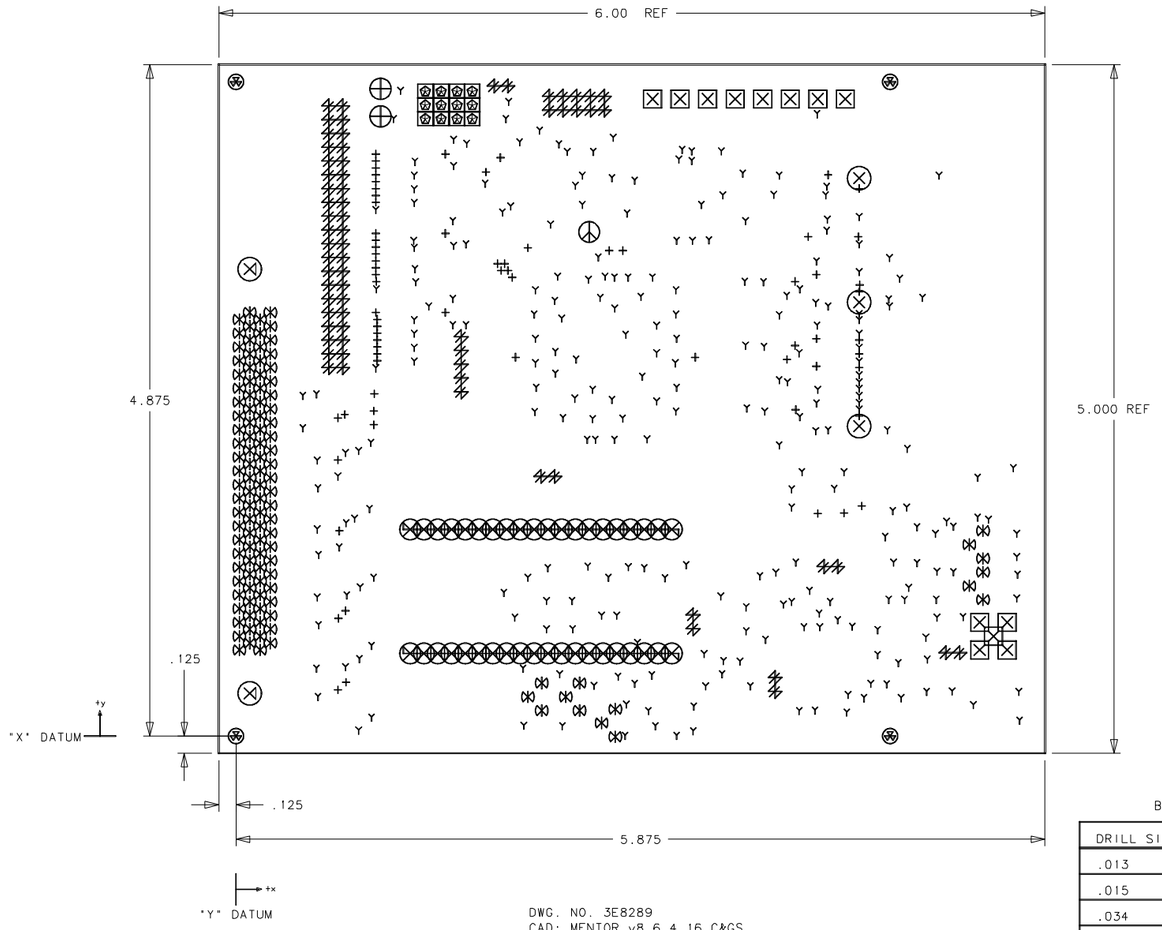
7. SOLDERMASK:
   7.1 SOLDERMASKING OF PRIMARY AND SECONDARY SIDES OF THE BOARD SHALL BE PER MASKING ARTWORK OVER BARE COPPER (SMOBC) USING PHOTOIMAGEABLE PERMANENT POLYMER FILM PER IPC-SM-840, CLASS T, 0.001 - 0.002 THICK.
   7.2 RESIZING FOR MINIMAL LAND TO MASK CLEARANCE PERMISSIBLE.

8. MARKING:
   8.1 MARKING OF PRIMARY AND SECONDARY SIDES SHALL BE PER MARKING ARTWORK USING WHITE NON-CONDUCTIVE EPOXY INK.

9. BOARD WARPAGE:
   9.1 BOARD WARPAGE 0.75% MAX.

10. TESTING:
    10.1 BOARDS SHALL BE TESTED USING CAD SUPPLIED IPC-D-356 FORMAT NET LIST. ELECTRICAL TESTING SHALL FOLLOW GUIDELINES ESTABLISHED BY IPC-ET-652.

11. MISCELLANEOUS NOTES:
    11.1 X,Y DATUMS INDICATE DRILL ORIGIN
    11.2 TEST COUPONS TO BE MADE AVAILABLE UPON REQUEST

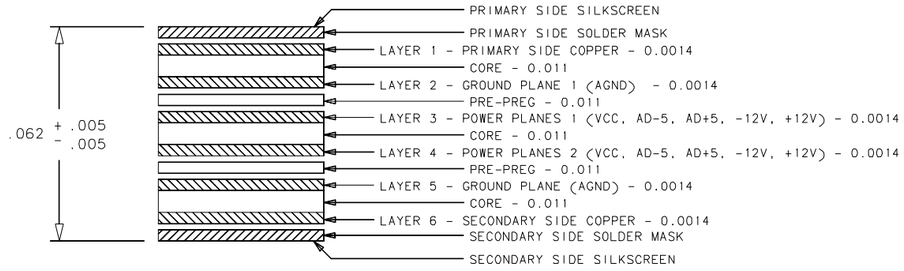


DWG. NO. 3E8289
CAD: MENTOR v8.6_4.16 C&GS
16 BIT TIMING BOARD
HOLE SYMBOLOGY
REV 1
VIEWED FROM PRIMARY SIDE
Nov 16 2002

BOARD's DRILL SCHEDULE

DRILL SIZE	DRILL SYMBOL	PLATED	COUNT	
.013	+	YES	70	VIA
.015	Y	YES	279	VIA
.034	⊠	YES	115	
.038	⊡	YES	12	
.042	⊹	YES	67	
.046	⊕	YES	2	
.047	⊗	YES	40	
.050	⊗	YES	3	
.052	⊠	YES	13	
.065	☮	YES	1	
.110	⊗	YES	2	
.125	⊗	YES	4	

TOTAL DRILL COUNT ON BOARD: 608



DETAIL A

LAYER STACKING CONFIGURATION
SCALE = NONE

REF: DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.				MATERIAL:		DWN B.NOEL 11-16-02	ON Semiconductor
DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE IS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.				UNLESS OTHERWISE SPECIFIED		DFTG X.XXXXX XXXXXXXX	TITLE PCB, 16 BIT TIMING
				DATUM PRECEDENCE PRI A SEC B TER C		BNGR R.BROLLY 11-16-02	
				DIMENSIONS ARE IN INCHES		BNGR X.XXXXX XXXXXXXX	
DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS ETC), MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	3E8290		1	TOLERANCES		CHK X.XXXXX XXXXXXXX	
	NEXT ASSY	USED ON	NEXT ASSY / FINAL ASSY	ANGLES ± 5° / 1 PL ± N/A	THIRD ANGLE PROJECTION	APVD X XXXXX XXXXXXXX	SIZE D / ITEM NO 3E8289 / REV 1
	APPLICATION		QUANTITY REQD	2 PL ± .010 / 3 PL ± .005		APVD X.XXXXX XXXXXXXX	
						APVD X.XXXXX XXXXXXXX	
						CONTRACT #	CODE / WT / SCALE 2X / SH 1 OF 3