4.25-GBPS CABLE AND PC BOARD EQUALIZER

FEATURES

- **Multirate Operation up to 4.25 Gbps**
- **Compensates up to 12 dB Loss at 2.1 GHz**
- **Suitable to Receive 4.25 Gbps Data Over up to 36 Inches (0.91 Meters) of FR4 PC Boards**
- **Suitable to Receive 4.25 Gbps Data Over up to 30 Feet (9.1 Meters) of CX4 Cable**
- **Ultralow Power Consumption**
- **Input Offset Cancellation**
- **High-Input Dynamic Range**
- **Output Disable**
- **Output Polarity Select**
- **Selectable Loss-of-Signal (LOS) Detection**
- **Selectable Squelch Function**
- **CML Data Outputs**
- **Single 3.3-V Supply**
- **Surface-Mount, Small-Footprint, 3-mm × 3-mm, 16-Pin QFN Package**

APPLICATIONS

- **1.0625-Gbps, 2.125-Gbps, and 4.25-Gbps Fibre Channel Systems**
- **High-Speed Links in Communication and Data Systems**
- **Backplane Interconnect**
- **Rack-to-Rack Interconnect**

DESCRIPTION

The TLK4201EA is a versatile, high-speed limiting equalizer for applications in digital high-speed links with data rates up to 4.25 Gbps.

This device provides a high-frequency boost of 12 dB at 2.1 GHz as well as sufficient gain to ensure a fully differential output swing for input signals as low as 100 mV_{P-P} (at the input of the interconnect line or cable).

The high input signal dynamic range ensures low-jitter output signals even when overdriven with input signal swings as high as 2000 mV_{P-P}.

The TLK4201EA includes fixed loss-of-signal (LOS) detection, which can be used to implement a squelch function by connecting the LOS output to the adjacent DISABLE input. The LOS function can be disabled by pulling LOSDIS to high level.

The TLK4201EA is available in a small-footprint, 3-mm × 3-mm, 16-pin QFN package. It requires a single 3.3-V supply.

This very power-efficient equalizer is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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BLOCK DIAGRAM

A simplified block diagram of the TLK4201EA is shown in Figure 1. This compact, low-power, 4.25-Gbps equalizer consists of a high-speed data path with an offset cancellation circuitry, a loss-of-signal detection block, and a band-gap voltage reference and bias current generation block.

The equalizer requires a single 3.3-V supply voltage. All circuit parts are described in detail as follows.

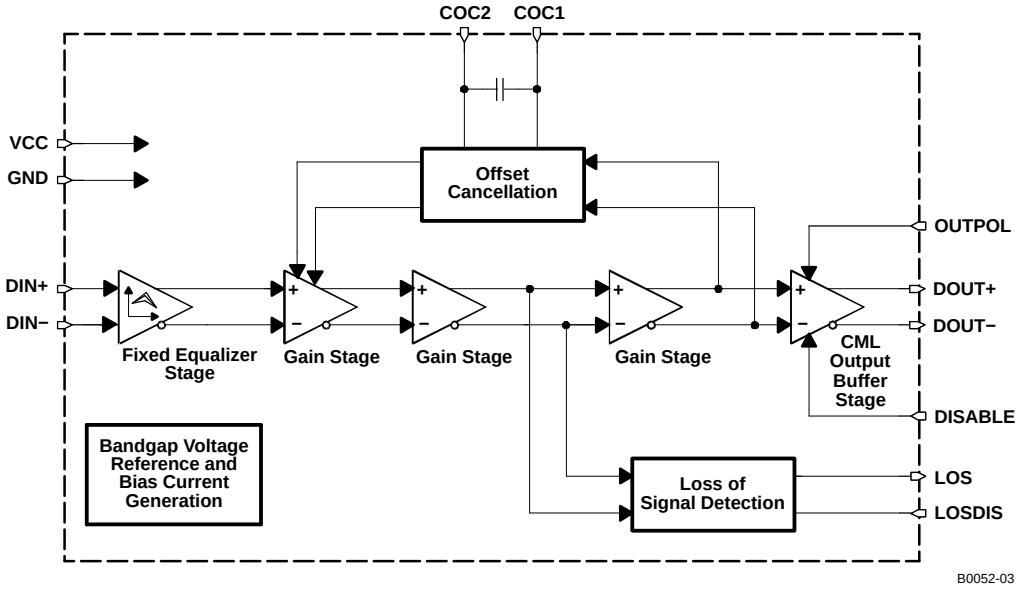


Figure 1. Simplified Block Diagram of the TLK4201EA

HIGH-SPEED DATA PATH

The high-speed data signal with frequency dependent loss is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the fixed equalizer input stage with 100-Ω on-chip differential line termination, three gain stages, which provide the required gain to ensure a limited output signal, and a CML output stage. The equalized and amplified data output signal is available at the output pins DOUT+/DOUT–, which provide 2 × 50-Ω back-termination to VCC. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input, and a disable function, controlled by the signal applied to the DISABLE input pin. An offset cancellation circuit compensates for inevitable internal offset voltages and thus ensures proper operation even for very small input data signals.

The low-frequency cutoff is as low as 10 kHz with the built-in filter capacitor. For applications which require even lower cutoff frequencies, an additional external filter capacitor can be connected to the COC1/COC2 pins.

LOSS OF SIGNAL DETECTION

The output signal of the second gain stage is monitored by the loss-of-signal detection circuitry. In this block, the input signal is compared to a fixed threshold. If the low-frequency components of the input signal fall below this threshold, a loss of signal is indicated at the LOS pin.

A squelch function can be easily implemented by connecting the LOS output to the adjacent DISABLE input. This measure avoids chattering of the output when no input signal is present. The LOS function can be disabled by pulling LOSDIS to high level.

BAND-GAP VOLTAGE AND BIAS GENERATION

The TLK4201EA equalizer is supplied by a single 3.3V ±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip band-gap voltage circuit generates a supply-voltage-independent reference from which all internally required voltages and bias currents are derived.

DEVICE INFORMATION

The TLK4201EA is available in a small-footprint, 3-mm × 3-mm, 16-pin QFN Package.

This quad package has a lead pitch of 0.5 mm. The pinout is shown in Figure 2.

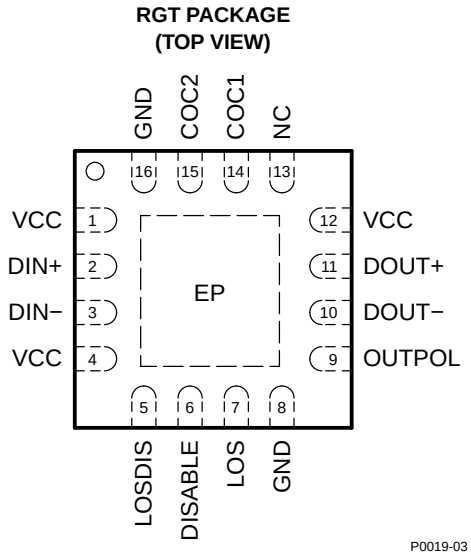


Figure 2. Pinout of TLK4201EA

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VCC	1, 4, 12	Supply	3.3V ± 10% supply voltage.
DIN+	2	Analog In	Noninverted data input. On-chip 100-Ω terminated to DIN–.
DIN–	3	Analog In	Inverted data input. On-chip 100-Ω terminated to DIN+.
LOSDIS	5	CMOS In	LOS disable input. High level disables LOS circuitry and sets LOS pin to low level. Low level enables LOS function. This pin has approximately 825-kΩ internal electronic pulldown resistor.
DISABLE	6	CMOS In	Disables CML output stage when set to high level. 400-kΩ on-chip pulldown resistor.
LOS	7	CMOS Out	High level indicates that the input signal amplitude is below the fixed threshold level.
GND	8, 16	Supply	Circuit ground
OUTPOL	9	CMOS In	Output data signal polarity select with approximately 715-kΩ internal electronic pullup resistor: Setting to high-level or leaving pin open selects normal polarity. Low-level selects inverted polarity.
DOUT–	10	CML Out	Inverted data output. On-chip 50-Ω back-terminated to VCC.
DOUT+	11	CML Out	Noninverted data output. On-chip 50-Ω back-terminated to VCC.
NC	13	—	Not connected
COC1	14	Analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
COC2	15	Analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
EP	EP		Exposed die pad (EP) must be grounded.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE(1)	UNIT
V_{CC}	Supply voltage at VCC(2)	–0.3 to 4	V
V_{DIN+}, V_{DIN-}	Input voltage at DIN+, DIN–(2)	0.5 to 4	V
V_{LOSDIS}, $V_{DISABLE}$, V_{OUTPOL}, V_{COC1}, V_{COC2}	Input voltage at LOSDIS, DISABLE, OUTPOL, COC1, COC2(2)	–0.3 to 4	V
$V_{COC,DIFF}$	Differential input voltage between COC1 and COC2	±1	V
$V_{DIN,DIFF}$	Differential input voltage between DIN+ and DIN–	±2.5	v
I_{DIN+}, I_{DIN-}	Continuous input current at input pins DIN+ and DIN–	–25 to 25	mA
ESD	ESD ratings at all pins, human body model (HBM)	2.5	kV
$T_{J,max}$	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 85	°C
T_A	Free-air operating temperature	–40 to 85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage, CMOS	2.1			V
V_{IL}	Low-level input voltage, CMOS			0.6	V
T_A	Free-air operating temperature	–40		85	°C

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{CC}	Supply current	LOSDIS = low, DISABLE = low, including CML output current		32	38	mA
R_I	Input resistance, data	Differential		100		Ω
R_O	Output resistance, data	Single-ended to V_{CC}		50		Ω
V_{OH}	High-level output voltage, LOS	I_{source} = 30 µA	2.4			V
V_{OL}	Low-level output voltage, LOS	I_{sink} = 1 mA			0.4	V

(1) Typical values are measured at V_{CC} = 3.3 V and T_A = 25°C

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
	Low frequency –3dB bandwidth	C_{OC} = open			10	50	kHz
		C_{OC} = 0.1 µF			0.8		
	Maximum data rate			4.25			Gbps
$V_{IN,MIN}$	Data input voltage sensitivity(2)	BER < 10^{-12}, input signal applied over 36 inches of 7-mil-wide stripline interconnect on standard FR4, voltage at the input of the interconnect line, K28.5 pattern at 4.25 Gbps.			100	120	mV_{P-P}
$V_{IN,MAX}$	Data input voltage overload	Voltage at the interconnect input		2000			mV_{P-P}
	High-frequency boost	f = 2.1 GHz		9	12	16	dB
V_{OD}	Data differential output voltage swing	DISABLE = high			0.25	10	mV_{P-P}
		DISABLE = low		600	780	1200	
DJ	Deterministic jitter	f = 4.25 GHz, K28.5 pattern, V_{IN} = 200 mV_{P-P} (differential voltage at the interconnect input)	No board or cable		20		ps_{P-P}
			24 inches of 7-mil-wide stripline on standard FR4		25		
			36 inches of 7-mil-wide stripline on standard FR4		20		
			30 feet CX4 cable		20		
			50 feet CX4 cable		35		
RJ	Random jitter	V_{IN} = 200 mV_{P-P} (differential voltage at the interconnect input)			4		ps_{RMS}
	Latency	From DIN+/DIN– to DOUT+/DOUT–			250		ps
t_r	Output rise time	20% to 80%, 4.25 Gbps, no board or cable			55	85	ps
t_f	Output fall time	20% to 80%, 4.25 Gbps, no board or cable			55	85	ps
t_{DIS}	Disable response time				20		ns
V_{AS}	LOS assert threshold voltage	Input signal applied over 36 inches of 7-mil-wide stripline interconnect on standard FR4, voltage at the input of the interconnect line, K28.5 pattern at 4.25 Gbps.(3)		40	80		mV_{P-P}
V_{DAS}	LOS de-assert threshold voltage	Input signal applied over 36 inches of 7-mil-wide stripline interconnect on standard FR4, voltage at the input of the interconnect line, K28.5 pattern at 4.25 Gbps. (3)			130	200	mV_{P-P}
	LOS hysteresis	K28.5 at 4.25 Gbps over 36 inches of 7-mil-wide stripline on standard FR4		3	4.5		dB
$t_{AS/DAS}$	LOS assert/de-assert time	K28.5 at 4.25 Gbps over 36 inches of 7-mil-wide stripline on standard FR4		2		100	µs

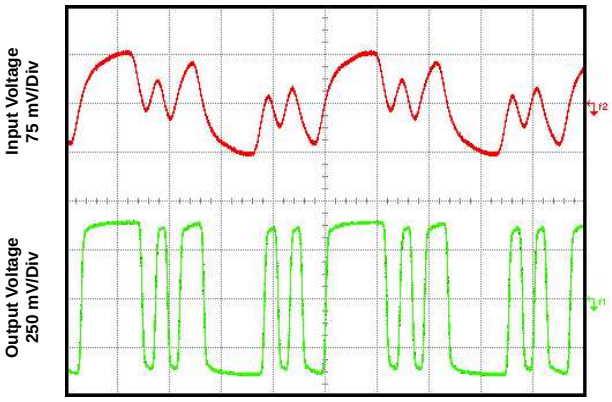
(1) Typical values are measured at V_{CC} = 3.3 V and T_A = 25°C.
(2) The given differential input signal swing is measured at the input of the interconnect. The high-frequency components of the signal at the output of the interconnect (connected to input pins DIN+/DIN– of the TLK4201EA) may be attenuated by as much as 12 dB at 2.1 GHz depending on the interconnect length and attenuation characteristics of the interconnect.
(3) Depending on the interconnect line length and performance, the bit pattern, and the data rate, the assert and de-assert threshold voltage levels vary. For more information, see the *Typical Characteristics* section.

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and V_{IN} = 200 mV_{P-P} (unless otherwise noted)

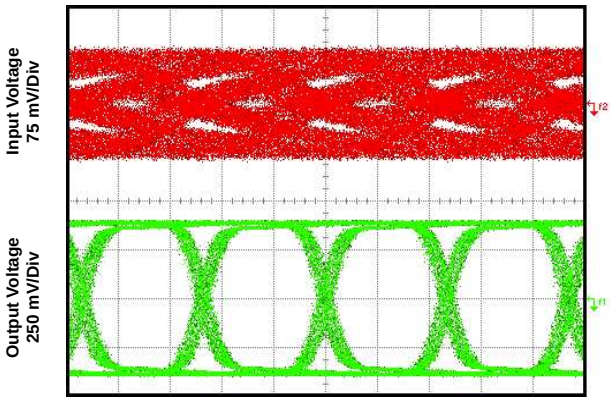
DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 4.25 GBPS USING A PRBS 2^{31} – 1 PATTERN

36 Inches x 7 mil Stripline



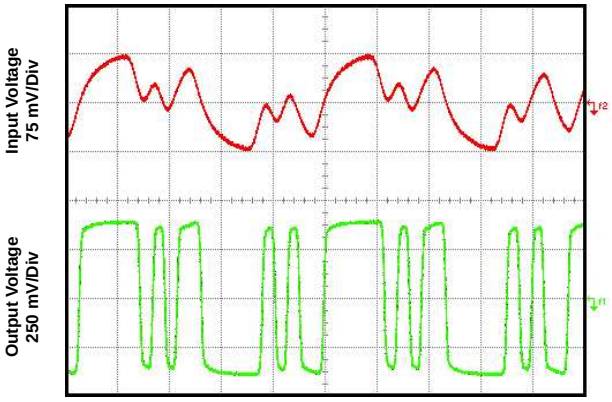
Time – 1 ns/Div

36 Inches x 7 mil Stripline



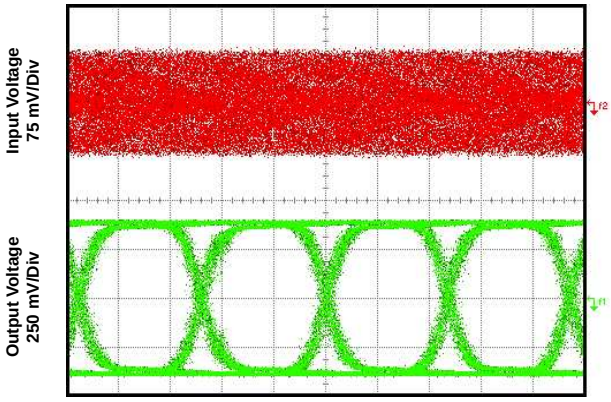
Time – 100 ps/Div

48 Inches x 7 mil Stripline



Time – 1 ns/Div

48 Inches x 7 mil Stripline



Time – 100 ps/Div

G001

Figure 3. Equalizer Input And Output Signals With Different Interconnect Lines at 4.25 GHz

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and V_{IN} = 200 mV_{P-P} (unless otherwise noted)

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 2.125 GBPS USING A PRBS 2^{31} – 1 PATTERN

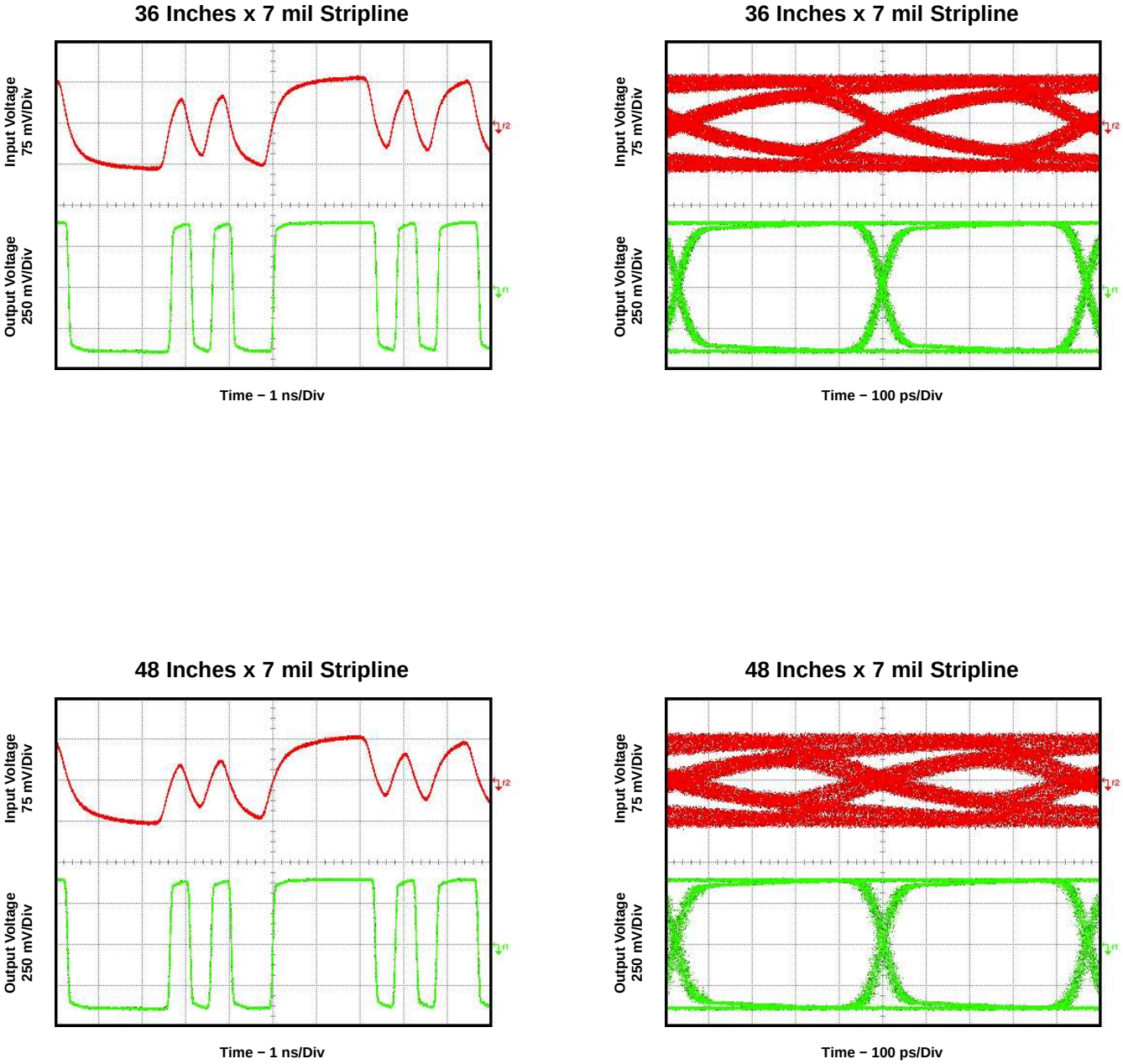


Figure 4. Equalizer Input And Output Signals With Different Interconnect Lines at 2.125 GHz

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and V_{IN} = 200 mV_{P-P} (unless otherwise noted)

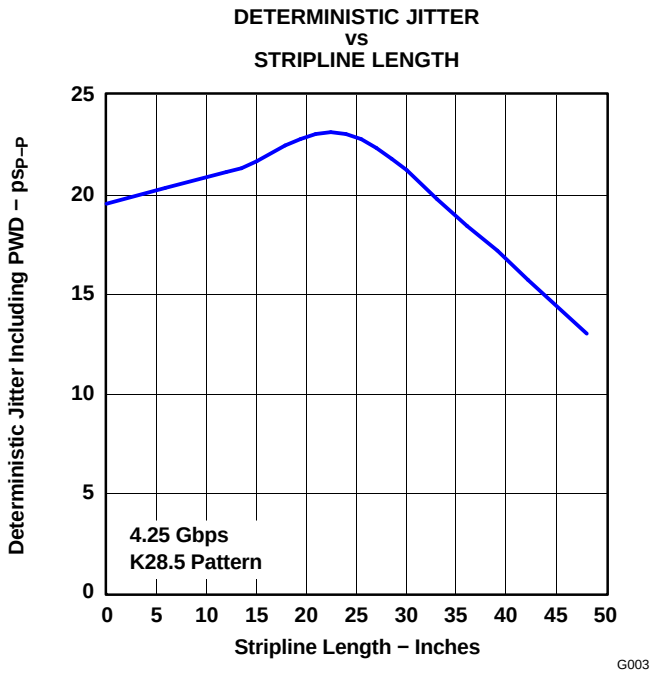


Figure 5.

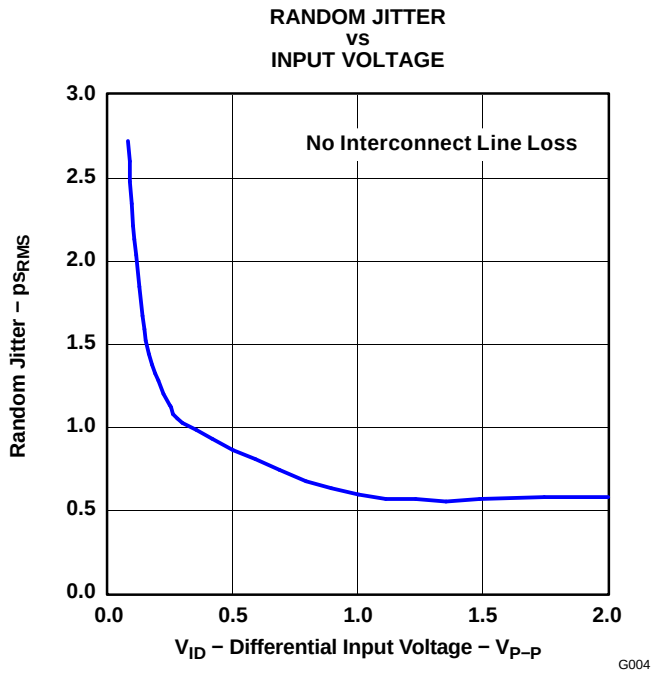


Figure 6.

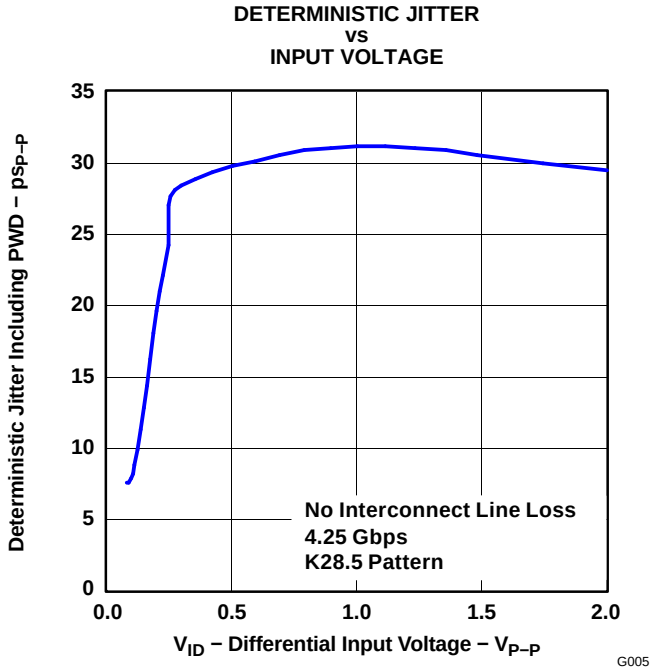


Figure 7.

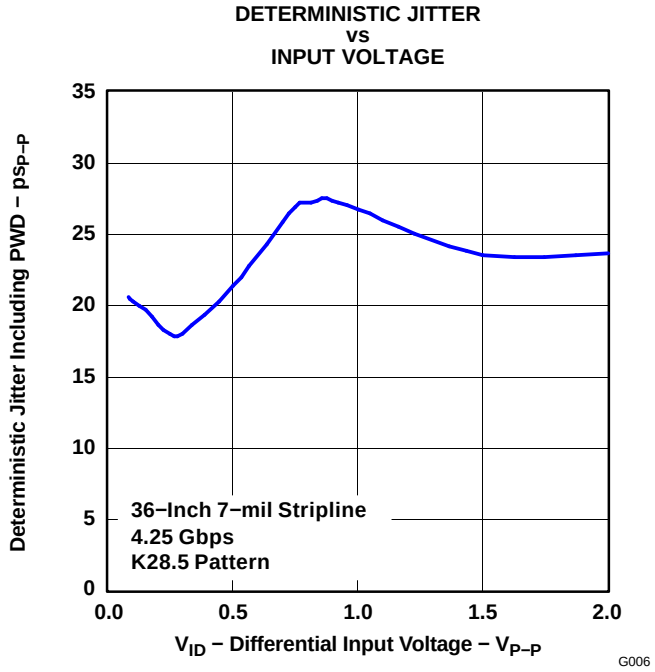


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and V_{IN} = 200 mV_{P-P} (unless otherwise noted)

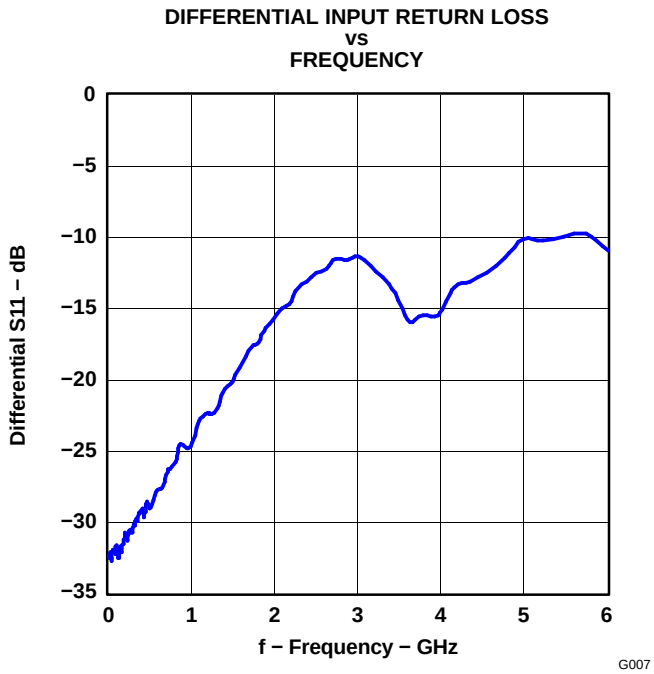


Figure 9.

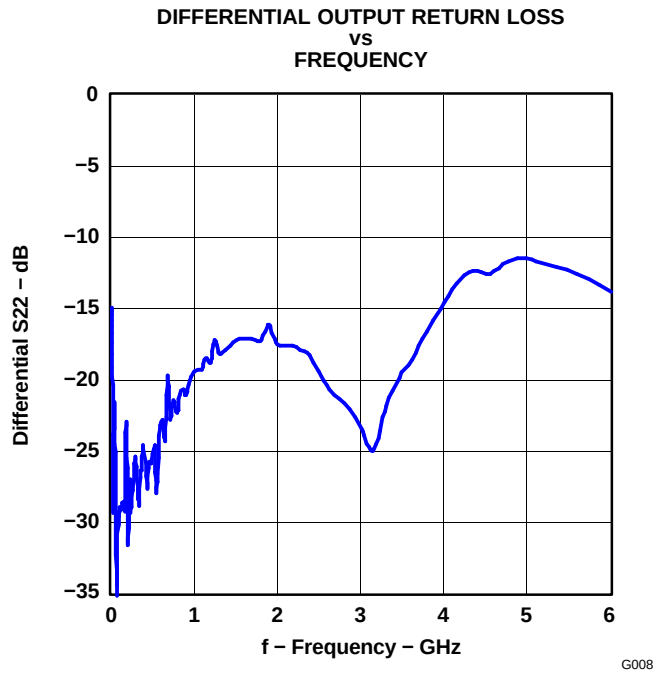


Figure 10.

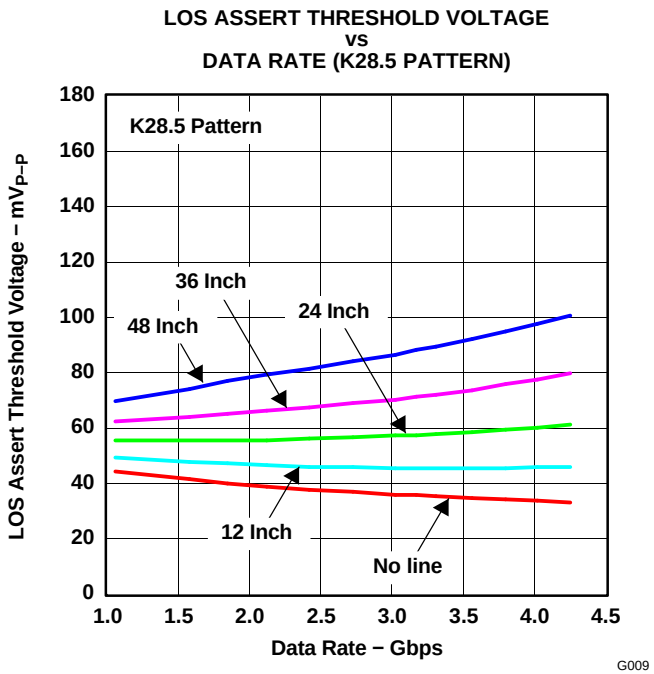


Figure 11.

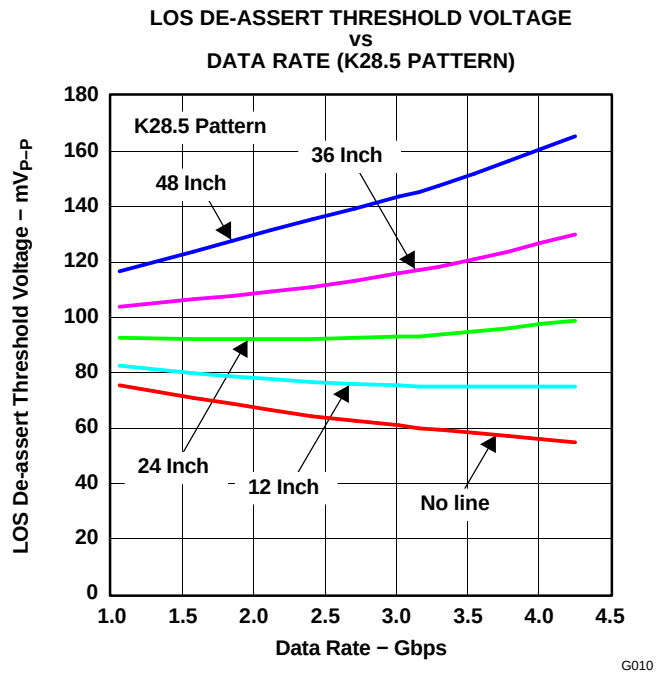


Figure 12.

APPLICATION INFORMATION

Figure 13 shows the TLK4201EA connected with an ac-coupled interface to the data signal source via a stripline interconnect line. The output load is ac-coupled as well.

The ac-coupling capacitors C_1 through C_4 in the input and output data signal lines are the only required external components. In addition, if a very low cutoff frequency is required, as an option, an external filter capacitor C_{OC} may be used.

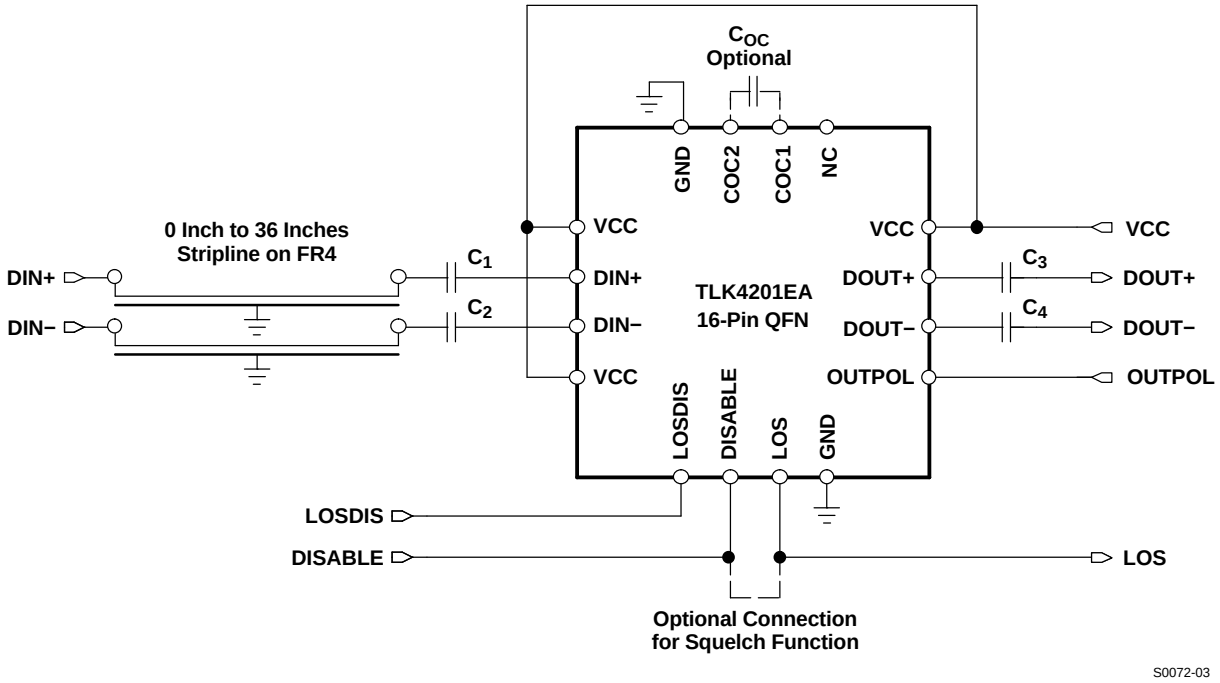


Figure 13. Basic Application Circuit with AC-Coupled I/Os

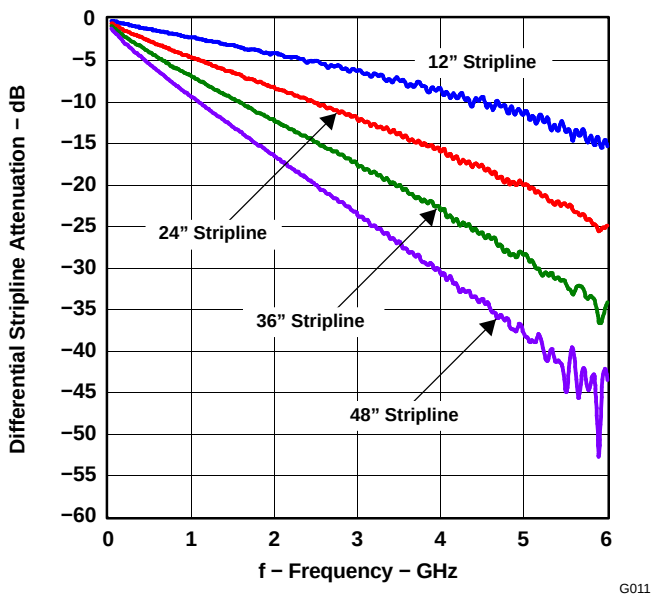


Figure 14. Attenuation Characteristics of Stripline Interconnect Lines

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK4201EARGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	420E	Samples
TLK4201EARGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	420E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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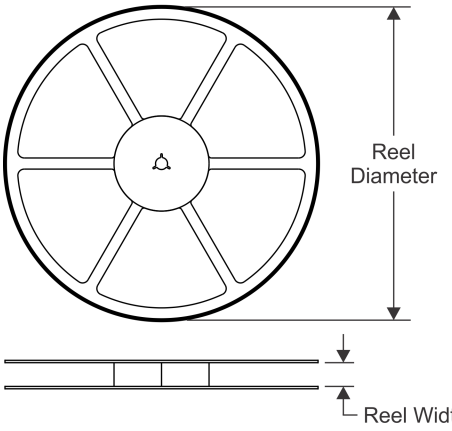
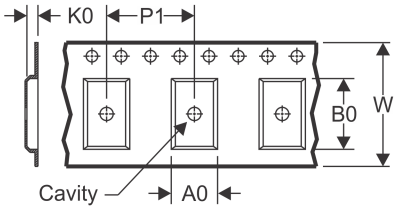
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

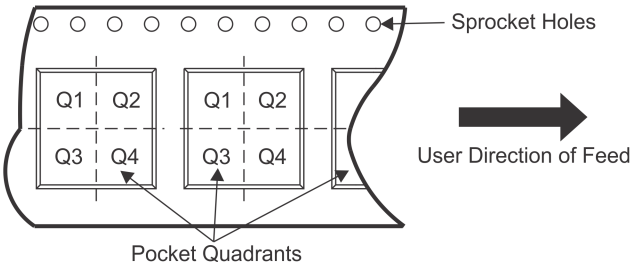


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

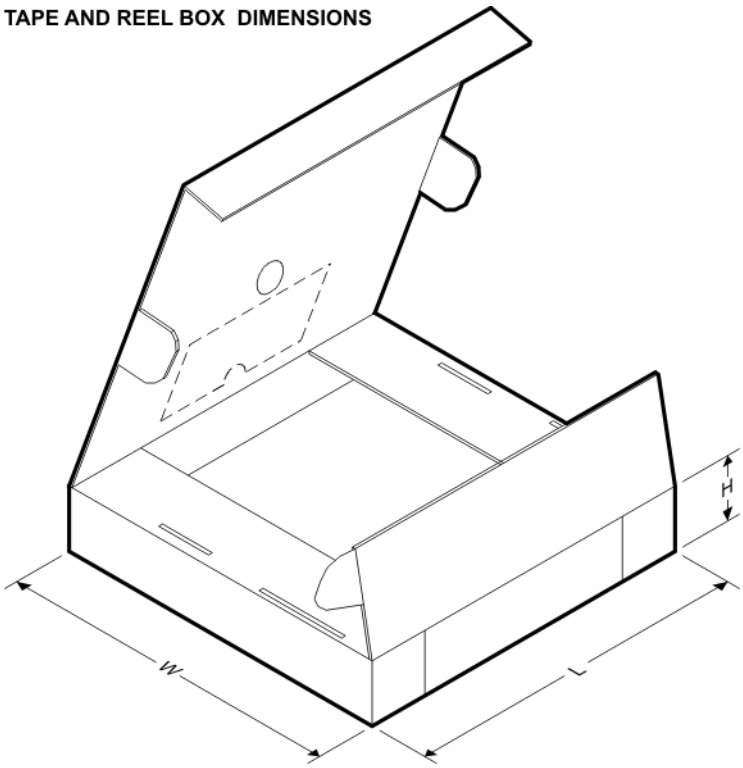
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK4201EARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLK4201EARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



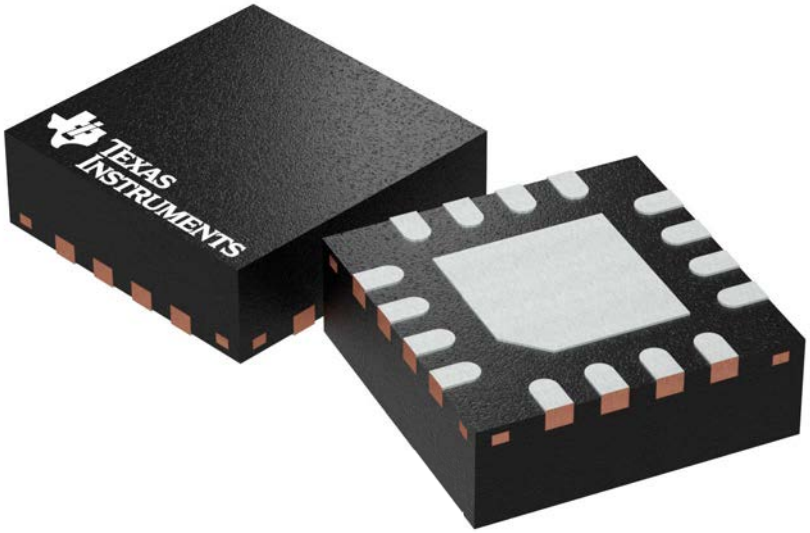
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK4201EARGTR	VQFN	RGT	16	3000	350.0	350.0	43.0
TLK4201EARGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

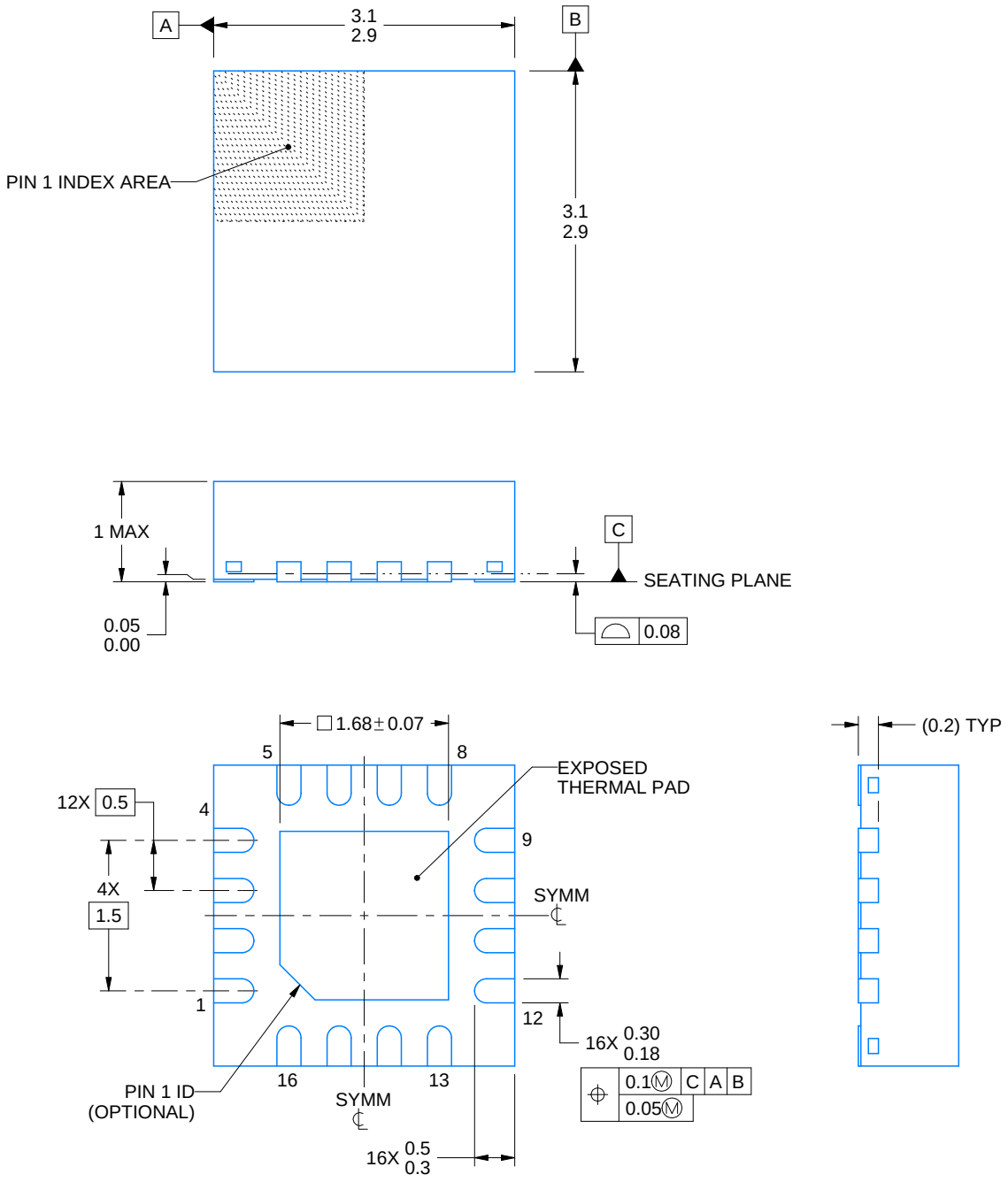
4203495/I

RGT0016C

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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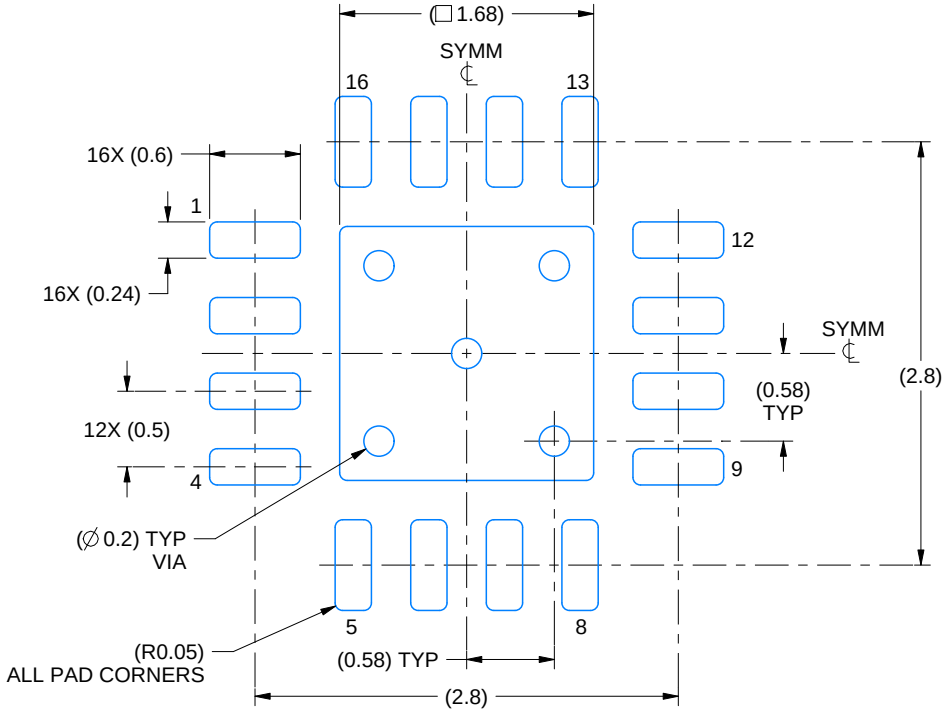
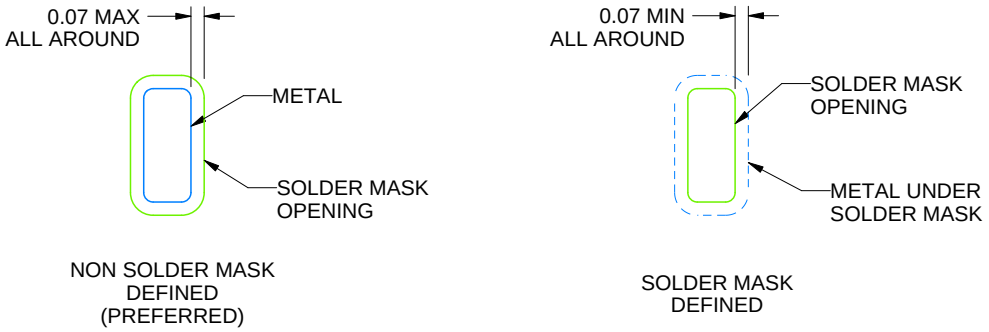
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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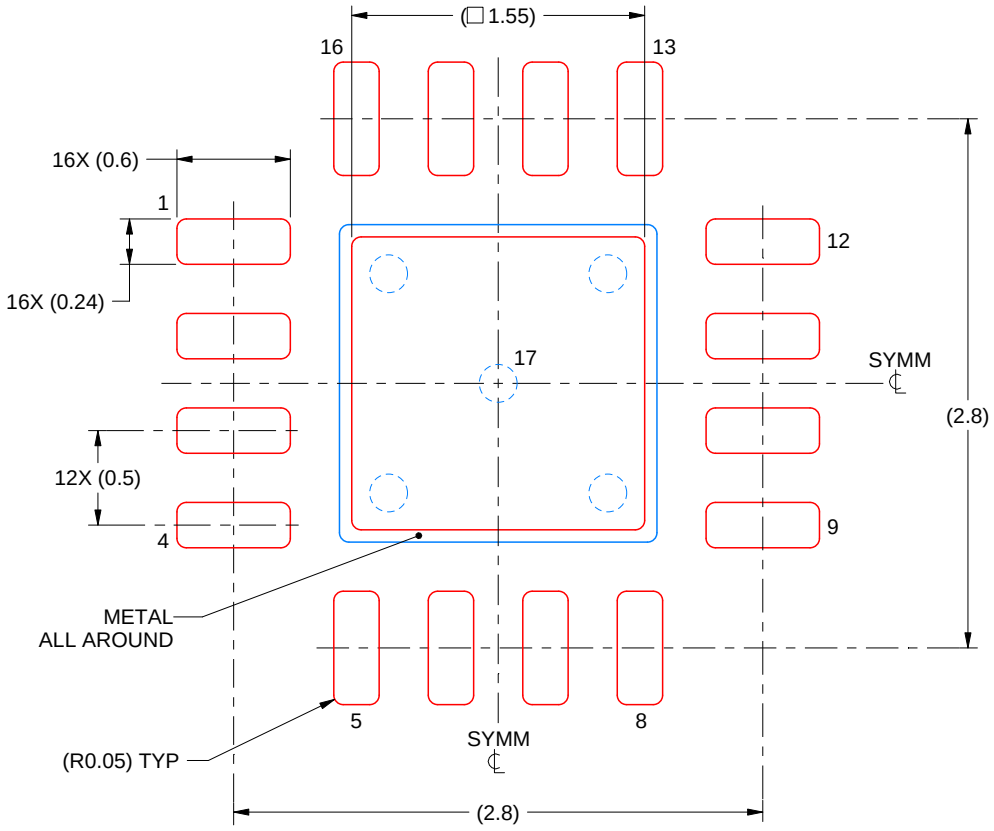
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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